

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,  
Petitioner

v.

MARLIN SEMICONDUCTOR LIMITED,  
Patent Owner

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Case IPR2025-01527  
U.S. Patent No. 9,117,909

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**PETITIONER'S UPDATED EXHIBIT LIST**

***Mail Stop "PATENT BOARD"***  
Patent Trial and Appeal Board  
U.S. Patent and Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450

Petitioner files this Updated Exhibit List to accompany the filing of Corrected Exhibit 1003, The Declaration of Dr. Sayeef Salahuddin. The Board granted authorization to file this corrected copy on October 7, 2025.

**PETITIONER’S UPDATED EXHIBIT LIST**

<b>Exhibit No.</b>	<b>Description</b>
<b>1001</b>	U.S. Patent No. 9,117,909 to Kuo et al. (“909 patent”)
<b>1002</b>	Prosecution History of U.S. Patent No. 9,117,909 to Kuo et al.
<b>1003</b>	Declaration of Dr. Sayeef Salahuddin [ <b>Corrected</b> ]
<b>1004</b>	U.S. Patent No. 7,994,020 to Lin et al. (“Lin”)
<b>1005</b>	U.S. Patent No. 8,629,512 to Liaw (“Liaw”)
<b>1006</b>	U.S. Patent No. 8,546,891 to Chang et al. (“Chang”)
<b>1007</b>	<i>Intentionally Left Blank</i>
<b>1008</b>	<i>Intentionally Left Blank</i>
<b>1009</b>	U.S. Patent Application Pub. No. 2013/0056826 to Liu et al. (“Liu”)
<b>1010</b>	U.S. Patent No. 9,368,388 to Liaw (“Liaw-388”)
<b>1011</b>	U.S. Patent Application Pub. No. 2013/0045580 to Cho (“Cho”)
<b>1012</b>	<i>Curriculum Vitae</i> of Dr. Sayeef Salahuddin
<b>1013</b>	U.S. Patent Application Pub. No. 2011/0068405 to Yuan et al. (“Yuan”)
<b>1014</b>	Park, D., et al., “Present and Future of Si-based Transistor Technology for Memories,” <i>ECS Transactions</i> , 2(11):11-26 (2006) (“Park”)
<b>1015</b>	U.S. Patent No. 7,148,120 to Chen et al. (“Chen-120”)
<b>1016</b>	U.S. Patent No. 7,611,950 to Kim (“Kim”)
<b>1017</b>	U.S. Patent Application Pub. No. 2011/0298041 to Renn (“Renn”)
<b>1018</b>	U.S. Patent Application Pub. No. 2007/0148979 to Lee et al. (“Lee-979”)
<b>1019</b>	U.S. Patent No. 6,413,802 to Hu et al. (“Hu”)

Exhibit No.	Description
1020	Chau, R., et al., “Silicon nano-transistors and breaking the 10 nm physical gate length barrier,” 61st Device Research Conference. Conference Digest, Salt Lake City, UT, USA, 123-126 (2003) (“Chau”)
1021	Colinge, J., et al.,” FinFETs and Other Multi-Gate Transistors,” Springer (2008) (“Colinge”)
1022	Hu, C., “Modern Semiconductor Devices for Integrated Circuits,” 1st ed. (2009) (Excerpt) (“Hu-2009”)
1023	Huang, X., et al., “Sub 50-nm FinFET: PMOS,” International Electron Devices Meeting 1999. Technical Digest (Cat. No.99CH36318), Washington, DC, USA, 67-70 (1999) (“Huang”)
1024	Bohr, M. et al., “Intel’s Revolutionary 22nm Transistor Technology,” available at <a href="http://download.intel.com/newsroom/kits/22nm/pdfs/22nm-Details_Presentation.pdf">http://download.intel.com/newsroom/kits/22nm/pdfs/22nm-Details_Presentation.pdf</a> (accessed through <a href="https://newsroom.intel.com/press-kits/intel-22nm-3-d-tri-gatetransistor-technology/">https://newsroom.intel.com/press-kits/intel-22nm-3-d-tri-gatetransistor-technology/</a> ), (“Bohr”)
1025	Kundu, S., et al., “Nanoscale CMOS VLSI Circuits: Design for Manufacturability,” 1st ed. (2010) (“Kundu”)
1026	Huang, X., et al., “Sub-50 nm P-channel FinFET,” IEEE Transactions on Electron Devices, 48(5):880-886 (2001) (“Huang-2001”)
1027	U.S. Patent No. 7,172,943 to Yeo et al. (“Yeo”)
1028	Park, T., et al., “Fabrication of body-tied FinFETs (Omega MOSFETs) using bulk Si wafers,” 2003 Symposium on VLSI Technology, Digest of Technical Papers, Kyoto, Japan, 135-136 (2003) (“Park-2003”)
1029	Wolf, S. and Tauber, R., “Silicon Processing For The VLSI Era,” Vol. 2, Lattice Press (1990) (“Wolf”)
1030	U.S. Patent No. 8,110,466 to Shieh et al. (“Shieh”)

<b>Exhibit No.</b>	<b>Description</b>
<b>1031</b>	Shamiryan, D., et al. "Dry etching process for bulk finFET manufacturing," <i>Microelectron. Engineering</i> , 86(10):96-98 (2009) ("Shamiryan")
<b>1032</b>	U.S. Patent No. 2012/0049294 to Chen et al. ("Chen-294")
<b>1033</b>	Engelhardt, M., et al. "A new CBrF <sub>3</sub> process for etching tapered trenches in Silicon," <i>Journal of Electrochemical Society: Solid-State Science and Technology</i> , 134(8):1985-1988 (1987) ("Engelhardt")
<b>1034</b>	Makovejev, S., et al. "Improvement of high-frequency FinFET performance by fin width engineering," 2012 IEEE International SOI Conference (SOI), Napa, CA, USA, 2012, pp. 1-2
<b>1035</b>	Jan, C., et al. "A 22nm SoC Platform Technology Featuring 3-D Tri-Gate and High-k/Metal Gate, Optimized for Ultra Low Power, High Performance and High Density SoC Applications," 2012 International Electron Devices Meeting, San Francisco, CA, USA, 2012, pp. 3.1.1-3.1.4
<b>1036</b>	U.S. Patent Application Pub. No. 2012/0001197 to Liaw et al. ("Liaw-197")
<b>1037</b>	U.S. Patent Application Pub. No. 2014/0131813 to Liaw et al. ("Liaw-813")

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Respectfully submitted,

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**CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e))**

I certify that the above-captioned **PETITIONER'S UPDATED EXHIBIT LIST** and **CORRECTED EXHIBIT 1003** were served in their entireties on October 8, 2025 upon the following parties via electronic mail:

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