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(54) **FIN FIELD EFFECT TRANSISTOR**

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257/E29.264

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(57) **ABSTRACT**

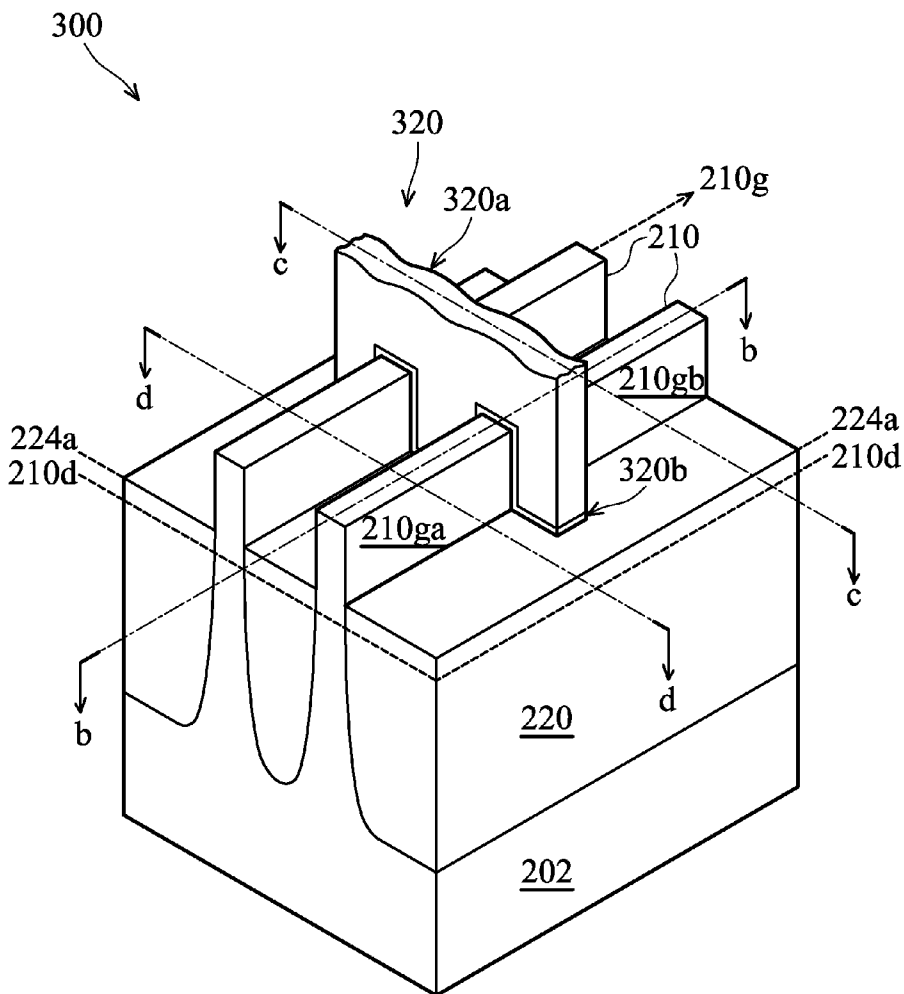
An exemplary structure for the fin field effect transistor comprises a substrate comprising a major surface; a plurality of fin structures protruding from the major surface of the substrate, wherein each fin structure comprises an upper portion and a lower portion separated at a transition location at where the sidewall of the fin structure is at an angle of 85 degrees to the major surface of the substrate, wherein the upper portion has sidewalls that are substantially perpendicular to the major surface of the substrate and a top surface having a first width, wherein the lower portion has tapered sidewalls on opposite sides of the upper portion and a base having a second width larger than the first width; and a plurality of isolation structures between the fin structures, wherein each isolation structure extends from the major surface of the substrate to a point above the transition location.

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Related U.S. Application Data

(60) Provisional application No. 61/245,485, filed on Sep. 24, 2009.



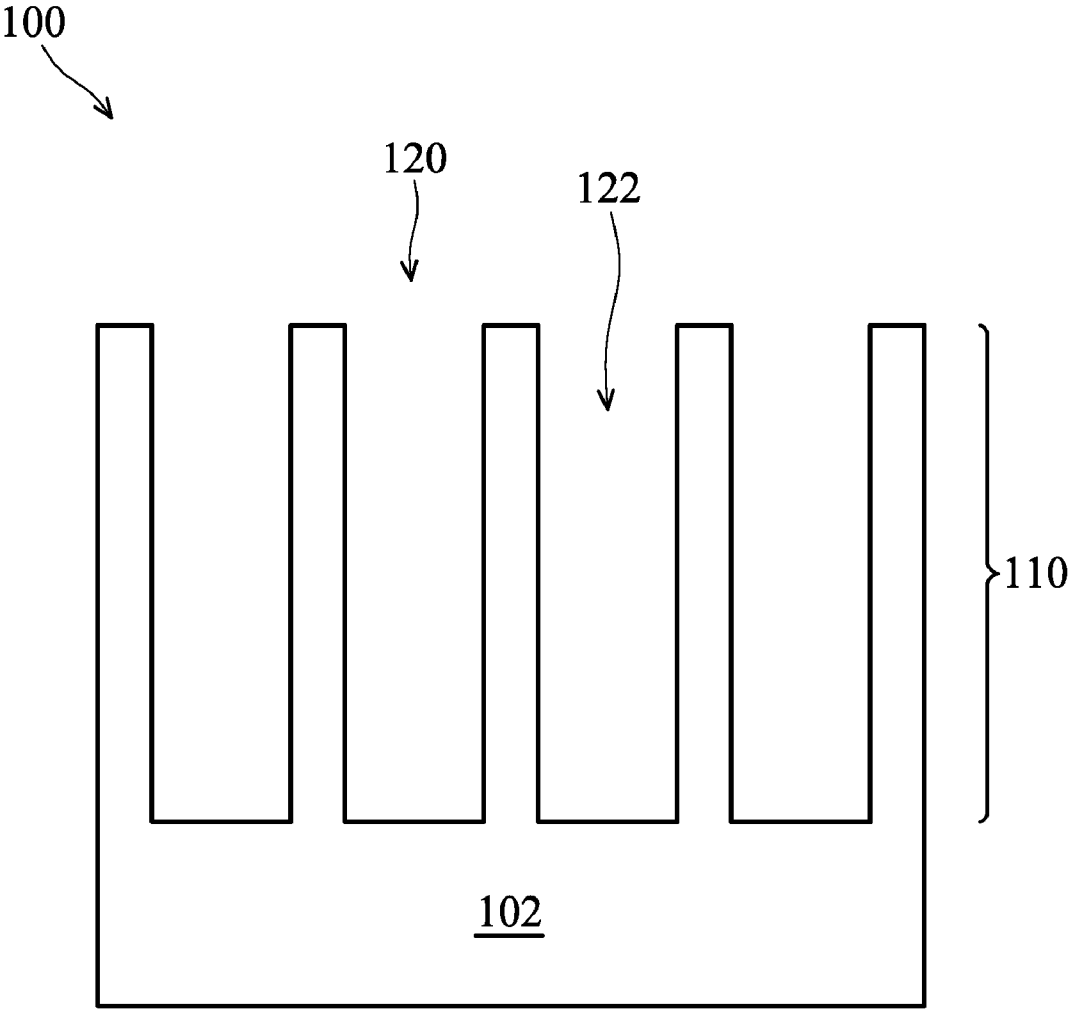


FIG. 1A (PRIOR ART)

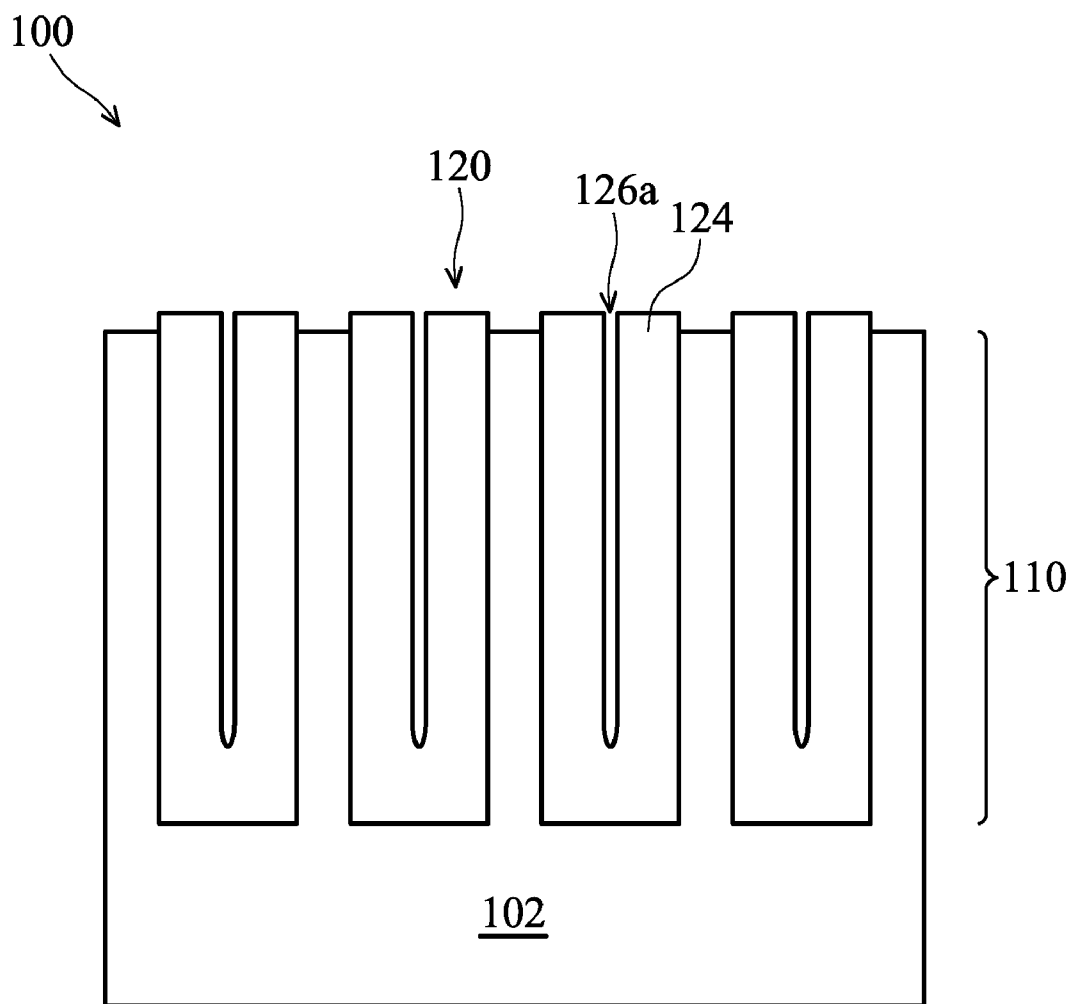


FIG. 1B (PRIOR ART)

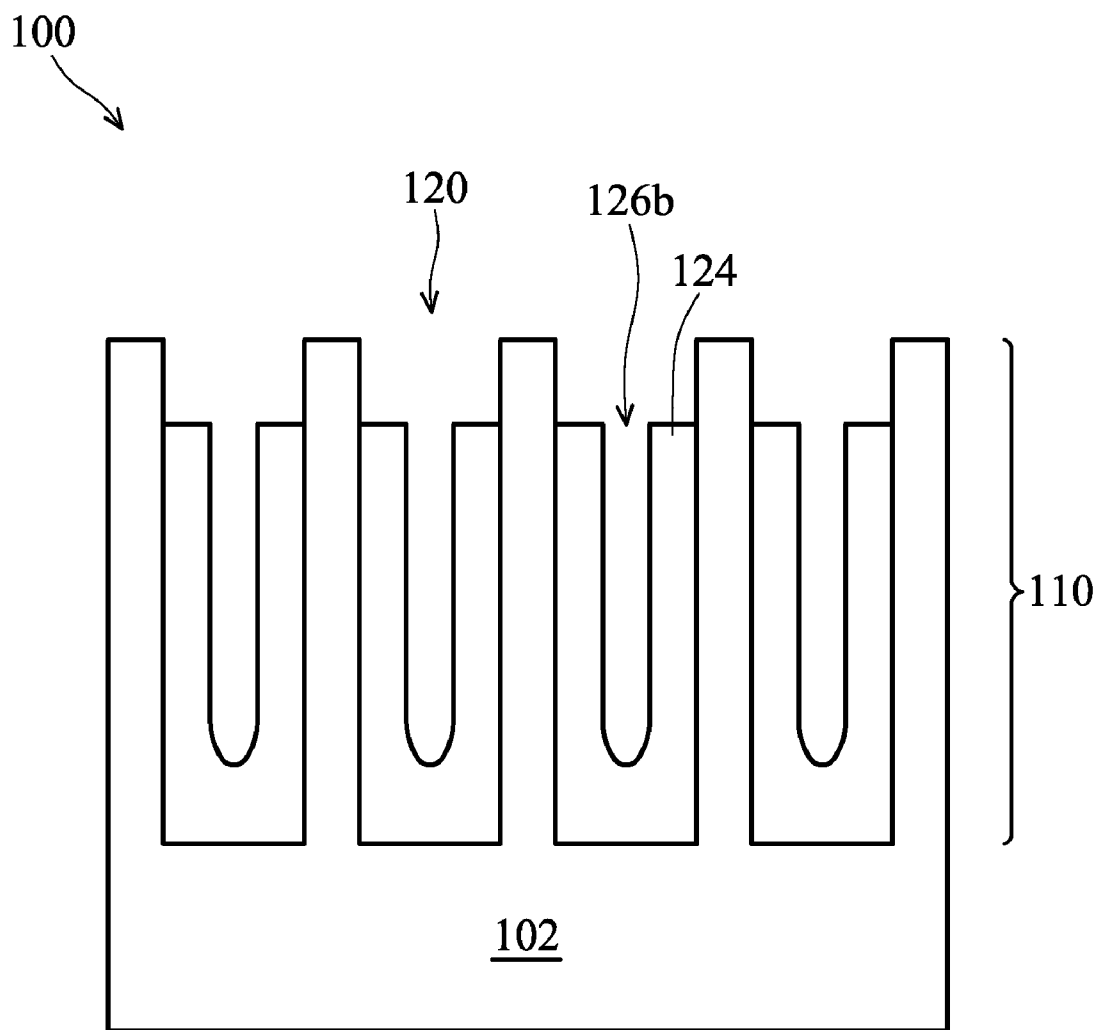


FIG. 1C (PRIOR ART)

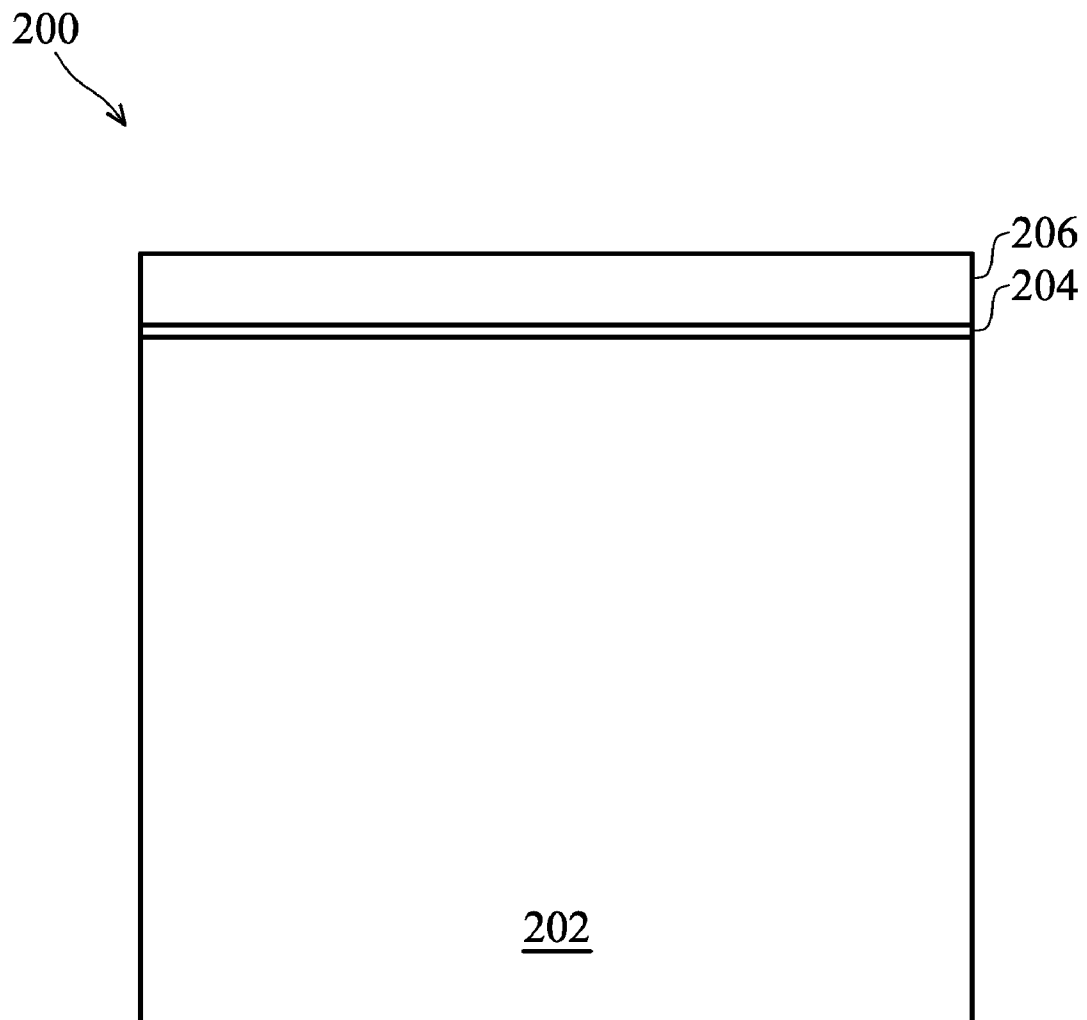


FIG. 2A

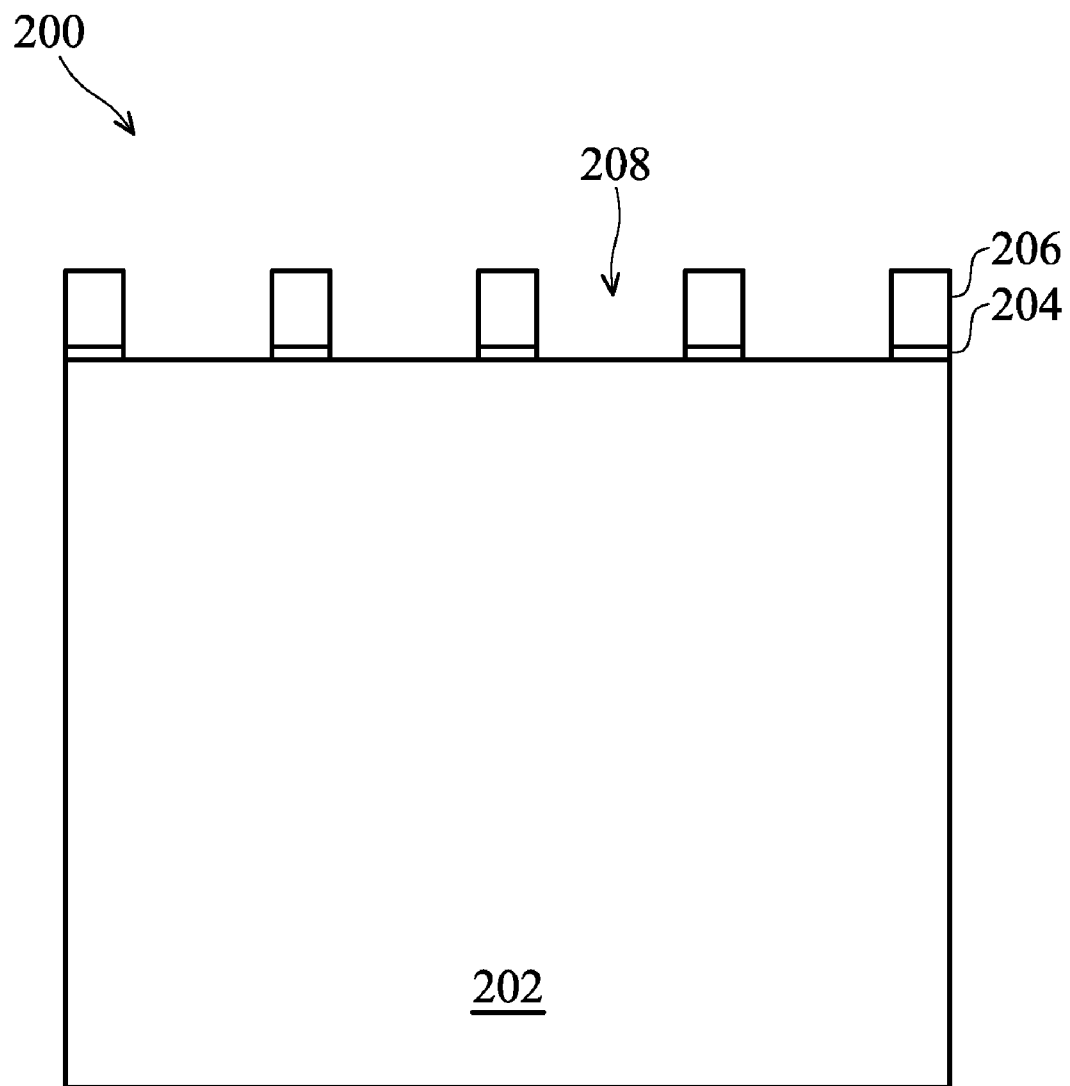


FIG. 2B

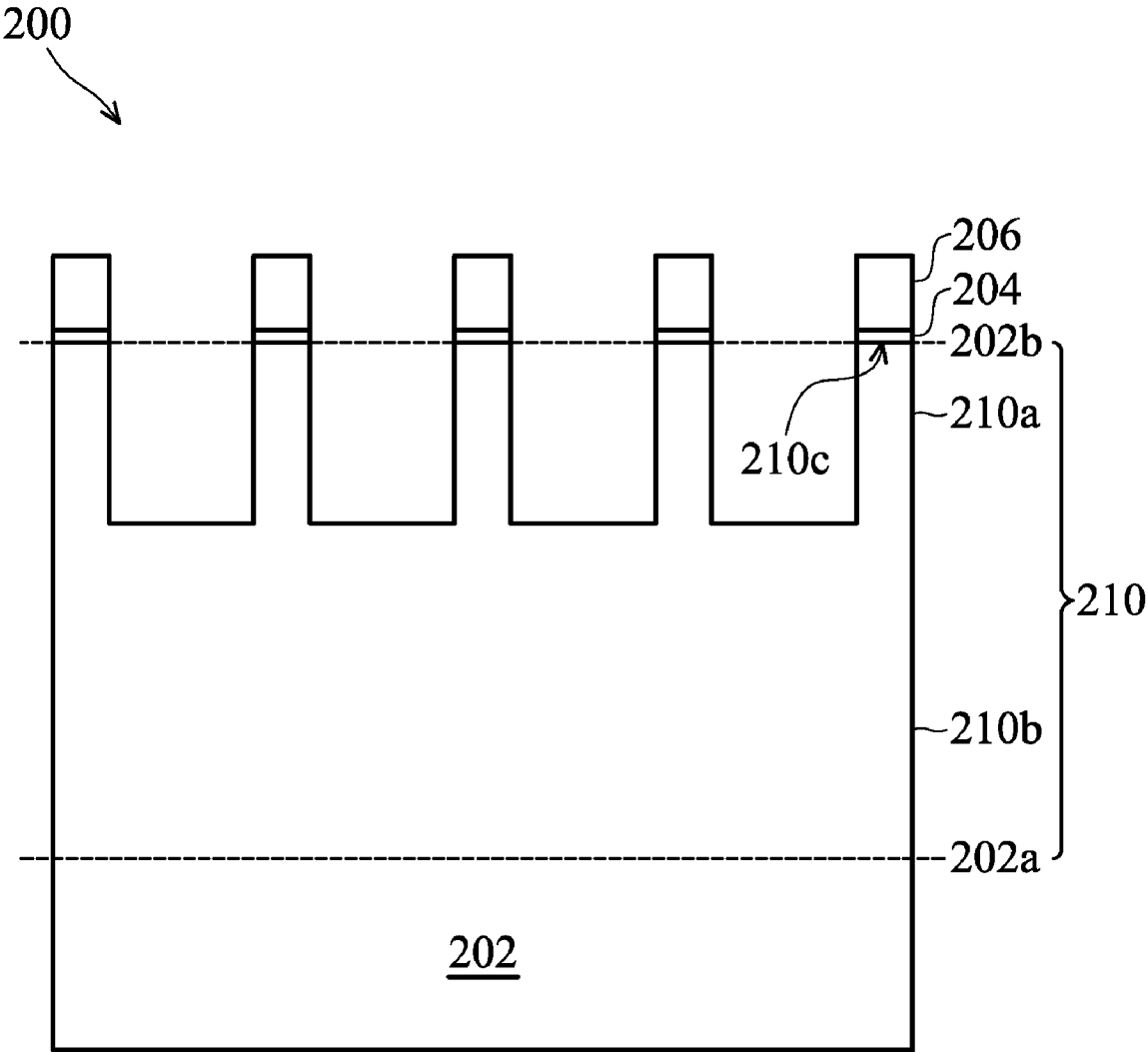


FIG. 2C

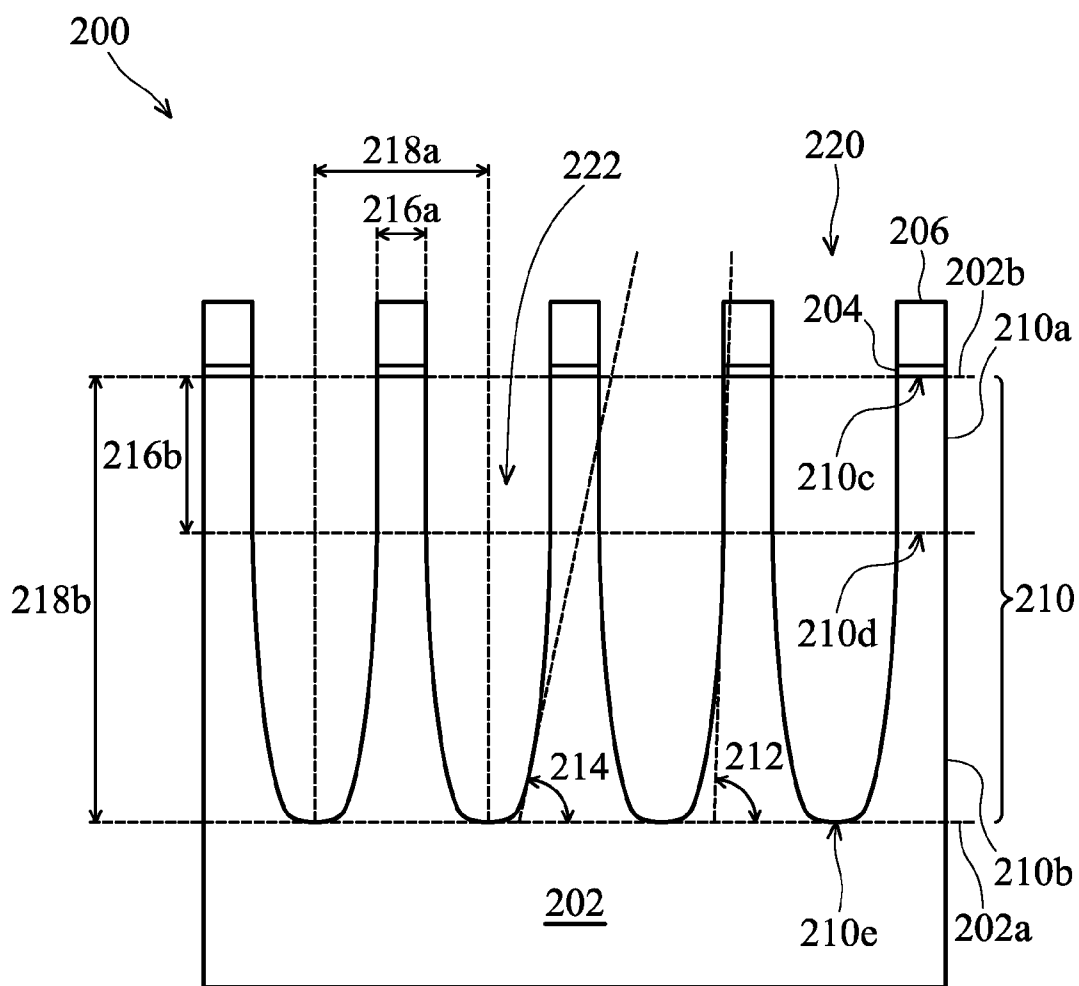


FIG. 2D

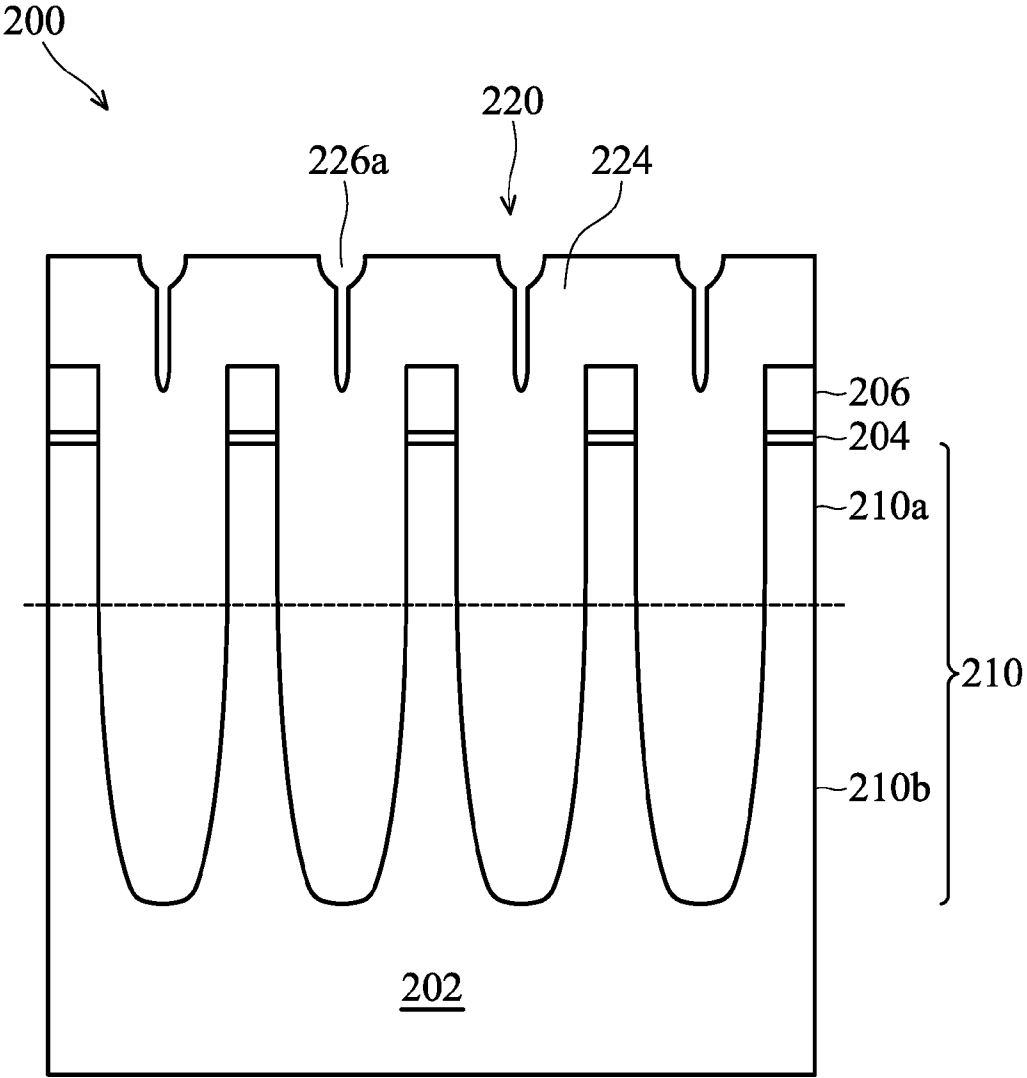


FIG. 2E

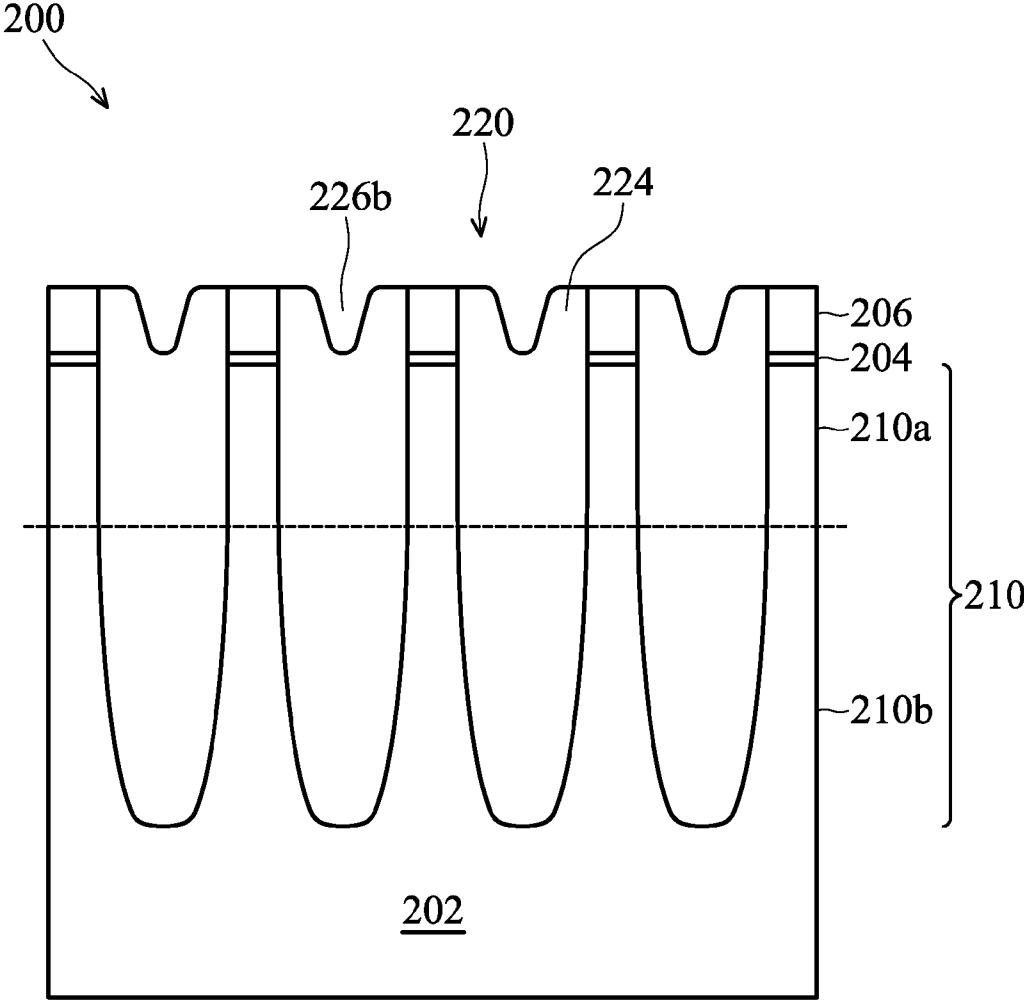


FIG. 2F

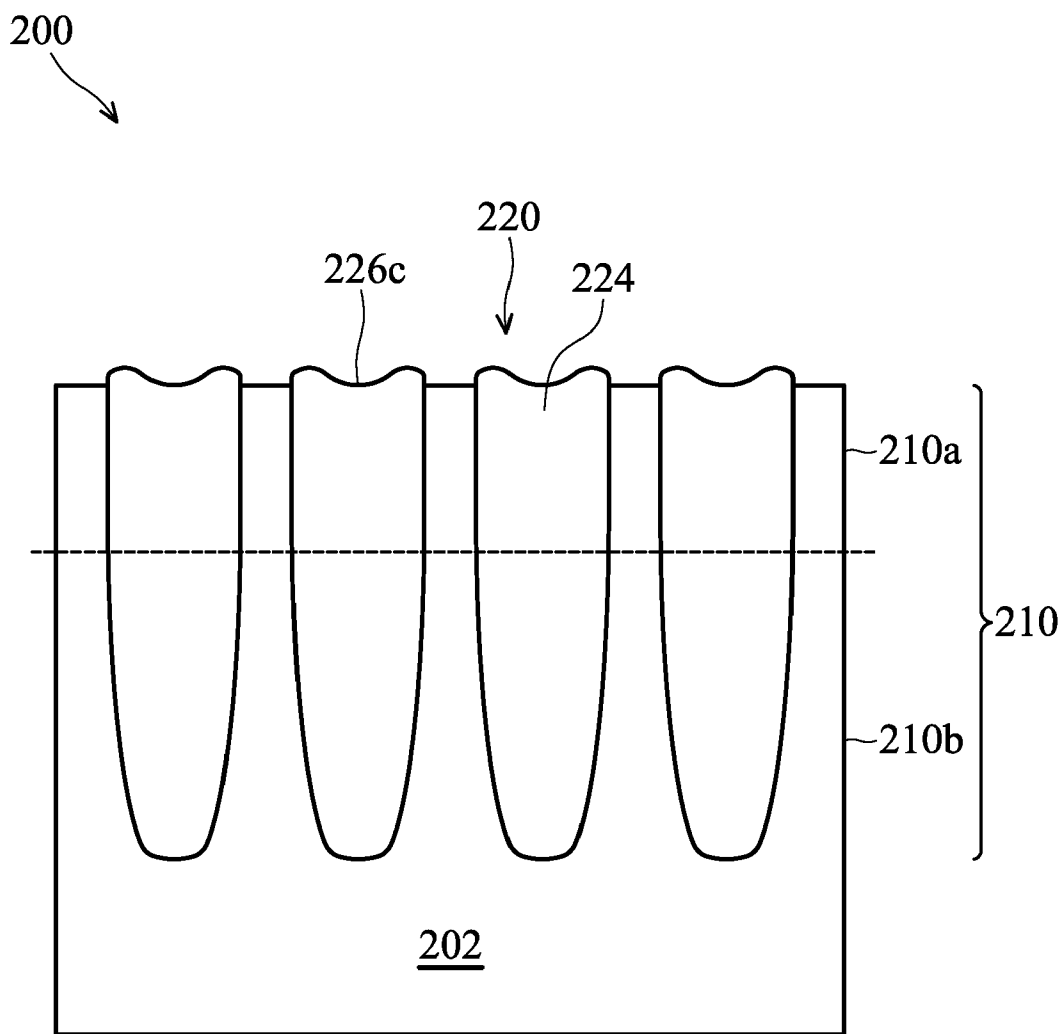


FIG. 2G

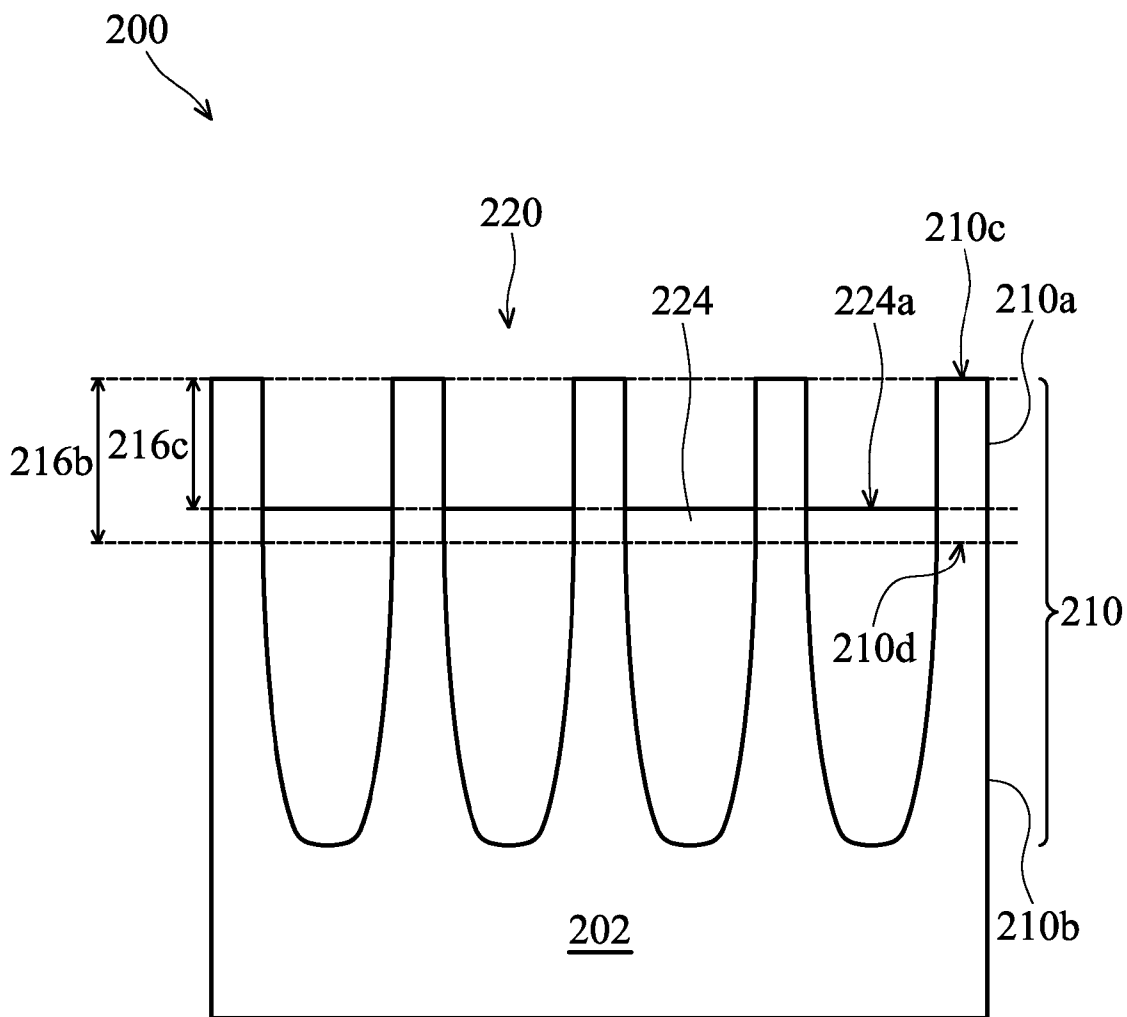


FIG. 2H

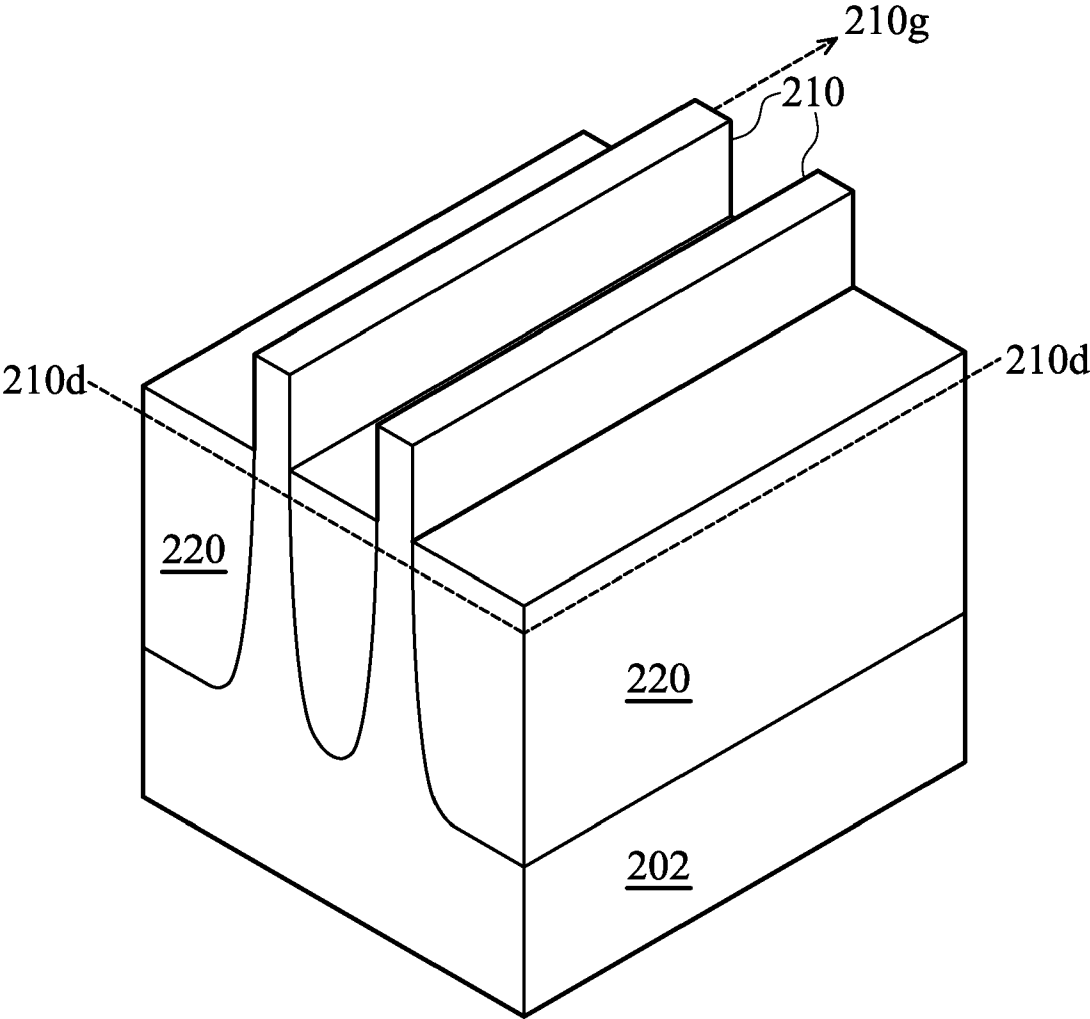


FIG. 2I

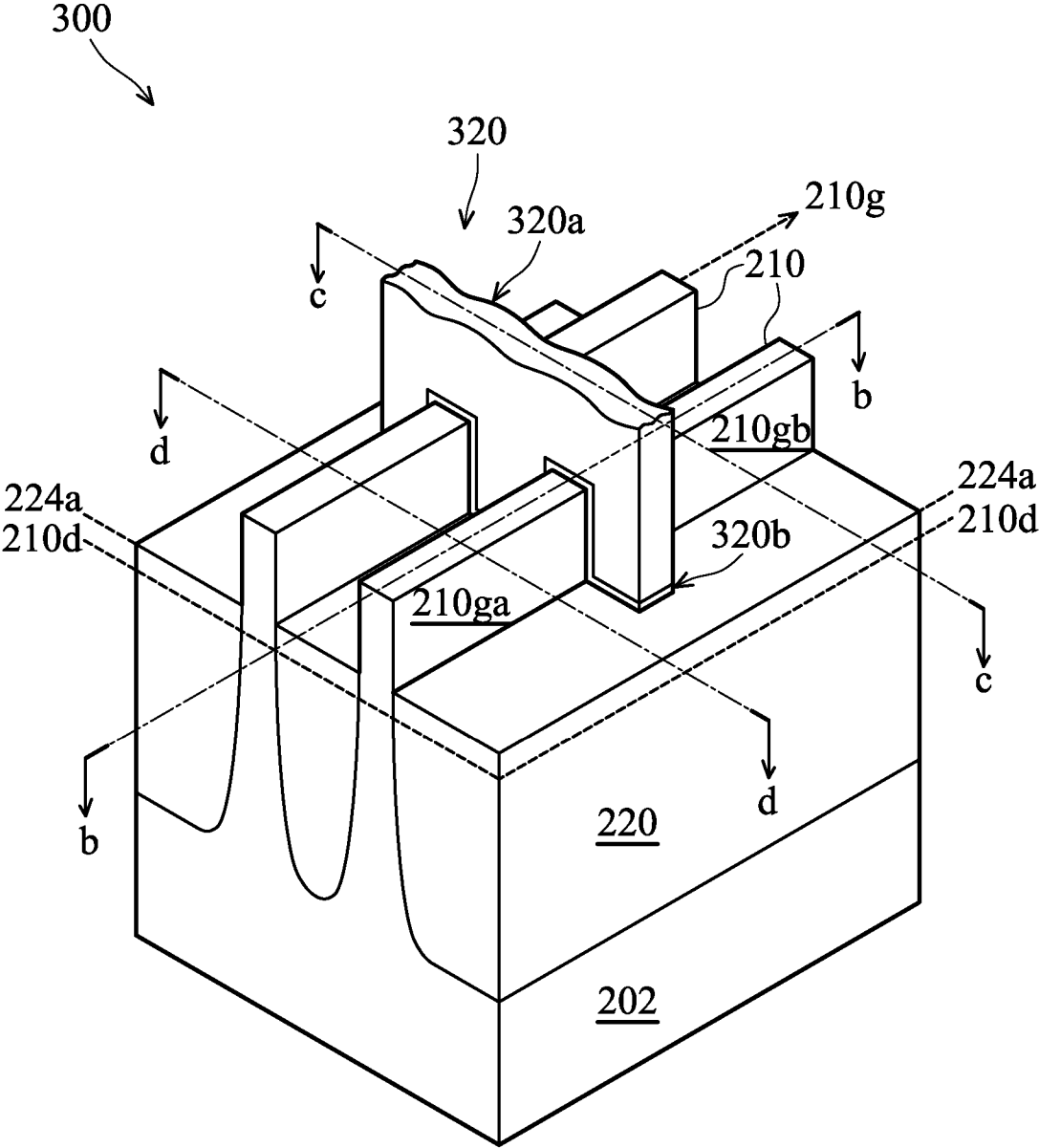


FIG. 3A

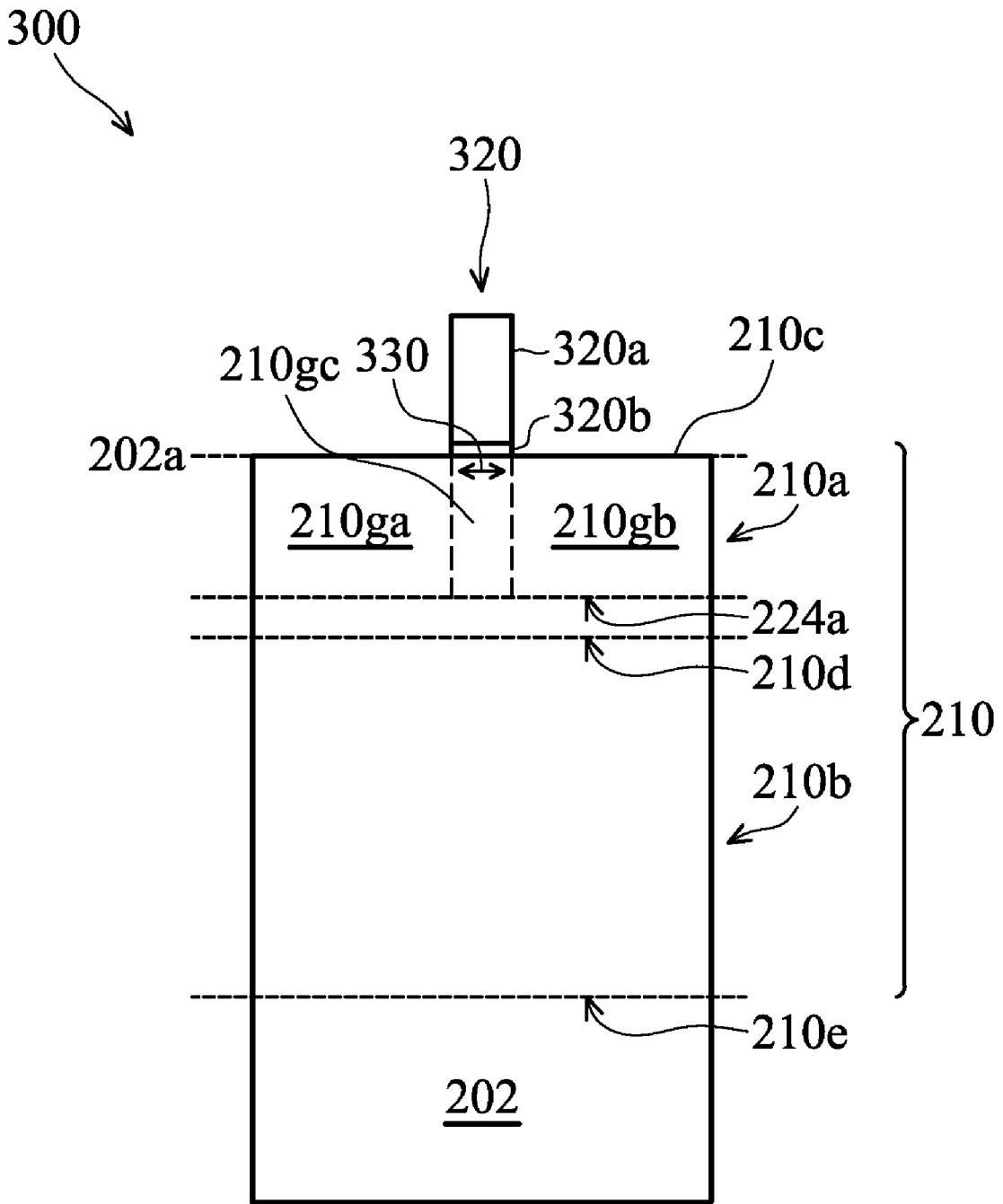


FIG. 3B

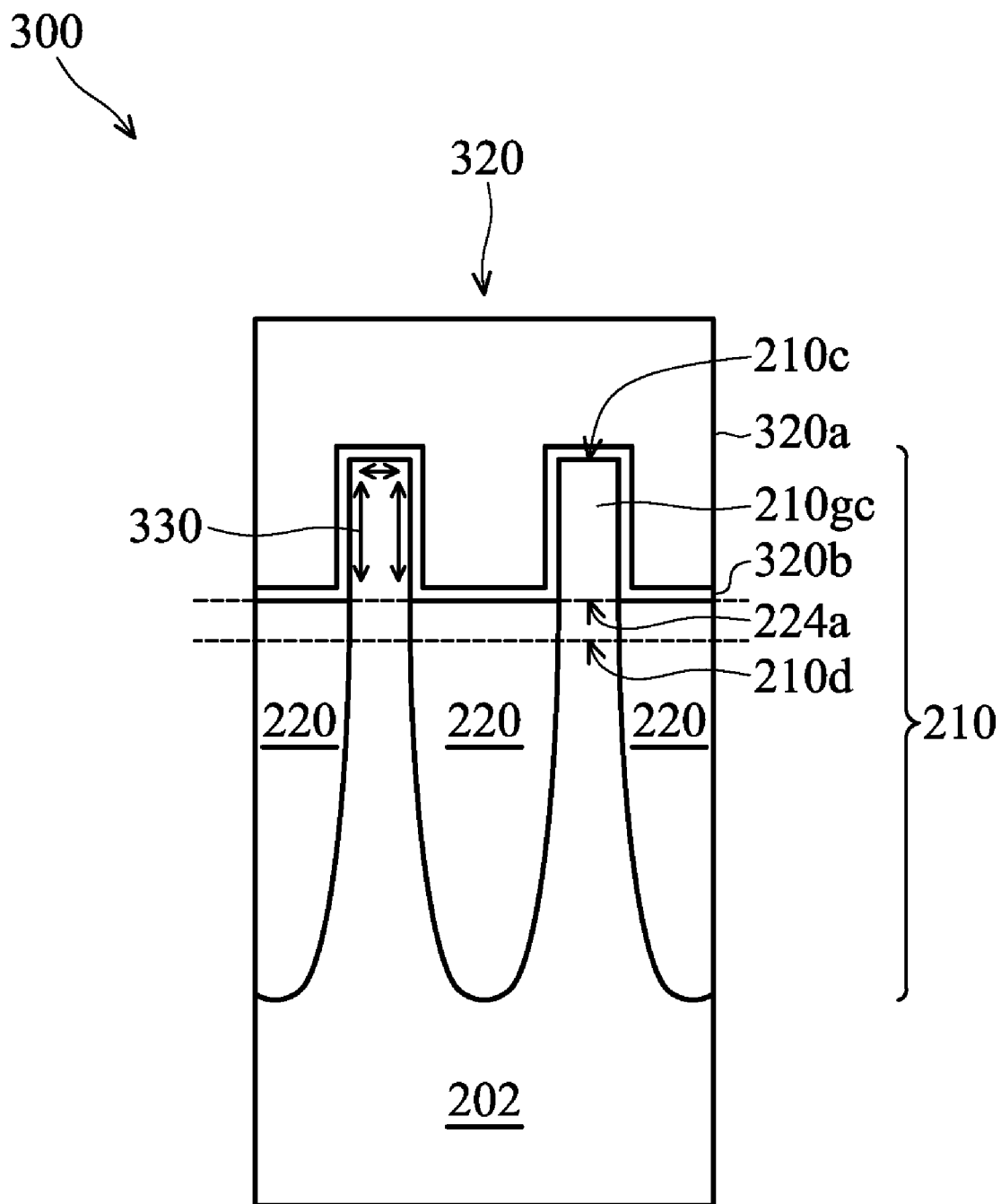


FIG. 3C

300
↙

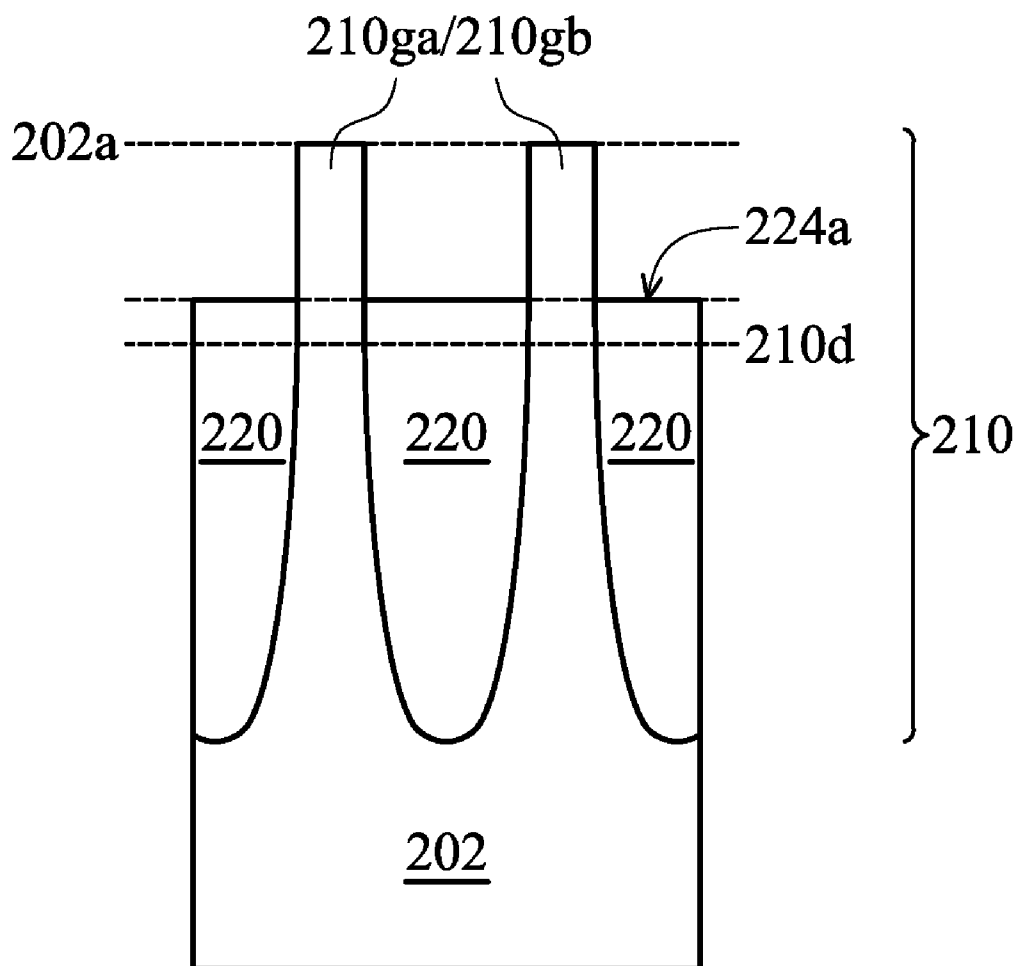


FIG. 3D

FIN FIELD EFFECT TRANSISTOR

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims priority of U.S. Provisional Patent Application Ser. No. 61/245,485, filed on Sep. 24, 2009, which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present invention relates generally to transistors, and more particularly to a fin field effect transistor with an isolation structure.

BACKGROUND

[0003] Semiconductor devices are used in a large number of electronic devices, such as computers, cell phones, and others. Semiconductor devices comprise integrated circuits (ICs) that are formed on semiconductor wafers by depositing many types of thin films of material over the semiconductor wafers, and patterning the thin films of material to form the integrated circuits. The ICs include field-effect transistors (FETs), such as metal-oxide-semiconductor field-effect transistors (MOSFETs).

[0004] One of the goals of the semiconductor industry is to continue shrinking the size and increasing the speed of individual MOSFETs. To achieve these goals, three dimensional (3-D) or non-planar transistor structures such as fin FETs (FINFETs), multiple gate transistors, or gate-all-around transistors are being investigated for use in sub 22 nm transistor nodes. Such transistors not only improve area density, but also improve gate control of the channel.

[0005] However, fabrication of the FINFETs is complex and requires overcoming a number of challenging problems. One of the challenges is forming recess-free isolation structures. These recesses can be formed in a dielectric material in the early stages of forming the isolation structure. FIGS. 1A-C show cross-sectional views of a plurality of conventional isolation structures **120** for FINFETs **100** having recesses **126b** present in the isolation structures **120** at various stages of fabrication. FIG. 1A illustrates the plurality of isolation structures **120** may be formed by etching a substrate **102** to form a plurality of trenches **122** separating a plurality of fin structures **110**, then filling the plurality of trenches **122** with a dielectric material **124** (shown in FIG. 1B), such as high-density plasma (HDP) oxides, tetraethoxysilane (TEOS) oxides, or the like. The dielectric material **124** may comprise a plurality of deep slims/recesses **126a** due to the high aspect ratio of the plurality of trenches **122**. FIG. 1C shows a plurality of recesses **126b** in the plurality of isolation structures **120** may be formed along the plurality of deep slims/recesses **126a** during and after removing the upper portions of the dielectric material **124**. The plurality of recesses **126b** is problematic in various respects. For example, the plurality of recesses **126b** present in the plurality of isolation structures **120** can become a receptacle of polysilicon and/or metals during subsequent processing thereby increasing the likelihood of device instability and/or device failure.

[0006] Accordingly, what is needed is an isolation structure for a FINFET having no recess.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The present disclosure is best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale and are used for illustration purposes only. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0008] FIGS. 1A-C show cross-sectional views of a plurality of conventional isolation structures for FINFETs having recesses present in the isolation structures at various stages of fabrication;

[0009] FIGS. 2A-H show schematic cross-sectional views of a substrate being processed to fabricate a plurality of FINFETs according to an embodiment, showing various stages of fabrication;

[0010] FIG. 2I shows a perspective view of the plurality of the FINFETs fabricated using the steps shown in FIG. 2A-H; and

[0011] FIG. 3A-D shows a complete FINFET device having a plurality of isolation structures fabricated using the steps shown in FIG. 2A-H, wherein FIG. 3A shows a perspective view, and wherein FIGS. 3B-D show cross-section views taken along the respective lines of FIG. 3A.

DESCRIPTION

[0012] It is understood that the following disclosure provides many different embodiments, or examples, for implementing different features of the invention. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed. Various features may be arbitrarily drawn in different scales for the purpose of simplicity and clarity.

[0013] FIGS. 2A-H show schematic cross-sectional views of a substrate being processed to fabricate a plurality of FINFETs according to an embodiment, showing various stages of fabrication, and FIG. 2I shows a perspective view of the plurality of the FINFETs fabricated using the steps shown in FIG. 2A-H. It is understood that part of the FINFETs **200** may be fabricated with normal complementary metal-oxide-semiconductor (CMOS) technology processes, and thus some processes are briefly described herein. Also, FIGS. 2A-H are simplified for a better understanding of the inventive concepts of the present disclosure. For example, although the figures illustrate the FINFET **200**, it is understood the ICs may also include a number of various devices including resistors, capacitors, inductors, fuses, etc.

[0014] Referring to FIG. 2A, the FINFETs **200** may include a semiconductor substrate **202** such as a silicon substrate. In some embodiments, the substrate **202** may alternatively include silicon germanium, gallium arsenic, or other suitable semiconductor materials. The substrate **202** may further include other features such as various doped regions, a buried layer, and/or an epitaxy layer. Furthermore, the substrate **202** may be a semiconductor on insulator such as silicon on insulator (SOI). In other embodiments, the semiconductor substrate **202** may include a doped epi layer, a gradient semiconductor layer, and/or may further include a semiconductor layer overlying another semiconductor layer of a different type such as a silicon layer on a silicon germanium layer. In other examples, a compound semiconductor substrate **202** may include a multilayer silicon structure or a silicon substrate **202** may include a multilayer compound semiconductor structure.

[0015] Still referring to FIG. 2A, a pad oxide layer **204** is formed over the top surface of the substrate **202**. In some embodiments, the pad oxide layer **204** is preferably formed of silicon oxide grown by a thermal oxidation process, having a thickness of about 80 to 150 Å. For example, the pad oxide layer **204** can be grown by the rapid thermal oxidation (RTO) process or in an annealing process, which include oxygen. A hardmask layer **206**, for example a silicon nitride or silicon oxynitride layer, is formed over the pad oxide layer **204**. The hardmask layer **206** can be deposited by, for example, a chemical vapor deposition (CVD) process, or a low pressure CVD (LPCVD) process. Preferably, in some embodiments, the formed hardmask layer **206** has a thickness of about 600 to 1500 Å.

[0016] Referring to FIG. 2B, following formation of the hardmask layer **206**, a patterned photo-sensitive layer (not shown) is formed on the hardmask layer **206**. A reactive ion etching (RIE) or a high density plasma (HDP) process may, for example, be used to anisotropically etch through the hardmask layer **206** and the pad oxide layer **204** to form openings **208** in the hardmask layer **206** and the pad oxide layer **204**, exposing a portion of the substrate **202**.

[0017] Referring to FIG. 2C, upper portions **210a** of a plurality of fin structures **210** protruding from the major surface **202a** of the substrate **202** may be formed by etching the substrate **202** using a first etch process. For example, the first etch process may be performed under a source power of about 550 to 650 W, a bias power of about 55 to 65 W, and a pressure of about 2 to 10 mTorr, using CH₂F₂, SF₆, N₂, and He as etching gases. The substrate **202** comprises a major surface **202a** parallel to a substrate surface **202b**. The upper portion **210a** of each fin structure **210** has sidewalls that are substantially perpendicular to the major surface **202a** of the substrate **202** and a top surface **210c**.

[0018] Referring to FIG. 2D, lower portions **210b** of the plurality of fin structures **210** protruding from the major surface **202a** of the substrate **202** may be formed by further etching the substrate **202** using a second etch process. For example, the second etch process may be performed under a source power of about 1100 to 1250 W, a bias power of about 200 to 220 W, and a pressure of about 10 to 20 mTorr, using HBr, SF₆, and He as etching gases. The upper portion **210a** and the lower portion **210b** of each fin structure **210** are separated at a transition location **210d** at, in some embodiments, where the sidewall of the fin structure at an angle **212** of 85 degrees to the major surface **202a** of the substrate **202**. The lower portion **210b** of each fin structure **210** has tapered

sidewalls on opposite sides of the upper portion **210a** and a base **210e**. In some embodiments, the tapered regions of the lower portion **210b** of each fin structure **210** is preferably at an angle **214** in the range of 60 degrees to 85 degrees to the major surface **202a** of the substrate **202**. In one embodiment, a plurality of trenches **222** formed between the tapered fin structures **210** have lower aspect ratio than the plurality of trenches **122** formed between the vertical fin structures **110**. The lower aspect-ratio trenches **222** have better gap-fill performance than the higher aspect-ratio trenches **122**.

[0019] Still referring to FIG. 2D, the top surface **210c** of the upper portion **210a** of each fin structure **210** having a first width **216a**, the first width **216a** is in the range of about 5 to 40 nanometers. In one embodiment, the base **210e** of the lower portion **210b** of each fin structure **210** having a second width **218a**, the second width **218a** is in the range of about 10 to 60 nanometers. In some embodiments, a ratio of the first width **216a** to the second width **218a** is preferably from 0.3 to 0.5.

[0020] Still referring to FIG. 2D, in some embodiments, a first offset distance **216b** between the transition location **210d** and the top surface **210c** is in the range of about 40 to 100 nanometers. In some embodiments, a second offset distance **218b** between the base **210e** and the top surface **210c** is in the range of about 100 to 300 nanometers. A ratio of the first offset distance **216b** between the transition location **210d** and the top surface **210c** to the second offset distance **218b** between the base **210e** and the top surface **210c**, in some embodiments, is preferably from 0.15 to 0.3.

[0021] Referring to FIG. 2E, following formation of the plurality of the fin structures **210**, the plurality of the isolation structures **220** between the fin structures **210** may be formed in the plurality of the trenches **222**. In some embodiments, a liner layer (not shown) may be formed substantially conformal over the substrate **202**, including along the sidewalls of the plurality of the trenches **222**. The liner layer is a dielectric layer (e.g., an oxide layer, nitride layer, oxynitride layer or combination thereof) formed by a thermal oxidation process or CVD process. Preferably, the liner layer may have a thickness of about 30 to 200 Å. In some embodiments, the liner layer is provided for reducing damage on the surface of the fin structures **210** created by the trench-etch process as set forth above. In some embodiments, the liner layer is not used.

[0022] Still referring to FIG. 2E, following formation of the liner layer, a dielectric material **224** is formed over the liner layer to a sufficient thickness within and above the plurality of the trenches **222**. For example, the dielectric material **224** is preferably deposited to a thickness from the base **210e** of 4000 to 8000 Å. In one embodiment, the dielectric material **224** can be formed using a CVD process, such as HDP CVD process or sub-atmospheric CVD (SACVD) process. For example, the dielectric material **224** comprises HDP-CVD oxide layer. The dielectric material **224** can be deposited under a low frequency power less than 5000 W, a high frequency power less than 3500 W, a pressure less than 10 mTorr and a temperature of about 500 to 1000° C., using silane and oxygen as reacting precursors. For another example, the dielectric material **224** comprises a sub-atmospheric undoped-silicon glass (SAUSG) layer. The dielectric material **224** can be deposited under a pressure of about 500 to 700 torr and a temperature of about 500 to 600° C., using tetraethoxysilane (TEOS) and O₃ as reacting precursors. The dielectric

material 224 may comprise a plurality of shallow slims/recesses 226a due to reduced aspect ratio of the plurality of trenches 222.

[0023] Still referring to FIG. 2E, following formation of the dielectric material 224 within and above the plurality of trenches 222, an annealing process is performed to increase the density of the dielectric material 224. This results in an interface between the liner layer and the dielectric material 224 that will disappear after the anneal process. The anneal process can be performed, for example, in a furnace, a rapid thermal process (RTP) system or other thermal system that is adapted to provide a thermal treatment for the dielectric material 224 to obtain a desired film quality. In some embodiments, the annealing process may be performed at about 1000° C. for about 20 seconds in a RTP system in an environment containing nitrogen, an inert gas or other gas that will not substantially react with the dielectric material 224.

[0024] FIG. 2F shows the substrate 202 of FIG. 2E after a planarization process, such as a chemical mechanical polishing (CMP) process, is performed to remove portions of the dielectric material 224 above the hardmask layer 206 to expose the hardmask layer 206, thereby leaving the dielectric material 224 filling the trenches 222. The hardmask layer 206 also serves as a stop layer for stopping the planarization process on the hardmask layer 206. In some embodiments, a top surface of the dielectric material 224 is or substantially coplanar with the hardmask layer 206. The plurality of the shallow slims 226b of the dielectric material 224 after the planarization process may become even shallower in depth and broader in width than the plurality of shallow slims 226a of the dielectric material 224 before the planarization process.

[0025] Referring to FIG. 2G, after the planarization process, the hardmask layer 206 has been removed by a wet chemical etching process, for example, by dipping the substrate 202 in hot phosphoric acid (H₃PO₄), exposing a top surface of the pad oxide layer 204. Because the wet chemical etching process has higher etch selectivity for nitride than to oxide, the etch process removes the hardmask layer 206 faster than the dielectric material 224. Accordingly, the remaining dielectric material 224 extends over a top surface of the pad oxide layer 204. Subsequent to the hardmask layer 206 removal process, the pad oxide layer 204 has been removed by a wet etching process, for example, by dipping the substrate 202 in hydrofluoric (HF), exposing the top surface of the substrate 202. Since the wet chemical etching process has almost no selectivity for the pad oxide layer 204 and the dielectric material 224, the dielectric material 224 may lose almost the same thickness as the pad oxide layer 204 does. Accordingly, the dielectric material 224 still protrudes over the top surface 210c of each fin structure 210 and each shallow slim 226c in the dielectric material 224 almost disappear.

[0026] FIG. 2H shows the substrate 202 of FIG. 2G after a dry etching process, for example, by etching the substrate 202 in a plasma comprising tetrafluoromethane (CF₄) and trifluoromethane (CHF₃), is performed to remove upper portions of the dielectric material 224 to expose the upper portion 210a of each fin structure 210. The fin structure could also form part of other devices, such as resistors, capacitors, inductors, fuses, etc. Accordingly, at the end of the etching process, the dielectric material 224 made has almost no recess and serves as the isolation structures 220 between the semiconductor devices. Each isolation structure 220 extends from the substrate surface 202a to a point 224a above the transition location 201d. A third offset distance 216c between the point 224a

of the isolation structure 220 and the top surface 210c should be well controlled. If the third offset distance 216c between the point 224a of the isolation structure 220 and the top surface 210c is too small, shallow slims/recesses may still remain on the point 224a of the isolation structure 220. If the third offset distance 216c between the point 224a of the isolation structure 220 and the top surface 210c is too large, short channel effects may degrade device performance. Accordingly, in some embodiments, the third offset distance 216c between the point 224a of the isolation structure 220 and the top surface 210c is preferably in the range of about 15 to 45 nanometers. In some embodiments, the ratio of the third offset distance 216c between the point 224a of the isolation structure 220 and the top surface 210c to the first offset distance 216b between the transition location 210d and the top surface 210c is preferably from 0.3 to 0.6. FIG. 2I shows a perspective view of the FINFETs 200 fabricated using the steps shown in FIG. 2A-H. Each fin structure 210 extends in a longitudinal direction 210g. As previously described the isolation structure 220 in FIG. 2I has no recesses.

[0027] FIG. 3A-D shows a complete FINFET device 300 having a plurality of isolation structures 220 fabricated using the steps shown in FIG. 2A-H, wherein FIG. 3A shows a perspective view, and wherein FIGS. 3B-D show cross-sectional views taken along the respective lines of FIG. 3A. Similar features in FIGS. 2 and 3 are numbered the same for the sake of simplicity and clarity.

[0028] Referring to FIG. 3A, the FINFET 300 includes the plurality of fin structures 210 separated by the plurality of isolation structures 220. Each fin structure 210 extends in a longitudinal direction 210g. A gate structure 320 comprising a gate electrode 320a and a gate insulator 310b is disposed over the fin structures 210. FIG. 3A also illustrates the source/drain regions 330a, 330b of the FINFET 300.

[0029] FIG. 3B illustrates a cross-sectional view of the FINFET 300 taken along the line b-b of FIG. 3A. Each fin structure 210 extending in a longitudinal direction 210g comprises an upper portion 210a and a lower portion 210b separated at a transition location 210d at where the sidewall of the fin structure 210 at an angle of 85 degrees to the major surface 202a of the substrate 202, the upper portion 210a has sidewalls that are substantially perpendicular to the major surface 202a of the substrate 202 and a top surface 210c, the upper portion 210a comprises a first longitudinal portion 210ga, a second longitudinal portion 210gb, and a third longitudinal portion 210gc disposed between the first and the second longitudinal portions 210ga, 210gb. A channel region 330 is defined within the third longitudinal portion 210gc of the upper portion 210a. A gate structure 320 comprising a gate electrode 320a and a gate insulator 310b may be disposed over the channel region 330. A silicide layer (not shown) may be disposed within the first and the second longitudinal portions 210ga, 210gb form source/drain regions in the FINFET 300. The lower portion 210b under the upper portion 210a has a base 210e and bottom-up tapered sidewalls.

[0030] Referring to the cross sectional view of FIG. 3C taken along the line c-c of FIG. 3A, the gate structure 320 comprises the gate electrode 320a and the gate insulator 320b. The gate electrode 320a is disposed over the gate insulator 320b. If the thickness of the gate insulator 320b is uniform on all the surfaces of the fin structures 210, a triple gate transistor is formed. The channel 330 of the triple gate transistor is disposed under the gate structure 320 and within

the top surface 210c and sidewalls of the third longitudinal portion 210gc of the upper portion 210a of the fin structures 210. However, in some embodiments, an additional dielectric layer (not shown) may be formed over the top surface 210c of the third longitudinal portion 210gc of the upper portion 210a before or after forming the gate insulator 310, the channel 330 of the FINFET 300 is formed only along the sidewalls of the third longitudinal portion 210gc, forming a double gate transistor.

[0031] FIG. 3D illustrates a cross-sectional view of the FINFET 300 taken along the line d-d of FIG. 3A. The fin structures 210 disposed between the isolation structures 220 are extending in a longitudinal direction 210g and continuous pieces of the underlying substrate 202. In some embodiments, the fin structures 210 may be separated from the substrate 202 by an insulation layer (not shown). In some embodiments, the first and the second longitudinal portions 210ga, 219gb of the upper portion 210a of the fin structures 210 comprise dopant-rich regions (not shown), and a silicide layer (not shown) may be disposed within the first and the second longitudinal portions 210ga, 219gb forming source/drain regions in the FINFET 300. In various embodiments, the thickness of the dopant-rich regions is about 0.5 nm to about 10 nm. Then, subsequent processes, including interconnect processing, must be performed after forming the FINFET 300 to complete the IC fabrication.

[0032] While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements. The invention can be used to form or fabricate a fin structure for a FINFET having no isolation recess.

What is claimed is:

- 1. A semiconductor device comprising:
 - a substrate comprising a major surface;
 - a plurality of fin structures protruding from the major surface of the substrate, wherein each fin structure comprises an upper portion and a lower portion separated at a transition location at where at least one of sidewalls of the fin structure is at an angle of 85 degrees to the major surface of the substrate, wherein the upper portion has a top surface having a first width, and the lower portions of adjacent fin structures define a base, the bases defined by each fin structure are separated by a second width larger than the first width; and
 - a plurality of isolation structures between the fin structures, wherein each isolation structure extends from the major surface of the substrate to a point above the transition location.
- 2. The semiconductor device of claim 1, wherein the substrate comprises silicon or germanium or gallium arsenic.
- 3. The semiconductor device of claim 1, wherein the first width is in the range of about 5 to 40 nanometers.
- 4. The semiconductor device of claim 1, wherein the second width is in the range of about 10 to 60 nanometers.
- 5. The semiconductor device of claim 1, wherein a ratio of the first width to the second width is from 0.3 to 0.5.
- 6. The semiconductor device of claim 1, wherein a first distance between the transition location and the top surface is in the range of about 40 to 100 nanometers.

7. The semiconductor device of claim 1, wherein a second distance between the base and the top surface is in the range of about 100 to 300 nanometers.

8. The semiconductor device of claim 1, wherein a ratio of a first distance between the transition location and the top surface to a second distance between the base and the top surface is from 0.15 to 0.3.

9. The semiconductor device of claim 1, a third distance between the point and the top surface is in the range of about 15 to 45 nanometers.

10. The semiconductor device of claim 1, wherein the ratio of a third distance between the point and the top surface to a first distance between the transition location and the top surface is from 0.3 to 0.6.

11. A fin field effect transistor comprising:

- a substrate comprising a major surface;
- a fin structure protruding from the major surface of the substrate and extending in a longitudinal direction, wherein the fin structure comprises a cross-section perpendicular to the longitudinal direction, wherein the cross-section comprises an upper portion and a lower portion separated at a transition location at where at least one of sidewalls of the fin structure is at an angle of 85 degrees to the major surface of the substrate, wherein the upper portion has a top surface having a first width, and the lower portion has two bases on each side of the fin structure defining a second width larger than the first width; wherein the upper portion comprises a first longitudinal portion, a second longitudinal portion, and a third longitudinal portion disposed between the first and the second longitudinal portions;
- a channel region disposed within the third longitudinal portion of the upper portion;
- a gate structure disposed over the channel region;
- a silicide layer disposed within the first and the second longitudinal portions forming source/drain regions; and
- an isolation structure surrounding the fin structures, wherein the isolation structure extends from the major surface of the substrate to a point above the transition location.

12. The fin field effect transistor of claim 11, wherein the fin structure comprises silicon or germanium or gallium arsenic.

13. The fin field effect transistor of claim 11, wherein the first width is in the range of about 5 to 40 nanometers.

14. The fin field effect transistor of claim 11, wherein the second width is in the range of about 10 to 60 nanometers.

15. The fin field effect transistor of claim 11, wherein a ratio of the first width to the second width is from 0.3 to 0.5.

16. The fin field effect transistor of claim 11, wherein a first distance between the transition location and the top surface is in the range of about 40 to 100 nanometers.

17. The fin field effect transistor of claim 11, wherein a second distance between the base and the top surface is in the range of about 100 to 300 nanometers.

18. The fin field effect transistor of claim 11, wherein a ratio of a first distance between the transition location and the top surface to a second distance between the base and the top surface is from 0.15 to 0.3.

19. The fin structure of claim 11, a third distance between the point and the top surface is in the range of about 15 to 45 nanometers.

20. The fin structure of claim 11, wherein the ratio of a third distance between the point and the top surface to a first distance between the transition location and the top surface is from 0.3 to 0.6.