Fabrication of Body-Tied FinFETs (Omega MOSFETs) Using Bulk Si Wafers

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Abstract

Nano scale body-tied FinFETs have been firstly fabricated. They have fin top width of 30 nm, fin bottom width of 61 nm, fin height of 99 nm, and gate length of 60 nm. This Omega MOSFET shows excellent transistor characteristics, such as very low subthreshold swing, Drain Induced Barrier Lowering (DIBL) of 24 mV/V, almost no body bias effect, and orders of magnitude lower I_{SUB}/I_D than planar type DRAM cell transistors.

Keywords: FinFET, omega, MOSFET, bulk, DIBL, SCE

Introduction

FinFETs have been on focus among the double-gate transistors because of the compatibility with the conventional device manufacturing process. So far, FinFETs have been demonstrated on SOI substrates (e.g., [1] and [2]) to overcome problems associated with Short Channel Effect (SCE). However, heat transfer problem and high wafer cost necessitate the device development on conventional bulk Si wafers.

In this work, we propose a new body-tied FinFET based on bulk Si wafers, and report the fabrication procedure and the physical and electrical characteristics of this device. Because the body shape resembles Greek letter Omega (Ω), we call the device Omega MOSFET [3].

Experimental

A 3-dimensional view of the Ω MOSFET schematic is shown in Fig. 1. The fin body is directly connected to the substrate. Processes to fabricate the device are explained briefly as follows.

On p-type (100) wafers, an anti-reflective layer and a photo resist were coated, and a 120 nm design-ruled KrF photo-lithography step was performed to define active regions. Trenches were etched with the depth of 300 nm. After removing the anti-reflective layer and the photo resist, a thermal oxidation with the thickness of 35 nm was carried out. The thermal oxide was completely etched in a diluted HF solution, leaving thin fins standing vertically in which the channel and the S/D are formed.

A thermal oxide with the thickness of 5 nm was grown, a SiN layer was deposited with the thickness of 50 nm, and the remaining of the trenches were filled with HDP CVD SiO_2. CMP was performed until the SiN layer was opened. Top portion of the SiN layer was etched in a phosphoric acid solution, sacrificial oxide was grown, and ion implantation steps for well formation, isolation punchthrough stopping, channel punchthrough stopping, and 2 times of channel threshold voltage adjustment were performed.

The SiN layer was additionally recessed with the depth of 100 nm and fin sidewalls were opened. After removing the thermal SiO_2, 2 nm and 4 nm thicknesses of gate SiO_2 were grown on some of the wafers, respectively. Subsequently, an in-situ phosphorous doped poly-Si (200 nm) and a 180 nm thick SiN mask layer were deposited.

Gate electrodes were patterned also by using the 120 nm design ruled KrF photo-lithography and etching step. Some of the wafers went through a Chemical Dry Etching (CDE) process to trim the gate length down to 60 nm. After P^+ ions for LDD were implanted, 45 nm thick SiN spacer was formed, and also ion implantations were performed to dope source/drain regions.

The rest of the process steps were carried out by using the same processes as for the conventional DRAM fabrication.

Results and Discussion

Fig. 2 shows SEM micrographs taken after the gate poly-Si etching (a) and the final step (b). As shown in Fig. 2 (a), no poly-Si residue was remained at either side of the recessed region. Fig. 2 (b) shows that top corners of the fin were rounded because of the repetitive oxidation and isotropic etching, which lead to the suppression of possible leakage along the side-channel. As shown in Fig. 2 (b), flat top of the gate poly-Si obtained by the narrow SiN region filling helped gate photo-lithography and etching.

Cross-sectional TEM micrographs in Fig. 3 show that process induced defects were not generated.

In Fig. 4, subthreshold swing distribution of the Ω MOSFETs is compared with that of the conventional DRAM cell transistors. It is shown that the Ω MOSFET has much lower values and smaller deviation.

Body bias dependencies of the transistors are compared as shown in Fig. 5. The Ω MOSFET shows very small dependency, whereas the significant one with the conventional DRAM cell transistor at a fixed gate length. It is mainly due to fully depleted fin body by the hetero-junction between the fin body and the oxide.

As shown in Fig. 6, Drain Induced Barrier Lowering (DIBL) of 24 mV/V is obtained with the Ω MOSFET while the conventional DRAM cell transistor shows 108 mV/V.

I_D-V_{DS} characteristics (Fig. 7) show that the Ω MOSFET apparently has flat regions in high V_{DS} whereas the conventional DRAM cell transistor suffers from SCE.

I_{SUB}/I_D characteristics (Fig. 8) illustrate one of the superiorities of the Omega MOSFETs. The Ω MOSFET shows much lower I_{SUB}/I_D than conventional DRAM cell transistor, which is mainly attributed to drain field perturbation by both gates.

Finally, Figs. 9 and 10 demonstrate reasonable I_D-V_{GS} and I_D-V_{DS} characteristics of the Omega MOSFET with the gate oxide thickness of 2 nm and channel length of 60 nm. Top fin width, bottom fin width, and fin height are around 30 nm, 61 nm, and 99 nm, respectively.

Conclusions

World's first body tied FinFETs (Omega MOSFETs) on bulk Si wafer instead of SOI wafer were fabricated and their outstanding device characteristics were demonstrated. By slight modification, the Omega MOSFET is expected to be a promising candidate for the nano era CMOS devices.

Acknowledgment

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References

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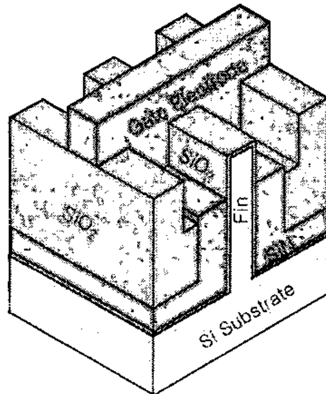
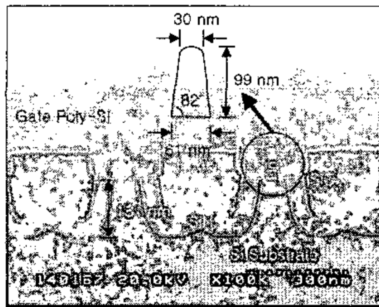


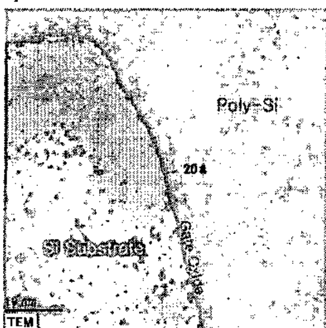
Fig. 1 Bird's eye view of the Ω MOSFET. For effective sidewall opening without field SiO_2 level lowering, SiN liner with the thickness of 50 nm was chosen. This SiN is also used as the stopping layer in STI CMP.

(a) SEM view after gate etch

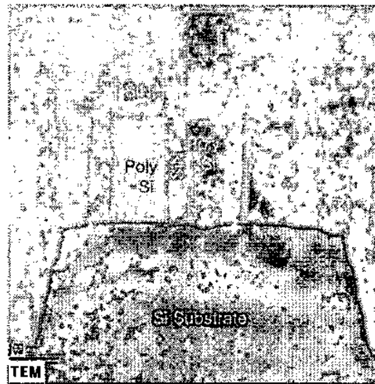


(b) Final SEM view

Fig. 2 Cross-sectional SEM micrographs. No poly-Si residue is observed around the dimples.



(a) Gate oxide at fin edge. To minimize thickness variation depending upon crystallographic orientation, In-Situ Steam Generated (ISSG) radical SiO_2 was grown.



(b) X-section along fin top at the DRAM cell region.

Fig. 3 Cross-sectional TEM micrographs.

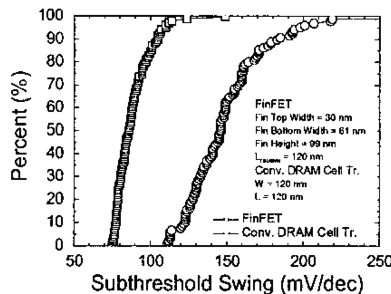


Fig. 4 Comparison of subthreshold swing distributions. L_{DRAWN} = 116 nm, T_{GOX}=4 nm and 5.4 nm for the Ω MOSFET and conventional DRAM Cell Transistors, respectively.

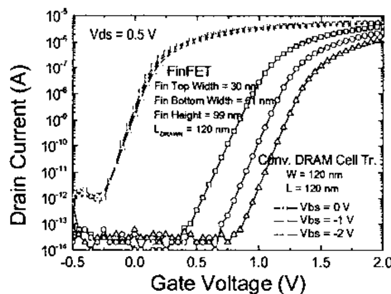


Fig. 5 Comparison of the body bias dependency of the Ω MOSFET with that of the conventional DRAM transistor.

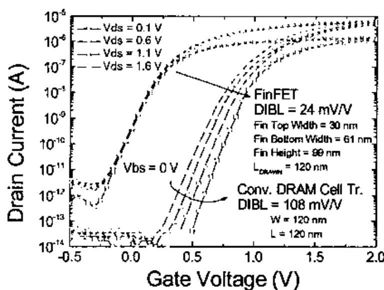


Fig. 6 Drain Induced Barrier Lowering (DIBL) comparison. L_{DRAWN} = 116 nm, T_{GOX}=4 nm and 5.4 nm for the Ω MOSFET and conventional DRAM Cell Transistors, respectively.

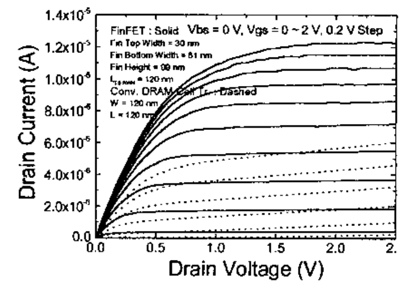


Fig. 7 I_D-V_{DS} comparison. L_{DRAWN} = 116 nm, T_{GOX}=4 nm and 5.4 nm for the Ω MOSFET and conventional DRAM Cell Transistors, respectively.

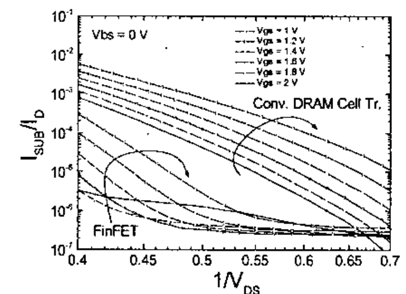


Fig. 8 I_{SUB}/I_D comparison of the Ω MOSFET with the conventional DRAM cell transistor. L_{DRAWN} = 116 nm, T_{GOX}=4 nm and 5.4 nm for the Ω MOSFET and conventional DRAM Cell Transistors, respectively.

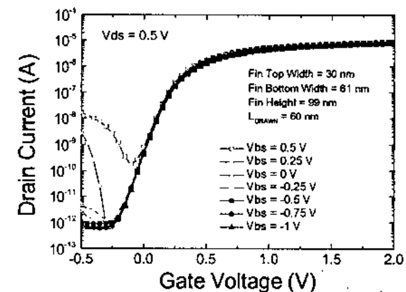


Fig. 9 I_D-V_{GS} characteristics of the Ω MOSFET with the gate oxide thickness of 2 nm and channel length of 60 nm.

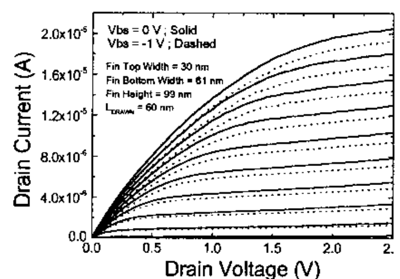


Fig. 10 I_D-V_{DS} characteristics of the Ω MOSFET with the gate oxide thickness of 2 nm and channel length of 60 nm.

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