

# Intel's Revolutionary 22 nm Transistor Technology

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# Key Messages

- Intel is introducing revolutionary Tri-Gate transistors on its 22 nm logic technology
- Tri-Gate transistors provide an unprecedented combination of improved performance and energy efficiency
- 22 nm processors using Tri-Gate transistors, code-named Ivy Bridge, are now demonstrated working in systems
- Intel is on track for 22 nm production in 2H '11, maintaining a 2-year cadence for introducing new technology generations
- This technological breakthrough is the result of Intel's highly coordinated research-development-manufacturing pipeline
- Tri-Gate transistors are an important innovation needed to continue Moore's Law



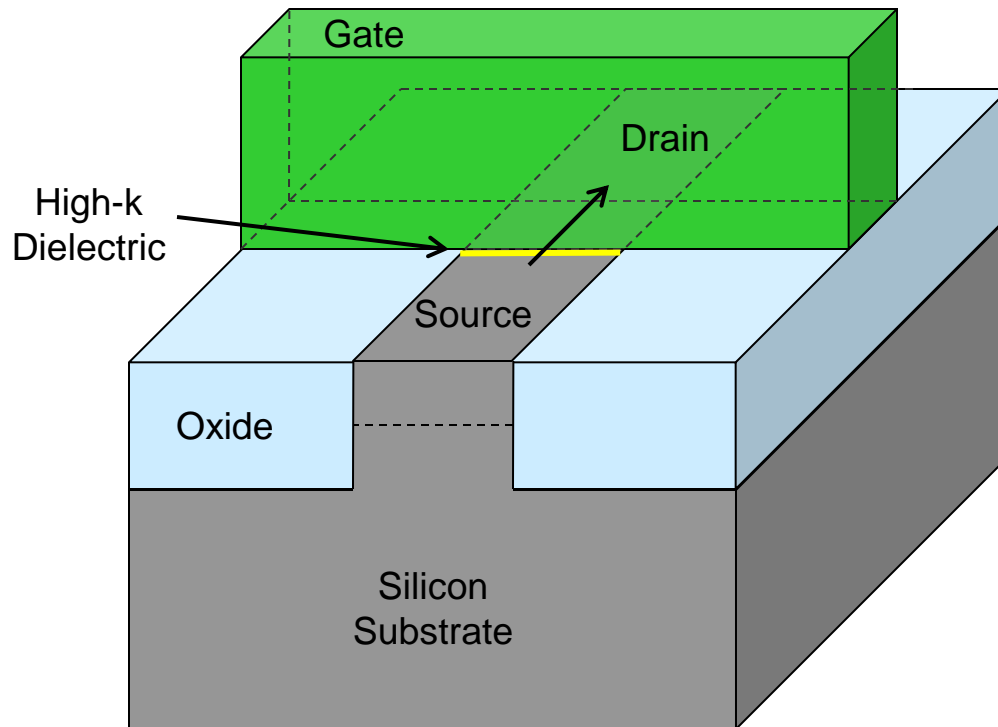
# Intel Technology Roadmap

Process Name	<u>P1266</u>	<u>P1268</u>	<u>P1270</u>	<u>P1272</u>	<u>P1274</u>
Lithography	45 nm	32 nm	22 nm	14 nm	10 nm
1 <sup>st</sup> Production	2007	2009	2011	2013	2015

Intel continues our cadence of introducing a new technology generation every two years

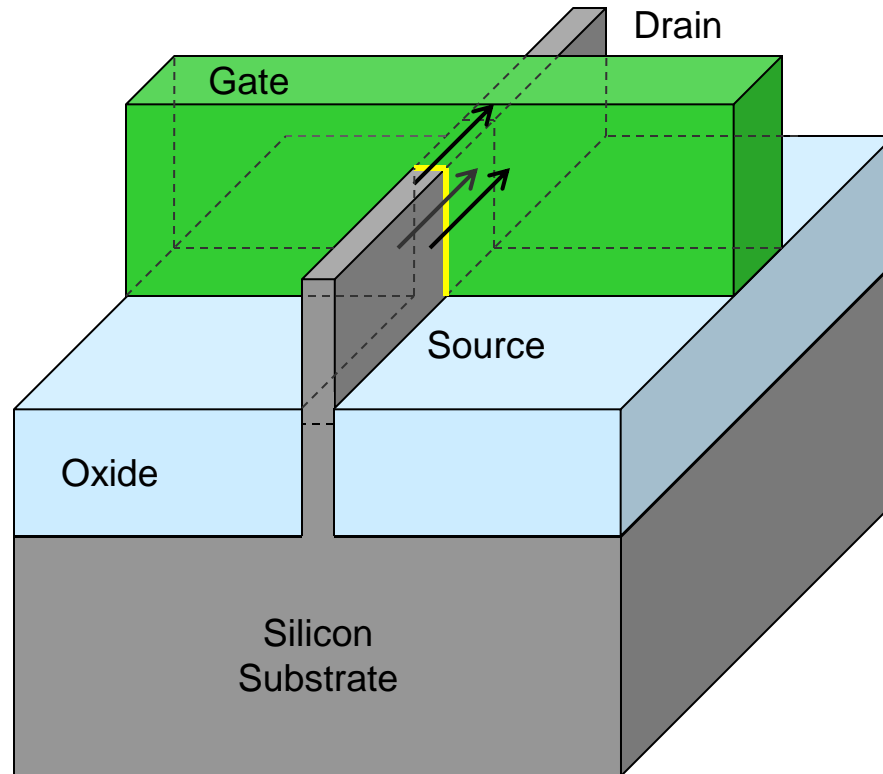


# Traditional Planar Transistor



Traditional 2-D planar transistors form a conducting channel in the silicon region under the gate electrode when in the “on” state

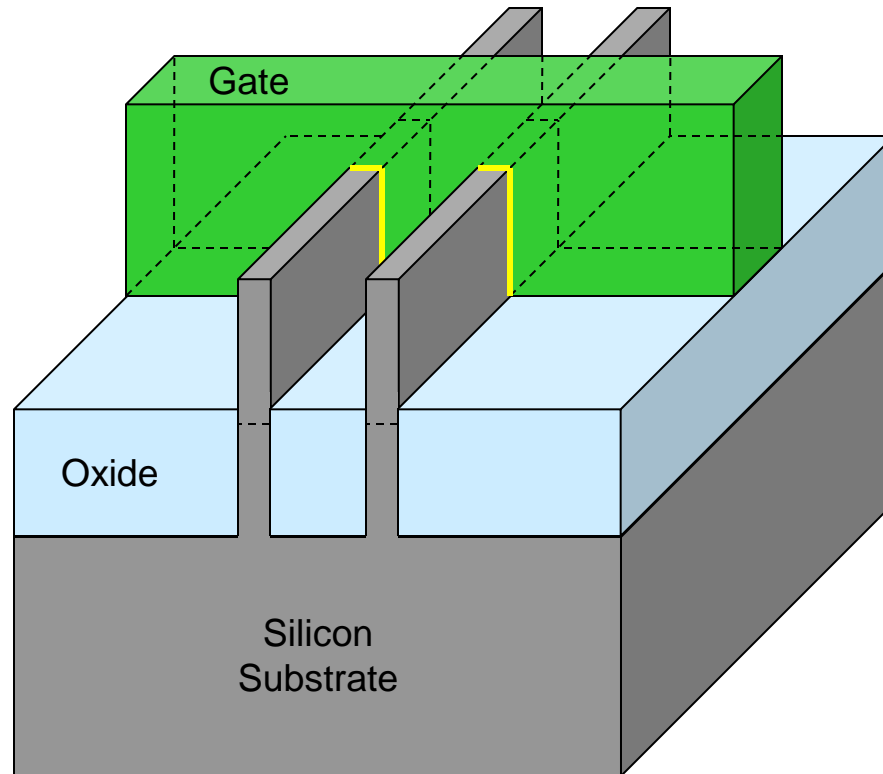
# 22 nm Tri-Gate Transistor



3-D Tri-Gate transistors form conducting channels on three sides of a vertical fin structure, providing “fully depleted” operation

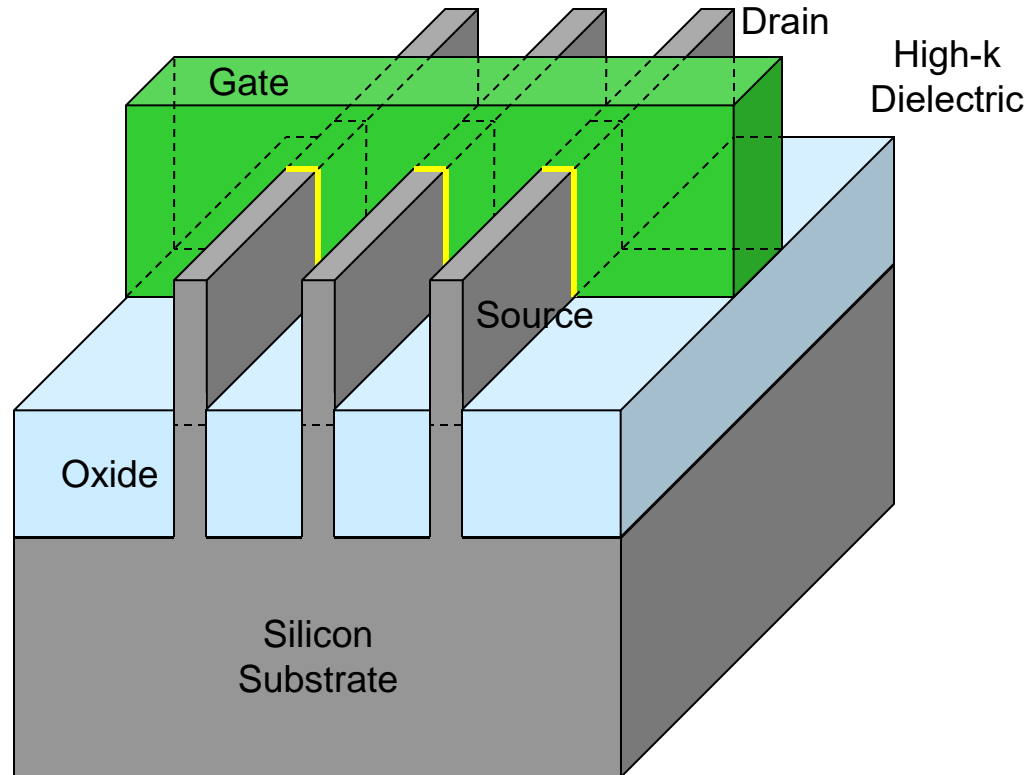
*Transistors have now entered the third dimension!*

# 22 nm Tri-Gate Transistor



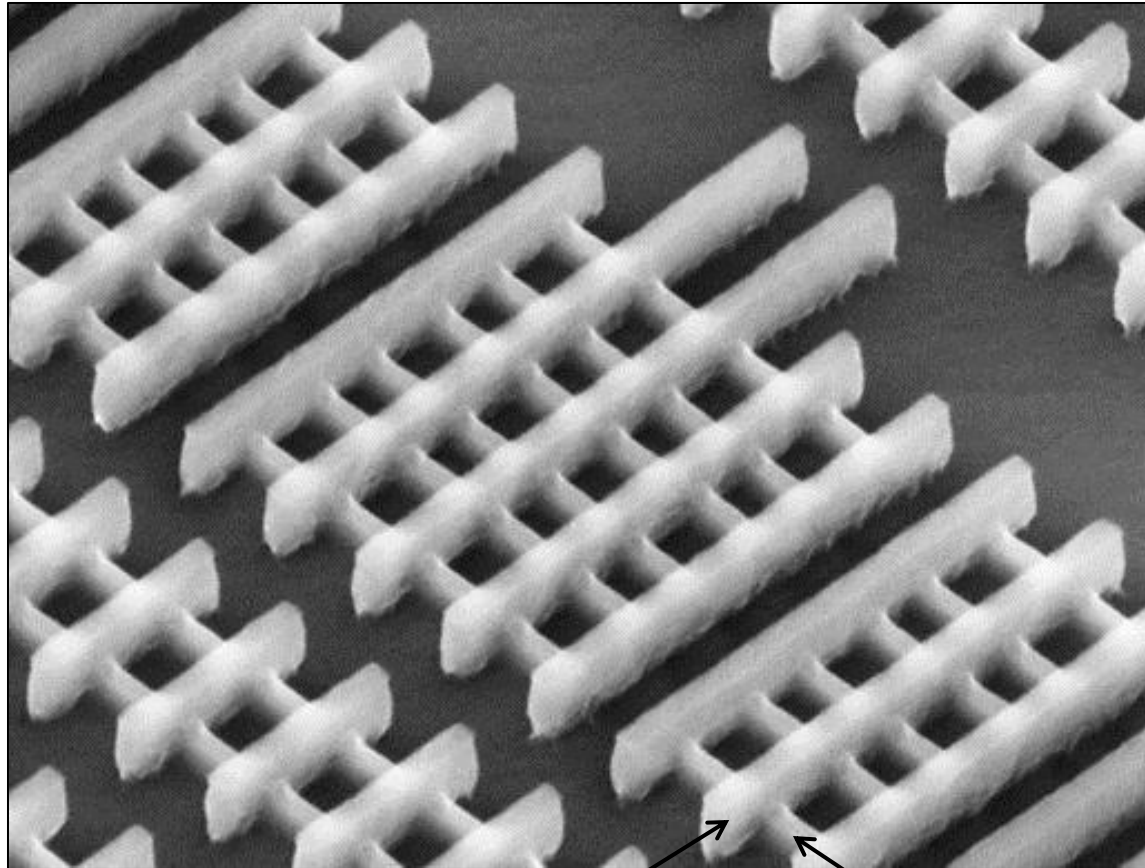
Tri-Gate transistors can have multiple fins connected together to increase total drive strength for higher performance

# 22 nm Tri-Gate Transistor



Tri-Gate transistors can have multiple fins connected together to increase total drive strength for higher performance

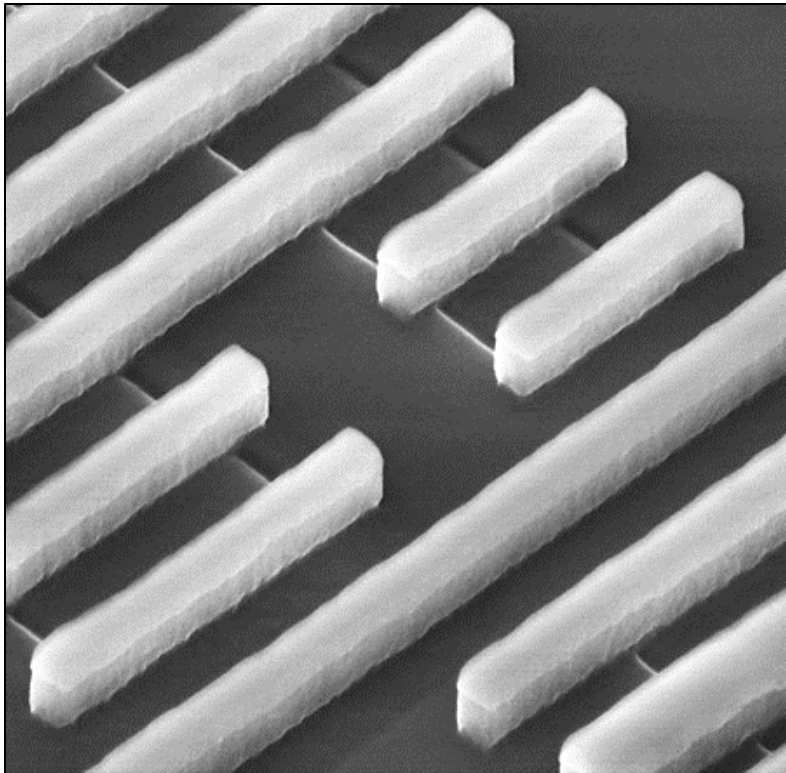
# 22 nm Tri-Gate Transistor



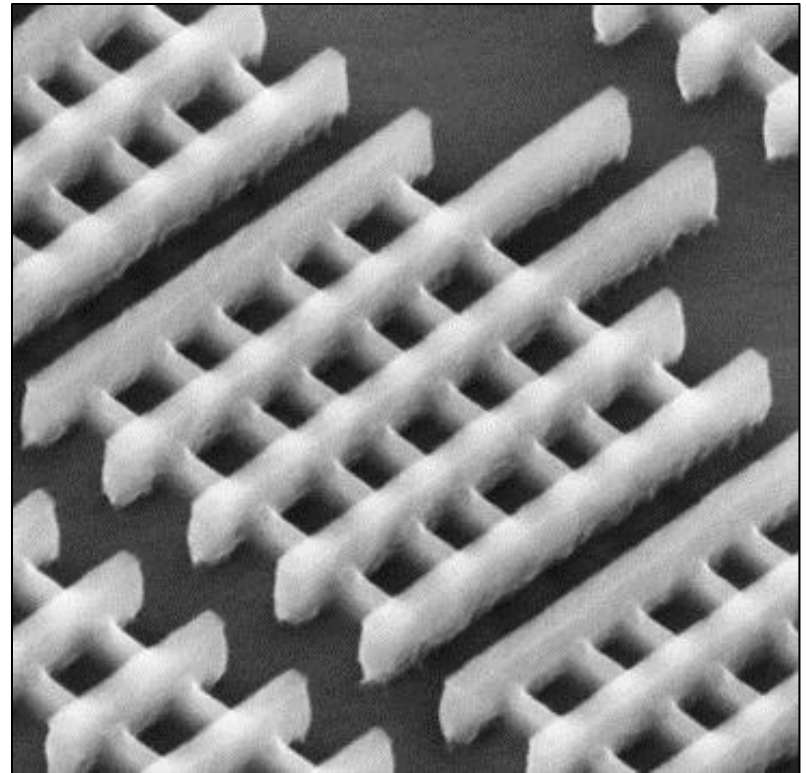
Gates

Fins

## 32 nm Planar Transistors



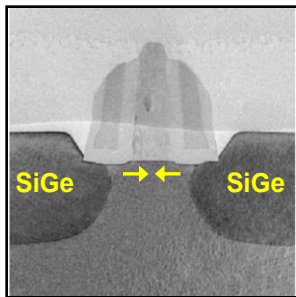
## 22 nm Tri-Gate Transistors



# Intel Transistor Leadership

2003

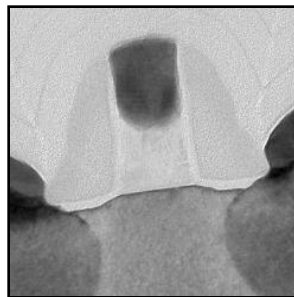
90 nm



Invented  
SiGe  
Strained Silicon

2005

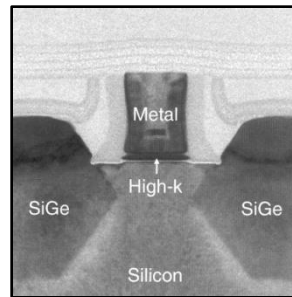
65 nm



2<sup>nd</sup> Gen.  
SiGe  
Strained Silicon

2007

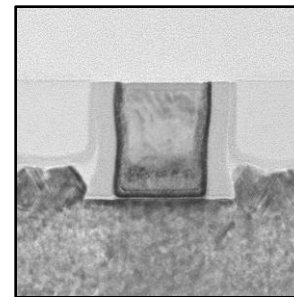
45 nm



Invented  
Gate-Last  
High-k  
Metal Gate

2009

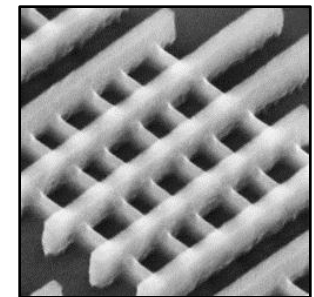
32 nm



2<sup>nd</sup> Gen.  
Gate-Last  
High-k  
Metal Gate

2011

22 nm



First to  
Implement  
Tri-Gate

Strained Silicon

High-k Metal Gate

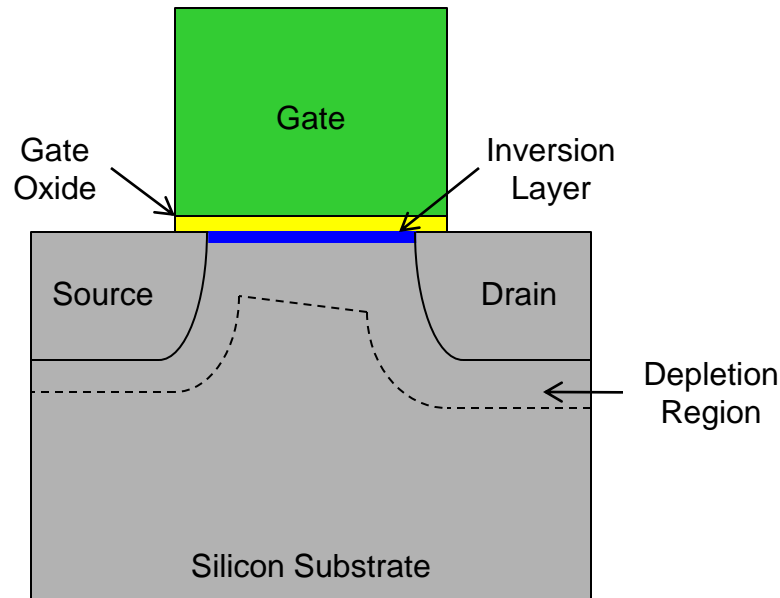
Tri-Gate



# Std vs. Fully Depleted Transistors

“Transistor 101”

## Bulk Transistor



Silicon substrate voltage exerts some electrical influence on the inversion layer (where source-drain current flows)

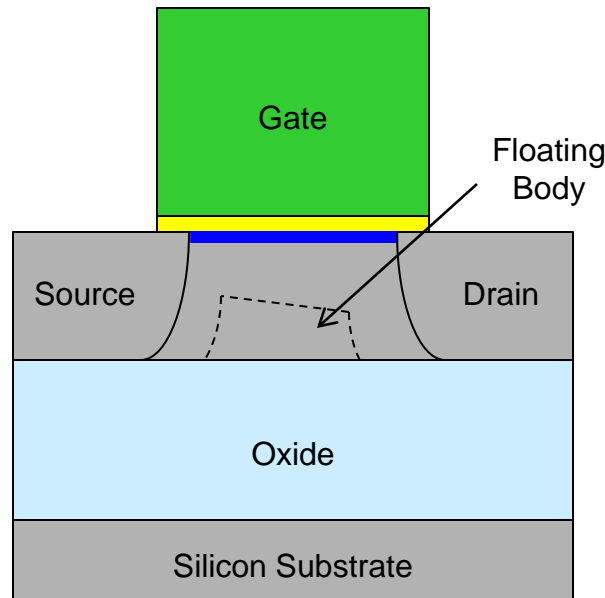
The influence of substrate voltage degrades electrical sub-threshold slope (transistor turn-off characteristics)

NOT fully depleted

# Std vs. Fully Depleted Transistors

## Partially Depleted SOI (PDSOI)

“Transistor 101”



Floating body voltage exerts some electrical influence on the inversion layer, degrading sub-threshold slope

NOT fully depleted

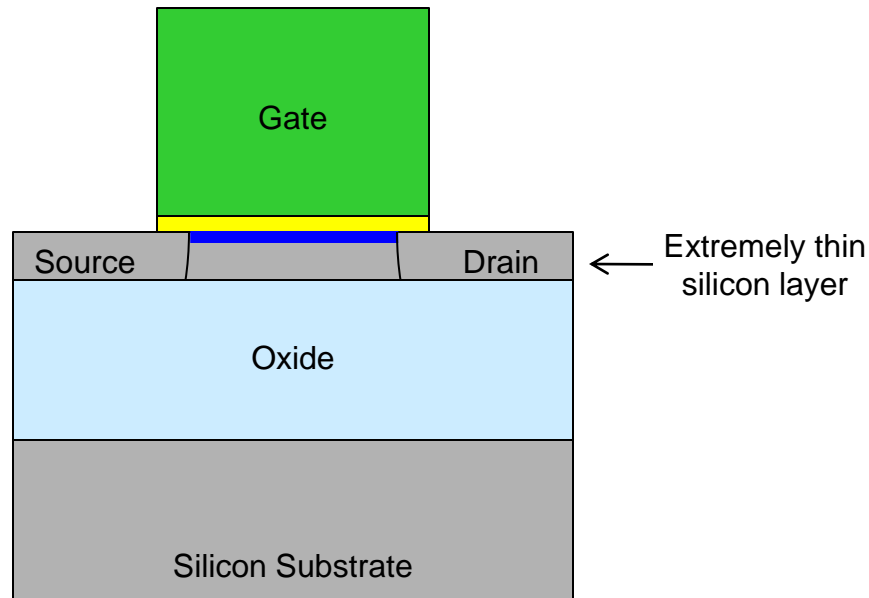
Not used by Intel



# Std vs. Fully Depleted Transistors

## Fully Depleted SOI (FDSOI)

“Transistor 101”



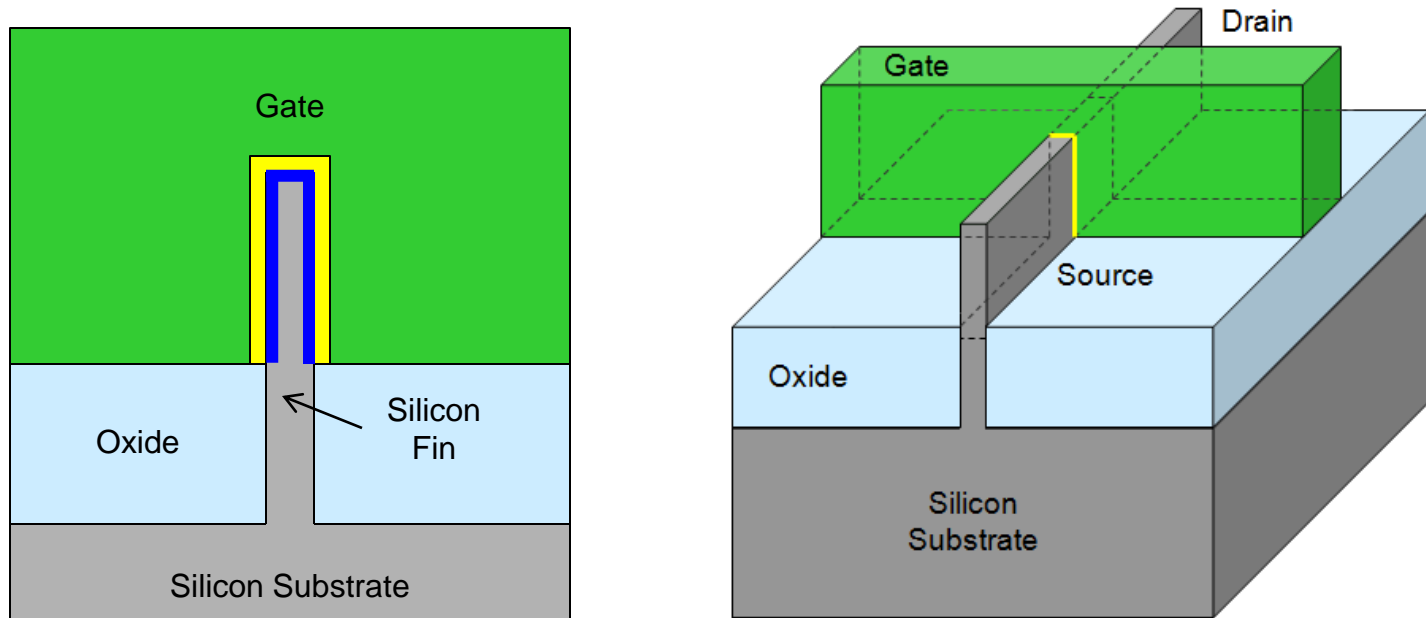
Floating body eliminated and sub-threshold slope improved

Requires expensive extremely-thin SOI wafer,  
which adds ~10% to total process cost

Not used by Intel

# Std vs. Fully Depleted Transistors

## Fully Depleted Tri-Gate Transistor



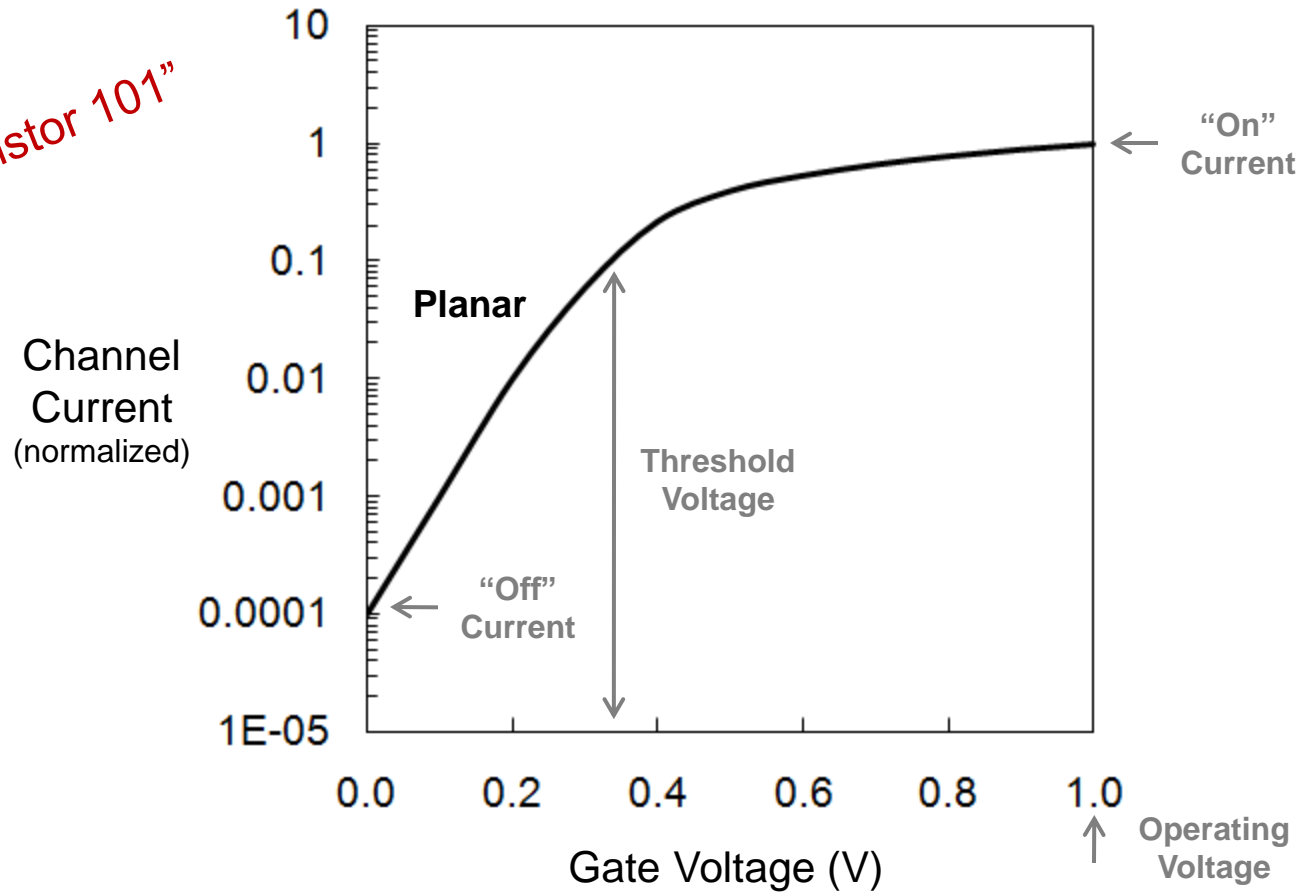
Gate electrode controls silicon fin from three sides  
providing improved sub-threshold slope

Inversion layer area increased for higher drive current

Process cost adder is only 2-3%

# Transistor Operation

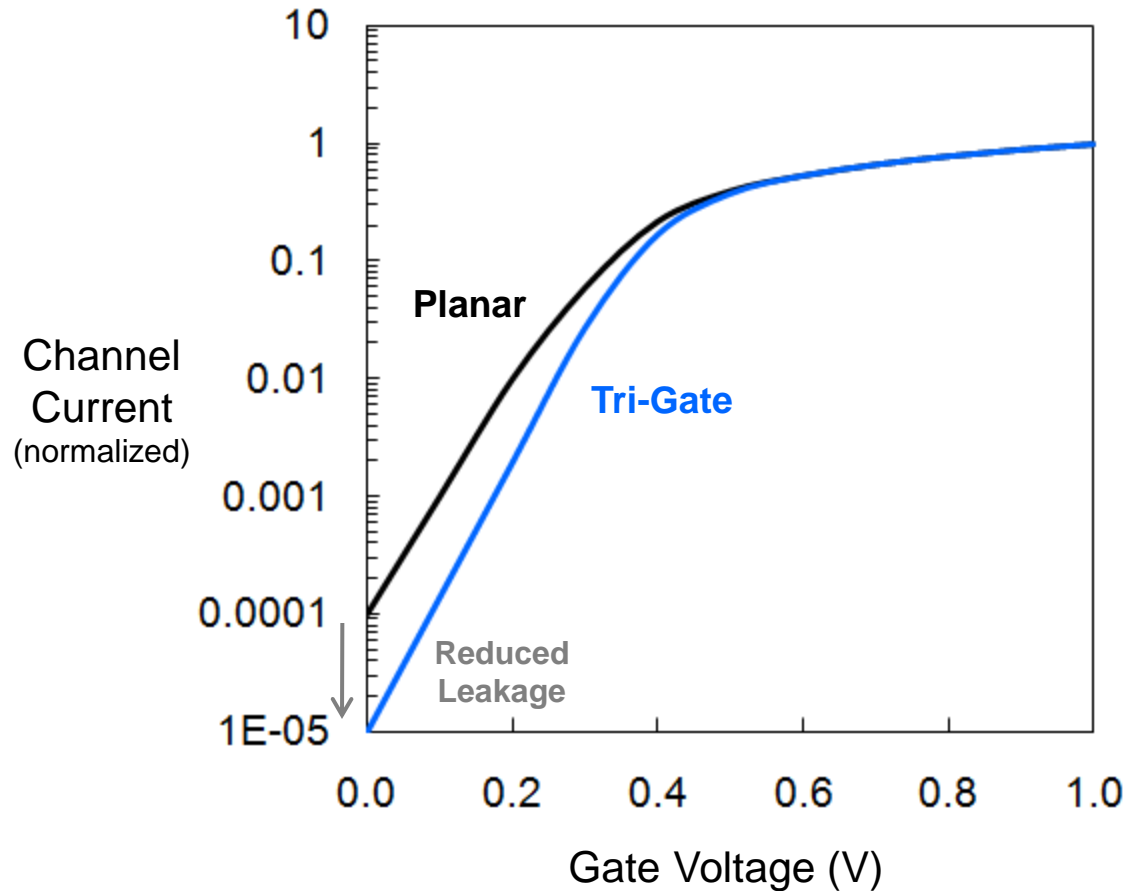
*“Transistor 101”*



Transistor current-voltage characteristics



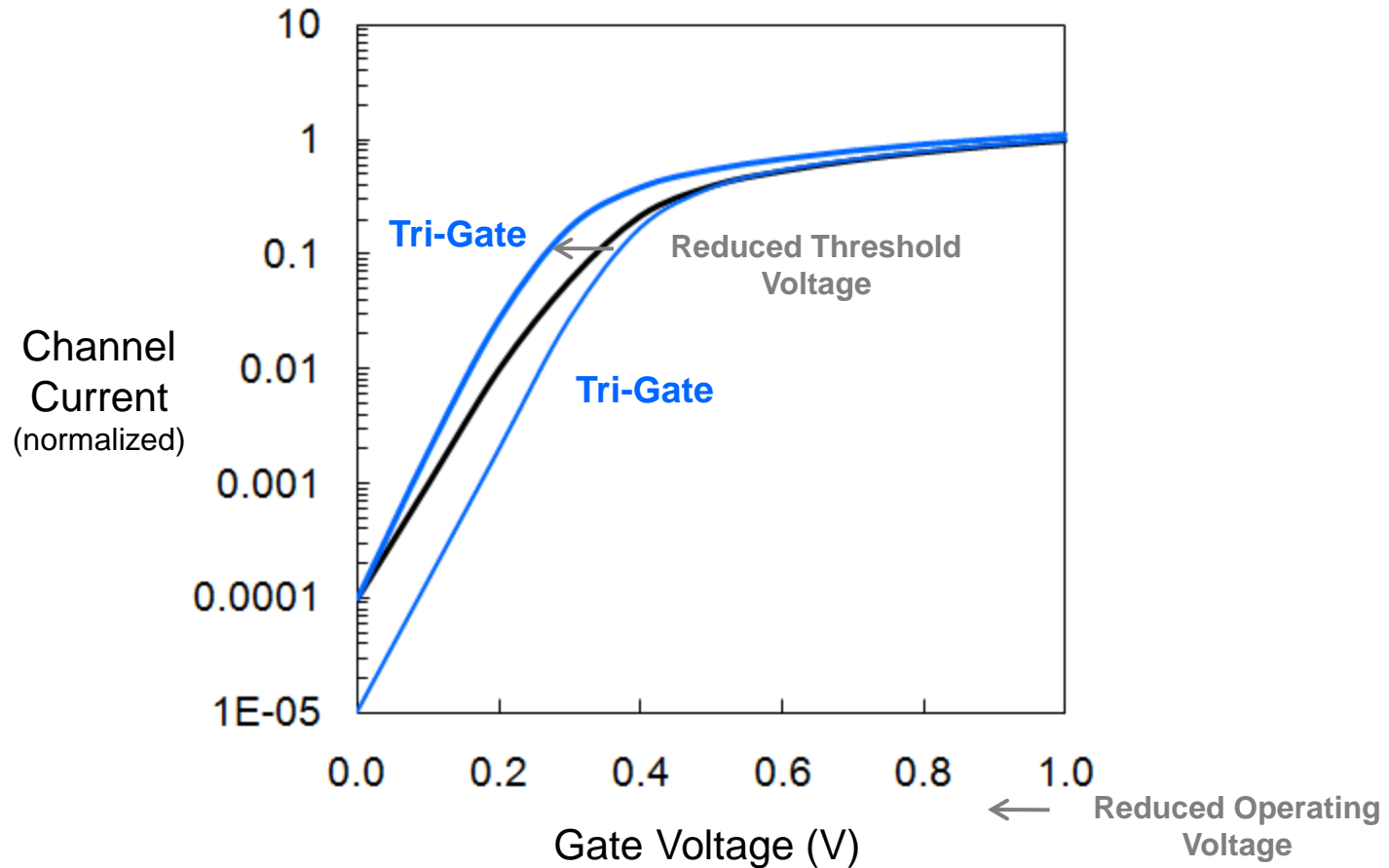
# Transistor Operation



The “fully depleted” characteristics of Tri-Gate transistors provide a steeper sub-threshold slope that reduces leakage current



# Transistor Operation



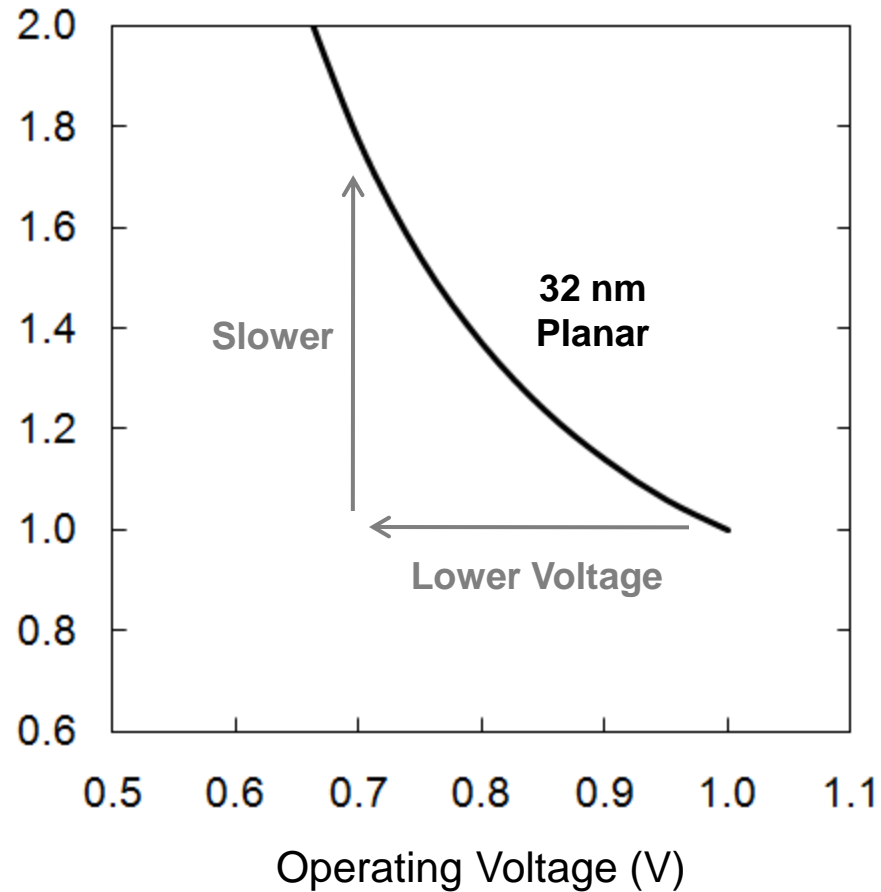
The steeper sub-threshold slope can also be used to target a lower threshold voltage, allowing the transistors to operate at lower voltage to reduce power and/or improve switching speed



# Transistor Gate Delay

*“Transistor 101”*

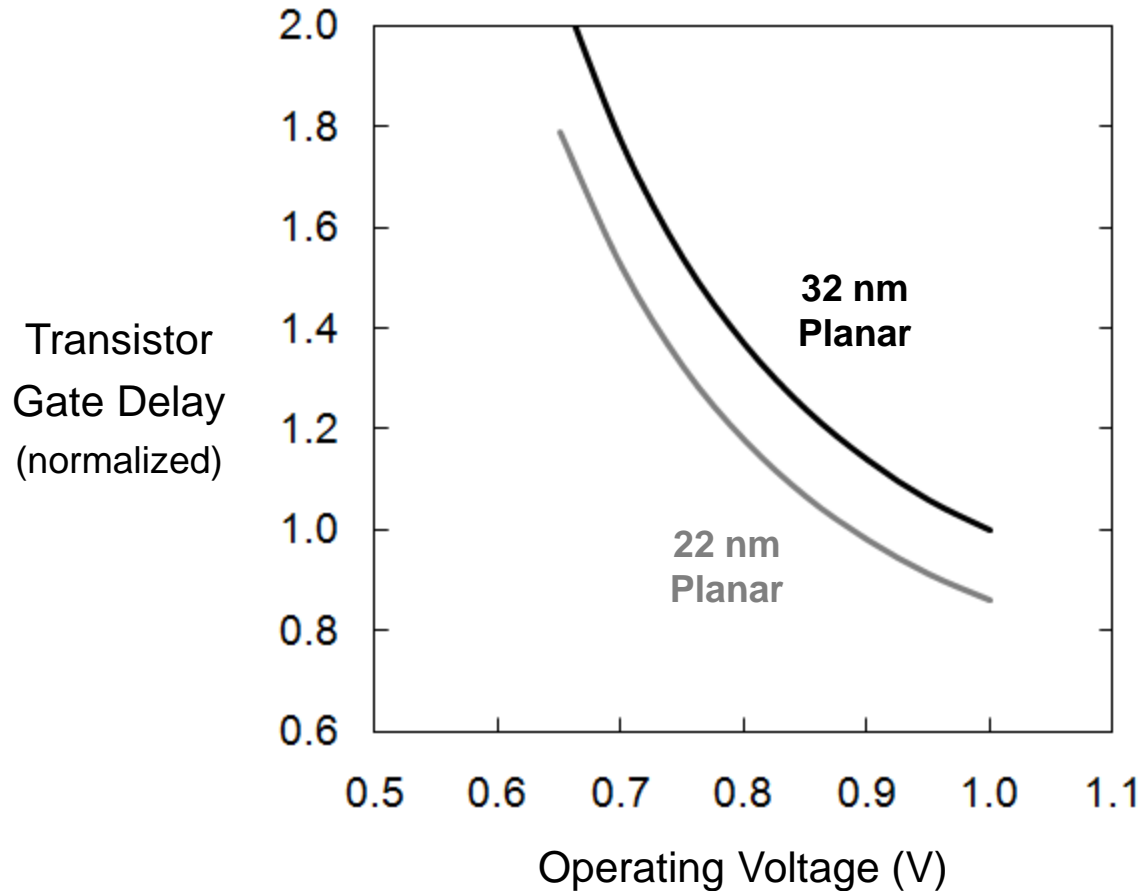
Transistor  
Gate Delay  
(normalized)



Transistor gate delay (switching speed) slows down  
as operating voltage is reduced



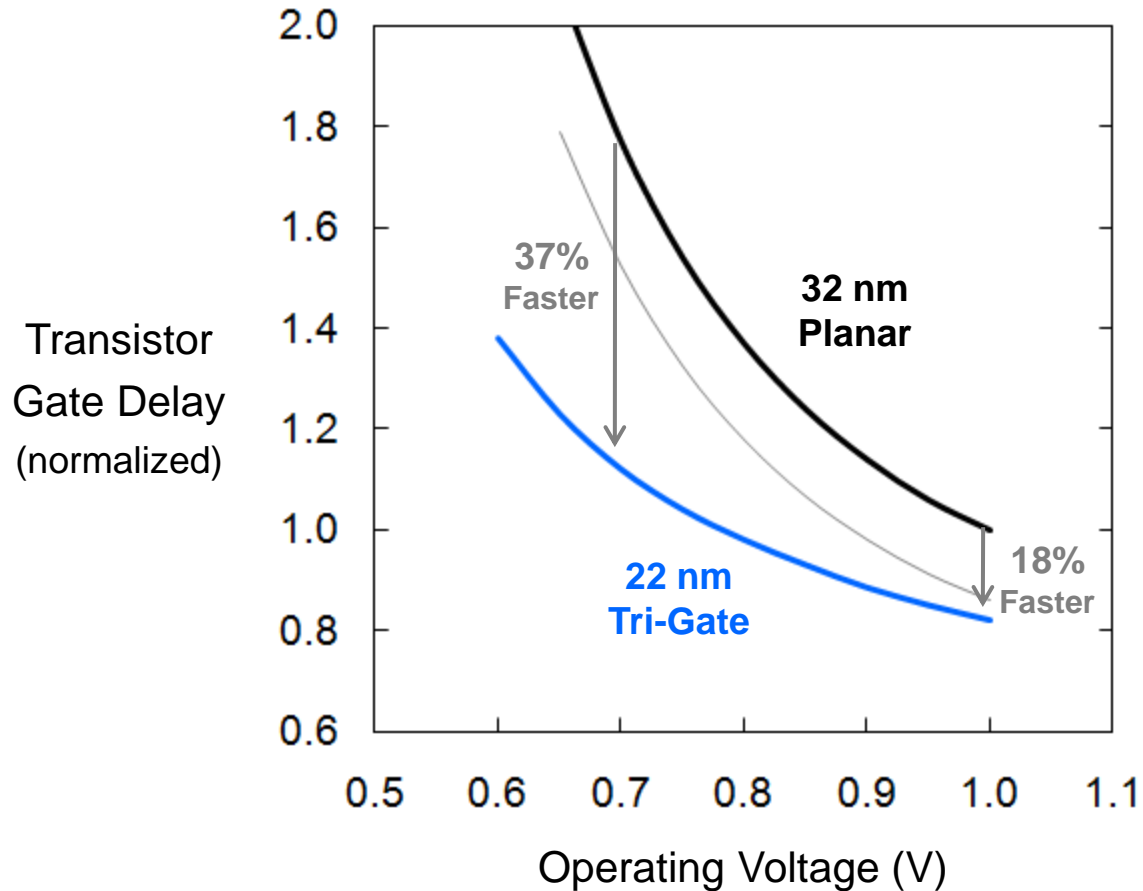
# Transistor Gate Delay



22 nm planar transistors could provide some performance improvement, but would still have poor gate delay at low voltage



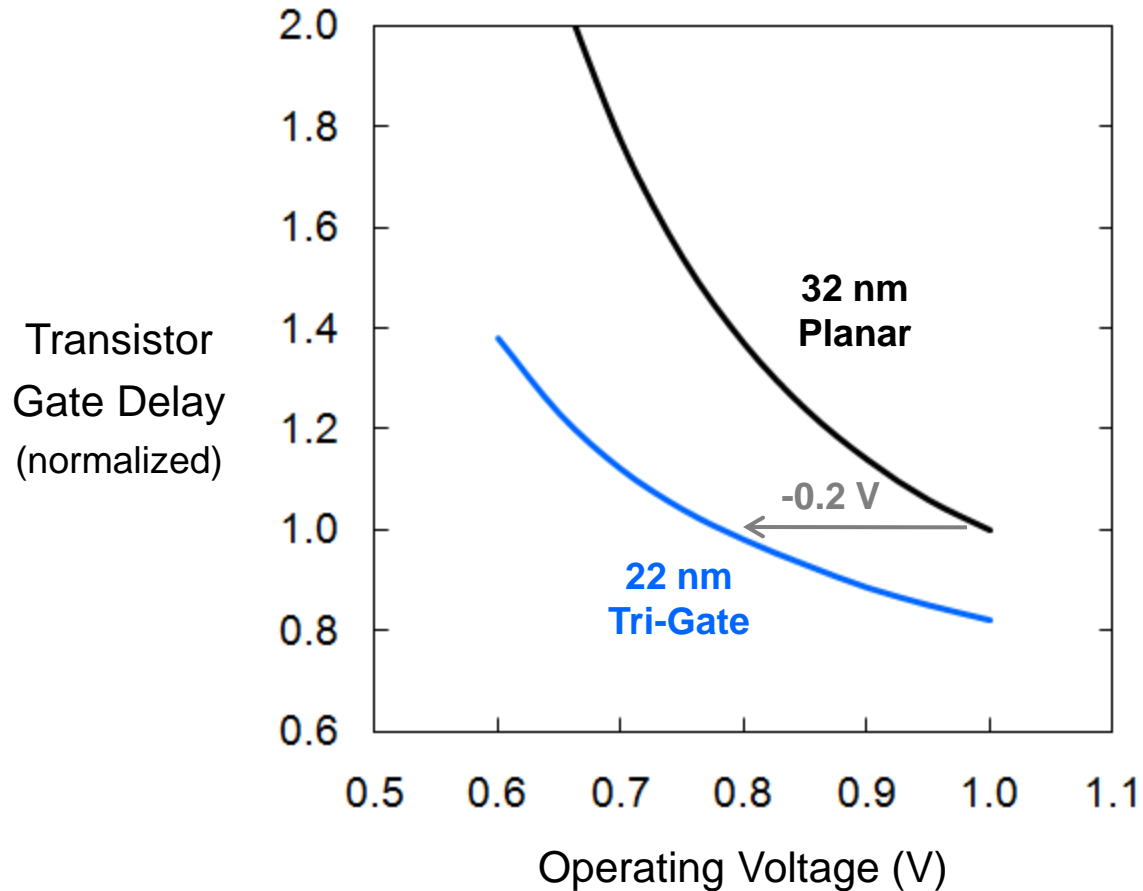
# Transistor Gate Delay



22 nm Tri-Gate transistors provide improved performance at high voltage and an *unprecedented* performance gain at low voltage



# Transistor Gate Delay

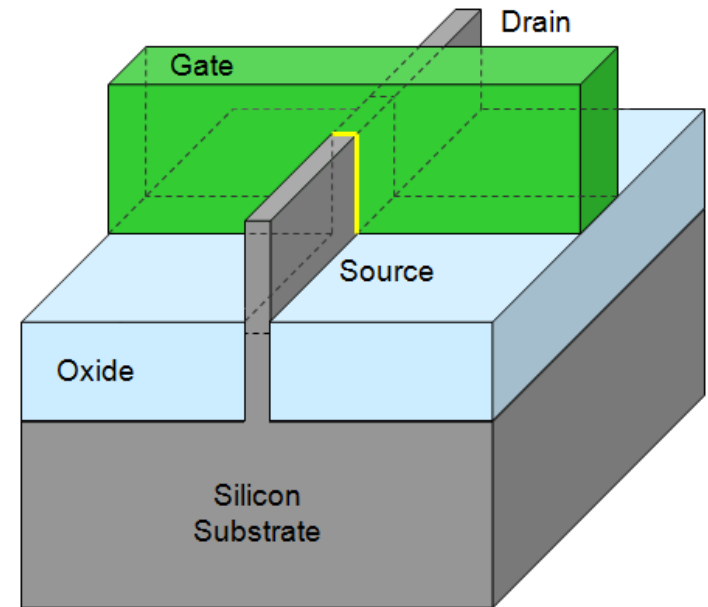


22 nm Tri-Gate transistors can operate at lower voltage with good performance, reducing active power by >50%



# Tri-Gate Transistor Benefits

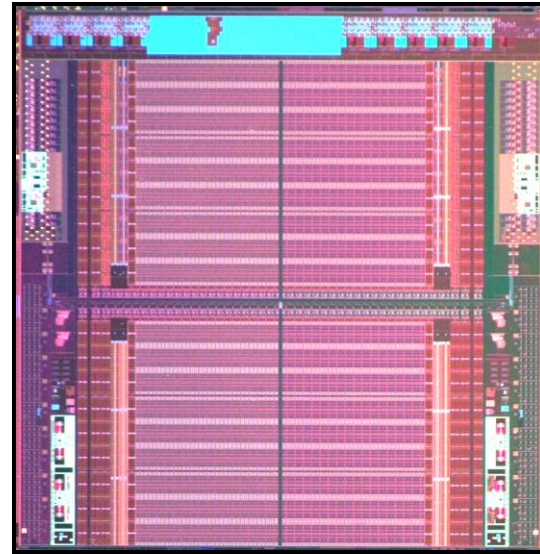
- Dramatic performance gain at low operating voltage, better than Bulk, PDSOI or FDSOI
  - 37% performance increase at low voltage
  - >50% power reduction at constant performance
- Improved switching characteristics (On current vs. Off current)
- Higher drive current for a given transistor footprint
- Only 2-3% cost adder (vs. ~10% for FDSOI)



Tri-Gate transistors are an important innovation needed to continue Moore's Law

# 22 nm Tri-Gate Circuits

- 364 Mbit array size
- >2.9 billion transistors
- 3<sup>rd</sup> generation high-k + metal gate transistors
- Same transistor and interconnect features as on 22 nm CPUs



22 nm SRAM, Sept. '09

22 nm SRAMs using Tri-Gate transistors were first demonstrated in Sept. '09

Intel is now demonstrating the world's first 22 nm microprocessor (Ivy Bridge)  
and it uses revolutionary Tri-Gate transistors

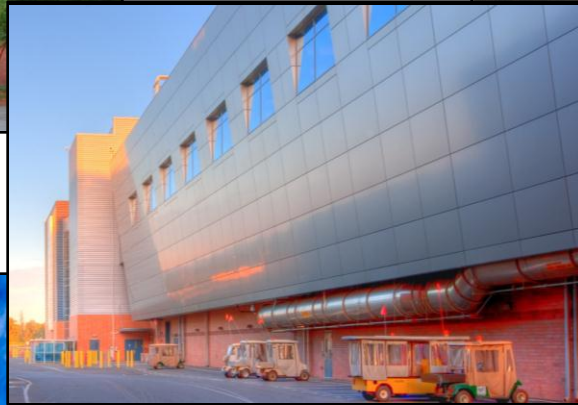
# 22 nm Manufacturing Fabs



D1C Oregon



Fab 28 Israel



D1D Oregon



Fab 32 Arizona



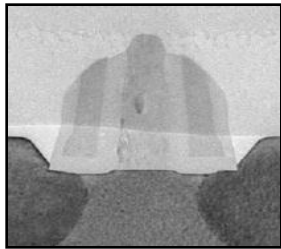
Fab 12 Arizona



# On-Time 2 Year Cycles

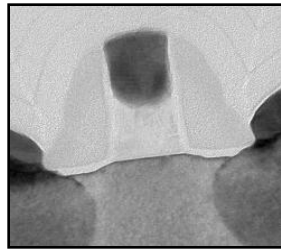
90 nm

2003



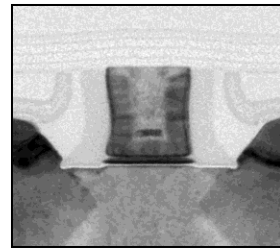
65 nm

2005



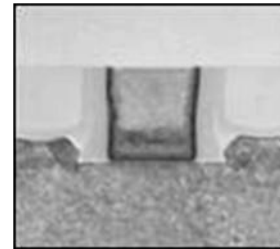
45 nm

2007



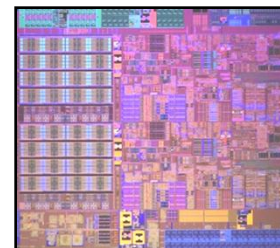
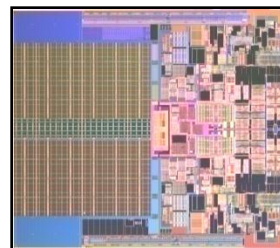
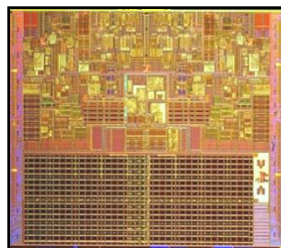
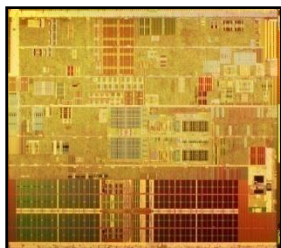
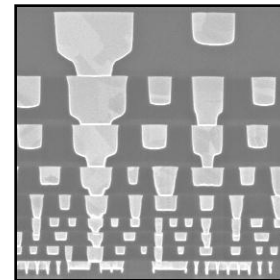
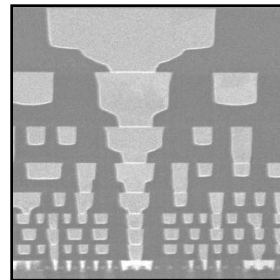
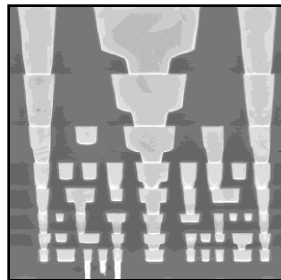
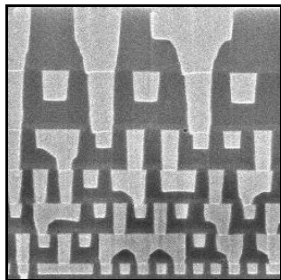
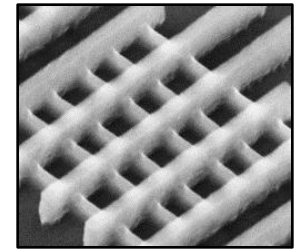
32 nm

2009



22 nm

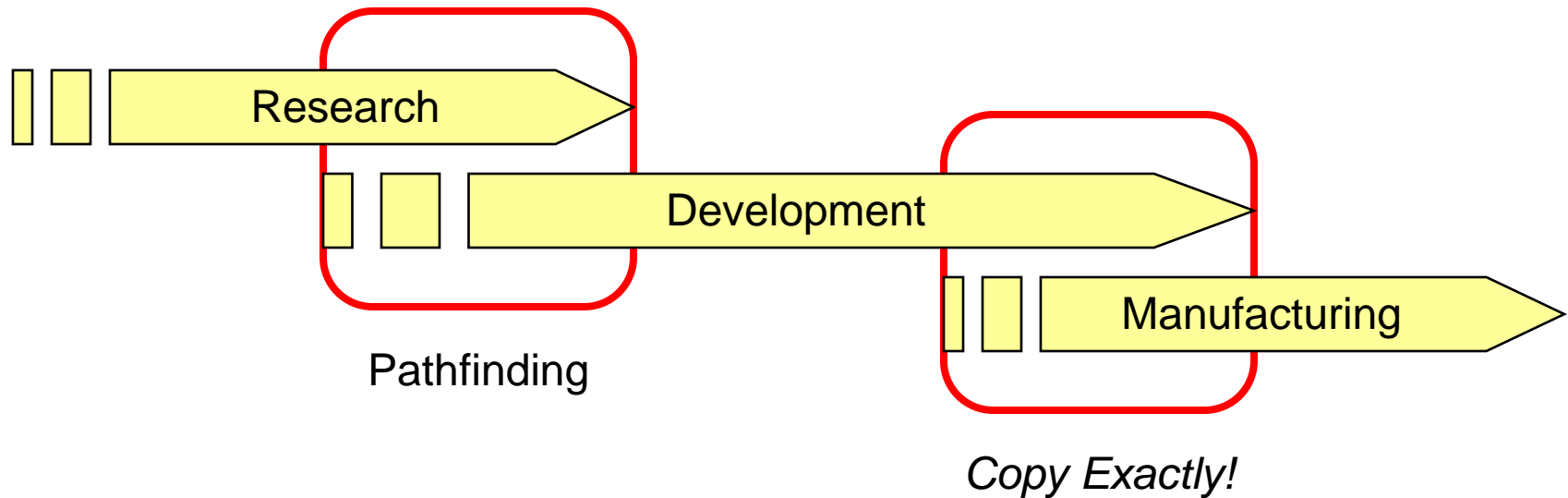
2011



Intel continues to successfully introduce leading edge process + products on a 2 year cadence



# Intel's R-D-M Pipeline



Bringing innovative technologies to high volume manufacturing is the result of a highly coordinated internal research-development-manufacturing pipeline



# Key Messages

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