A Spacer Patterning Technology for Nanoscale CMOS

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***Abstract*—A spacer patterning technology using a sacrificial layer and a chemical vapor deposition (CVD) spacer layer has been developed, and is demonstrated to achieve sub-7 nm structures with conventional dry etching. The minimum-sized features are defined not by the photolithography but by the CVD film thickness. Therefore, this technology yields critical dimension (CD) variations of minimum-sized features much smaller than that achieved by optical or e-beam lithography. In addition, it also provides a doubling of device density for a given lithography pitch. This method is used to pattern silicon fins for double-gate metal-oxide semiconductor field effect transistors (MOSFETs) (FinFETs) and gate electrode structures for ultrathin body MOSFETs. Process details are presented.**

***Index Terms*—Fin, FinFET, nanoscale-CMOS, spacer patterning process technology, sub-10 nm pattern, thin-body SOI, ultrathin body (UTB) MOSFET.**

I. INTRODUCTION

THIN-BODY SOI devices are promising for scaling CMOS devices into the nanoscale regime. Two promising structures are the ultrathin body (UTB) FET with a single gate [1] and the double-gate FinFET [2], [3]. The UTB structure minimizes subsurface leakage paths between the source and drain because the leakage current flows primarily along the bottom of the thin body, where the electric potential is the least effectively controlled by the gate. Therefore, a thinner body allows for more aggressive gate-length scaling. The FinFET, with a double-gate surrounding a narrow silicon fin, provides an ideal 60 mV/dec subthreshold swing and robustness against short-channel effects [4], [5]. In these thin-body devices, the threshold voltage is mostly determined by the gate work function, so that statistical dopant fluctuation effects are reduced [6], [7], and impurity scattering is minimized.

For the FinFET, short-channel effects can be suppressed by employing a body thickness (silicon fin width) which is approximately half of gate length L_g [3], [8]. This is clearly impossible to accomplish with standard lithography technologies when L_g is at the limit of lithography. Ashing and trimming technologies have been successfully used to make ~17 nm lines [9], but the uniformity of these approaches is poor. E-beam lithography has produced 15 nm gates [10]. However, the throughput of e-beam lithography is low and its uniformity is not yet satisfactory for sub-30 nm gate length fabrication as shown in Fig. 1. Extreme ultraviolet (EUV) lithography has generated 38 nm period patterns [11], but is not yet readily available. Uniformity is especially critical for the FinFET because variation in fin thickness (W_{fin}) can cause a change in the channel potential and subband structure, which governs short-channel behavior and quantum confinement effects [12], [13].

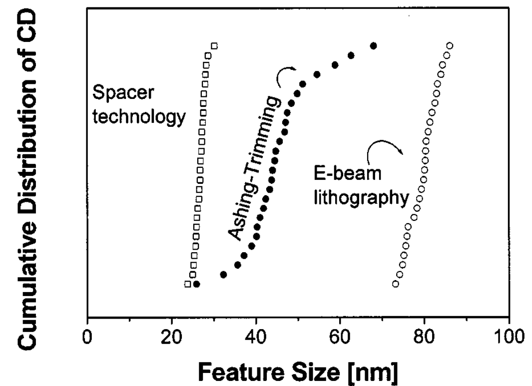

Fig. 1. CD variations of three lithography technologies. CD uniformity of the spacer technology is overwhelmingly better than the other two technologies. Measurements are taken after PSG spacer etch in the spacer technology, after hard mask oxide trimming in the ashing and trimming technology, and after resist development in e-beam lithography.

In addition to small linewidth, increased silicon fin pitch is desirable because multiple fins are needed to increase the effective channel width. Thus, the pitch of silicon fins limits device density and layout-area efficiency [14].

A spacer patterning technology is attractive for overcoming the limits of conventional lithography techniques in terms of pattern fidelity, CD variation, and pattern density. Johnson *et al.* [15] made 0.25 μm poly-Si spacer gates and To *et al.* [16] have reported 90 nm poly-Si spacer gates. However, these minimum feature sizes are not small enough for nano-scale CMOS devices. The spacer patterning technology described in this paper can produce extremely narrow and uniform silicon fins for FinFET devices as well as narrow gates for short-channel UTBFET devices. Furthermore, it provides for a doubling of fin density in the FinFET, which doubles the drive current for a given lithography pitch, as shown in Fig. 2(a) and (b). One drawback of prior spacer technologies is that only one line width (gate length) is available. By combining a conventional masking process and the spacer process in a novel manner, we overcome this limitation. A 6.5 nm silicon fin is formed and UTB devices with 30 nm gate length are successfully fabricated.

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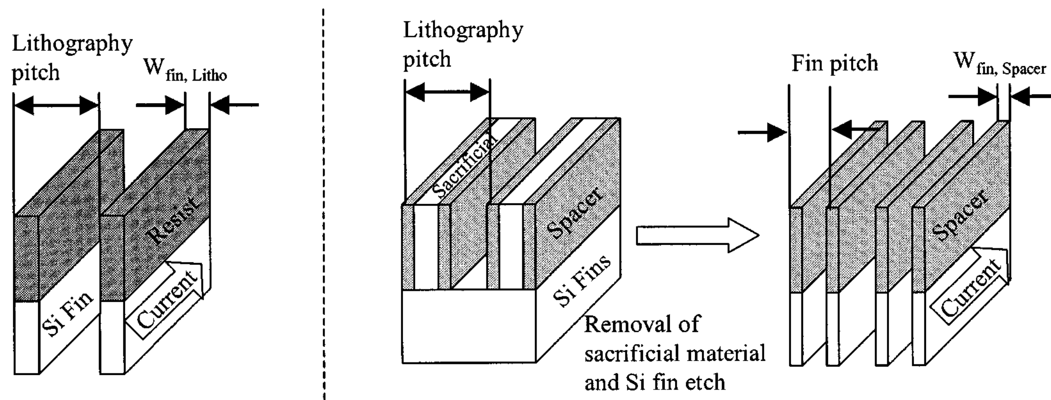

Fig. 2. Comparison of fin density between (a) conventional lithography and (b) spacer patterning technology. The spacer patterning technology can provide double the device density.

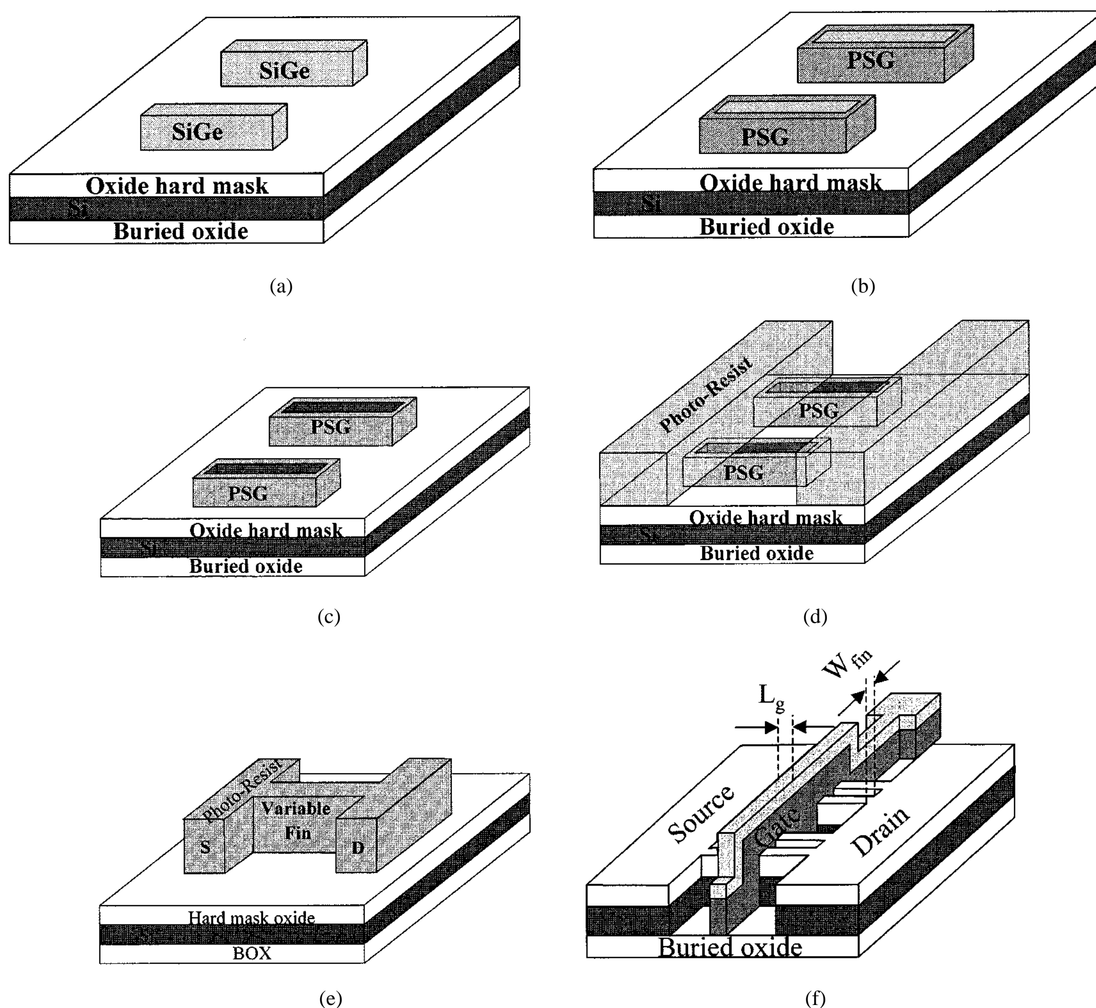

Fig. 3. FinFET process flow with spacer patterning technology (a) after sacrificial $Si_{0.4}Ge_{0.6}$ plasma etch, (b) after PSG spacer etch, (c) after removal of sacrificial $Si_{0.4}Ge_{0.6}$, (d) after S/D pad mask, (e) fins of larger widths defined with the same S/D pad mask, and (f) after gate formation.

II. Silicon Fin Formation in FinFETs

A spacer patterning technology was first used in fin formation in a FinFET process [2], [3]. As the starting material, (100) SOI wafers were used. The 100 nm silicon film was reduced to 50 nm by thermal oxidation. A remaining 50 nm oxide serves as a hard mask to protect the silicon fin during the subsequent etch. 200 nm $Si_{0.4}Ge_{0.6}$ was then deposited by LPCVD as a sacrificial layer. $Si_{0.4}Ge_{0.6}$ is chosen because it is easily etched by (5 : 1 : 1) $H_2O : NH_4OH : H_2O_2$ at 75 °C with high selectivity. As the Ge mole fraction in $Si_{1-x}Ge_x$ increases, this wet etch rate increases dramatically.

The SiGe layer was then patterned into sacrificial structures (to support the spacers) with optical lithography and plasma

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etching as shown in Fig. 3(a). The process conditions of the anisotropic $Si_{0.4}Ge_{0.6}$ etch were as follows: 50 sccm Cl_2, 150 sccm HBr, 15 mTorr, 300 W RF top power, and 150 W RF bottom power in a Lam Research 9400 TCP etcher. The etch rate was 1.1 μm/min. A vertical profile is crucial to the spacer patterning technology because sloped $Si_{0.4}Ge_{0.6}$ sidewalls would lead to sloped spacers, thus resulting in increased final line widths. It is also important to completely remove polymers after the $Si_{0.4}Ge_{0.6}$ plasma etch. The estimated residual polymer thickness adhering to the sidewalls of $Si_{0.4}Ge_{0.6}$ was 20$\sim$30 nm, which would significantly enlarge a minimum-sized feature. As a postetch treatment for the removal of polymers, the following steps were performed: (100 : 1) HF 10 s, photoresist strip with oxygen plasma, (100 : 1) HF 10 s, and piranha [(4 : 1) $H_2SO_4 : H_2O_2$ @ 120 °C) cleaning.

Phospho–silicate glass (PSG) thickness of 10 nm or 30 nm was then deposited by LPCVD over the patterned sacrificial $Si_{0.4}Ge_{0.6}$ layer. Low PSG deposition rate ($\sim$8 nm/min) was achieved with the following process conditions: $SiH_4 = 5$ sccm, $O_2 = 70$ sccm, $PH_3 = 11.3$ sccm, and 450 °C. The thickness of PSG at the sidewalls of the sacrificial $Si_{0.4}Ge_{0.6}$ structures determines the final fin width. An extremely small fin width, beyond the lithographic limit as well as very uniform fin width can therefore be obtained with this spacer patterning technology. A subsequent anisotropic PSG spacer etch removed the PSG film on top of the sacrificial $Si_{0.4}Ge_{0.6}$ structure [Fig. 3(b)], to generate an even number of spacers (fins). A 100% PSG over etch was applied to eliminate any spacer tails at the bottom of the $Si_{0.4}Ge_{0.6}$ which would otherwise result in a broadened fin width. The process conditions for the PSG spacer etch were: 100 sccm CF_4, 13 mTorr, 200 W RF top power and 40 W RF bottom power. The etch rate was 120 nm/min. This recipe produced spacers with vertical walls as shown in Figs. 3(c) and 4(b). The step coverage of the PSG film was around 70%, which yielded spacer widths of 6.5 nm and 20 nm. This spacer technique provides very low CD variation when compared to ashing–trimming [9] and e-beam lithography with SAL-601 resist (Fig. 1).

The $Si_{0.4}Ge_{0.6}$ structures were then removed by dry etch with 200 sccm HBr, 5 sccm O_2, 35 mTorr, 250 W RF top power, and 120 W RF bottom power at rate of 800 nm/min. This anisotropic etch did not result in any loss of the thermally grown oxide because the etch selectivity of $Si_{0.4}Ge_{0.6}$ to SiO_2 is higher than 400. $Si_{0.4}Ge_{0.6}$ residues after plasma etch were removed with (5 : 1 : 1) $H_2O : NH_4OH : H_2O_2$ at 75 °C [17]. PSG, thermally grown oxide, and silicon are not etched significantly in this solution. The final PSG spacer profile is seen in Figs. 3(c) and 4(b). I-line optical lithography was used to define large S/D contact pads as shown in Figs. 3(d) and 4(c). Therefore, a combined active pattern is defined by hard-mask PSG spacers for the fins and photoresist for the S/D contact regions [Figs. 3(f) and 4(d)]. Because the spacer technique forms only one line width, variable fin widths can be achieved by using photoresist to define the entire active region as shown in Fig. 3(e). This technoque, however, can only be used to define large line widths.

The active pattern was then transferred to the underlying oxide hard mask and SOI film. 100 sccm CF_4, 13 mTorr, 200 W RF top power, and 40 W RF bottom power was used for the oxide hard mask etch. 50 sccm Cl_2, 150 sccm HBr, 15 mTorr,

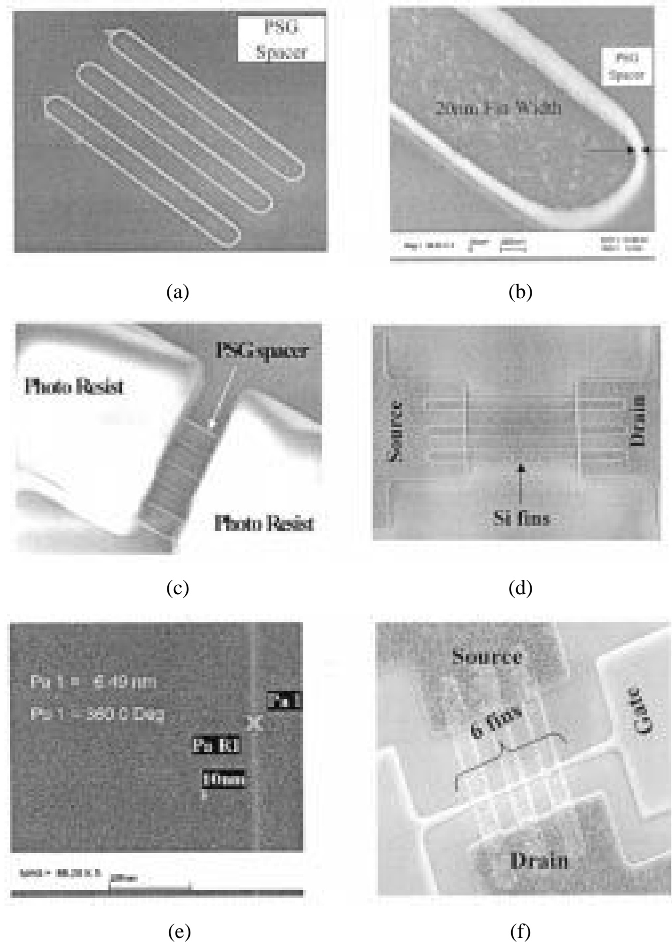

Fig. 4. SEM photographs of the FinFET structure: (a) PSG spacers as depicted in Fig. 3(c) after removal of sacrificial $Si_{0.4}Ge_{0.6}$, (b) close-up and tilted SEM view of a 20 nm PSG spacer showing its vertical structure, (c) S/D pad resist and PSG spacers as shown in Fig. 3(d), (d) six fins and S/D pads of silicon after silicon plamsa etch as depicted in Fig. 3(f) without the gate, (e) close-up SEM view (90 ° rotation) of 6.5 nm silicon fin in Fig. 4(d), and (f) fins with gate electrode depicted in Fig. 3(f).

300 W RF top power, and 150 W RF bottom power was used for the silicon etch. The silicon etch rate was 550 nm/min and the oxide etch rate was 40 nm/min. Silicon fins as narrow as 6.5 nm were obtained with the spacer patterning technology as shown in Fig. 4(e).

A sacrificial oxidation step was then used to remove etch damage. 10 nm of thermal oxide was grown in 12 min @ 900 °C in O_2. The bowed profile of the fin in the cross-sectional tunneling electron microscope (TEM) photograph shown in Fig. 5(a) and (b) resulted from a faster oxidation rate at the middle of the fins. This phenomenon was verified with TSUPREM4 simulation as shown in the inset of Fig. 5(b). Optimization of the sacrificial oxidation process is thus required to minimize the bowing effect. During HF removal of the sacrificial oxide, the PSG spacers and the hard mask oxide was also removed, and the buried oxide beneath the fin was undercut. The gate oxide was then grown at 750 °C, 12 min. An *in-situ* 900 °C, 30 min N_2 anneal was used to improve the gate-oxide quality. The gate electrode is then patterned over the fin using conventional lithography and etch processes as shown in Figs. 3(f) and 4(f). SiGe was chosen as the gate

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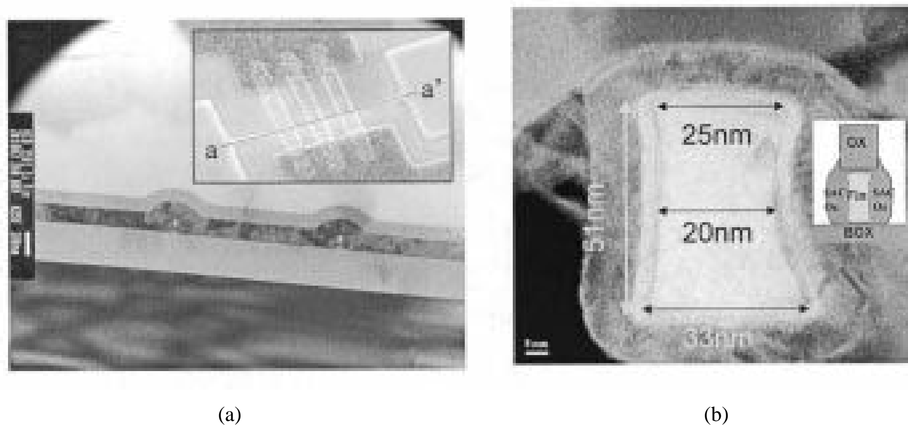

(a) (b)

Fig. 5. (a) Cross-sectional TEM view (along a–a' direction of the inset) of two silicon fins covered by the gate and (b) zoomed-in view of (a). The inset in (b) confirms the concave profile of the silicon fin caused by sacrificial oxidation using TSUPREM4 process simulation.

material to produce an appropriate threshold voltage using gate work-function engineering [18]–[20].

III. Gate Formation in UTB MOSFETs

This spacer patterning technology is also applied to obtain short gate lengths beyond the lithographic limit in planar ultra-thin body (UTB) transistor structures [1], [21]. This avoids the formation of "stringers" in the gate hard mask, which can be problematic in nonplanar structures. Up through gate and hard mask deposition, the fabrication process is similar to that reported in [1], [21]. As in fin patterning for the FinFET structure, 200 nm sacrificial $Si_{0.4}Ge_{0.6}$ was deposited and patterned, as shown in Fig. 6(a). 30 nm PSG spacers were then formed. The CF_4-based etch recipe for patterning PSG spacers made a microtrench along the $Si_{0.4}Ge_{0.6}$ pattern [22]. This pattern was transferred to the underlying ultrathin silicon body during the subsequent gate etch and the thin body silicon for S/D was disconnected from a channel (not seen in the Figures). The etch conditions without the micro-trench are 90 sccm CHF_3, 200 sccm Ar, 20 mTorr, 200 W RF top power, and 40 W RF bottom power, yielding an etch rate of 120 nm/min. This recipe generates a sloped profile, which results in an enlargement of the final gate length from 30 nm to 47 nm.

Because the spacer patterning technology always produces lines in pairs, one of the lines needs to be removed in order to obtain a single gate. As shown in Fig. 6(c), a separate resist mask was used for this purpose. This mask is not necessary for certain gate layouts as in the case of shorted NMOS and PMOS gate electrodes in a CMOS inverters. Diluted (25 : 1) HF was used to remove the PSG spacer not protected by the photoresist as shown in Fig. 6(d). The etch selectivity of PSG to HTO was more than 10 : 1.

A photoresist mask was used to define contact pads and also to provide variable channel lengths as shown in Fig. 6(e). The gate length of the transistor on the right in Fig. 6(f) can be varied using conventional lithography whereas the minimum channel length is defined by the spacer mask.

The gate plasma etch consisted of four steps: a two part HTO hard mask etch, main etch of poly-SiGe gate, and overetch of poly-SiGe gate. 100 sccm CF_4, 13 mTorr, 200 W RF top power, and 40 W RF bottom power were used to etch 90%

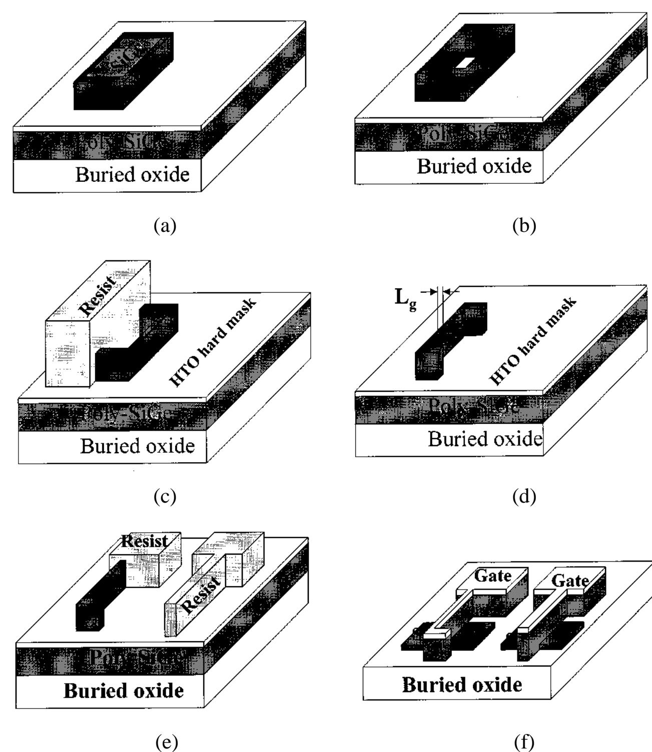

Fig. 6. UTBFET process flow with gate defined by spacer lithography: (a) formation of PSG spacer around a sacrificial $Si_{0.4}Ge_{0.6}$ pattern, (b) PSG spacer after removal of the sacrificial $Si_{0.4}Ge_{0.6}$, (c) photoresist mask and PSG spacer after masking process, (d) partial PSG spacer by removal with diluted HF, (e) PSG spacer and photoresist mask for gate pad and for larger gates (right), and (f) final gate pattern over ultrathin bodies that are hidden in Fig. 6(a)–(e).

of the HTO. 90 sccm CHF_3, 200 sccm Ar, 20 mTorr, 200 W RF top power, and 40 W RF bottom power were used for the remaining 10% of HTO and overetch. The first etch provided a vertical sidewall and a micro-trench along the bottom etch profile [22] while the second etch produced a sloped sidewall and no micro-trench. The combination of both recipes produced a vertical HTO hard mask with minimal micro-trench. For 90% of the poly-SiGe etch, 50 sccm Cl_2, 150 sccm HBr, 15 mTorr, 300 W RF top power, and 150 W RF bottom power were used for high anisotropy. 200 sccm HBr, 5 sccm O_2, 35 mTorr, 250 W RF top power, and 120 W RF bottom power were used for the last 10% of the poly-SiGe and overetch for high

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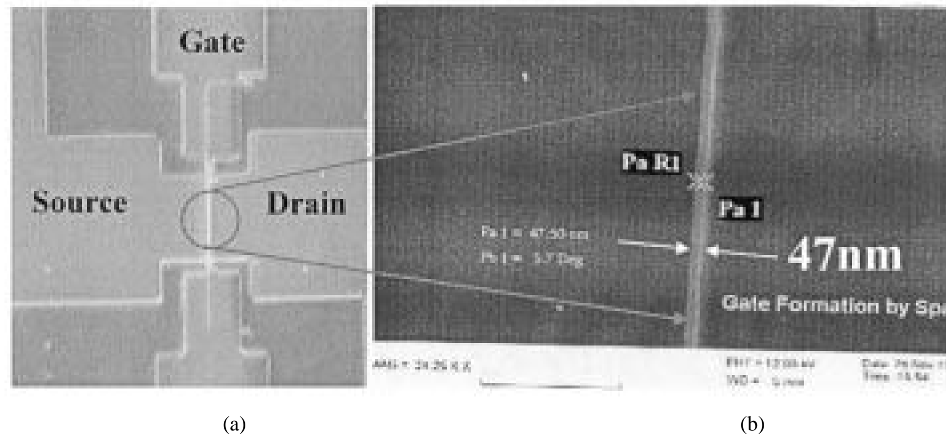

(a) (b)

Fig. 7. (a) Top view micrograph of UTBFET with spacer gate as depicted in the left half of Fig. 6(f). (b) SEM photograph of a 47 nm (top gate CD) gate in (a).

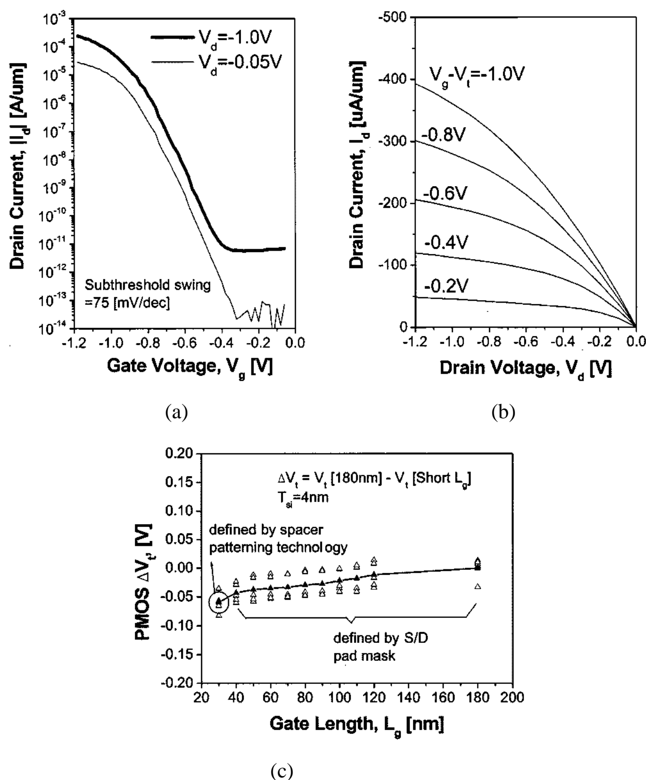

Fig. 8. Characteristics of UTB PMOSFET with $L_g = 30$ nm, $T_{ox} = 2.1$ nm, $T_{si} = 4$ nm, and $N_{body} = 1.0 \times 10^{17}$ cm^{-3}: (a) subthreshold characteristics, (b) output characteristics, and (c) V_t roll off for L_g down to 30 nm.

selectivity (>400 : 1). This HBr-based etch recipe produced a notched T-shaped (in a cross-section) gate [1]. A 10 nm lateral undercut (depends on etch time) on each side of the gate at the interface of the poly-SiGe and gate oxide was made. As a postetch treatment for polymer removal, (100 : 1) HF was used, which also removed the PSG spacer on the HTO hard mask. Fig. 7 shows a UTB transistor fabricated with this process with a top-surface gate length of 47 nm. The actual gate length at the bottom is estimated to be around 30 nm or less due to the lateral undercut on each side of the T-shaped gate.

After the definition of the SiGe gate using the spacer patterning technology, oxide/nitride spacers are formed on the sides of the gate. A selective Ge deposition process was used to create a raised source/drain structure to reduce the series resistance [21]. Fig. 8(a) and (b) shows PMOS characteristics of UTB devices with 30 nm gates defined by spacer patterning technology over 2.1 nm gate oxide and 4 nm UTB. 380 μA/μm drive current at $V_g - V_t = V_d = -1.0$ V, 10 pA/μm leakage current, and 75 mV/dec subthreshold swing were achieved. Fig. 8(c) shows that the threshold voltage roll-off characteristics and short-channel effects are very well controlled.

IV. Conclusion

A spacer patterning technology was developed for defining narrow-width silicon fins in the FinFET and small gate-lengths in the UTB MOSFET. Linewidths down to 6.5 nm were successfully defined. UTB devices with 30 nm gate length and 4 nm body thickness were fabricated with this process and exhibited excellent on and off state performances. This spacer technology provides higher device density, shorter channel lengths, and more uniform pattern size than optical and e-beam lithography.

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