

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
Petitioner

v.

MARLIN SEMICONDUCTOR LIMITED,
Patent Owner

Case IPR2025-01484
U.S. Patent No. 9,786,510

**PETITIONER'S OPPOSITION TO PATENT OWNER'S
DISCRETIONARY DENIAL REQUEST**

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Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

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PETITIONER’S UPDATED EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 9,786,510 to Shen et al. (“510 patent”)
1002	Prosecution History of U.S. Patent No. 9,786,510 (“510 File History”)
1003	Declaration of Dr. Salahuddin
1004	Curriculum Vitae of Dr. Salahuddin
1005	U.S. Patent Application Publication No. 2013/0244392 A1 to Oh et al. (“Oh”)
1006	U.S. Patent Application Publication No. 2010/0276756 A1 to Rachmady et al. (“Rachmady”)
1007	U.S. Patent Application Publication No. 2013/0093026 A1 to Wann et al. (“Wann”)
1008	U.S. Patent Application Publication No. 2014/0256093 A1 to Lin et al. (“Lin”)
1009	Colinge et. al., <i>FinFETs and Other Multi-Gate Transistors</i> , 2008 (“Colinge”)
1010	Hu, C., “MOSFETs in ICs – Scaling, Leakage, and Other Topics,” Chapter 7 of <i>Modern Semiconductor Devices for Integrated Circuits</i> , 1st ed., 2009 (“Hu”)
1011	Choi et al., “A Spacer Patterning Technology for Nanoscale CMOS,” <i>IEEE Transactions on Electron Devices</i> , Vol. 49, No. 3, pp. 436-441, March 2002 (“Choi”)
1012	U.S. Patent Application Publication No. 2013/0277759 A1 to Chen et al. (“Chen”)
1013	U.S. Patent Application Publication No. 2016/0027895 A1 to Akarvardar et al. (“Akarvardar”)
1014	U.S. Patent Application Publication No. 2012/0068264 A1 to Cheng et al. (“Cheng”)

Exhibit No.	Description
1015	Chang et al., “Scaling of SOI FinFETs down to Fin Width of 4 nm for the 10 nm technology node,” <i>IEEE Transactions on Electron Devices</i> , 2011 Symposium on VLSI Technology - Digest of Technical Papers, Kyoto, Japan, 2011, pp. 12-13 (“Chang”)
1016	U.S. Patent Application Publication No. 2013/0200483 A1 to Tung (“Tung”)
1017	U.S. Patent Application Publication No. 2013/0149826 A1 to Lee et al. (“Lee”)
1018	U.S. Patent Application Publication No. 2008/0303095 A1 to Xiong et al. (“Xiong”)
1019	Guo et al., “FinFET-Based SRAM Design,” ISLPED ’05, Proceedings of the 2005 International Symposium on Low Power Electronics and Design, San Diego, CA, USA, August 2005, pp. 2-7 (“Guo”)
1020	U.S. Patent Publication No. 2010/0148234 A1 to Torek et al. (“Torek”)
1021	U.S. Patent Publication No. 2014/0335673 A1 to Kim et al. (“Kim”)
1022	Prosecution History for Chinese Patent Application No. CN 2014104540915 with Certified English-Language Translation
1023	Chinese Patent No. CN103050533 A to Wann et al. with Certified English-Language Translation (“Wann CN”)
1024	United States Securities and Exchange Commission, United Microelectronics Corporation Form 20-F Annual Report, Dec. 31, 2017
1025	Docket Navigator Case Search, Marlin Litigation Docket, captured Dec. 1, 2025
1026	USPTO Assignment Data for U.S. Patent No. 9,786,510
1027	Docket Navigator Case Search, U.S. Patent No. 9,786,510, captured Dec. 1, 2025
1028	Patent Assignment for U.S. Patent No. 9,786,510, Reel and Frame No. 56991/0292

Exhibit No.	Description
1029	<p>“16/12nm Technology” TSMC, captured Dec. 2, 2025 https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_16_12nm</p>
1030	<p>“Another Historic Investment Secured Under President Trump,” The White House, Published Mar. 3, 2025 https://www.whitehouse.gov/articles/2025/03/another-historic-investment-secured-under-president-trump/</p>
1031	<p>“CNBC Transcript: United States Commerce Secretary Howard Lutnick Speaks with CNBC’s Brian Sullivan on “The Exchange” Today,” CNBC, Published Apr. 29, 2025 https://www.cnbc.com/2025/04/29/cnbc-transcript-united-states-commerce-secretary-howard-lutnick-speaks-with-cnbc-brian-sullivan-on-the-exchange-today.html</p>
1032	<p>“Removing Barriers To American Leadership In Artificial Intelligence,” The White House, Published Jan. 23, 2025 https://www.whitehouse.gov/presidential-actions/2025/01/removing-barriers-to-american-leadership-in-artificial-intelligence/</p>
1033	<p>Excerpt of “TSMC Annual Report 2024,” https://investor.tsmc.com/english/annual-reports</p>
1034	<p>Shilov, A., “Both Trump and Biden expected to attend TSMC's Arizona fab grand opening ceremony — Fab 21 opens in December,” Yahoo! Finance – tom’sHardware, Published Nov. 8, 2024 https://finance.yahoo.com/news/both-trump-biden-expected-attend-151941592.html</p>
1035	<p><i>Longitude Licensing Ltd. et al v. Apple Inc. et al</i>, Case No. WDTX-1-25-cv-00215, Docket Report, Docket Navigator, captured Dec. 2, 2025</p>
1036	<p>Docket Navigator Case Search, United Microelectronics Corporation (UMC) Litigation Docket, captured Dec. 2, 2025</p>

Exhibit No.	Description
1037	Nasdaq – This 1 Number May Ensure TSMC’s Market Dominance https://www.nasdaq.com/articles/1-number-may-ensure-tsmcs-market-dominance , captured Dec. 9, 2025
1038	U.S. Patent No. 8,214,007 B2 to Baker et al. (“Baker”)
1039	IDS Citation Sheet, Prosecution History of U.S. Patent No. 11,309,423 (April 29, 2019)
1040	TSMC-Ansys Collaboration Press Release https://investors.ansys.com/news-releases/news-release-details/ansys-strengthens-collaboration-tsmc-advanced-node-processes , captured Dec. 9, 2025
1041	TSMC-Cadence Press Release https://www.cadence.com/en_US/home/company/newsroom/press-releases/pr/2025/cadence-and-tsmc-advance-ai-and-3d-ic-chip-design-with-certified.html , captured Dec. 9, 2025
1042	TSMC’s Resurgence: What Lies Ahead for the Architect of AI https://www.cmcmarkets.com/en-au/market-news/tsmc-resurgence , captured Dec. 9, 2025
1043	Decoding TSMC’s Contribution to the AI and 5G Ecosystem https://graniteshares.com/institutional/us/en-us/research/decoding-tsmc-s-contribution-to-the-ai-and-5g-ecosystem/ , captured Dec. 9, 2025

I. INTRODUCTION

A core purpose of the PTAB under the AIA is to strengthen the integrity of the U.S. patent system by ensuring that only valid and properly granted patents remain in force. The challenged patent, U.S. Patent No. 9,786,510 (“’510 patent”), issued as a result of an Examiner (1) overlooking the teachings of the references applied in the prosecution, including the “closest prior art” (Torek) that teach all limitations of claim 1 and (2) failing to conduct an adequate search that would have identified a primary reference (Wann) applied in the Petition whose CN counterpart was applied by a CN Examiner to reject a claim having the same scope as the ’510 patent’s claim 1. Institution is warranted to address these material Examiner errors.

The settled expectations of TSMC and its customers outweigh any settled expectations of Marlin and warrant merits consideration. TSMC and its customers had a settled expectation of non-enforcement due to the lack of assertion by UMC, an alleged “primary” competitor of TSMC’s, during the first four years of the ’510 patent’s life. During this time, TSMC invested billions of dollars to manufacture FinFET chips, including for American customers who expected to be able to integrate those chips into their own products without incident. Marlin, a foreign entity which only recently acquired the patent, has no comparable expectations.

Institution is an efficient use of Board resources in view of *Fintiv* because

the '510 patent is not currently asserted in a parallel litigation. There is, however, a threat of enforcement, as evidenced by Marlin's claim of infringement and existing lawsuits in the ITC and district court. In response, TSMC diligently challenged the '510 patent's validity in the PTAB to provide a true alternative to district court or ITC litigation. Moreover, this case involves complicated semiconductor technologies, and trained PTAB judges are best suited to adjudicate the merits of the Petition and to correct the past errors of this Office.

Finally, compelling national security, economic, and public interests make review an appropriate use of the Board's resources. TSMC is the world's largest chip maker, by some accounts providing around 90% of the world's advanced chips (i.e., 7nm and smaller). EX1037, 2. Its advanced semiconductor technology is vital to the U.S. supply chain, with a wide range of applications including AI, 5G, health care, and national security and defense. Given TSMC's vital and strategic contribution to the U.S. supply chain, the Administration has a heightened interest in ensuring that the USPTO corrects its error in issuing this patent.

II. INSTITUTION IS WARRANTED IN VIEW OF MATERIAL ERRORS BY THE EXAMINER.

A. The Examiner materially erred by overlooking the teachings in the references applied during prosecution.

During prosecution, claim 1 was rejected as being obvious over Lee (EX1017) in view of Kim (EX1021) and as being anticipated by Torek (EX1020).

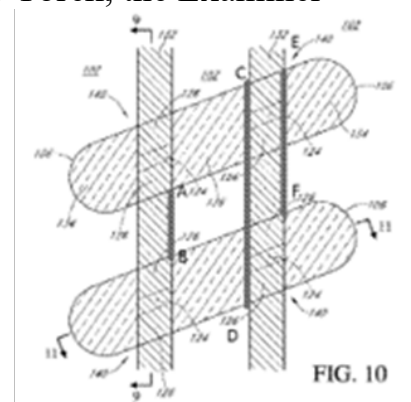
EX1002, 144-145, 178-179, 282-283. However, the Examiner erred in allowing the '510 patent claims both over Torek and over the Lee-Kim combination.

a. The Examiner erred by overlooking teachings in the “closest prior art” when allowing the claims.

The Examiner materially erred by failing to consider critical teachings of Torek, even though it was identified by the Examiner as the “closest prior art,” when allowing the '510 patent claims. EX1002, 310-311.

The Examiner determined Torek did not teach “wherein a first distance between adjacent top corners of the first fin and the second fin of the first fin-shaped structures is less than a second distance between adjacent top corners of the third fin and the fourth fin of the second fin-shaped structures ... and wherein the adjacent top corners are directly opposite each other” in issued claim 1 (“relative distances” limitation) and allowed the claims. EX1002, 303-313.

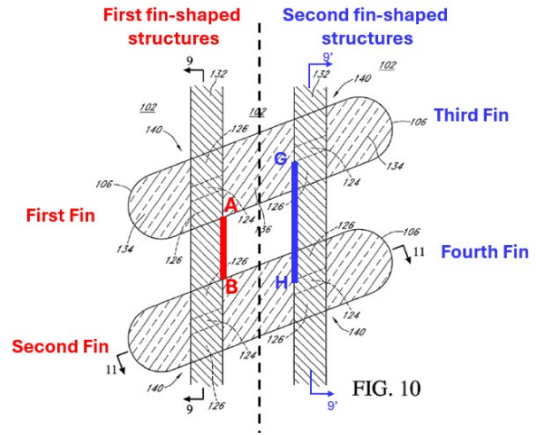
In mapping the “relative distances” limitation to Torek, the Examiner mapped active area mesas 106 (each including a lower region 126 and an upper region 124) to the claimed “first fin,” “second fin,” “third fin,” and “fourth fin.” EX1002, 310-311. The Examiner annotated Torek’s Figure 10 (top view of a FinFET array) to show three line segments: AB, CD, EF.



EX1020, FIG. 10
(as annotated by Examiner,
EX1002, 310).

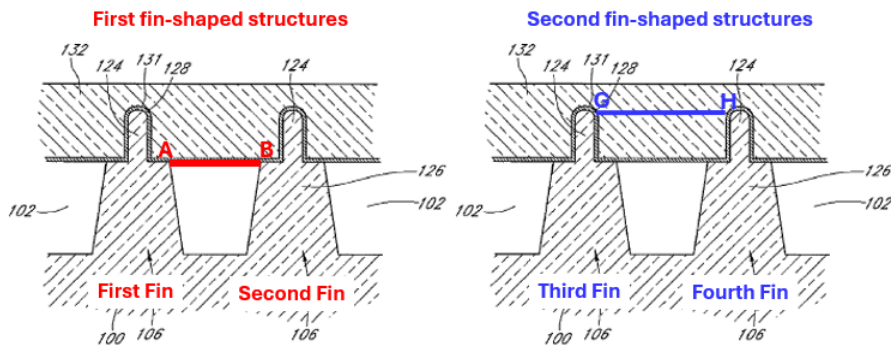
The Examiner mapped: (1) line segment AB between top corners of lower

mapping Torek to the “relative distances” limitation. For example, referring to Torek’s Figure 10, a line segment GH (blue) can be a “second distance” between adjacent and directly opposite top corners of upper regions 124. Here, the “first distance” of line segment AB (red) used by the Examiner is less than the “second distance” of line segment GH (blue) at the upper regions 124. This overlooked teaching by the Examiner discloses the alleged missing limitation of claim 1 that led to allowance.



EX1020, FIG. 10 (annotated).

Cross-sectional views of Torek’s Figure 10 further highlight the teachings overlooked by the Examiner. Figure 9 (below) shows: (1) on the left, a cross-sectional view of the “first fin” and “second fin” in Figure 10 (from the 9–9 cut line), which the Examiner identified, and (2) on the right, a cross-sectional view of the “third fin” and “fourth fin” in Figure 10 (from the 9’–9’ cut line), which the Examiner overlooked.



EX1020, FIG. 9 (annotated).

As the annotated Figures 9 and 10 illustrate, the Examiner failed to consider the “top corner” structures of the upper fin regions 124 of Torek in assessing the “relative distances” limitation. If the Examiner had compared the previously-identified AB segment to the missed GH segment, the claims would have been rejected. IPR is an appropriate use of Board resources to rectify this material error.

b. The Examiner erred by overlooking teachings in the originally applied Lee and Kim references.

The originally-filed claims were directed to a *single-fin* embodiment of a FinFET device. Claim 1 was twice rejected over the Lee-Kim combination. EX1002, 144, 178-179. In response, Applicant amended the claims to focus on a *multi-fin* embodiment. A different Examiner then took over prosecution, rejecting the amended claim 1 over Torek, but indicating there was allowable subject matter in newly-added claim 21.

However, the Examiner materially erred in overlooking the teachings of the originally-cited art—Lee and Kim, the combination of which also teaches the “relative distances” limitation that led to allowance. *Apple Inc. v. Advanced Coding Techs. LLC*, IPR2025-01103, Paper 11, 2-3 (PTAB Oct. 17, 2025).

The first reference, Lee, discloses the use of different fin-shaped structures in different device regions. EX1017, ¶¶18, 24, FIGs. 5, 6. The second reference, Kim, discloses various shaped single-fin and shaped multi-fin embodiments. EX1021, ¶¶36-44, 58-71, FIGs. 2A-8C, 13A-16B. The first Examiner applied

Kim's shaped single-fin embodiment to address the recited shaped single-fin structure. EX1002, 144, 179. To overcome the rejection, Applicant shifted the claims to a shaped multi-fin structure. EX1002, 193-204, 252-261.

A new Examiner then took over prosecution, rejecting application claim 1 as anticipated by Torek, but determining that the "relative distances" limitation in new independent claim 21 (which issued as claim 1) renders the claim allowable. EX1002, 279-288, 308-311. But the second Examiner overlooked the Lee-Kim combination, particularly the shaped multi-fin structure embodiment of Kim, when allowing the claims.

The Lee-Kim combination teaches the claimed multi-fin structure with the "relative distances" limitation as follows. Applying Kim's fin-shaping process for a multi-fin structure in Figure 16B to the fin structures on the left side of Lee's Figure 5, the left side then includes a shaped multi-fin structure and the right side remains a non-shaped multi-fin structure. As determined by the first Examiner, a POSA would have found it obvious to apply Kim's teachings (e.g., fin-shaping process on multiple fins, EX1021, FIG. 16B) to Lee's fin structures (e.g., third and fourth fins) in this way because "only one fin region of Lee (e.g. 100, ¶0014) is to be used as a transistor region, so that the modification [with Kim's fin-shaping process] would obviously not need to be made on both regions." EX1002, 144.

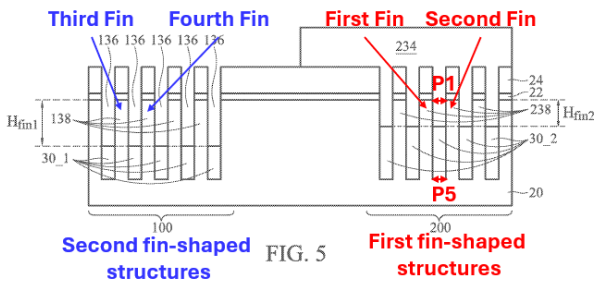
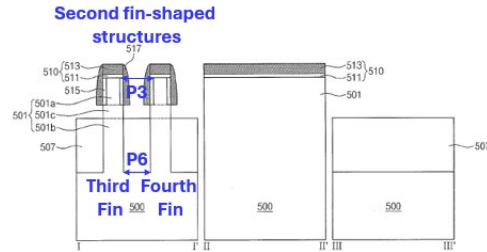


FIG. 5

EX1017 (Lee), FIG. 5 (annotated).



EX1021 (Kim), FIG. 16B (annotated).

Thus, the Lee-Kim the combination teaches a “first distance [(P1)] between adjacent top corners of the first fin and the second fin of the first fin-shaped structures is less than a second distance [(P3)] between adjacent top corners of the third fin and the fourth fin of the second fin-shaped structures while a third distance [(P5)] between adjacent lower parts of the first fin and the second fin is the same as a fourth distance [(P6)] between adjacent lower parts of the third fin and the fourth fin; and wherein the adjacent top corners are directly opposite each other.” The Lee-Kim combination thus teaches the very limitation that led to allowance. Institution is warranted to correct the material errors identified above.

B. The Examiner materially erred by conducting an inadequate search that failed to identify and apply material prior art.

The art is replete with other teachings of the alleged missing limitation of the ’510 patent’s independent claim 1, including the references raised in the Petition, such as Wann (EX 10007), a primary reference whose CN counterpart was applied by the CN Examiner to reject a claim having the same scope as the ’510 patent’s claim 1. For example, the Examiner’s failure to locate Wann is the result of an

inadequate prior art search. Indeed, the Examiner conducted a search that *should have* identified the Wann reference, but *did not*. As seen in the search report excerpt below, the Examiner searched Wann’s field of classification (H01L27/088), further narrowing the search with the keywords “fin and pitch and width”—all terms included in Wann. EX1002, 213; EX1007, Cover (51), ¶¶15-22. Yet, the Examiner did not identify Wann in the search result. This is material error.

S3	737	H01L21/8234.cpc. and (@ad< "20141013")	US-PGPUB; USPAT; USOOR; FFRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/09/20 17:00
S4	9953	H01L27/088.cpc. and (@ad< "20141013")	US-PGPUB; USPAT; USOOR; FFRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/09/20 17:00
S5	0	("2015/0318215").URFN.	USPAT	ADJ	ON	2016/09/20 17:02
S6	1	(US-20150318215-\$.)did.	US-PGPUB	ADJ	ON	2016/09/20 17:02
S7	94	(S3 or S4) and fin and pitch and width	US-PGPUB; USPAT; USOOR; FFRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/09/20 17:04

(10) Pub. No.: US 2013/0093026 A1
(43) Pub. Date: Apr. 18, 2013

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H01L 21/762 (2006.01)
H01L 29/78 (2006.01)
- (52) **U.S. Cl.**
 USPC **257/401**; 257/288; 438/400; 257/E27.06;
 257/E29.255; 257/E21.545

EX1002 (’510 Pros. Hist.), 213 (annotated). EX1007 (Wann), Cover (annotated).

Notably, the keywords that the Examiner was apparently searching for—“fin,” “pitch,” and width”—appear in Wann, and should have attracted the Examiner’s attention:

method. The exposed **fin** portions **107** has a height dimension (h), a **width dimension (w)** and a length dimension (l). Some electrical properties of the **FinFET** can be defined relative to these dimensions. For example, an effective channel **width** for the transistor may be calculated using the dimension of the **fins** under the gate. As shown in FIG. 1, the effective channel **width is 2 fins, or 2x(2h+w)**. Note that the effective channel **width** does not include the distance between **fins**. These **fins** are referred to herein as regular **fins** because they all have the same height and **width** dimensions.

[0022] Referring back to FIG. 2, in operation **217** a photoresist layer is patterned over the **fins**. Lithographic dimensions limit a minimum size that a photoresist layer may protect and a minimum size opening that a photoresist pattern may create. The minimum opening is smaller than the minimum area to be protected. In other words, an opening may be created with a dimension of one **fin pitch**, but the opposite, of a protective area covering one **fin pitch** may be too small. In FIGS. 3A and 3B, a photoresist layer **307** is deposited and patterned to create an opening **309**. If the dielectric layer of

EX1007, ¶¶15, 22 (excerpted, annotated).

Confirming that failing to identify and consider Wann was error, during prosecution of the priority foreign counterpart application of the ’510 patent

(Chinese Patent App. No. CN 201410454915, “the ’915 CN application”), substantially similar claims were rejected over the patent application publication of Wann’s CN counterpart (Chinese Patent No. CN 103050533, “Wann CN”). EX1001, Cover (30); EX1023, Cover (30). The Chinese Examiner in that action, reviewing substantially the same claims as the ’510 patent, identified Wann CN and rejected those claims. EX1022, 6-9, 15-26. Wann CN discloses the same subject matter as Wann.

- This Office Action is prepared with searches being conducted.
- This Office Action cites the following reference document(s) (the same document numbers will be used throughout the examination process):

No.	Document No. or Title	Publication Date (or Filing Date of Conflicting Application)
1	CN 103050533A	20130417
2	CN 104022116A	20140903

EX1022 (’915 CN Appl. Pros. Hist.), 6 (annotated).

The ’915 CN application was examined after the ’510 patent issued.

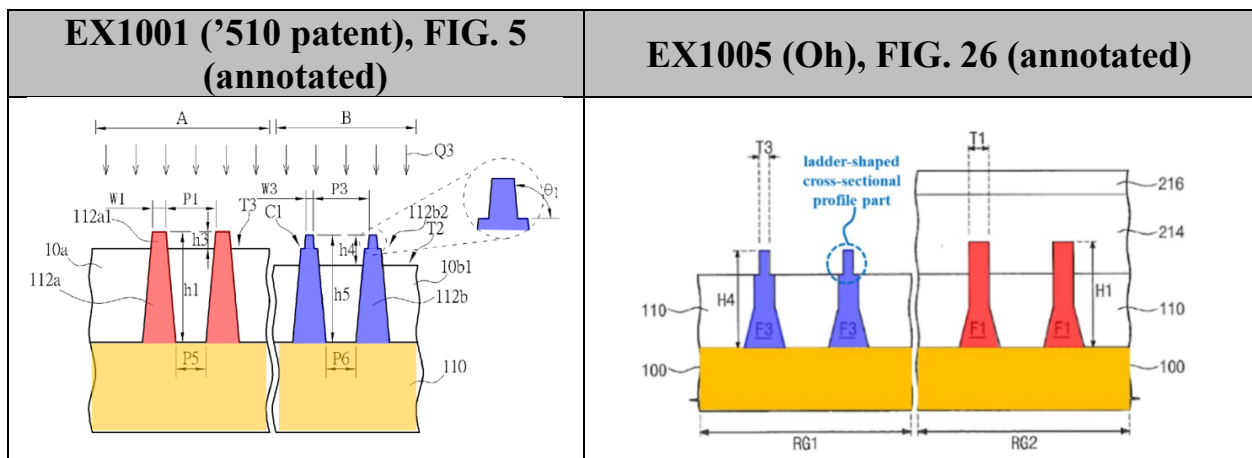
EX1022, 6. During prosecution of the ’915 CN application, Applicant amended claim 1 to have the same scope as the issued claim 1 of the ’510 patent. EX1022, 15. These amended claims were directly rejected over Wann CN. EX1022, 22-24. Ultimately, Applicant pursued other claims having a significantly different scope than the ’510 patent claims. EX1022, 27-46.

The Examiner’s flawed search is exactly the type of Examiner error IPRs are designed to address. Institution is warranted for this reason alone. *See, e.g., Anthony Inc. v. ControlTec, LLC*, IPR2025-00559, Paper 12 (PTAB July 16, 2025)

(finding material prosecution error where examiner failed to locate a petition reference).

III. INSTITUTION IS WARRANTED BECAUSE OF THE STRENGTH OF THE PETITION, WHICH INVALIDATES ALL CLAIMS OVER TWO SEPARATE PRIMARY REFERENCES.

The merits are strong, well-supported, and well-reasoned, and the invalidity positions are straightforward. TSMC presents one anticipation ground over Oh, and two obviousness grounds over (i) Oh in view of Rachmady and (ii) Wann in view of Lin. Pet., 14-76. Marlin identifies no substantive deficiencies in any of these references. As set forth in the Petition, each primary reference discloses all claim 1 limitations, including the “respective distances” limitation allegedly not found in the prior art. Moreover, the Petition’s compelling merits can be gleaned even just from the side-by-side figures below, which show the striking similarities between the alleged invention and Oh, raised as Ground 1 in the Petition.



IV. MERITS CONSIDERATION IS WARRANTED BECAUSE THE SETTLED EXPECTATIONS OF PETITIONER AND OTHERS OUTWEIGH MARLIN'S ALLEGED EXPECTATIONS.

Marlin's main contention in requesting denial is that the patent issued eight years ago, allegedly creating "settled expectations" that, alone, effectively trump all other considerations. DD Br. (Paper 6), 2-9. Focusing only on Marlin's expectations, without regard for the expectations of TSMC, its customers, and the public, is not balanced or fair. TSMC, its customers, and the public have "settled expectations," and they heavily outweigh Marlin's expectations.

Since acquiring the '510 patent in June 2021 (EX1026; EX1028), Marlin began an enforcement campaign against the semiconductor industry, including TSMC's customers. EX2104. And Marlin has since asserted patents against TSMC and its customers in the ITC, seeking an exclusion order. The Petition can resolve patentability of the '510 patent's claims before Marlin sues TSMC or its customers and disturbs the parties' well-settled expectations that the '510 patent remains dormant.

First, TSMC and its customers had settled expectations that the '510 patent would not be asserted due to the prior patent owner's (UMC's) inaction. TSMC has been engaged in FinFET manufacture since 2013. EX1029, 1. Since the issuance of the '510 patent, TSMC has invested billions of dollars in fabrication facilities to manufacture millions of wafers per year using the FinFET technology,

and its customers similarly invested significant resources into designs based on that technology. *See* EX1030. During this time, UMC, who Marlin claims is “TSMC’s main competitor,” DD Br., 3, remained silent and inactive.

Indeed, UMC does not have a history of asserting its patents *at all*. In 2017 when the ’510 patent issued, UMC had “5,341 U.S. patents.” EX1024, 0058. And according to DocketNavigator, UMC has been involved in a *total* of 19 patent actions since 1992. EX1036. In most of those cases, UMC was the ITC *respondent* or district court *defendant*. UMC is a listed plaintiff/complainant in only five cases, and *none of these* are after 2009. Despite its large patent portfolio, UMC did not have a history of patent enforcement. UMC’s inactivity created settled expectations for TSMC and its customers that the patent would remain dormant.

Marlin’s activities cannot unwind the settled expectations of TSMC and its customers created by UMC’s longstanding inaction with the patent. In analogous bodies of law, the expectations of others would exceed those of a new property owner under such circumstances. *See* Restatement (First) of Prop. § 459 cmt. a (1993) (“Through lapse of time old rights become obscure. A long continued use raises reasonable expectations of its continuance.”); *Anaheim Gardens, L.P. v. United States*, 953 F.3d 1344, 1350-51 (Fed. Cir. 2020); *Nordlinger v. Hahn*, 505 U.S. 1, 12-13 (1992) (“[A]n existing owner rationally may be thought to have vested expectations in his property or home that are more deserving of protection

than the anticipatory expectations of a new owner at the point of purchase.”).

Second, Marlin has not presented persuasive evidence that ’510 patent was ever “commercialized, asserted, marked, licensed, or otherwise applied” in the same “particular technology space” where it now seeks enforcement. *Shenzhen Tuozhu Tech. Co., Ltd. v. Stratasys, Inc.*, IPR2025-00531, Paper 10, 3 (PTAB July 17, 2025). This weighs against any claim by Marlin of “settled expectations.” *Id.*; *Home Depot U.S.A., Inc. v. H2 Intellect LLC*, IPR2025-00480, Paper 11, 2-3 (PTAB Sept. 4, 2025). The ’510 patent has not been asserted in litigation in any venue against any party. EX1027. Marlin alleges that UMC is “another Taiwanese semiconductor foundry” and “TSMC’s main business competitor.” DD Br., 1. Yet Marlin has not pointed to any evidence suggesting UMC enforced or demanded a license for the ’510 patent against TSMC (or anyone) during the 4 years UMC owned the patent.

Marlin also misleadingly argues that the ’510 patent “has been commercialized, at least in the form of licensing” with Intel and Samsung.¹ DD Br., 4-5. Marlin’s sole support for this argument is a bare assertion by its corporate

¹ The parties have recently reached agreement that Marlin will provide the same discovery of these licenses as authorized by the Board in IPR2025-01054. TSMC intends to request additional briefing when Marlin produces these licenses.

representative Paul Ahern (EX2104) that fails to provide *any details* regarding this license by which to assess its relevance or significance. Moreover, Marlin fails to put forth any evidence its purported licensees marked their products in any way to evidence commercialization that would disturb TSMC's settled expectations. At bottom, when Marlin acquired patents (including the '510 patent) that had never been asserted with the intention of enforcing them, the only reasonable expectation it could have is that their validity would be challenged. *See Anaheim Gardens*, 953 F.3d at 1350-51 (“timing” of property purchase and “knowledge of the purchaser” are relevant in determining whether purchaser had reasonable investment-backed expectations); *Celgene Corp. v. Peter*, 931 F.3d 1342, 1361-63 (Fed. Cir. 2019) (owners know patents may be subject to post-issuance reconsideration)

Relying on *iRhythm, Inc. v. Welch Allyn, Inc.*, IPR2025-00363, Marlin argues that TSMC's alleged knowledge of the '510 patent through prosecution of its own patent applications favors denial. DD Br., 4. But Marlin's argument is distinguishable. In two of three instances², the '510 patent was cited by the Examiner, not in an IDS as in *iRhythm*. EX2103 (indicated by a “*”). And in the third, unlike *iRhythm*, where the patent owner in the IPR proceeding owned the

² The other applications do not refer to the '510 patent at all, but rather to family members. EX2103, 6.

patent at the time of issuance, the citation occurred before Marlin acquired the patent. EX1038 (U.S. Patent No. 8,214,007 issued to Welch Allyn, Inc.); EX1040, Cite No. 11 (IDS citation of '510 patent in U.S. 11,309,423). As described above, TSMC has settled expectations, based on UMC's conduct, that the '510 patent would not be asserted. A petitioner's expectation of non-enforcement has been deemed sufficient to overcome any alleged settled expectations based on the age of the patent. *See, e.g., Globus Medical, Inc. v. Spinelogik, Inc.*, IPR2025-00225, Paper 8 (PTAB June 12, 2025) (patent expired for failure to pay maintenance fees prior to enforcement); *Home Depot USA, Inc. v. H2 Intellect LLC*, IPR2025-00480, Paper 11 (PTAB Sept. 4, 2025) (no expectation of enforcement against hardware store); *Apple v. Ferid Allani*, IPR2025-00856, Paper 11 (PTAB Sept. 5, 2025) (delay of enforcement of 11 years after patent expired).

Finally, Marlin also argues that licensing negotiations between the parties beginning in 2024 weigh against any claim of settled expectations by TSMC. DD Br., 7 (citing *DataDome S.A. v. Arkose Labs Holdings, Inc.* IPR2025-00693, Paper 13, 7 (PTAB Aug. 14, 2025)). Marlin's reliance on *DataDome* is unavailing. First, in *DataDome*, there was a parallel proceeding and no argument regarding material error by the Examiner. *DataDome*, Paper 6 at 7; Paper 39, 26-31. Both of these factors differ in the present case and weigh in favor of institution. Moreover, TSMC filed this Petition just a year after receiving a licensing proposal, which was

followed by a period of evaluation and good faith negotiations, and just 6 months after those negotiations discontinued due to Marlin asserting patents against TSMC in court. TSMC was far more diligent than the *DataDome* Petitioner who waited over two years after receiving an initial demand and 15 months after refusing a license to file its Petition. *DataDome*, Paper 13 at 7; *DataDome*, EX1013 (Jan. 11, 2023 letter seeking license on one challenged patent).

V. INSTITUTION IS AN EFFICIENT USE OF BOARD RESOURCES.

Institution here is an efficient use of Board resources in view of *Fintiv* because there is no parallel litigation involving the '510 patent. *See, e.g., Intas Pharms. Ltd. v. Atossa Therapeutics, Inc.*, IPR2025-00799, Paper 12, 2-3 (PTAB Aug. 12, 2025); *Azurity Pharms., Inc. v. Helsinn Healthcare S.A.*, IPR IPR2025-00945, Paper 11, 2-3 (PTAB Sept. 19, 2025) (no parallel proceeding and Examiner error outweigh patent owner settled expectations (age of patent and commercialization)). No other tribunal is set to resolve the merits; therefore, no risk of duplicated efforts, inconsistent decisions, or unnecessary expense exists.

Marlin argues this fact is not dispositive because the petitions in *Intel Corp. v. Proxense LLC* were discretionarily denied despite having no *trial date*. DD Br., 7 (citing IPR2025-00327, Paper 12, 2 (PTAB June 26, 2025)). However, in *Intel*, the Acting Director explained the discretionary denial decision was based upon Petitioner's failure to "provide any persuasive reasoning as to why an *inter partes*

review is an appropriate use of Board resources.” *Intel*, Paper 12 at 2. Here, TSMC presents several compelling reasons why IPR is an appropriate use of resources, e.g., to address the Examiner’s material errors and to resolve the parties’ dispute in an efficient manner avoiding “unnecessary and counterproductive litigation costs” before Marlin asserts this patent in a court against TSMC.

Marlin has already alleged infringement of the ’510 patent and shown a willingness to bring TSMC to court. Institution before litigation promotes the very ideals that underlie the IPR process and is an appropriate use of Board resources.

VI. NATIONAL SECURITY, ECONOMIC, AND PUBLIC INTEREST CONSIDERATIONS STRONGLY FAVOR INSTITUTION.

Marlin acknowledges it has alleged infringement of the ’510 patent by TSMC. EX2104. Given Marlin’s chosen forum for enforcement is the ITC, this threat to weaponize the ’510 patent undermines the U.S. semiconductor supply chain, harming priorities this Administration has made clear are vital to U.S. economic interests and national security. EX1031, 3; EX1032, 1. This makes IPR of the ’510 patent an appropriate use of the Office’s resources—indeed a compelling one. TSMC’s FinFET fabrication capabilities are vital to leading U.S. companies (such as Apple, NVIDIA, Amazon, Broadcom, Qualcomm, and AMD). More specifically, TSMC’s 5 nm processing node supports U.S. advanced semiconductor research and development in industries including AI, health care, and national security/defense. EX1033, 18-19. Promoting these emerging

industries is an important step in advancing the Administration’s priorities.

EX1031, 3; EX1032, 1.

Indeed, the U.S. government has recognized AI’s importance to national security, and TSMC is an important part of the American AI-dominance strategy. EX1040; EX1041. For example, TSMC “produces the advanced processors that Nvidia [] and Apple [] rely on to bring AI to life,” including, NVIDIA’s next-generation Blackwell AI chips for NVIDIA’s AI supercomputers. EX1042, 2. Moreover, healthcare is a key area of projected growth in the AI semiconductor market, where the demand for “advanced chips—TSMC’s specialty—will continue to surge.” EX1043, 5. Blocking or burdening access to TSMC-made advanced semiconductors could create a catastrophic single-point failure for medical R&D, causing direct effects on future patient care and far-reaching consequences for the development of life-saving technology.

Marlin does not dispute the serious impact a ban on importing FinFET products into the United States would have to vital U.S. national security, public health, or economic interests. Instead, Marlin sets up a strawman—painting itself as protector of local industries. DD Br., 10. The facts belie Marlin’s pronouncement. Marlin does not practice the ’510 patent, nor any patent it holds. There is no evidence that Marlin, a foreign entity, has invested in the U.S. semiconductor technology space, except by trying to assert its recently acquired

patents. Given Marlin's assertion of its patents in the ITC against U.S.-based companies (e.g., Apple, Qualcomm, Broadcom), *see* EX1035, Marlin's arguments that it is a protector of "local industry" ring hollow.

Finally, trying to cast TSMC as a "foreign entity" that "import[s] infringing products" and must be protected against twists the facts beyond recognition. There is zero evidence, other than a bare, unsupported statement from an interested party, Mr. Ahern, that any product of TSMC infringes any patent in Marlin's portfolio, including the '510 patent. Additionally, Marlin ignores TSMC's commitment to invest \$165 billion in building manufacturing facilities in the United States in support of this Administration's goal to onshore advanced semiconductor manufacturing to bolster U.S. economic and national security interests. EX1031, 3. Indeed, TSMC's Arizona facilities are already producing 4 nm chips for American customers. EX1034, 2. Marlin's enforcement campaign against TSMC seeks to damage the core supply chain of semiconductor chips from TSMC to the United States. These considerations therefore warrant institution.

VII. CONCLUSION

For these reasons, the Director should deny Marlin's request to discretionarily deny this IPR and should institute review of the challenged claims.

Respectfully submitted,

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CERTIFICATION OF SERVICE (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that, on December 10, 2025, true and correct copies of the foregoing **PETITIONER'S OPPOSITION TO PATENT OWNER'S DISCRETIONARY DENIAL REQUEST** and **Exhibits 1020-1043** were served electronically via e-mail in their entireties on the following counsel for Patent Owner:

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