UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
Petitioner

v.

MARLIN SEMICONDUCTOR LIMITED,
Patent Owner

Case IPR2025-01484
U.S. Patent No. 9,786,510

DECLARATION OF SAYEEF SALAHUDDIN, PH.D., IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT NO. 9,786,510

Mail Stop "PATENT BOARD"
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

TABLE OF CONTENTS

I. INTRODUCTION 1
II. BACKGROUND AND QUALIFICATIONS 2
III. LIST OF DOCUMENTS CONSIDERED 6
IV. LEGAL STANDARDS FOR MY ANALYSIS 8
V. THE ’510 PATENT 13
A. Overview of the ’510 Patent 13
B. Prosecution History Summary 17
C. Level of Ordinary Skill in the Art 18
D. Claim Construction 19
VI. STATE OF THE ART 19
A. FinFET Characteristics 20
B. Fin Formation with Mandrel/Spacer Process 21
C. Fin Shaping Techniques 27
VII. OVERVIEW OF THE APPLIED REFERENCES 31
A. Oh 31
B. Rachmady 34
C. Wann 36
D. Lin 40
VIII. GROUNDS OF UNPATENTABILITY 42
A. Ground 1: Oh renders obvious claims 1, 2, and 6. 43
1. Independent Claim 1 43
a. [1.P]: A fin-shaped structure, comprising: 43
b. [1.a]: a substrate having a plurality of first fin-shaped structures and a plurality [of] second fin-shaped structures, and the first fin-shaped structures comprising a first fin and a second fin, the second fin-shaped structures comprising a third fin and a fourth fin, ... 44
c. [1.b]: wherein a first distance between adjacent top corners of the first fin and the second fin of the first fin-shaped

structures is less than a second distance between adjacent top corners of the third fin and the fourth fin of the second fin-shaped structures 48

d. [1.c]: while a third distance between adjacent lower parts of the first fin and the second fin is the same as a fourth distance between adjacent lower parts of the third fin and the fourth fin; 51

e. [1.d]: and wherein the adjacent top corners are directly opposite each other. 65

2. Dependent Claim 2: wherein the width of each top part of the first fin shaped structures is larger than the width of each top part of the second fin-shaped structures. 67

3. Dependent Claim 6: wherein a height of the first fin-shaped structures protruding from the substrate is higher than a height of the second fin-shaped structures protruding from the substrate. 68

B. Ground 2: The combination of Oh and Rachmady renders obvious claims 3-5. 69

1. A POSA would have been motivated to combine Oh and Rachmady. 69

a. A POSA would have been motivated to apply Rachmady's selective fin height teachings to Oh's fin-shaped structure to adjust drive current. 72

b. A POSA would have reasonably expected to succeed in modifying Oh's fin-shaped structure based on Rachmady's selective fin height teachings. 76

c. Additional rationales for combining Oh's and Rachmady's teachings. 79

2. Dependent Claim 3 81

a. [3.a]: an isolation structure disposed beside the first fin-shaped structures and beside the second fin-shaped structures respectively, ... 81

b. [3.b]: and ladder-shaped cross-sectional profile parts of the second fin-shaped structures are higher than a top surface of the isolation structure. 83

3. Dependent Claim 4: wherein a top surface of the isolation structure of a first area is higher a top surface of the isolation structure of a second area. 88

4. Dependent Claim 5: wherein a height of the first fin-shaped structures protruding from the isolation structure is lower than a height of the second fin-shaped structures protruding from the isolation structure.. 91

C. Ground 3: The combination of Wann and Lin renders obvious claims 1-6. 95

1. A POSA would have been motivated to combine Wann and Lin. 95

a. A POSA would have been motivated to apply Lin's mandrel/spacer process to Wann's fin-shaped structures. 97

b. A POSA would have reasonably expected to succeed in applying Lin's mandrel/spacer process to Wann's fin-shaped structures..101

2. The Wann-Lin five-fin FinFET structure. 102

a. Wann's disclosure applies to a wide variety of FinFETs with various fin arrangements. 104

b. Wann's fin-shaping process applies to various fin arrangements of FinFETs, including Wann's five-fin FinFET embodiment. 107

3. Independent Claim 1 126

a) [1.P]: A fin-shaped structure, comprising:...................126

b) [1.a]: a substrate having a plurality of first fin-shaped structures and a plurality [of] second fin-shaped structures, and the first fin-shaped structures comprising a first fin and a second fin, the second fin-shaped structures comprising a third fin and a fourth fin,........................128

c) [1.b]: wherein a first distance between adjacent top corners of the first fin and the second fin of the first fin-shaped structures is less than a second distance between adjacent top corners of the third fin and the fourth fin of the second fin-shaped structures 130

d) [1.c]: while a third distance between adjacent lower parts of the first fin and the second fin is the same as a fourth distance between adjacent lower parts of the third fin and the fourth fin; 134

e) [1.d]: and wherein the adjacent top corners are directly opposite each other. 137

4. Dependent Claim 2: wherein the width of each top part of the first fin shaped structures is larger than the width of each top part of the second fin-shaped structures. 138

5. Dependent Claim 3 139

a) [3.a]: an isolation structure disposed beside the first fin-shaped structures and beside the second fin-shaped structures respectively,...139

b) [3.b]: and ladder-shaped cross-sectional profile parts of the second fin-shaped structures are higher than a top surface of the isolation structure. 141

6. Dependent Claim 4: wherein a top surface of the isolation structure of a first area is higher a top surface of the isolation structure of a second area...146

7. Dependent Claim 5: wherein a height of the first fin-shaped structures protruding from the isolation structure is lower than a height of the second fin-shaped structures protruding from the isolation structure..148

8. Dependent Claim 6: wherein a height of the first fin-shaped structures protruding from the substrate is higher than a height of the second fin-shaped structures protruding from the substrate. 150

IX. CLAIMS APPENDIX..153

X. CONCLUSION 155

I, Sayeef Salahuddin, hereby declare as follows.

I. INTRODUCTION

1. I have been retained as an expert witness on behalf of Taiwan Semiconductor Manufacturing Company Ltd. ("TSMC"; "Petitioner") for the above-captioned *inter partes* review (IPR). I am being compensated for my time in connection with this IPR at my standard consulting rate, which is $400 per hour.

2. I understand that this Declaration accompanies a petition for IPR involving U.S. Patent No. 9,786,510 ("the '510 patent") (EX1001), which resulted from U.S. Patent Application No. 14/512,475 ("the '475 application"), filed on October 13, 2014. A foreign counterpart application was filed on September 9, 2014, from which I understand that the '510 patent allegedly claims priority. I refer to this date throughout this Declaration.

3. In preparing this Declaration, I have reviewed the '510 patent and each of the documents cited herein, in light of general knowledge in the art before September 9, 2014. In formulating my opinions, I have relied upon my experience, education, and knowledge in the relevant art. In formulating my opinions, I have also considered the viewpoint of a person of ordinary skill in the art ("POSA") (i.e., a person of ordinary skill in the semiconductor field, as defined further below in Section V.C) prior to September 9, 2014. It is my opinion that each of the challenged claims of the '510 patent is unpatentable for at least the reasons I

discuss below.

II. BACKGROUND AND QUALIFICATIONS

4. My academic and professional pursuits are closely related to the subject matter of the ’510 patent. I have over 20 years of experience in advanced semiconductor research, especially in device physics, device design, material synthesis, nanoscale fabrication, and testing. My research at the University of California, Berkeley in the aforementioned areas led to more than 100 publications in the most prestigious journals. Based on my education and work experience, I am well qualified to serve as a technical expert in this matter.

5. I received a Bachelor of Engineering (B.E.) degree in Electrical and Electronics Engineering in 2003 from the Bangladesh University of Engineering and Technology in Dhaka, Bangladesh. I also received a Doctor of Philosophy (Ph.D.) degree in Electrical and Computer Engineering in 2007 from Purdue University in West Lafayette, Indiana.

6. Following my Ph.D. degree, I worked as a Post-doctoral Research Associate at Purdue University. In 2008, I joined University of California, Berkeley as an Assistant Professor and was later promoted to Associate Professor in 2014 and to Professor in 2017.

7. Currently, I am the TSMC Distinguished Chair Professor[1] of Electrical Engineering and Computer Sciences at the University of California Berkeley. My current research interests relate to the following areas: (i) negative capacitance effect in ferroelectric materials and negative capacitance transistors; (ii) thin film ferroelectricity; (iii) spintronics and nanomagnetic logic computing; (iv) electrical driven ferromagnetic resonance free from external magnetic field; and (v) two-dimensional semiconductors and quantum tunneling effect in low dimensional materials and devices.

8. I co-directed the ASCENT Center, which is jointly funded by the Semiconductor Research Corporation (SRC), a consortium composed of major semiconductor companies around the world, and the United States Defense Advanced Research Agency (DARPA). I was selected as a member of a panel to advise the U.S. government on advanced semiconductor manufacturing through DARPA. Further, I received the Inventor Recognition Award by the SRC.

9. I was elected a Fellow of the Institute of Electrical and Electronics

---

[1] The TSMC Distinguished Chair is an endowed chair at the University of California Berkeley. Chair holders are selected by the Dean of the College of Engineering. TSMC has no say in choosing the holder of the chair, nor does it constitute any obligation of loyalty to or sponsorship from TSMC.

Engineers (IEEE), the American Physical Society (APS), and American Association for Advancement of Science (AAAS) for my contributions to semiconductor devices. I am a member of the Technical Advisory Board of the Natcast, the operator of the National Semiconductor Technology Center. My work on semiconductor devices was also recognized by the Presidential Early Career Award for Scientists and Engineers by President Barack Obama.

10. In addition, I have consulted for leading semiconductor companies, such as Sandisk Corporation (now part of Western Digital Corporation) on advanced two-dimensional (2D) and three-dimensional (3D) memory design, semiconductor process innovation, and semiconductor fabrication. In this role, I reviewed process flows, process recipes, lithography, and material integration issues, as well as their impact on the device and system level. Based on my review, I advised Sandisk Corporation on optimizing these areas. Further, I have advised on device reliability issues that may arise from certain semiconductor processing. Additionally, I have consulted for advanced semiconductor companies in the context of Front End of the Line (e.g., transistor level) process integration, where I reviewed process flows, recipes, and material integration issues. Similarly, I have consulted on fin field effect transistor (FinFET) fabrication processes, heteroepitaxy and conformal synthesis of materials for advanced transistor fabrication, and simulation of structures and current flow for advanced transistors.

In this work, I also reviewed process flows, recipes, and training materials.

11. Further, I am a member of the founding team of Sunrise Memory Corp., a startup company commercializing innovative 3D memory solutions. At Sunrise3D, I led the design of the memory bit cell and advised on process innovations. I conceived multiple process integration solutions for 3D device structures and established Design of Experiments (DOE) for optimization. In addition, I am a co-founder at Sonera Magnetics, a company developing innovative device solutions for augmented/virtual reality. I have 15 patents (including granted and pending applications) in the area of advanced semiconductor devices and technology.

12. I have authored or co-authored over 150 technical papers, in technical journals and conferences in my field of expertise and have been the inventor or co-inventor of over 20 patents. I have supervised over 20 doctoral students, over 20 post-doctoral researchers, and over 150 undergraduate students in research areas in material physics and electronic applications. I received the NSF CAREER Award and the IEEE Nanotechnology Council Early Career Award in 2012, the Army Research Office (ARO) Young Investigator Program Award and the Air Force Office of Scientific Research Young Investigator Award in 2013, the Presidential Early Career Award for Scientist and Engineers in 2016, the IEEE George E Smith Award in 2019, and the IEEE Andrew Grove Award in 2025.

13. A full list of my research and professional experience, my consultant and work experience, and other activities and awards is further detailed in my curriculum vitae (CV), which I understand is being included as Exhibit 1004.

III. LIST OF DOCUMENTS CONSIDERED

14. In formulating my opinions, I considered all of the references cited in this Declaration, including the documents listed below. All citations to the documents listed below in this declaration are to the page number of the original reference, not the stamped exhibit page numbers.

Exhibit No.	Description
1001	U.S. Patent No. 9,786,510 to Shen et al. ("'510 patent")
1002	Prosecution History of U.S. Patent No. 9,786,510 ("'510 File History")
1005	U.S. Patent Application Publication No. 2013/0244392 A1 to Oh et al. ("Oh")
1006	U.S. Patent Application Publication No. 2010/0276756 A1 to Rachmady et al. ("Rachmady")
1007	U.S. Patent Application Publication No. 2013/0093026 A1 to Wann et al. ("Wann")
1008	U.S. Patent Application Publication No. 2014/0256093 A1 to Lin et al. ("Lin")
1009	Colinge et. al., *FinFETs and Other Multi-Gate Transistors*, 2008 ("Colinge")

Exhibit No.	Description
1010	Hu, C., "MOSFETs in ICs – Scaling, Leakage, and Other Topics," Chapter 7 of *Modern Semiconductor Devices for Integrated Circuits*, 1st ed., 2009 ("Hu")
1011	Choi et al., "A Spacer Patterning Technology for Nanoscale CMOS," *IEEE Transactions on Electron Devices*, Vol. 49, No. 3, pp. 436-441, March 2002 ("Choi")
1012	U.S. Patent Application Publication No. 2013/0277759 A1 to Chen et al. ("Chen")
1013	U.S. Patent Application Publication No. 2016/0027895 A1 to Akarvardar et al. ("Akarvardar")
1014	U.S. Patent Application Publication No. 2012/0068264 A1 to Cheng et al. ("Cheng")
1015	Chang et al., "Scaling of SOI FinFETs down to Fin Width of 4 nm for the 10 nm technology node," *IEEE Transactions on Electron Devices*, 2011 Symposium on VLSI Technology - Digest of Technical Papers, Kyoto, Japan, 2011, pp. 12-13 ("Chang")
1016	U.S. Patent Application Publication No. 2013/0200483 A1 to Tung ("Tung")
1017	U.S. Patent Application Publication No. 2013/0149826 A1 to Lee et al. ("Lee")
1018	U.S. Patent Application Publication No. 2008/0303095 A1 to Xiong et al. ("Xiong")
1019	Guo et al., "FinFET-Based SRAM Design," ISLPED '05, Proceedings of the 2005 International Symposium on Low Power Electronics and Design, San Diego, CA, USA, August 2005, pp. 2-7 ("Guo")

IV. LEGAL STANDARDS FOR MY ANALYSIS

15. I am not an attorney and have not been asked to offer my opinion on the law. However, as an expert offering an opinion on whether the claims in the '510 patent are patentable, I have been told that I am obliged to follow existing law.

16. I have been told that a patent may not be obtained, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. I have been told that, in *inter partes* review proceedings, a patent claim may be deemed unpatentable if it is shown by preponderance of the evidence (i.e., it is more likely than not) that it would have been obvious.

17. When considering the issues of obviousness, I have been told that I am to do the following:

a. Determine the scope and content of the prior art;

b. Ascertain the differences between the prior art and the claims at issue;

c. Resolve the level of ordinary skill in the pertinent art; and

d. Consider evidence of secondary indicia of obviousness or non-obviousness (if available).

18. I have been told that the relevant time for considering whether a claim would have been obvious to a POSA is the time of alleged invention, which I have been asked to assume is just before the alleged earliest claimed priority date of the ’510 patent (i.e., September 9, 2014).

19. I have been told that a prior art reference may be combined with one or more other references and/or the knowledge of a person of ordinary skill in the art to show obviousness. I also have been told that a person of ordinary skill in the art is presumed to know all relevant prior art. I have been told that the obviousness analysis may account for the inferences and creative steps that a person of ordinary skill in the art would have employed at the time of invention.

20. In determining whether the teachings contained in one prior art reference would have been combined with the teachings contained in another reference or information known to a person of ordinary skill in the art, I have been told that the following principles may be considered, and I have been asked to consider them:

a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
b. The substitution of one known element for another is likely to be obvious if it yields predictable results;
c. The use of a known technique to improve similar items or

methods in the same way is likely to be obvious if it yields predictable results;

d. The application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;

e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;

f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and

g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a "reasonable expectation of success"—not "absolute predictability" of success—in achieving the claimed invention by combining prior art references.

21. I have been told that whether a prior art reference renders a patent claim unpatentable as obvious is determined from the perspective of a POSA. I have been told that there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, but a suggestion to combine known elements to achieve the claimed invention may come from the prior art, as filtered through the knowledge of a POSA. In addition, I have

been told that the inferences and creative steps a POSA would have employed are also relevant to the obviousness inquiry.

22. I have been told the reasons a POSA would have wanted to modify teachings available in the prior art teachings do not need to match the inventor's reasons for making the claimed invention. In determining whether the subject matter of a patent claim is obvious, I have been told that what matters is the objective reach of the claim and whether it covers an obvious variation of the prior art. I have been told it would be improper to consider only the specific problem the patentee was trying to solve.

23. I have been told that when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been told that if a POSA would have implemented a predictable variation and would have seen the benefit of doing so, that variation was likely to have been obvious. I have been told that in many fields, there may be little discussion of obvious combinations, and, in these fields, market demand, not scientific literature, may drive design trends. I have been told that when there was a design need or market pressure and there were a finite number of predictable solutions, a POSA would have had good reason to pursue those known options.

24. I have been told that there is no rigid rule that a reference or combination of references must contain a "teaching, suggestion, or motivation" to

combine them. But I also understand that any "teaching, suggestion, or motivation" present in the prior art may be useful in establishing a rationale for combining aspects of the prior art. I have been told this "teaching, suggestion, or motivation" test poses the question as to whether the prior art contains an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

25. I have been told that a claimed invention may be obvious even when the prior art does not teach each claim limitation, so long as the record contains some reason why a POSA would have applied the prior art to obtain the claimed invention.

26. I have been told that when there is a known technique to address a known problem using prior art elements according to their established functions, then a POSA would have had a motivation to combine.

27. I have been informed that, in an obviousness analysis, the prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address; or (2) reasonably pertinent to the particular problem being solved by the challenged

patent.

V. THE '510 PATENT

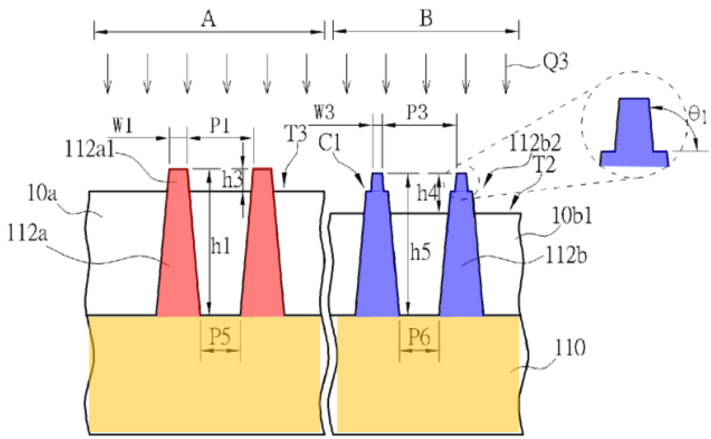
A. Overview of the '510 Patent

28. The '510 patent describes a fin-shaped structure including a substrate having a first fin-shaped structure in a first area and a second fin-shaped structure located in a second area. EX1001, Abstract. The second fin-shaped structure can include a "ladder-shaped" cross-sectional profile part. EX1001, Abstract. The '510 patent states that it "provides a fin-shaped structure and method thereof, which selectively forms fin-shaped structures having ladder-shaped cross-sectional profile parts in some areas, so that fin-shaped structures of different heights and critical dimensions (CD) can be formed, in order to form transistors for each area that meet each area's specific electrical demands." EX1001, 1:34-40.

29. The '510 patent claims a substrate having first fin-shaped structures (including a first fin and a second fin) and second fin-shaped structures (including a third fin and a fourth fin). The first and second fin-shaped structures are formed such that a distance between directly opposite top corners of adjacent first fin-shaped structures is less than a distance between directly opposite top corners of adjacent second fin-shaped structures. The first and second fin-shaped structures are also formed such that a distance between lower parts of the adjacent first fin-shaped structures is the same as a distance between lower parts of the adjacent

second fin-shaped structures. EX1001, 1:34-40. The ’510 patent describes a first embodiment of the fin-shaped structure illustrated by Figures 1-5 and a second embodiment of the fin-shaped structure illustrated by Figures 6-10. EX1001, 2:43-48. I discuss these two embodiments below with respect to the ’510 patent’s Figures 5 and 8.

30. Figure 5 (reproduced below with annotations) shows the first embodiment in which **first fin-shaped structures 112a** (red) and **second fin-shaped structures 112b** (blue) are formed on a **substrate 110** (orange). EX1001, 4:65-5:12. **First fin-shaped structures 112a** and **second fin-shaped structures 112b** are formed by a removal process: “a removing process Q3 is performed to remove the modified parts 120 and a part of the isolation structures 10a and 10b1 simultaneously, to form a top part 112a1 of each of the first fin-shaped structures 112a and a second top part 112b2 of each of the second fin-shaped structures 112b.” EX1001, 4:66-5:4. Each of **second fin-shaped structures 112b** has what the ’510 patent referred to as a “ladder-shaped” cross-sectional profile part C1 shown in a dashed line inset of Figure 5 below, where “[t]he ladder-shaped cross-sectional profile part C1 has a bending angle θ1, which is preferably larger than or equal to 90°.” EX1001, 5:13-18. In this first embodiment, “[t]he ladder-shaped cross-sectional profile part C1 of each of the **second fin-shaped structures 112b** is higher than a top surface T2 of the isolation structure 10b1.” EX1001, 5:32-44.



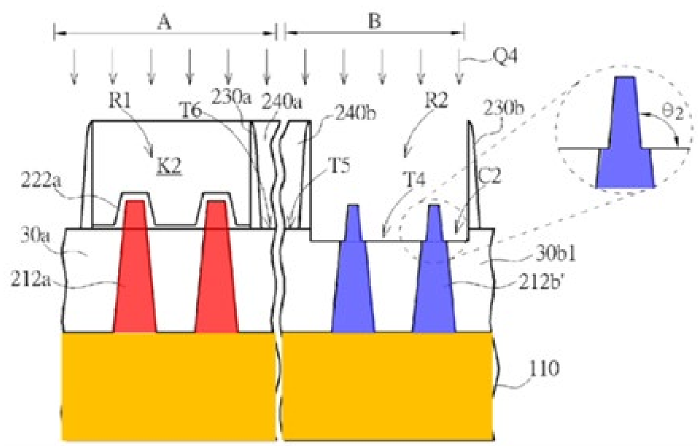
EX1001, FIG. 5 (annotated).

31. The ’510 patent states that the fin width and the distance of the top part of the first fin-shaped structures 112a and second fin-shaped structures 112b are different. EX1001, 5:20-32. For example, the ’510 patent states that “[t]he width w1 of the top part of each of the **first fin-shaped structures 112a** … is larger than a width w3 of a top part of each of the **second fin-shaped structures 112b**.” EX1001, 5:20-24. The ’510 patent further states that “[t]he first distance p1 between adjacent top corners of the first fin and the second fin of the **first fin-shaped structures 112a** is less than a second distance P3 between adjacent top corners of the third fin and the fourth fin of the **second fin-shaped structures 112b**, while a third distance P5 between adjacent lower parts of the first fin and the second fin is the same as a fourth distance P6 between adjacent lower parts of the third fin and the fourth fin.” EX1001, 5:24-32. Width w1, width w3, first distance P1, second distance P3, third distance P5, and fourth distance P6 are shown in

Figure 5 (reproduced above with annotations).

32. Figure 8 (reproduced below with annotations) shows the second embodiment in which **first fin-shaped structures 212a** (red) and **second fin-shaped structures 212b'** (blue) are formed on **substrate 110** (orange). EX1001, 5:62-6:5. **First fin-shaped structures 212a** and **second fin-shaped structures 212b'** are formed by a removal process: "a removing process Q4 [is] performed to remove an external surface S1 of a top part of each of the second fin-shaped structures 212b … to form **second fin-shaped structures 212b'** having ladder-shaped cross-sectional profile parts C2, wherein the ladder-shaped cross-sectional profile parts C2 have a bending angle θ2, and the bending angle θ2 is preferably larger than or equal to 90°." EX1001, 7:14-21. The ladder-shaped cross-sectional profile part C2 is shown in a dashed line inset of Figure 8. The '510 patent states that "the second dielectric layer 222b and the second fin-shaped structures 212b below the second dielectric layer 222b are removed by the removing process Q4" to form the ladder-shaped cross-sectional profile part C2. EX1001, 7:36-39. The '510 patent further states that "[a]n isolation structure 30b1 is formed, and a top surface T4 of the isolation structure 30b1 at the bottom of the recess R2 is lower than a top surface T5 of isolation structure 30b1 beside the recess R2, and even lower than a top surface T6 of the isolation structure 30a in the first area A, depending upon the etchants of the removing process Q4 and a desired formed

structure." EX1001, 7:25-32.



EX1001, FIG. 8 (annotated).

B. Prosecution History Summary

33. I have been told that the application leading to the '510 patent issued after receiving five Office Actions: a restriction requirement, two non-final Office Actions, and two final Office Actions. EX1002, 0125-0130, 0141-0147, 0176-0182, 0207-0212, 0279-0288. After electing to pursue structure claims in reply to the restriction requirement, I have been told that Patent Owner made a series of amendments in its Office Action replies directed to the "ladder-shaped cross-sectional profile part" concept and relative spacing between fin structures. EX1002, 0131-0135, 0162-0174, 0239-0242, and 0238, 0244-0245. I have been told that these amendments moved the claims to allowance. EX1002, 0309.

34. In its statement of reasons for allowance, the Examiner stated that the "prior art fails to teach or suggest: 'wherein a first distance between adjacent top

corners of the first fin and the second fin of the first fin-shaped structures is less than a second distance between adjacent top corners of the third fin … and wherein the adjacent top corners are directly opposite each other.'" EX1002, 0310. But, as I discuss in further detail below, this limitation is not new.

35. As detailed below, all the claimed concepts—including the purported novel concept above—were well known before the '510 patent. In my opinion, if any of the prior art references applied herein been before the Examiner during prosecution, the '510 patent would not have been allowed.

C. Level of Ordinary Skill in the Art

36. I have been informed that a person of ordinary skill in the art ("POSA") is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

37. I have been instructed to assume a POSA is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

38. In my opinion, a POSA in reference to the '510 patent would have had a master's degree in electrical engineering, physics chemistry, materials science, or a related field and at least three years of work experience in semiconductor design

and manufacturing, including FinFETs. Additional relevant education could substitute for professional experience, and significant work experience or training could substitute for formal education.

39. I have not analyzed the priority date of the ’510 patent, but I note that the alleged earliest claim of priority listed on the face of the ’510 patent is its foreign application priority date of September 9, 2014. Because all the prior art discussed in this Declaration predates September 9, 2014, I have been asked for simplicity to treat September 9, 2014 as the priority date for the ’510 patent. I have also treated this date as the date from which to assess the knowledge available to a POSA.

D. Claim Construction

40. I have been told that, in an *inter partes* review, all claim terms must be given their ordinary and customary meaning as understood by a POSA at the time of the invention, in light of the specification and the prosecution history of the patent. Solely for the purposes of this Declaration in this *inter partes* review proceeding, I submit that all claim terms should receive their plain and ordinary meaning in the context of the ’510 patent specification.

VI. STATE OF THE ART

41. The ’510 patent discloses “fin-shaped structures having ladder-shaped cross-sectional profile parts in some areas, so that fin-shaped structures of different

heights and critical dimensions (CD) can be formed, in order to form transistors for each area that meet each area's specific electrical demands." Ex-1001, 1:35-40. The claimed fin shapes and arrangements were known before the '510 patent.

A. FinFET Characteristics

42. FinFET technology was known in the semiconductor area well before the time of the '510 patent. EX1009, 8-17; EX1010, 280-282; EX1011, 436. The term "FinFET" refers to a three-dimensional, non-planar field-effect transistor (FET). EX1009, 11; EX1010, 280-282. Below, I describe a representative FinFET as shown in Illustration 1.

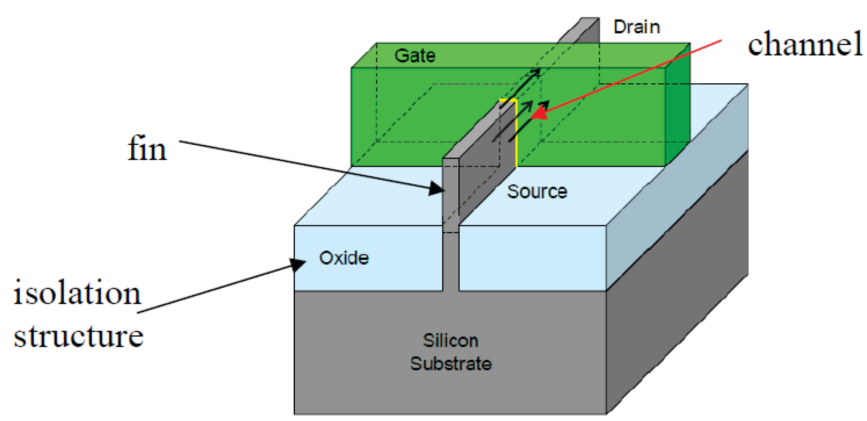


Illustration 1.

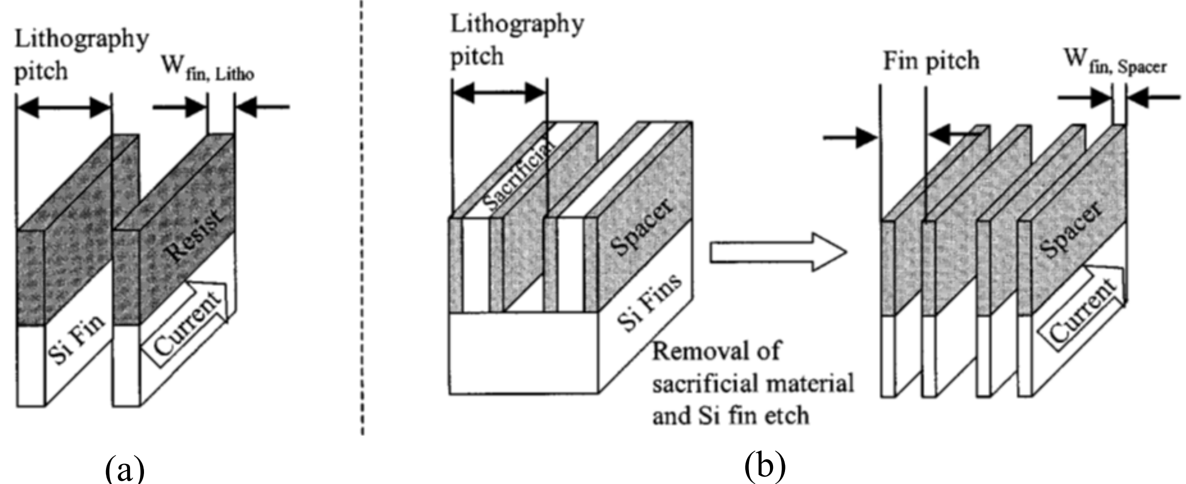
43. As shown in Illustration 1, the FinFET includes a semiconductor structure (commonly called a "fin") protruding from a substrate (e.g., a silicon substrate). EX1009, 66; EX1010, 282. The fin of the FinFET is formed by patterning and etching processes: "[a] thin fin of Si is created by lithography and

etching." EX1010, 281. The height of the fin above the substrate is determined by the fin etch step: "the fin height of bulk-based multi-gate devices are entirely determined by the fin etch step," where "fin height variation translates into transistor width variation." EX1009, 65. The FinFET also includes a gate structure surrounding the fin and source/drain regions on opposite sides of the gate structure. The gate structure is formed over the fin with patterning and etching processes: "gate material is deposited over the fin and the gate is patterned by lithography and etching." EX1010, 281. As shown in Illustration 1, a top portion of the fin under the gate structure acts as a channel of the FinFET for current flow between the source and drain regions. The isolation structure on the substrate surrounding a bottom portion of the fin electrically isolates the fin from adjacent fins. The height and the width of the fin top portion above the isolation structure and under the gate structure affect the drive current between the source and drain regions.

B. Fin Formation with Mandrel/Spacer Process

44. As early as 2002, mandrel/spacer processes for fin formation were well known. EX1011, Abstract. For example, Choi discloses a mandrel/spacer process that uses a sacrificial layer (e.g., a mandrel) and a spacer layer to pattern fins with critical dimension variations smaller than fins formed by conventional lithography processes. EX1011, Abstract. Benefits of the mandrel/spacer process include doubling fin density for a given lithography pitch and producing narrow

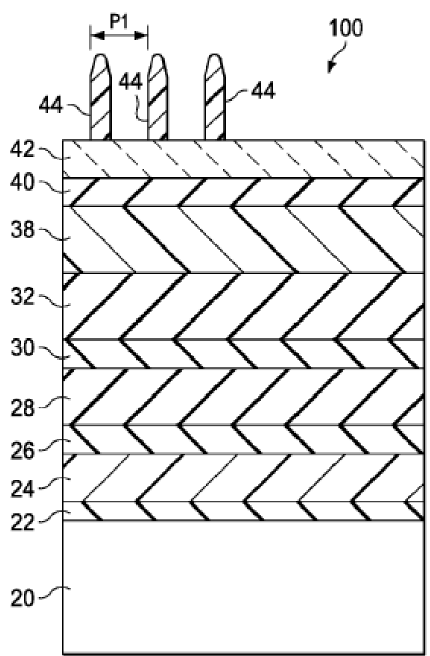
and uniform fins for FinFETs with critical dimension beyond the lithography limitation, as shown in Choi's Figure 2 (reproduced below). EX1011, Abstract, 436.

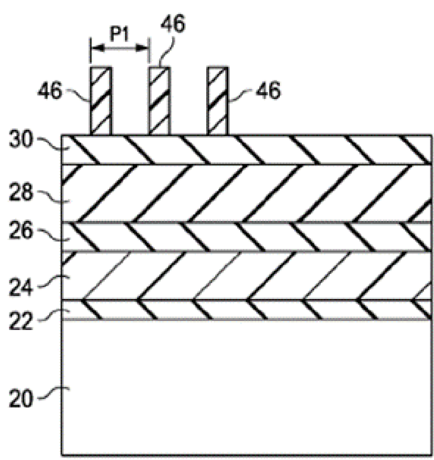


EX1011, FIG. 2 (comparison of fin density between (a) conventional lithography and (b) mandrel/spacer technology).

45. Generally, a mandrel/spacer process includes two stages. In a first stage, mandrels can be formed on a substrate using standard lithography techniques. Critical dimension of the mandrels, such as the minimum width of the mandrels and/or the minimal spacing between the mandrels, can be achieved within the limitation of lithography. In a second stage, spacers can be deposited on side surfaces of mandrels, which are subsequently removed. The spacers left on the substrate can be then used as masks for anisotropic etching of the substrate to form fin structures, whose critical dimension as defined by the thickness of the spacers can be smaller than the limitation of lithography.

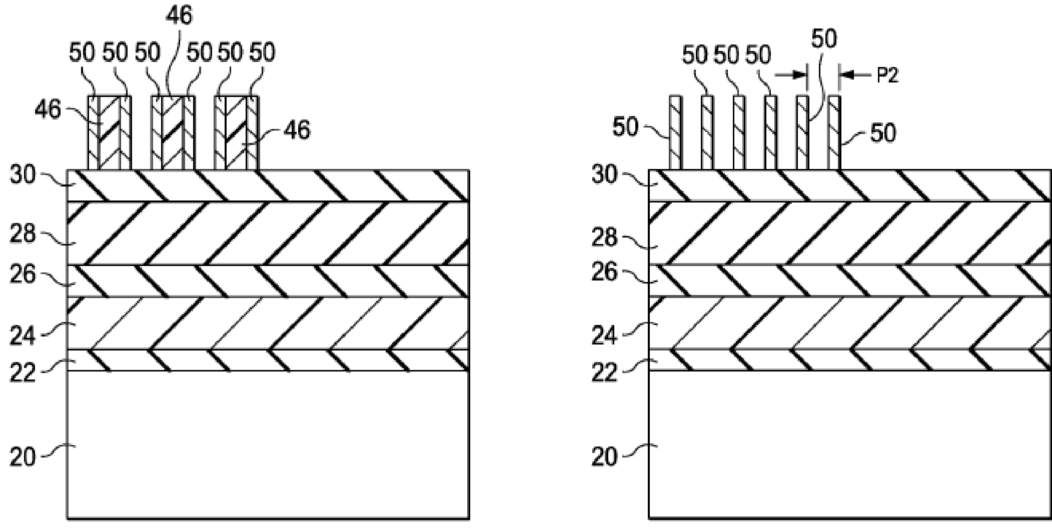
46. Chen provides details of a mandrel/spacer process to form fin structures with a minimum fin pitch. EX1012, Abstract. Referring to Chen's Figure 1 (reproduced below), a stack of layers, including oxide layers 22/26/30, hard masks 24/28/32/38, a silicon oxynitride layer 40, and a bottom anti-reflective coating (BARC) 42, is formed on a substrate 20, in which fin structures are to be formed. EX1012, ¶¶[0008]-[0010]. A patterned photo resist 44 having a minimum pitch P1 is formed on the stack of layers using a lithography method. EX1012, ¶ [0010]. Chen states that "the minimum pitch P1 of photo resist 44 may be close to, or equal to, the minimum pitch allowed by the technology for developing photo resist 44 and for performing the etch using photo resist 44 as an etching mask." EX1012, ¶[0010]. Further, referring to Chen's Figure 2 (reproduced below), photo resist 44 is used as a mask in a dry etching process to etch through BARC 42, layer 40, and hard masks 38/32, such that hard mask 32 is patterned into mandrels 46 separated from one another by pitch P1. EX1012, ¶ [0011].





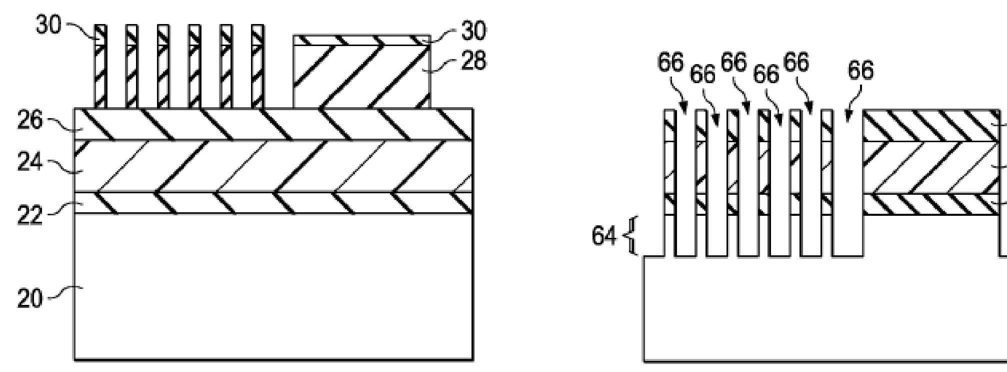
EX1012, FIGs. 1(left) and 2 (right).

47. Following the formation of mandrels 46, a spacer layer is conformally deposited on exposed surfaces of mandrels 46 and oxide layer 30 in an atomic layer deposition (ALD) process or a chemical vapor deposition (CVD) process. EX1012, ¶[0012]. Horizontal portions of the spacer layer on top surfaces of mandrels 46 and oxide layer 30 are then removed by an anisotropic etching process, leaving spacers 50 on side surfaces of mandrels 46, as shown in Chen's Figure 4 (reproduced below). EX1012, ¶[0013]. Mandrels 46 are then removed in an etching step with spacers 50 remained on oxide layer 30 and having a pitch P2, as shown in Chen's Figure 5 (reproduced below). EX1012, ¶[0013]. Pitch P2 is smaller than pitch P1. EX1012, ¶[0013]. The thickness of spacers 50 can be less than pitch P1 and the thickness of mandrels 46. EX1012, ¶[0012].



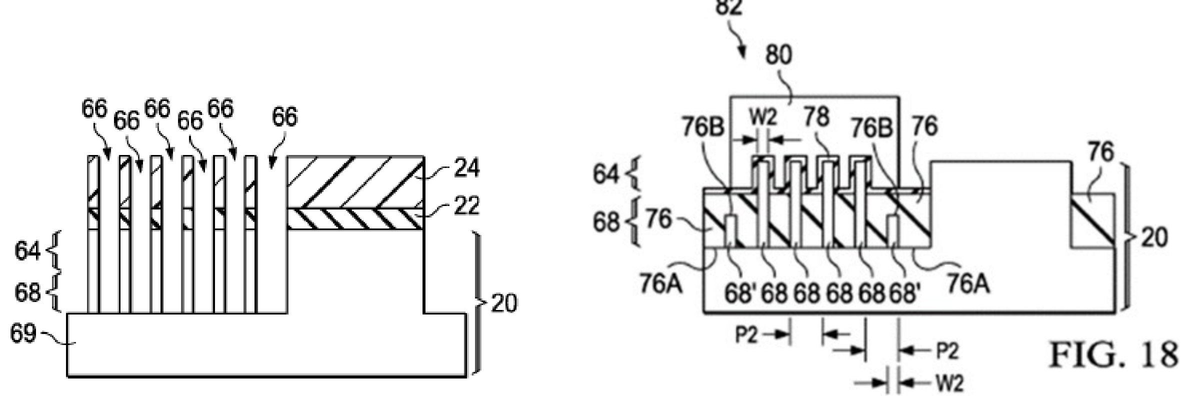
EX1012, FIGs. 4 (left) and 5 (right).

48. After a series of subsequent etching processes, as shown in Chen's Figure 11 (reproduced below), "hard mask layer 28 is etched using spacers 50," and "[t]he patterns of spacers 50 … are thus transferred into hard mask 28." EX1012, ¶[0017]. Similarly, "hard mask 28 is used as an etching mask to etch underlying layers including pad oxide layer 22, silicon nitride layer 24, and PE oxide layer 26," as well as substrate 20. EX1012, ¶[0018]. As a result, the portions of substrate 20 underlying spacers 50 form fin structures 64, as shown in Chen's Figure 12 (reproduced below). EX1012, ¶ [0018].



EX1012, FIGs. 11 (left) and 12 (right).

49. Substrate 20 can be further etched under the same hard mask pattern to form fin extensions 68 underneath fin structures 64, as shown in Figure 13 below. EX1012, ¶[0019]. As a result, fins with uniform dimensions and uniform spacing are formed by the mandrel/spacer process, as shown in Chen's Figure 18 (reproduced below), where "pitch P2 of fin extension residues 68' and its neighboring fin 64 may be the same as pitch P2 between neighboring fin extensions 68" and "widths W2 of fin extensions 68 may be substantially the same as widths W2 of fin extension residues 68'." EX1012, ¶[0023]. The space between fin extensions 68 and below fin structures 64 are then filled with a dielectric material to form shallow trench isolation (STI) regions 76. EX1012, ¶[0022]. A FinFET 82 is then formed on fin structures 64 above STI regions 76. EX1012, ¶[0023]. In particular, gate dielectric 78 and gate electrode 80 are formed over fin structures 64 to form a gate structure of FinFET 82. EX1012, ¶[0023].



EX1012, FIGs. 13 (left) and 18 (right).

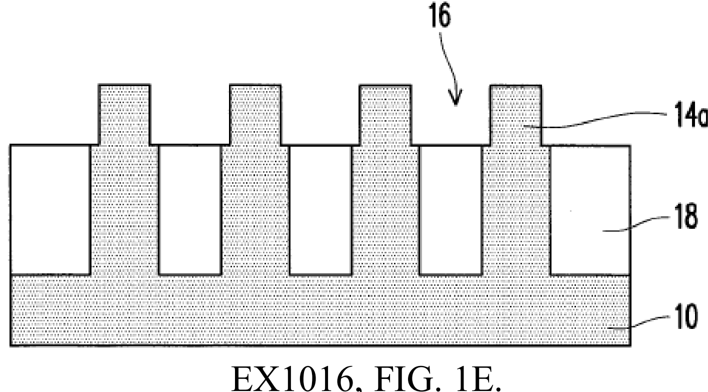
C. Fin Shaping Techniques

50. At the time of the ’510 patent, it was well known that different fin shapes can affect the electrical characteristics of FinFETs. EX1013, ¶[0013]; EX1014, ¶[0005]; EX1015, Abstract. For example, FinFETs with fins having different widths provide different threshold voltages. EX1005, ¶[0053]. In another example, FinFETs have increased drive current because of increased channel widths including fin sidewall portions and top surfaces, and FinFETs with fins having different heights provide different drive currents. EX1017, ¶¶[0003], [0024]. Accordingly, fin width and fin height can be adjusted to achieve desired FinFET electrical characteristics for particular circuit design requirements.

51. Before the time of ’510 patent, Tung described a method of adjusting widths of fin upper portions. EX1016, Abstract. Tung’s method included “forming a hard mask material layer on a substrate,” “patterning the hard mask material

layer to form a first hard mask layer," and removing "a portion of the substrate" to form two trenches and "a fin between the trenches." EX1016, ¶[0008]. Afterwards, Tung explained that "an insulating layer is formed in each trench" to "expose an upper portion of the fin" and "the upper portion of the fin is trimmed, so that the trimmed upper portion is narrower than a lower portion of the fin." EX1016, ¶[0008].

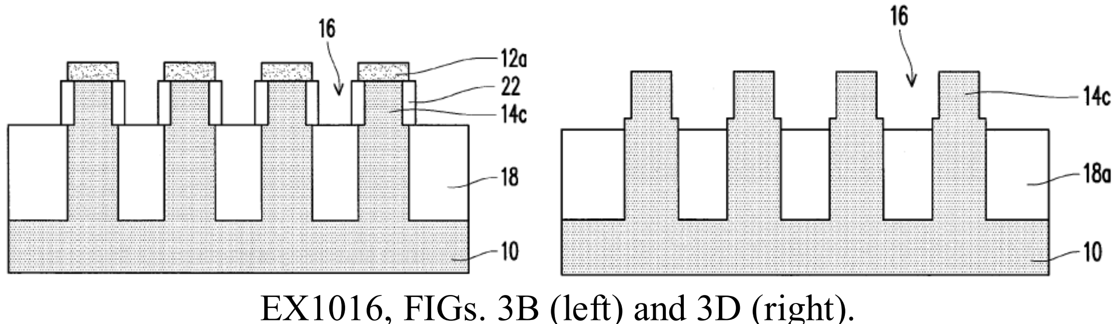
52. In one embodiment of Tung, as shown in Figure 1E (reproduced below), Tung discloses that upper portion of each fin 14a not covered by a hard mask layer is directly etched by an anisotropic etching process to form a trimmed upper portion narrower than the fin's lower portion. EX1016, ¶[0039].



EX1016, FIG. 1E.

53. In another embodiment of Tung, the trimming of the upper portion of the fin can include an oxidation process to "oxidize[] the sidewall of the upper portion of each fin 14 exposed by the hard mask layer 12a," as shown in Tung's Figure 3B (reproduced below). EX1016, ¶[0054]. Subsequently, an etching process removes the oxide layer to trim the upper portion of the fin: "the oxides 22 are

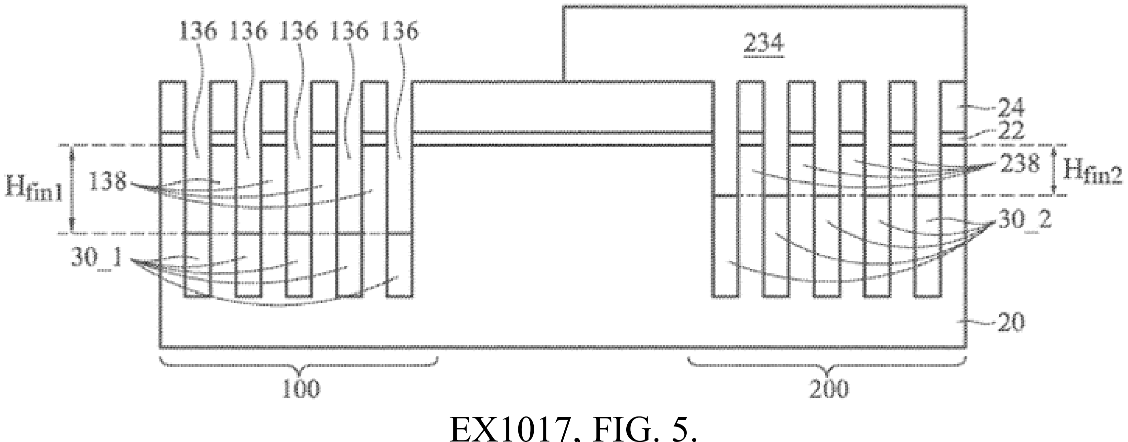
[re]moved, so as to expose a sidewall of the upper portion of each fin 14c." EX1016, ¶[0056]. Additionally, insulating layer 18 is also etched during the etching process: "each insulating layer 18 is a silicon oxide layer, and a portion of the insulating layers 18 are removed during the step of removing the oxides 22." EX1016, ¶[0056]. Therefore, after the etching process, the fin structure has a narrower upper portion, as shown in Figure 3D (reproduced below), "[e]ach remaining fin 14c is a fin structure in the shape of an inverse T having a narrower upper portion and a wider lower portion." EX1016, ¶[0056]. In addition to setting a threshold voltage of the subsequently-formed FinFET, the trimmed upper portion of each fin 14c "provides a fin structure to prevent the epitaxial layers respectively around the neighboring fin structures from connecting to each other." EX1016, ¶[0007].



EX1016, FIGs. 3B (left) and 3D (right).

54. Also, before the time of '510 patent, Lee described a method of forming fins with different heights to separately tune device performance. EX1017, ¶[0012]. The method includes forming shallow trench isolation (STI) regions in a

substrate and recessing top surfaces of the STI regions in different device areas to different depths. EX1017, ¶¶[0016]-[0019]. During the recessing of STI regions, STI regions of one device region can be masked by a photo resist to etch exposed STI regions in another device region: “device region 100 is masked by photo resist 134, leaving device region 200 exposed,” where “exposed STI regions 30_2 are then recessed through an etching step.” EX1017, ¶[0017]. After recessing the STI regions, portions of the substrate between the recesses become fins with different heights. EX1017, ¶¶[0017]-[0018]. For example, as shown in Lee’s Figure 5 (reproduced below), fins 138 in device region 100 have a fin height H_{fin1} greater than fin height H_{fin2} of fins 238 in device region 200. EX1017, ¶¶[0017]-[0018]. Different fin heights of the FinFETs can tune the device performance in different device regions: “[w]ith the FinFETs in different device regions having different fin heights, it is easier to tune the performance of devices in different device regions.” EX1017, ¶[0024].



EX1017, FIG. 5.

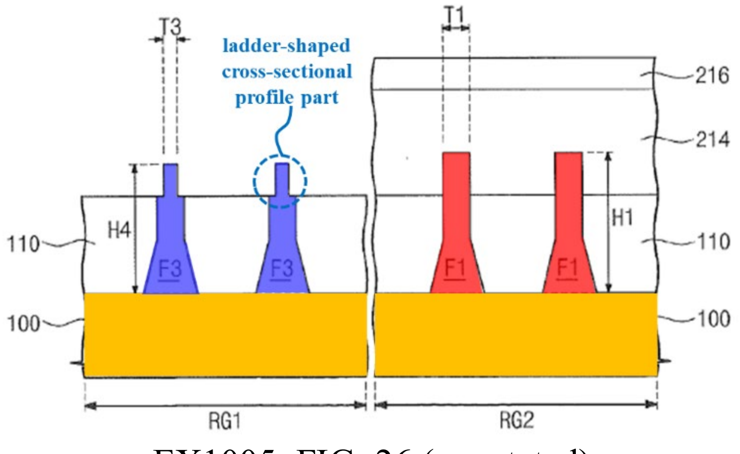
VII. OVERVIEW OF THE APPLIED REFERENCES

A. Oh

55. U.S. Patent Appl. Pub. No. 2013/0244392 to Oh et al. ("Oh"; EX1005) was filed on February 28, 2013 and published on September 19, 2013. EX1005, Cover. Oh is directed to forming FinFETs having different fin widths. EX1005, Title, ¶[0004]. In my opinion, Oh is analogous art because Oh is in the same field of endeavor as the '510 patent and reasonably pertinent to at least one problem the '510 patent purports to address—the formation of FinFETs. EX1001, 1:34-40; EX1005, ¶[0004].

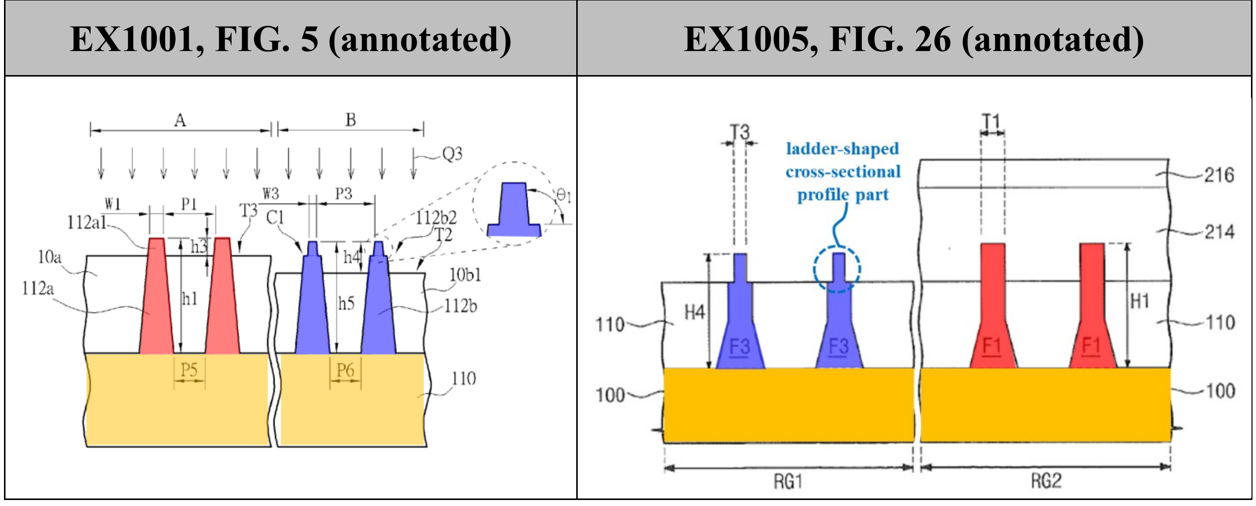
56. Oh discloses a method that includes "forming fin-shaped transistor channel regions protruding from first and second regions of a substrate" and "selectively altering respective widths of ones of the fin-shaped transistor channel regions protruding from the first region while maintaining respective widths of ones of the fin-shaped transistor channel regions protruding from the second region." EX1005, ¶[0005]. Oh states that "the changing of the widths of the fin portions may include etching the fin portions provided on the first region." EX1005, ¶[0018]. Oh also states that where "[t]he device isolation layers may be formed before the etching of the fin portions," "the etching of the fin portions may include etching top surfaces and upper sidewalls of the fin portions exposed by the first mask pattern and the device isolation layers." EX1005, ¶[0018]. Oh discloses

an embodiment of FinFETs having different fin widths in Figure 26 (reproduced below with annotations).



EX1005, FIG. 26 (annotated).

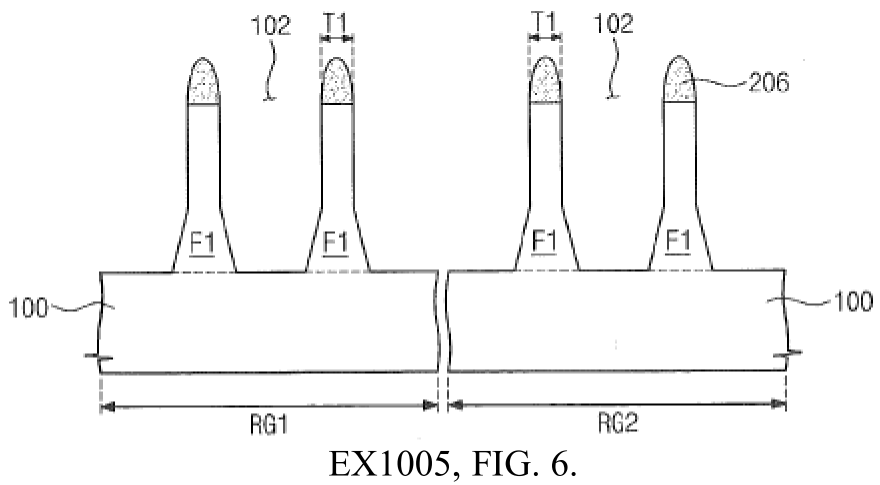
57. Comparing Figure 26 of Oh to Figure 5 of the '510 patent, it is my opinion that Oh teaches the same fin-shaped structure described in the '510 patent. The fin-shaped structures from Oh and the '510 patent are shown side-by-side below, which both have a **substrate** (orange; 100 and 110) with **first fin-shaped structures** (red; first fin portions F1 and 112a) and **second fin-shaped structures** (blue; third fin portions F3 and 112b). Similar to the '510 patent's two adjacent **first fin-shaped structures 112a** (red) in a first area A and two adjacent **second fin-shaped structures 112b** (blue) in a second area B, Oh has two adjacent **first fin portions F1** (red) in a second region RG2 and two adjacent **third fin portions F3** (blue) in a first region RG1, respectively.



58. Also, similar to the '510 patent's ladder-shaped cross-sectional profile parts of **second fin-shaped structures 112b** (blue) shown in dashed line inset in Figure 5 above, Oh's **third fin portions F3** (blue) are also shaped to include ladder-shaped cross-sectional profile parts, as shown in Figure 26 above. *Compare* EX1005, ¶[0070] *with* EX1001, 5:13-44. The '510 patent states that the bending angle θ1 in its ladder-shaped cross-sectional profile part can be larger than or equal to 90°, which is similar to the 90° bending angle shown in Oh's ladder-shaped cross-sectional profile part. *Compare* EX1005, ¶[0070] *with* EX1001, 5:16-18. Oh explains that "upper sidewalls of the first fin portions F1 with the first width T2 may be etched to form the third fin portions F3," where "the etching process may include an isotropy etching process." EX1005, ¶[0070].

59. Oh uses a mandrel/spacer process described in Figures 1-6 to form uniform fins. EX1005, ¶¶[0050], [0059], [0073]. Referring to Oh's Figure 6

(reproduced below), Oh explains that "the substrate 100 may be etched using the second mask patterns 206 as an etch mask to form first fin portions F1 (also referred to herein fin-shaped transistor active regions or channel regions) having a first width T1." EX1005, ¶[0050]. Oh explains that "the first fin portions F1 formed by the method described with reference to FIGS. 1 through 6 … have the same width as each other." EX1005, ¶[0059]. Oh's fin-shaped structures in Figure 26 (reproduced above with annotations) uses the same mandrel/spacer process as described in Figures 1-6: "FIGS. 25 and 26 … [are] described with reference to FIGS. 13 and 14" and "FIGS. 13 and 14 … [are] described with references to FIGS. 1 through 6." EX1005, ¶¶[0059], [0069].



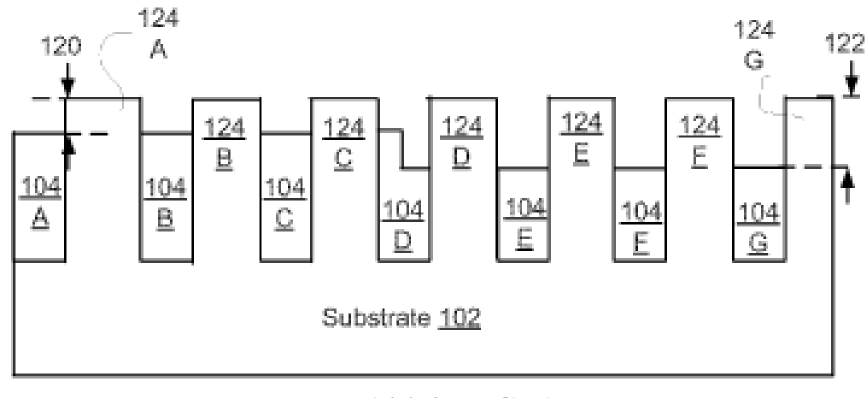
EX1005, FIG. 6.

B. Rachmady

60. U.S. Patent Appl. Pub. No. 2010/0276756 to Rachmady et al. ("Rachmady"; EX1006) was filed on July 15, 2010 and published on November 4, 2010. EX1006, Cover. Rachmady is directed to forming FinFETs having different

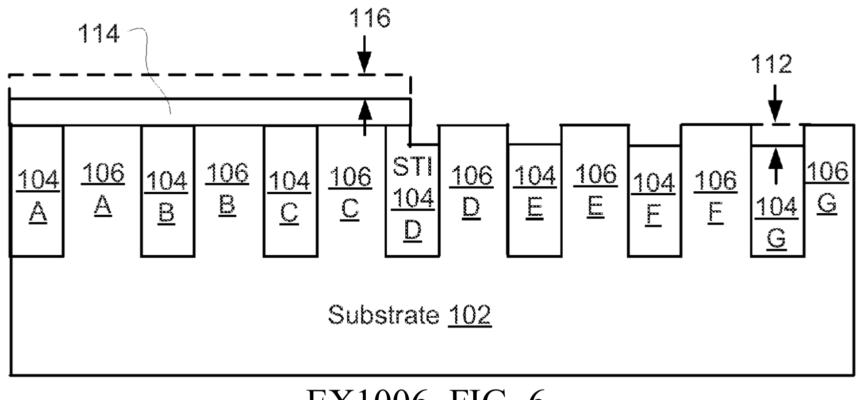
fin heights. EX1006, Title, ¶[0002]. In my opinion, Rachmady is analogous art because Rachmady is in the same field of endeavor as the '510 patent and reasonably pertinent to at least one problem the '510 patent purports to address—the formation of FinFETs. EX1001, 1:34-40; EX1006, ¶[0002].

61. Rachmady discloses a selective fin height process to adjust drive current in FinFETs. EX1006, Abstract. Referring to Figure 1 (reproduced below), Rachmady discloses that "[s]uch an ability to have fins 124 of different height allows multi-gate transistors to be made on the fins 124 with different desired properties." EX1006, ¶[0022]. Rachmady explains that "[a]s the drive current of a transistor is dependent on the gate channel 'width' of a multi-gate transistor, and the 'width' may be made greater by use of a taller fin 124 without increasing the area of the transistor, selectable multi-height fins 124 allow the transistors with the same area to have selected drive currents based on the fin heights." EX1006, ¶[0022].



EX1006, FIG. 1.

62. Rachmady discloses a selective etching and mask process to remove portions of isolation regions 104 while keeping adjacent fin portions intact. EX1006, ¶[0029]. Referring to Rachmady's Figure 6 (reproduced below), Rachmady explains that "[d]ifferent etchants and/or different materials may be used, selected based on the desired etchant rate difference between the mask layer 108 and the isolation regions 104, and the etch selectivity to etch the mask layer 108 and isolation regions 104 while leaving the substrate 102 and pre-fin regions 106 substantially intact." EX1006, ¶[0029]. The structure shown in Rachmady's Figure 6 is a precursor structure to Rachmady's Figure 1 (reproduced above): "FIGS. 2 through 9 are cross sectional side views that illustrate how fins 124 of different heights on the same substrate 102 [in FIG. 1] may be formed." EX1006, ¶[0023].



EX1006, FIG. 6.

C. Wann

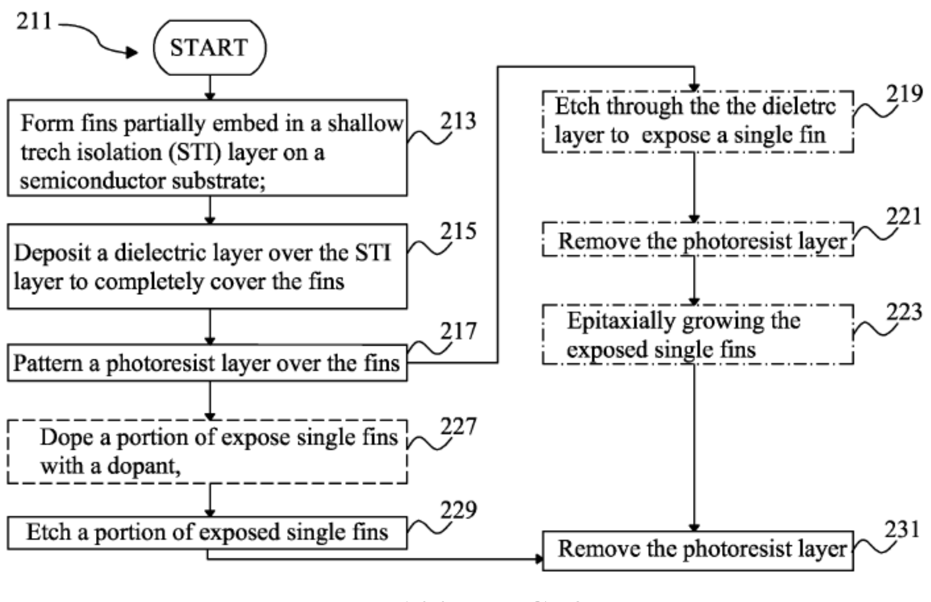
63. U.S. Patent Appl. Pub. No. 2013/0093026 to Wann et al. ("Wann";

EX1007) was filed on October 14, 2011 and published on April 18, 2013. EX1008, Cover. Wann is directed to forming FinFETs having shaped and regular fins. EX1007, Abstract. In my opinion, Wann is analogous art because Wann is in the same field of endeavor as the ’510 patent and reasonably pertinent to at least one problem the ’510 patent purports to address—the formation of FinFETs. EX1001, 1:34-40; EX1007, Abstract.

64. Wann “pertain[s] to a selective fin-shaping process to allow individual fin width and fin height control.” EX1007, ¶[0019]. Wann uses a mandrel/spacer process to form regular fins “hav[ing] the same height and width dimensions.” EX1007, ¶[0015]. Wann explains that “[b]y shaping one or more fins in a FinFET, the channel width of a FinFET may vary beyond an integer multiple of a single fin dimension.” EX1007, ¶[0019]. As a result, Wann states that the benefits of its selective fin-shaping process “may include improved circuit design flexibility and FinFET process margin for designers and foundries that are transferring from a planar-based design to a FinFET-based design.” EX1007, ¶[0019].

65. Referring to Wann’s Figure 2 (reproduced below), Wann discloses “a process flow 211 for selective fin-shaping.” EX1007, ¶[0020]. Wann’s process flow 211 can form enlarged fins, in which operations 213, 215, 217, 219, 221, 223, and 231 can be performed. EX1007, ¶[0038]. To form shorter and/or narrowly shaped fins, Wann’s process flow 211 can perform operations 213, 217, 229, and

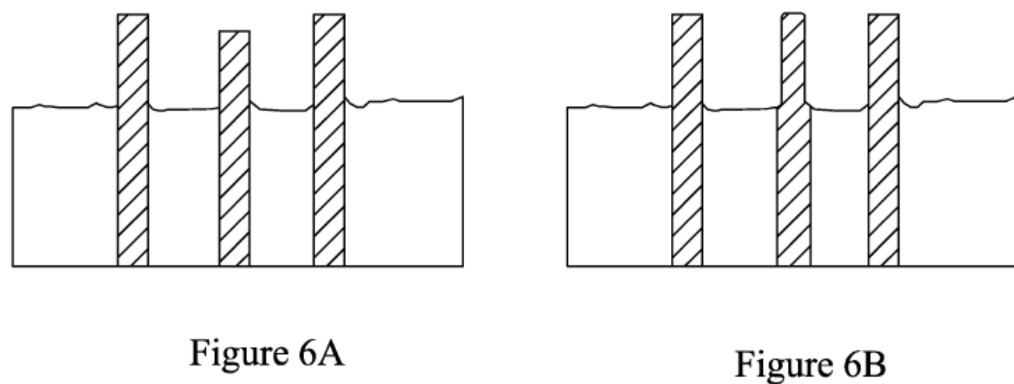
231. EX1007, ¶¶[0022]-[0037]. Operation 215 can be omitted as "[t]he optional dielectric layer is used if the one or more fins are to be enlarged." EX1007, ¶[0021]. Wann further discloses that "in optional (broken line) operation 227 a portion of the exposed single fin is doped with a dopant." EX1007, ¶[0023]. As such, operation 227 may be omitted. With or without operation 227, "a portion of the exposed single fins is etched and removed" in operation 229 to form shorter and/or narrowly-shaped fins. EX1007, ¶¶[0025], [0030].



EX1007, FIG. 2.

66. Wann discloses examples of three-fin fin-shaped structures in Wann's Figures 6A and 6B (reproduced below) formed using the selective fin-shaping process flow 211. Wann states that "[i]n FIG. 6A, the FinFET includes 3 fins, with 2 regular fins and 1 shaped fin," where "[t]he shaped fin has a shorter top portion." EX1007, ¶[0035]. Wann also states that "[i]n FIG. 6B, the FinFET also includes 3

fins, with 2 regular fins and 1 shaped fin," where "[t]he shaped fin has a narrower top portion that may be the same, slightly shorter, or longer than the neighboring regular fins." EX1007, ¶[0035]. Wann also states that "[t]he bottom portions of all three fins are substantially the same, because the bottom portions are not shaped." EX1007, ¶[0035]. Though Wann's Figures 6A and 6B do not appear to illustrate the removal of STI layer surrounding the shaped fin, Wann discloses that "[w]hile the shaped fin may be shorter than the regular fins, the top portion of the shaped fin may be the same length or longer than the top portion of regular fins because the STI layer is also etched and more of the top portion of the shaped fin may be exposed." EX1007, ¶[0035].



EX1007, FIGs. 6A and 6B.

67. Wann's selective fin-shaping process flow 211 is applicable to FinFETs with any number of fins and any fin arrangement. EX1007, ¶[0041]. Wann states that "[t]he present disclosure is not limited [to] a FinFET having a particular number of fins," and that "[i]n reality a FinFET may have any number of

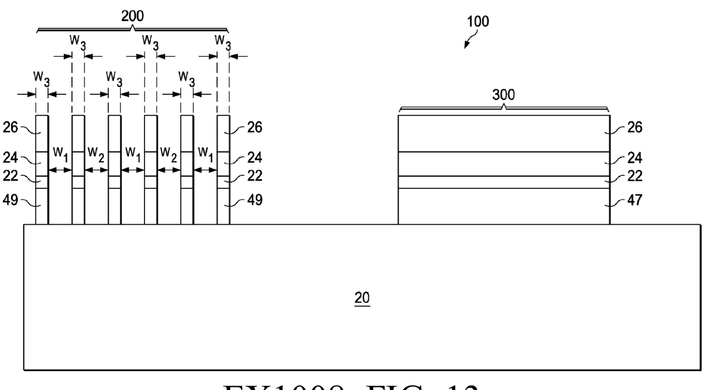
fins from 1 to several or even hundreds." EX1007, ¶[0041]. For example, Wann discloses "a five-fin FinFET [that] may have 2 regular fins, 2 fins shaped a particular way, and 1 fin shaped a different way," though Wann does not provide a figure for the disclosed five-fin FinFET. EX1007, ¶[0042]. With regard to fin arrangement, Wann states that "[t]he apparatus may include many FinFETs of different sizes having different number of fins," where "[s]ome FinFETs may have shaped fins and some FinFETs may not." EX1007, ¶[0042]. Wann further states that "for FinFETs having more than 3 fins, the shaped fin may be spaced apart from regular fins by 2 regular fins" and that "more than one fin may be shaped in the same opening." EX1007, ¶[0041]. For example, Wann discloses "a five-fin FinFET [that] may have 2 regular fins, 2 fins shaped a particular way, and 1 fin shaped a different way." EX1007, ¶[0042].

D. Lin

68. U.S. Patent Appl. Pub. No. 2014/0256093 to Lin et al. ("Lin"; EX1008) was filed on March 14, 2013 and published on September 11, 2014. EX1008, Cover. Lin claims the benefit of a provisional application filed on March 11, 2013. EX1008, Cover. Lin is directed to forming FinFETs. EX1008, Abstract. In my opinion, Lin is analogous art because Lin is in the same field of endeavor as the '510 patent and reasonably pertinent to at least one problem the '510 patent purports to address—the formation of FinFETs. EX1001, 1:34-40; EX1008,

Abstract.

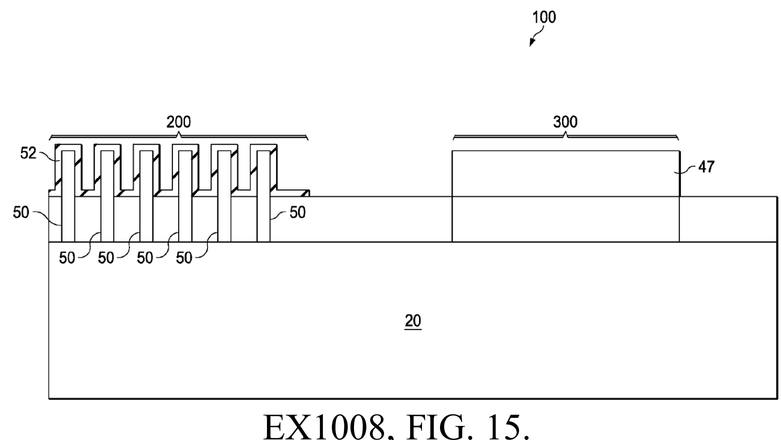
69. Lin discloses a mandrel/spacer process that forms fins with uniform dimensions and uniform spacing from one another. EX1008, ¶[0062]. Lin describes the mandrel/spacer process in Figures 1 through 15, which transfers a "pattern to substrate 20 … thereby forming semiconductor strips 49" as shown in Lin's Figure 13 (reproduced below). EX1008, ¶¶[0025]-[0051]. Lin explains that "[t]he spacing between the semiconductor strips 49 W_1 and W_2 are defined by the widths W_1 and W_2 between the fin spacers 42 (see FIGS. 5 and 8)." EX1008, ¶[0051]. Lin further explains that "the width W_1 is substantially equal to the width W_2." EX1008, ¶[0051].



EX1008, FIG. 13

70. Referring to Lin's Figure 15 (reproduced below), Lin describes the formation of uniform fins: "[t]he seventh dielectric layer 51 may be deposited over the semiconductor strips 49" and "thinned to below the level of the tops of the semiconductor strips 49" to form "fins 50 extending above a top surface of the

seventh dielectric layer 51." EX1008, ¶¶[0054]-[0055]. Lin states that in its mandrel/spacer process "the spacing and depth between the fins 50 are better controlled and may be substantially equal between all of the fins 50." EX1008, ¶[0062].



EX1008, FIG. 15.

VIII. GROUNDS OF UNPATENTABILITY

71. I provide my analysis below on the following grounds:

A. Ground 1: Oh renders obvious claims 1, 2, and 6 of the '510 patent;

B. Ground 2: The combination of Oh and Rachmady renders obvious claims 3-5 of the '510 patent; and

C. Ground 3: The combination of Wann and Lin renders obvious claims 1-6 of the '510 patent.

In providing my analysis, I refer to the '510 patent claim limitations using the claim mapping in the Claims Appendix, which can be found in Section IX of this

Declaration.

A. Ground 1: Oh renders obvious claims 1, 2, and 6.

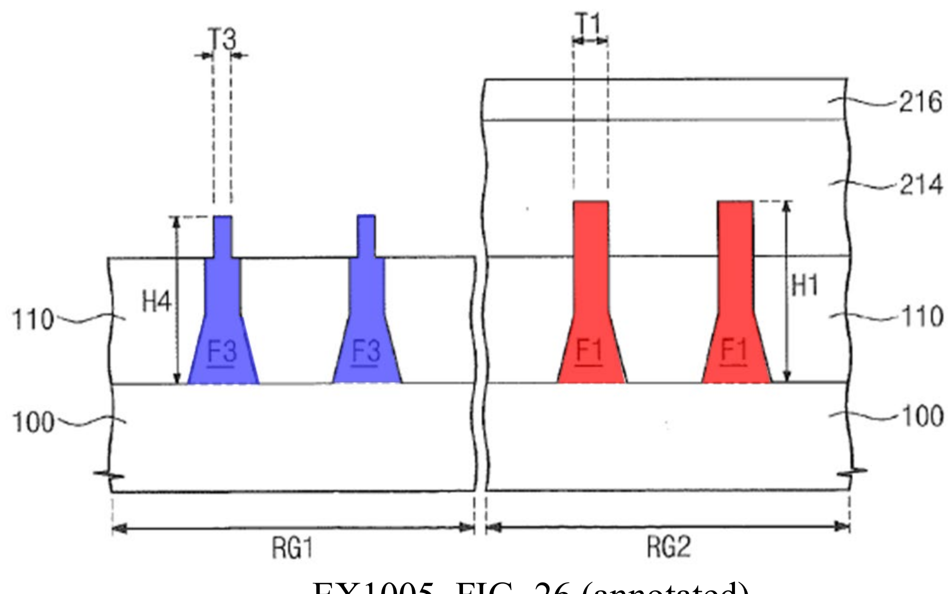
1. Independent Claim 1

a. [1.P]: A fin-shaped structure, comprising:

72. Oh discloses a fin-shaped structure and "relate[s] to field effect transistors, and in particular, to methods of fabricating fin field effect transistors," where "some of the field effect transistors are formed to include fin portions having different widths from each other." EX1005, ¶¶[0002], [0004]. Oh discloses methods of forming field effect transistors, where "[t]he method includes preparing a substrate with a first region and a second region, forming fin portions on the first and second regions, each of the fin portions protruding from the substrate and having a first width, forming a first mask pattern to expose the fin portions on the first region and cover the fin portions on the second region, and changing widths of the fin portions provided on the first region." EX1005, Abstract.

73. In one of its embodiments, Oh describes fin-shaped structures with reference to Figures 25-28. EX1005, ¶[0068]. Oh's Figure 26 (reproduced below with annotations) is a cross-sectional view taken along line A-A' of Figure 25. EX1005, ¶[0068]. The fin-shaped structure in Oh's Figure 26 shows **first fin portions F1** (red) with lower parts in a device isolation layer 110 and **third fin portions F3** (blue) with lower parts in device isolation layer 110. EX1005,

¶[0070].



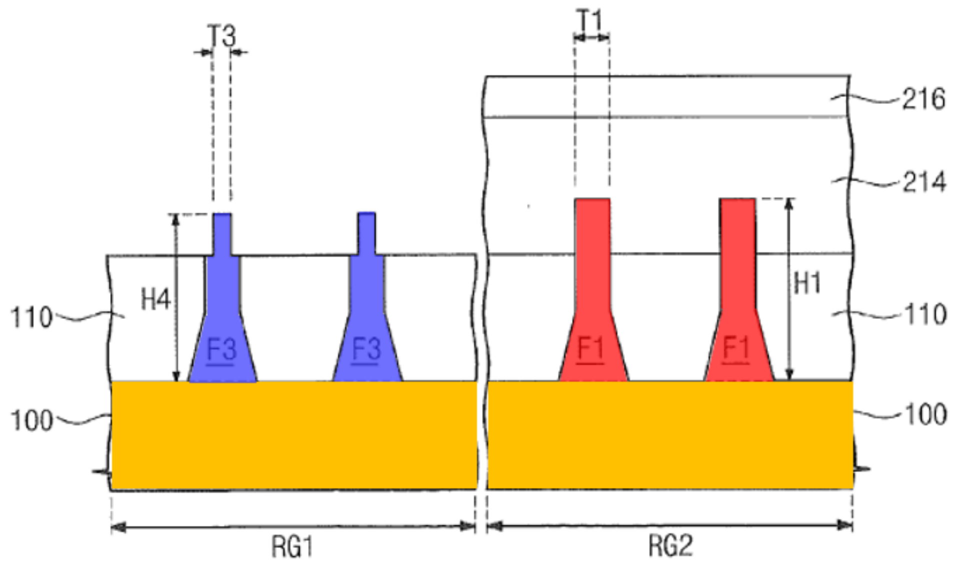
EX1005, FIG. 26 (annotated).

74. Thus, in view of the above, Oh discloses limitation [1.P].

b. [1.a]: a substrate having a plurality of first fin-shaped structures and a plurality [of] second fin-shaped structures, and the first fin-shaped structures comprising a first fin and a second fin, the second fin-shaped structures comprising a third fin and a fourth fin,

75. Oh discloses a substrate with first fin-shaped structures and second fin-shaped structures, where the first fin-shaped structures include a first fin and a second fin and where the second fin-shaped structures include a third fin and a fourth fin. Specifically, referring to Oh's Figure 26 (reproduced below with annotations), Oh shows a **substrate 100** (orange; "*substrate*") has **first fin portions F1** (red; "*a plurality of first fin-shaped structures*") and **third fin portions F3** (blue; "*a plurality [of] second fin-shaped structures*"). As shown in

Oh's Figure 26, **substrate 100** (orange) includes a first region RG1 with **third fin portions F3** (blue) thereon and a second region RG2 with **first fin portions F1** (red). EX1005, ¶[0047]. Also, as shown in Oh's Figure 26, **first fin portions F1** (red) include two fins ("*a first fin and a second fin*") and **third fin portions F3** (blue) include two fins ("*a third fin and a fourth fin*"). Below, I describe how **first fin portions F1** (red) and **third fin portions F3** (blue) are formed.

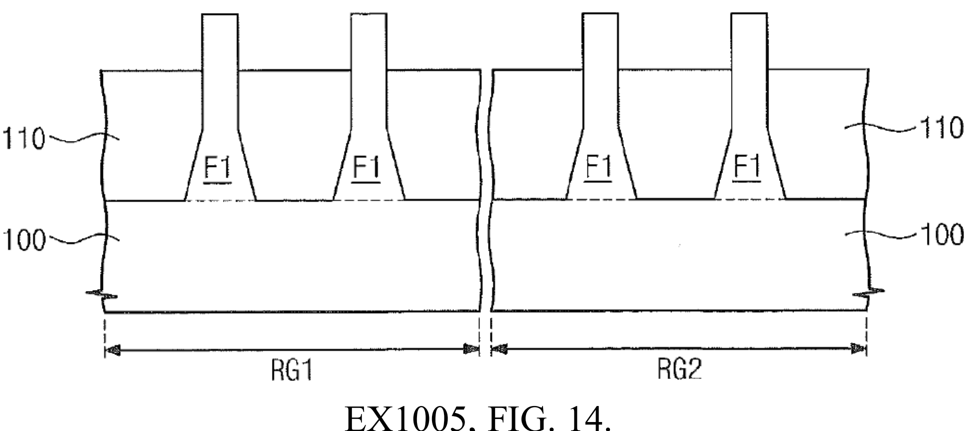


EX1005, FIG. 26 (annotated).

76. Initially, the fins in both first region RG1 and second region RG2 are formed as shown in Oh's Figure 14 (reproduced below). EX1005, ¶[0059]. The structure shown in Oh's Figure 14 is a precursor structure to Oh's Figure 26: "[r]eferring to FIGS. 25 and 26, an etching mask pattern 214 may be formed on the structure described with reference to FIGS. 13 and 14." EX1005, ¶[0069].

77. Referring to Oh's Figure 14, the first fin portions F1 are formed using

an etching process: "[t]he first fin portions F1 may be formed by an etching process using a mask pattern provided on the substrate 100 as an etch mask." EX1005, ¶[0059]. The first fin portions F1 can have the same width, where a device isolation layer 110 covers the lower parts of first fin portions F1: "[f]or example, the first fin portions F1 may be formed by the method described with reference to FIGS. 1 through 6, and thus, have the same width as each other," and "[t]he device isolation layers 110 may be formed to cover lower sidewalls of the first fin portions F1." EX1005, ¶[0059]. Since the lower parts of the first fin portions F1 are covered, upper parts of the first fin portions F1 are exposed, as shown in Oh's Figure 14: "[t]he formation of the device isolation layers 110 may include forming a dielectric layer to cover the first and second regions RG1 and RG2, and then, etching the dielectric layer to expose upper portions of the first fin portions F1." EX1005, ¶[0059].



EX1005, FIG. 14.

78. After forming the precursor structure shown in Oh's Figure 14

(reproduced above), referring to Oh's Figure 26 (reproduced above with annotations), the two fins in **third fin portions F3** (blue) in first region RG1 are shaped. Here, **third fin portions F3** (blue) in first region RG1 are formed from first fin portions F1 in first region RG1 shown in Oh's Figure 14 (reproduced above) with an etching process: "an etching mask pattern 214 may be formed on the structure described with reference to FIGS. 13 and 14," and "[t]he etching mask pattern 214 may be formed to cover the second region RG2 and expose the first region RG1." EX1005, ¶[0069]. Oh explains that "[t]he formation of the etching mask pattern 214 may include sequentially forming an etch mask layer and the fourth mask patter 216 on the structure provided with first fin portions F1, and then, removing the etch mask layer from the first region RG1 using the fourth mask pattern 216 as an etch mask." EX1005, ¶[0069].

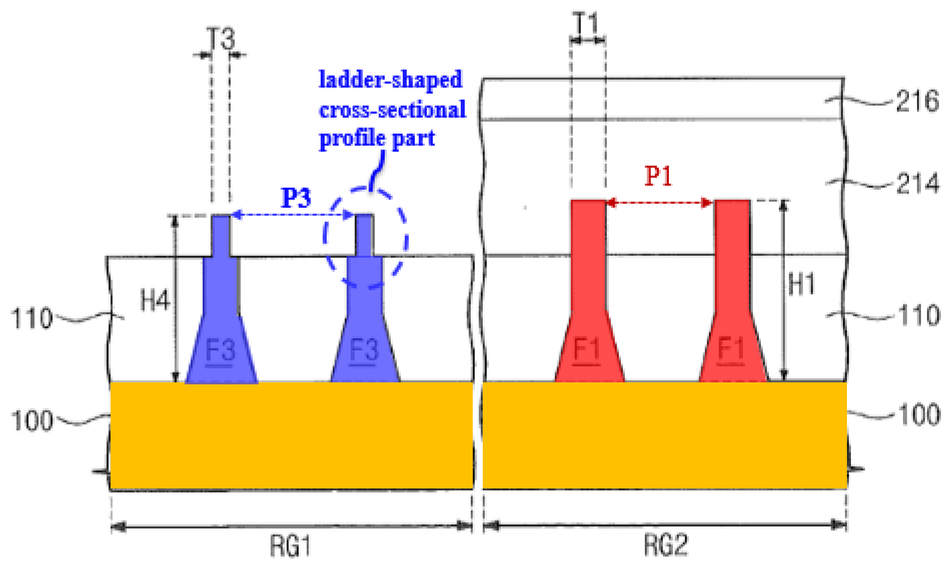
79. Next, upper sidewalls of the first portions F1 in the first region RG1 are etched to form the third fin portions F3 as shown in Oh's Figure 26 (reproduced above with annotations): "[t]he upper widths of the first fin portions F1 provided on the first region RG1 may be increased or decreased," where "upper sidewalls of the first fin portions F1 with the first width T1 may be etched to form the third fin portions F3, whose upper portions have the third width T3." EX1005, ¶[0070]. Due to the etching process, the heights of **first fin portions F1** (red) and **third fin portions F3** (blue) can be different: "[a]s a result of the etching process,

the third fin portions F3 may have a fourth height H4 smaller than the first height H1 of the first fin portions F1." EX1005, ¶[0070].

80. Thus, in view of the above, Oh discloses limitation [1.a].

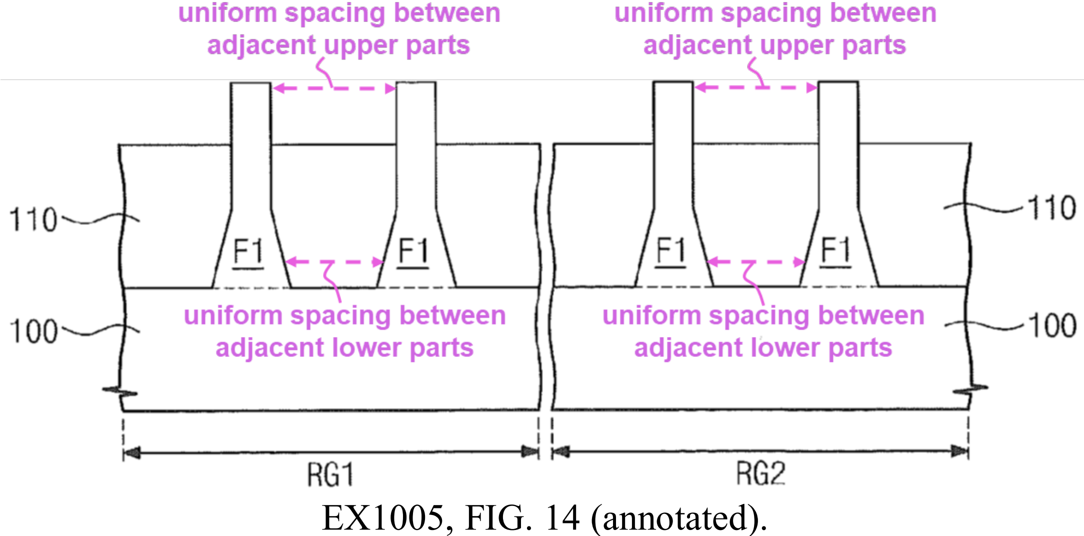
c. [1.b]: wherein a first distance between adjacent top corners of the first fin and the second fin of the first fin-shaped structures is less than a second distance between adjacent top corners of the third fin and the fourth fin of the second fin-shaped structures

81. Oh discloses or renders obvious a first distance between adjacent top corners of the two fins in the first fin portions F1 is less than a second distance between adjacent top corners of the two fins in the third fin portions F3. Specifically, referring to Oh's Figure 26 (reproduced below with annotations), in my opinion, a POSA would have understood that a **distance P1** (red; "*a first distance*") between adjacent top corners of the two fins in **first fin portions F1** (red; "*the first fin and the second fin of the first fin-shaped structures*") is less than a **distance P3** (blue; "*a second distance*") between adjacent top corners of the two fins in **third fin portions F3** (blue; "*the third fin and the fourth fin of the second fin-shaped structures*"). Below, I describe **distance P1** (red) and **distance P3** (blue).



EX1005, FIG. 26 (annotated).

82. Due to Oh's fin-shaping process, the **first distance P1** (red) is shorter than the **second distance P3** (blue). As I discuss in Section VIII.A.1.d below, in my opinion, Oh discloses or renders obvious that the initial formation of first fin portions F1 in first region RG1 and second region RG2 results in a distance between adjacent two fins (lower and upper parts) in first region RG1 being the same as a distance between adjacent two fins (lower and upper parts) in second region RG2. First fin portions F1 in first region RG1 and second region RG2 are shown in Oh's Figure 14 (reproduced below with annotations), where the distance between adjacent lower and upper parts of the two fins of first fin portions F1 in first region RG1 is the same distance between adjacent lower and upper parts of the two fins of first fin portions F1 in second region RG2.



EX1005, FIG. 14 (annotated).

83. To form **third fin portions F3** (blue) in Oh's Figure 26 (reproduced above with annotations), Oh explains that "upper sidewalls of the first fin portions F1 with the first width T1 may be etched to form the third fin portions F3, whose upper portions have the third width T3," where "[t]he third width T3 may be smaller than the first width T1." EX1005, ¶[0070]. Because first fin portions F1 on the first region RG1 in Oh's Figure 14 are etched to form the third fin portions F3 in first region RG1 in Oh's Figure 26, the third width T3 of the top parts of the third fin portions F3 is reduced from the first width T1 of the top parts of the first fin portions F1. EX1005, ¶[0070]. As the third width T3 of the third fin portions F3 is reduced after the etching process, the distance between top parts of two adjacent fins in the third fin portions F3 is increased. Because the first fin portions F1 in second region RG2 are masked and the lower parts of third fin portions F3 in first region RG1 are covered by a device isolation layer 110 in Oh's Figure 26, the first

fin portions F1 in second region RG2 and the lower parts of third fin portions F3 in first region RG1 are not etched by the etching process. As a result, the distance between top parts of adjacent first fin portions F1 in second region RG2 is not changed (or remains the same).

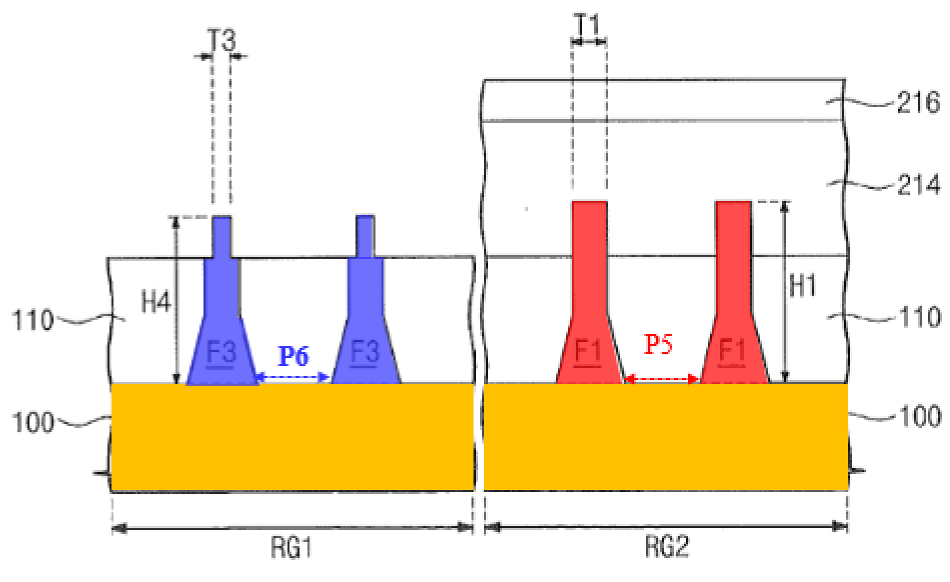
84. Referring to Oh's Figure 26 (reproduced above with annotations), because Oh's fin-shaping process affects the upper parts of fins where an upper part width of a shaped fin (e.g., width T3) is less than an upper part width of a non-shaped fin (e.g., first width T1), a POSA would have understood that Oh's fin-shaping process forming **third fin portions F3** (blue) results in a **distance P1** (red) between adjacent top corners of the two fins in **first fin portions F1** (red) being less than **distance P3** (blue) between adjacent top corners of the two fins in **third fin portions F3** (blue).

85. Thus, in view of the above, Oh discloses or renders obvious claim limitation [1.b].

d. [1.c]: while a third distance between adjacent lower parts of the first fin and the second fin is the same as a fourth distance between adjacent lower parts of the third fin and the fourth fin;

86. Oh discloses or renders obvious that a third distance between adjacent lower parts of the two fins in the first fin portions F1 is the same as a fourth distance between adjacent lower parts of the two fins in third fin portions F3.

Referring to Oh's Figure 26 (reproduced below with annotations), a POSA would have understood that a **distance P5** (red; "*a third distance*") between adjacent lower parts of the two fins in **first fin portions F1** (red; "*the first fin and the second fin*") is the same as a **distance P6** (blue; "*a fourth distance*") between adjacent lower parts of the two fins in **third fin portions F3** (blue; "*the third fin and the fourth fin*"). Below, I describe **distance P5** (red) and **distance P6** (blue).



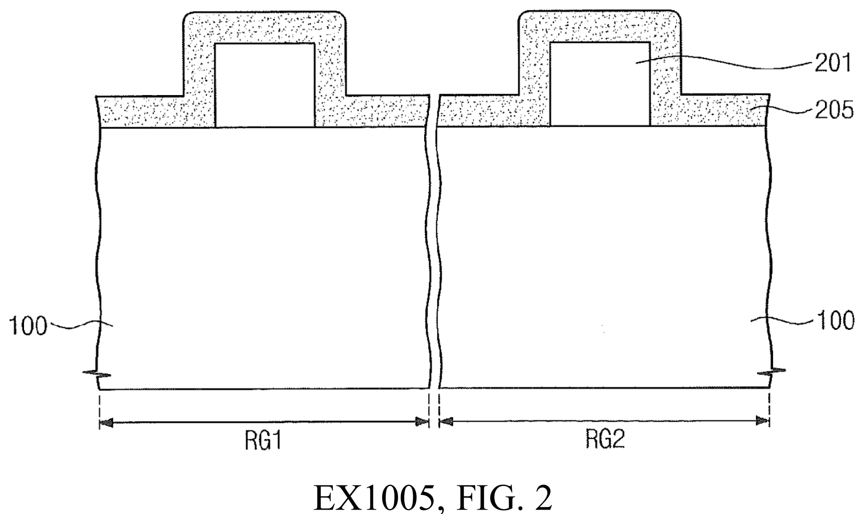
EX1005, FIG. 26 (annotated).

87. As I discuss further below, Oh discloses or renders obvious uniform spacing between fins when forming its fin-shaped structure. Oh discloses a fin formation process that uses spacers and uniform hardmask patterns to form uniform fins. EX1005, ¶¶ [0047]-[0050]. Oh's Figures 2, 4, 6, and 14—all precursor structures to Oh's Figure 26—show portions of Oh's initial fin formation process. The structure shown in Oh's Figure 26 is based on the structure shown in

Oh's Figure 14, which, in turn, is based on the method and structures associated with Oh's Figures 1-6. Oh explains that the structure shown in Oh's Figure 26 is based on the structure shown in Oh's Figure 14: "[r]eferring to FIGS. 25 and 26, an etching mask pattern 214 may be formed on the structure described with reference to FIGS. 13 and 14," where "[f]or conciseness, a previously described element may be identified by a similar or identical reference number without repeating an overlapping description thereof." EX1005, ¶¶[0068]-[0069]. With regard to the structure shown in Oh's Figure 14, Oh explains that this structure is based on the method and structures associated with Oh's Figures 1-6: "[f]or example, the first fin portions F1 [of FIG. 14] may be formed by the method described with reference to FIGS. 1 through 6, and thus, have the same width as each other," where "[f]or conciseness, a previously described element may be identified by a similar or identical reference number without repeating an overlapping description thereof." EX1005, ¶¶[0058]-[0059].

88. Referring to Oh's Figure 2 (reproduced below), first mask patterns 201 and a conformal second mask layer 205 are formed on a substrate 100 that includes a first region RG1 and a second region RG2. EX1005, ¶[0047]-[0048]. Oh then forms a second mask layer 205 on substrate 100 provided with mask patterns 201: "[a] second mask layer 205 may be formed on the substrate 100 provided with the first mask patterns 201," where "[t]he second mask layer 205 may be formed to

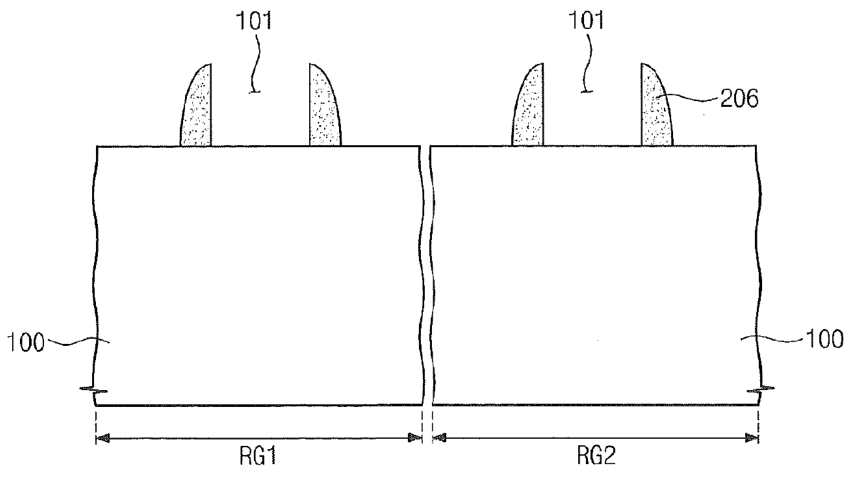
conformally cover the substrate 100 provided with the first mask patterns 201." EX1005, ¶[0048].



EX1005, FIG. 2

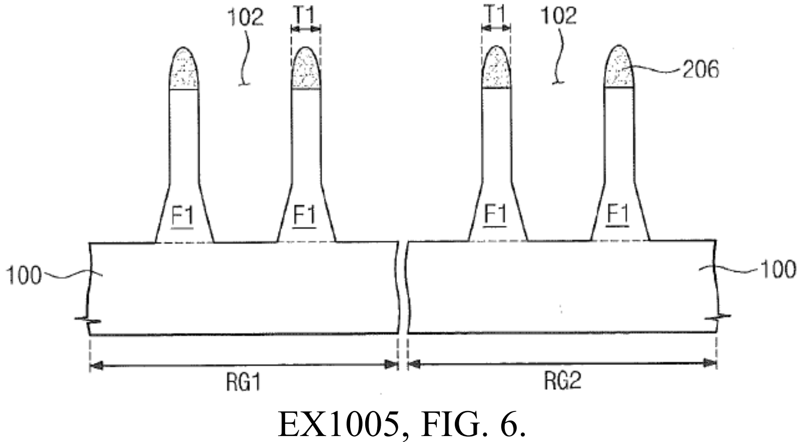
89. Referring to Oh's Figure 4 (reproduced below), second mask patterns 206 are formed after an etching process in the first region RG1 and second region RG2, in which second mask patterns 206 are spaced apart from one another by first trenches 101. EX1005, ¶[0049]. Referring to Oh's Figure 4 below, Oh's spacer forming process is performed to form a second mask patterns 206 with a trench 101 between adjacent second mask patterns 206: the "spacer forming process may be performed on the second mask layer 205 to form second mask patterns 206," where "[t]he second mask patterns 206 may be formed to expose the first mask patterns 201, thereby having a spacer shape." EX1005, ¶[0049]. For example, Oh discloses "the spacer forming process may include a plasma etching process performed in an anisotropic manner." EX1005, ¶[0049]. Oh explains that each of

mask patterns 206 is formed with the same width: "[t]he second mask patterns 206 may have the substantially same width as each other." EX1005, ¶[0049]. Oh further explains that "[t]he first mask patterns 201 exposed by the second mask patterns 206 may be removed to form first trenches 101 between the second mask patterns 206." EX1005, ¶[0049].



EX1005, FIG. 4.

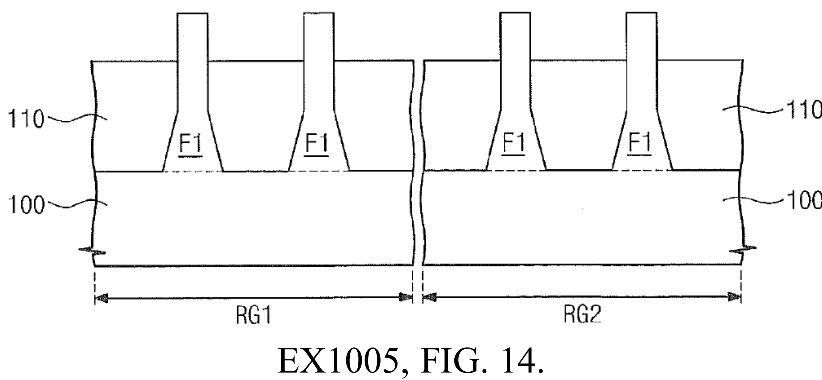
90. Following the formation of the second mask patterns 206, an etching process using second mask patterns 206 forms first fin portions F1 separated by second trenches 102, as shown in Oh's Figure 6 (reproduced below). EX1005, ¶[0050]. As I noted above, Oh's Figure 6 shows a precursor structure to Oh's Figure 14, in which Oh explains that "[r]eferring to FIGS. 13 and 14 . . . the first fin portions F1 may be formed by the method described with reference to FIGS. 1 through 6." EX1005, ¶[0059].



EX1005, FIG. 6.

91. After the formation of the structure in Oh's Figure 6, referring to Oh's Figure 14 (reproduced below), device isolation layers 110 are formed in second trenches 102 to cover lower parts of first fin portions F1. EX1001, ¶[0059]. Oh describes that "[t]he device isolation layers 110 may be formed to cover lower sidewalls of the first fin portions F1." EX1005, ¶[0059]. Since the lower parts of the first fin portions F1 are covered, upper parts of the first fin portions F1 are exposed, as shown in Oh's Figure 14: "[t]he formation of the device isolation layers 110 may include forming a dielectric layer to cover the first and second regions RG1 and RG2, and then, etching the dielectric layer to expose upper portions of the first fin portions F1." EX1005, ¶[0059]. A POSA would have understood that, based on Oh's teachings, the resulting distance between the first fin portions F1 in the first region RG1 and between the first fin portions F1 in the second region RG2 is the same. I also note that, in Oh's Figure 14, second mask patterns 206 (from Oh's Figure 6) have been removed. This removal process can

be performed by an etching process, such as the selective etching process to remove second mask patterns in other embodiments of Oh such as those illustrated in Oh's Figures 9 and 10: "Referring to FIGS. 9 and 10, the second mask patterns 206 . . . may be removed," where "[t]he removal of the second mask patterns 206 . . . may include a plurality of selective etching processes." EX1005, ¶[0055].



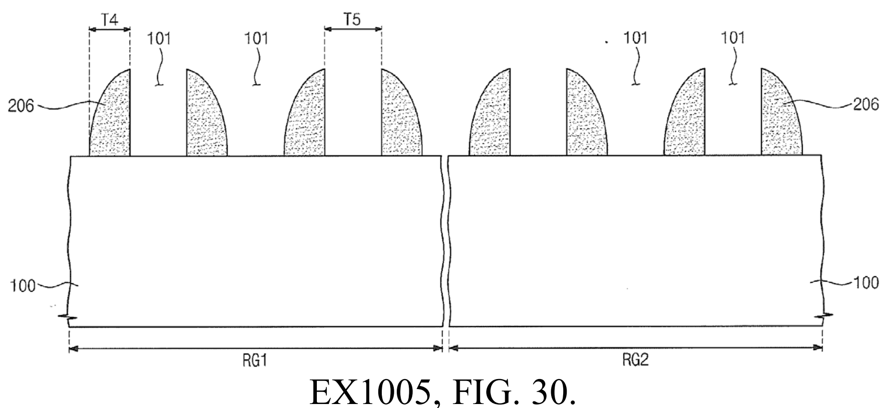
EX1005, FIG. 14.

92. As I discussed above regarding Oh's Figures 2, 4, and 6—which are all precursor structures to Oh's Figure 14—Oh describes a sequence to form the first fin portions F1 in the first region RG1 and second region RG2 from first mask patterns 201 (in Oh's Figure 2) to first trenches 101 (in Oh's Figure 4) to second trenches 102 (in Oh's Figure 6), and to device isolation layers 110 (in Oh's Figure 14). EX1005, ¶¶[0048]-[0050]. Many of the structural elements in these figures are associated with another, since Oh discloses that its "use of similar or identical reference numbers in the various drawings is intended to indicate the presence of a similar or identical element or feature." EX1005, ¶[0038]. Additionally, the same etching process is performed in the first region RG1 and second region RG2 to

form first trenches 101 in Figure 4. Similarly, the same etching process is performed in the first region RG1 and second region RG2 to form second trenches 102 in Figure 6. A POSA would have understood that, when performing the same etching process on trenches having the same properties and size, the resulting trenches will be the same. Therefore, in my opinion, a POSA would have understood that Oh teaches that the distance between the first fin portions F1 in the first region RG1 and second region RG2 are identical, because it teaches that the two first mask patterns 201 in Figure 2 are identical, as are first trenches 101 in Figure 4 and second trenches 102 in Figure 6.

93. In my opinion, Oh also renders obvious uniform spacing between fins. For example, referring to the embodiment in Oh's Figure 30 (reproduced below), using the same spacer process as Oh's Figure 4, Oh discloses that the lower widths of trenches 101 in the first region RG1 are the same and can each have a width T5. EX1005, ¶[0073]. Oh explains that "[r]eferring to FIGS. 29 and 30 . . . [t]he second mask patterns 206 may be formed by the process described with reference to FIGS. 1 through 4." EX1005, ¶[0073]. Similar to Oh's Figure 4, Oh's Figure 30 shows that "[t]he second mask patterns 206 may be spaced apart from each other by the first trenches 101" having "the lower width T5 of the first trench 101." EX1005, ¶[0073]. Oh states that "the width of a trench may refer to a lower width of the trench, and the width of a mask pattern may refer to a lower width of the mask

pattern." EX1005, ¶[0073]. Trenches 101 in Oh's Figure 30 are related to those in Oh's Figure 4 because Oh states that "[f]or conciseness, a previously described element may be identified by a similar or identical reference number without repeating an overlapping description thereof." EX1005, ¶[0072]. Accordingly, Oh discloses that its Figure 30 embodiment, which was formed by the same Figures 1-4 process as is used by Oh's Figure 14, has first trenches 101 separated by width T5. It would have been obvious to a POSA to adapt this teaching of first trenches 101 having the same width T5 to Oh's Figure 14 embodiment.



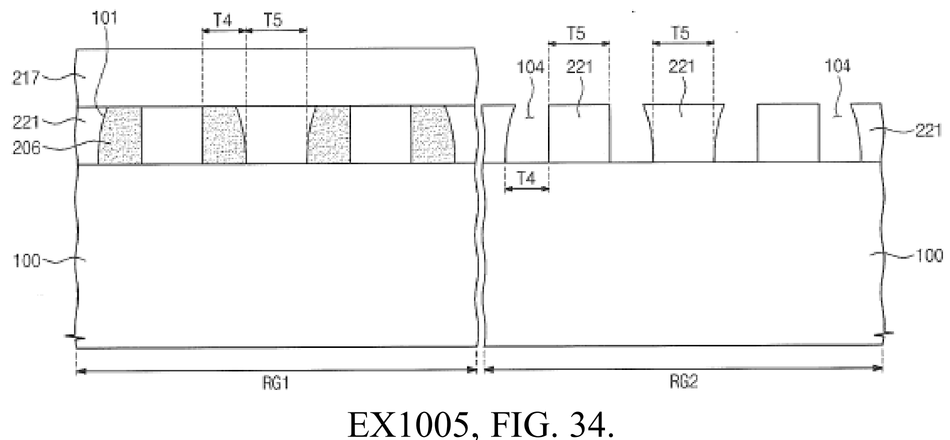
EX1005, FIG. 30.

94. In my opinion, if Oh does not expressly disclose that the spacing/distance between the fins in Figure 14 is the same, a POSA would have found it obvious to apply the same spacing/distance teachings from Oh's Figure 30 to have the same spacing/distance between the fins in Oh's Figure 14. This is because it is simply an application of a known technique of Oh's spacer process with trenches 101 having the same width T5, as shown in Oh's Figure 30, to a known structure of second mask patterns 206 and first trenches 101 in Oh's Figure

4 to yield predictable results of uniformly-spaced second mask patterns 206 and first trenches 101, which lead to uniformly-spaced fins in Oh's Figure 14. Therefore, Oh discloses or renders obvious that first trenches 101 in Oh's Figure 4 would have the same width.

95. Similarly, referring to Figure 34 (reproduced below)—another embodiment of Oh that uses the same spacer process as Oh's Figure 4—Oh explains that the width of first trench 101 is uniform and can have a width T5. Referring to Oh's Figure 34 (reproduced below), Oh explains that "[t]he fifth width T5 of the fifth mask pattern 221 may be substantially equal to the width of the first trench 101." EX1005, ¶[0075]. Oh's Figure 34 shows 2 fifth mask patterns 221 on first region RG1 and 2 fifth mask patterns 221 on second region RG2 that both have the same fifth width T5, which are substantially equal to the width of the first trench 101. EX1005, ¶[0075]. Trenches 101 in Oh's Figure 34 are related to those in Oh's Figure 4 because Oh states that "[f]or conciseness, a previously described element may be identified by a similar or identical reference number without repeating an overlapping description thereof." EX1005, ¶[0072]. Based on this disclosure, a POSA would have understood with respect to Oh's Figure 4 that first trenches 101 in first region RG1 and second region RG2 have the same width T5, thus creating the same uniform spacing between adjacent second mask patterns 206 in first region RG1 and between adjacent second mask patterns 206 in second

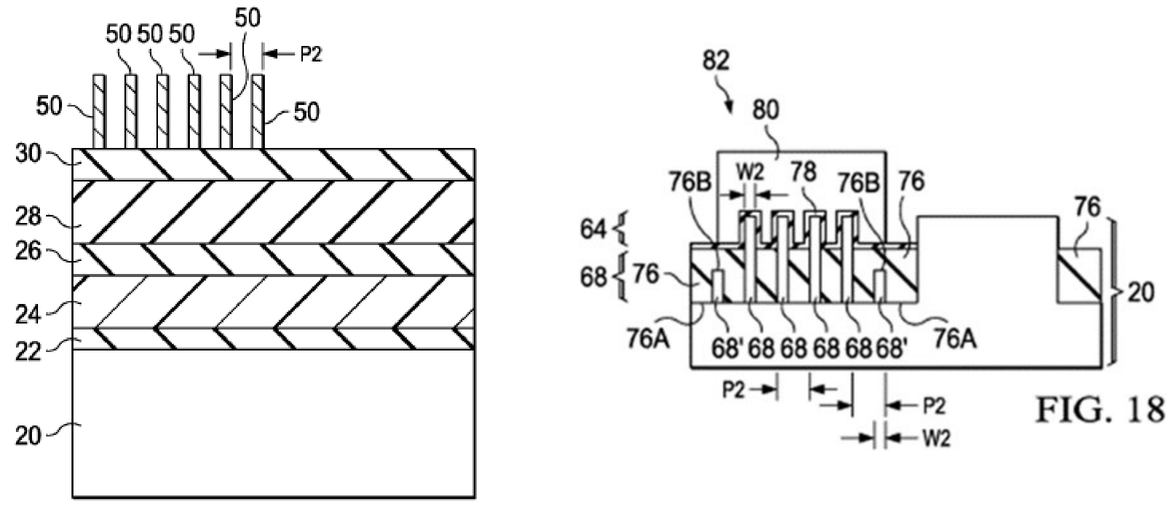
region RG2.



EX1005, FIG. 34.

96. Further, a POSA would have understood that Oh's fin formation process using spacers would form fins (e.g., first fin portions F1) with uniform spacing based on well-known techniques and design objectives. For example, as I discussed above in Section VI.B, Chen discloses a method of forming fins to address the increasing demand in the semiconductor industry to manufacture smaller integrated circuits. EX1012, ¶[0001] ("With the increasing down-scaling of integrated circuits and the increasingly demanding requirements to the speed of integrated circuits, transistors need to have higher drive currents."). Specifically, Chen discloses a spacer process to manufacture uniform fins having uniform and minimum spacing between adjacent fins. EX1012, ¶[0007]. Referring to Chen's Figure 5 (reproduced below), after mandrels 46 are removed via the same etching process for all mandrels 46, spacers 50 remain on oxide layer 30 and have a uniform pitch P2 between adjacent spacers 50. EX1012, ¶¶[0013], [0015]. After

further processing, referring to Chen's Figure 18, fins with uniform dimensions and uniform spacing are formed, where "pitch P2 of fin extension residues 68' and its neighboring fin 64 may be the same as pitch P2 between neighboring fin extensions 68" and "widths W2 of fin extensions 68 may be substantially the same as widths W2 of fin extension residues 68'." EX1012, ¶[0023]. The space between fin extensions 68 and below fin structures 64 are then filled with a dielectric material to form shallow trench isolation (STI) regions 76. EX1012, ¶[0022].



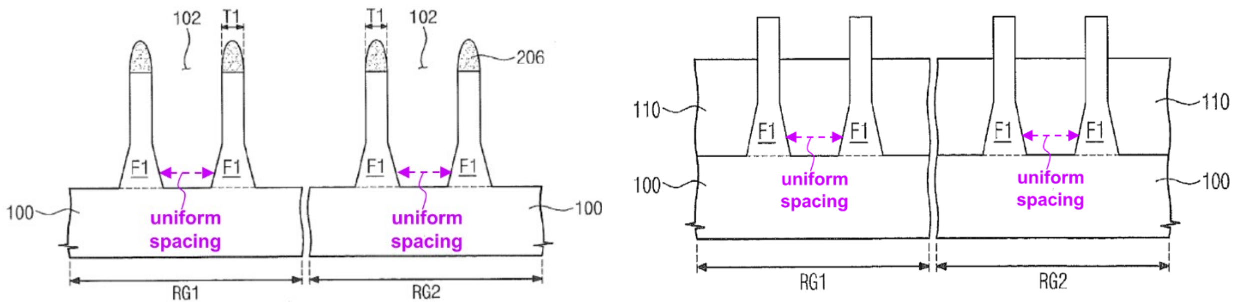
EX1012, FIGs. 5 (left) and 18 (right).

97. A POSA would have understood that the benefits of Chen's mandrel/spacer process with uniformly-spaced spacers (to form uniformly-spaced fins), which is similar to Oh's spacer process in Figures 30 and 34, include the manufacturing of smaller integrated circuits, mitigation of etch-loading effects during fin formation, and facilitation of epitaxial fin merging in multi-fin FinFETs. EX1013, ¶[0013]; EX1014, ¶[0005]. In addition, because uniform spacing between

mandrels (which is limited by a minimum mandrel pitch based on available lithography) will lead to a maximum density of spacers and therefore, fins, a POSA would have been motivated to form such a uniform arrangement of fins. Further, as described above, a POSA would have reasonably expected to succeed applying such teachings to second mask patterns 206 in Oh's Figure 4.

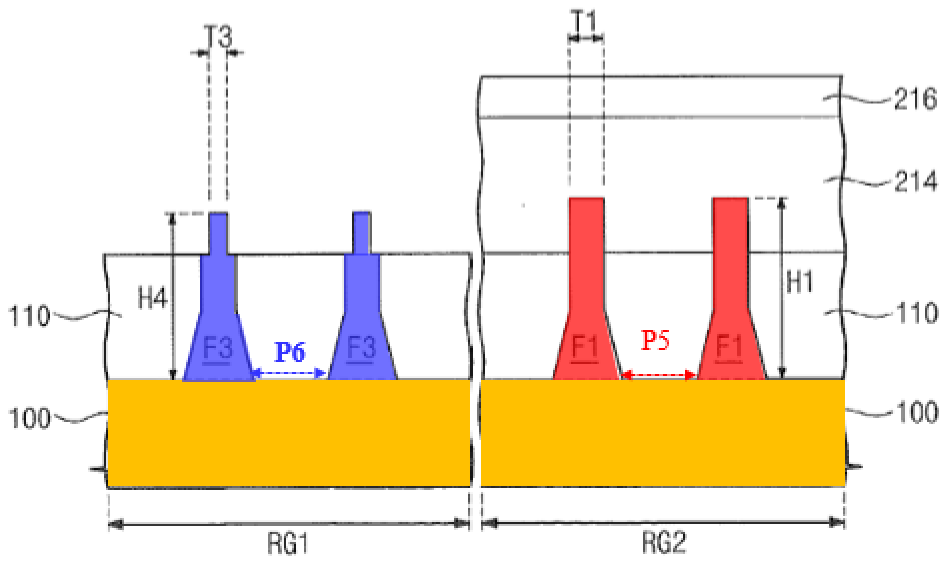
98. The subsequent formation of a device isolation layer 110 to cover lower parts of the first fin portions F1 (as shown in Oh's Figure 14, which is reproduced below with annotations) does not change the uniform spacing between lower parts of the fins in first region RG1 and second region RG2. Referring to Oh's Figures 6 and 14 (both reproduced below with annotations), device isolation layer 110 is formed over the structure shown in Oh's Figure 6 and then etched to expose upper portions of first fin portions F1 as shown in Oh's Figure 14: "[t]he formation of the device isolation layers 110 may include forming a dielectric layer to cover the first and second regions RG1 and RG2, and then, etching the dielectric layer to expose upper portions of the first fin portions F1. EX1005, ¶[0059]. Referring to Oh's Figure 14, as a result of Oh's fin formation process in both first region RG1 and second region RG2, the distance between adjacent lower parts of the two fins in first region RG1 is the same as the distance between adjacent lower parts of the two fins in second region RG2 because these parts of the fins in first region RG1 and second region RG2 are covered by device isolation 110 during

Oh's fin formation process.



EX1005, FIGs. 6 (left; annotated) and 14 (right; annotated).

99. The subsequent fin etching process to form third fin portions F3 (as shown in Oh's Figure 26, which is reproduced below with annotations) does not change the lower parts of the fins surrounded by device isolation layer 110 in first region RG1 and second region RG2. EX1005, ¶[0070]. After the formation of the two fins in first fin portions F1 in first region RG1 and second region RG2, referring to Oh's Figure 14 (reproduced above with annotations), the two fins in first region RG1 are shaped as I discussed above in Sections VIII.A.1.b and VIII.A.1.c. Specifically, the upper sidewalls of first fin portions F1 in first region RG1 are etched, while lower parts of these fins are unchanged because they are surrounded by device isolation layer 110. EX1005, ¶[0070]. As a result, Oh's fin-shaping process does not affect the uniformly-spaced lower parts of the fins in the first region RG1 and second region RG2.



EX1005, FIG. 26 (annotated).

100. Thus, referring to Oh's Figure 26 (reproduced above with annotations), a POSA would have understood that **distance P6** (blue) between adjacent lower parts of the two fins in **third fin portions F3** (blue) is the same as **distance P5** (red) between adjacent lower parts of the two fins in **first fin portions F1** (red). This is because Oh's fin-shaping process does not affect the uniformly-spaced lower parts of the fins in the first region RG1 and second region RG2.

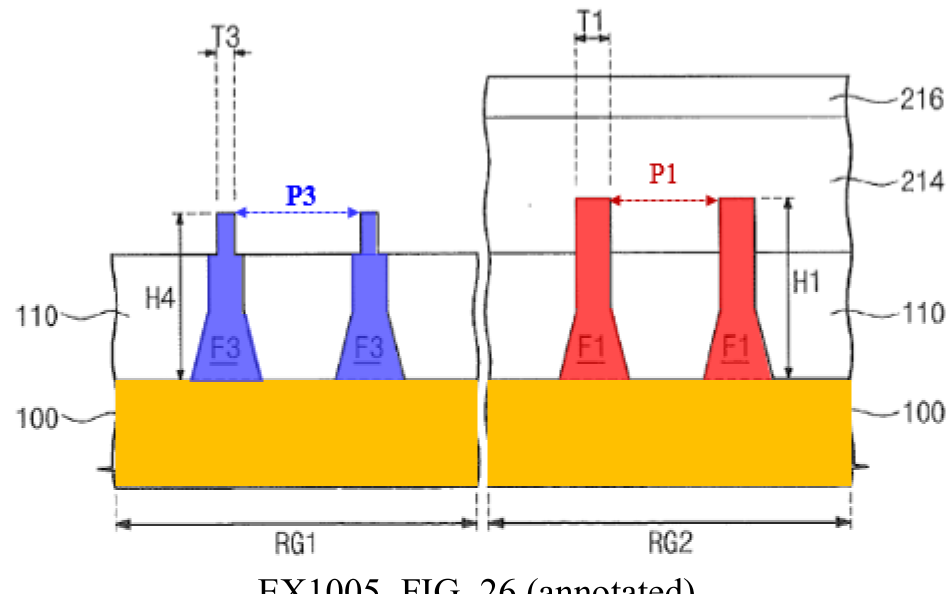
101. In view of the above, Oh discloses or renders obvious claim limitation [1.c].

e. [1.d]: and wherein the adjacent top corners are directly opposite each other.

102. Oh discloses the adjacent top corners of the two fins in the first fin portions F1 and the adjacent top corners of the two fins in the third fin portions F3 are directly opposite each other. Since there are two "*adjacent top corners*" recited

in limitation [1.b], the "*adjacent top corners*" in limitation [1.d] refers to "*adjacent top corners of the first fin and the second fin*" and/or to the "*adjacent top corners of the third fin and the fourth fin*" recited in limitation [1.b]. Below, I describe the adjacent top corners of Oh's first fin portions F1 and the adjacent top corners of Oh's third fin portions F3 being directly opposite each other.

103. As I discussed in Section VIII.A.1.c above, in my opinion, Oh discloses or renders obvious a first distance between adjacent top corners of the two fins in the first fin portions F1 being less than a second distance between adjacent top corners of the two fins in the third portions F3. Specifically, as shown in Oh's Figure 26 (reproduced below with annotations), the top corners of the two fins in **first fin portions F1** (red) are directly opposite each other and thus adjacent, and the top corners of the two fins in **third fin portions F3** (blue) are directly opposite each other and thus adjacent. These are the same top corners referred to in Section VIII.A.1.c above when addressing the measurement of **distance P1** (red) between adjacent top corners of the two fins in **first fin portions F1** (red) and **distance P3** (blue) between adjacent top corners of the two fins in **third fin portions F3** (blue).

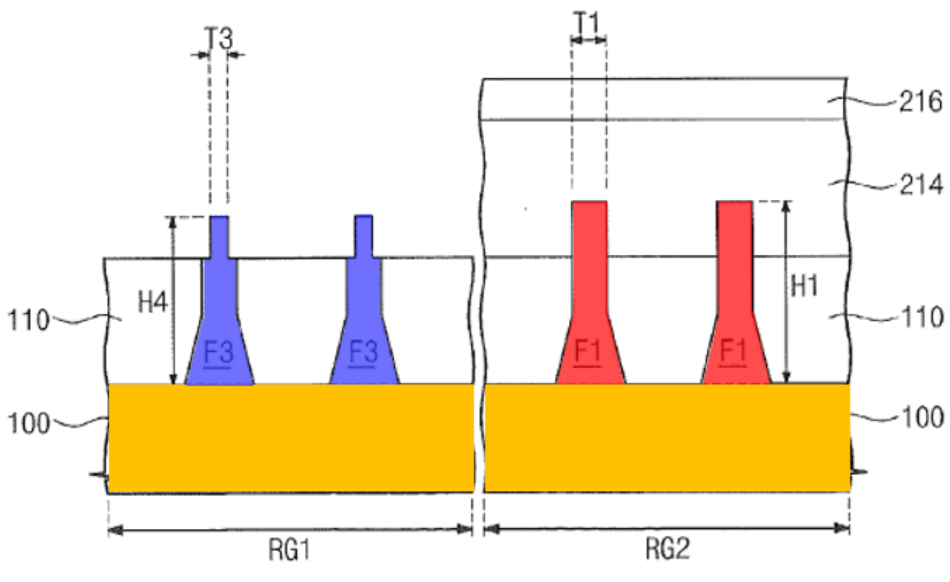


EX1005, FIG. 26 (annotated).

104. Thus, in view of the above, Oh discloses limitation [1.d].

2. Dependent Claim 2: wherein the width of each top part of the first fin shaped structures is larger than the width of each top part of the second fin-shaped structures.

105. Oh discloses that the width of each top part of the first fin portion F1 is larger than the width of each top part of the third fin portion F3. Specifically, referring to Oh's Figure 26 (reproduced below with annotations), a width T1 of each top part of **first fin portions F1** (red; "*first fin-shaped structures*") is larger than a width T3 of each top part of **third fin portions F3** (blue; "*second fin-shaped structures*"). Oh explains that "[t]he third width T3 may be smaller than the first width T1." EX1005, ¶[0070].

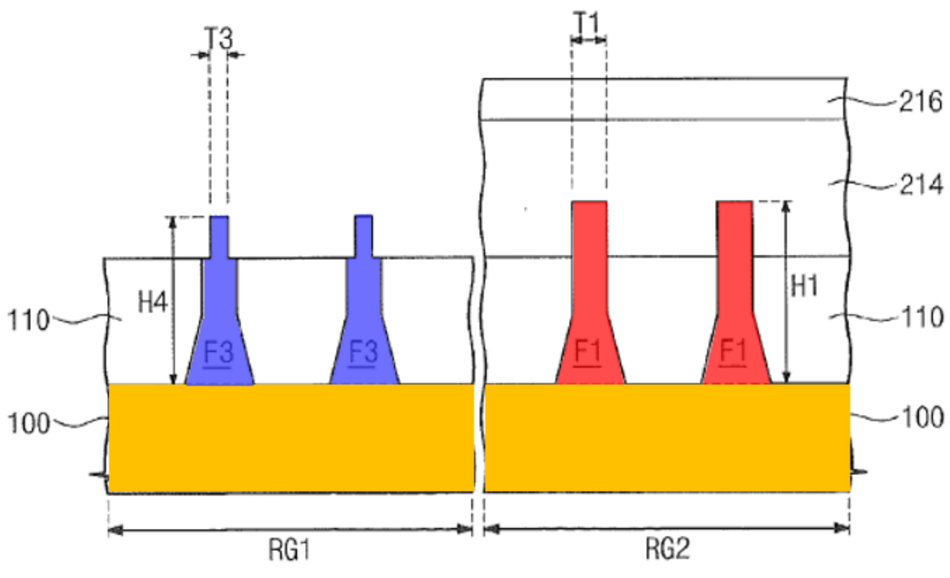


EX1005, FIG. 26 (annotated).

106. Thus, in view of the above, Oh discloses claim 2.

3. Dependent Claim 6: wherein a height of the first fin-shaped structures protruding from the substrate is higher than a height of the second fin-shaped structures protruding from the substrate.

107. Oh discloses that a height of the first fin portions F1 protruding from the substrate is higher than a height of the third fin portions F2. Specially, referring the Oh's Figure 26 (reproduced below with annotations), a height H1 of **first fin portions F1** (red; "*first fin-shaped structures*") protruding from **substrate 100** (orange) is higher than a height H4 of **third fin portions F3** (blue; "*second fin-shaped structures*") protruding from **substrate 100** (orange). Oh explains that "[a]s the result of the etching process, the third fin portions F3 may have a fourth height H4 smaller than the first height H1 of the first fin portions F1." EX1005, ¶[0070].



EX1005, FIG. 26 (annotated).

108. Thus, in view of the above, Oh discloses claim 6.

B. Ground 2: The combination of Oh and Rachmady renders obvious claims 3-5.

1. A POSA would have been motivated to combine Oh and Rachmady.

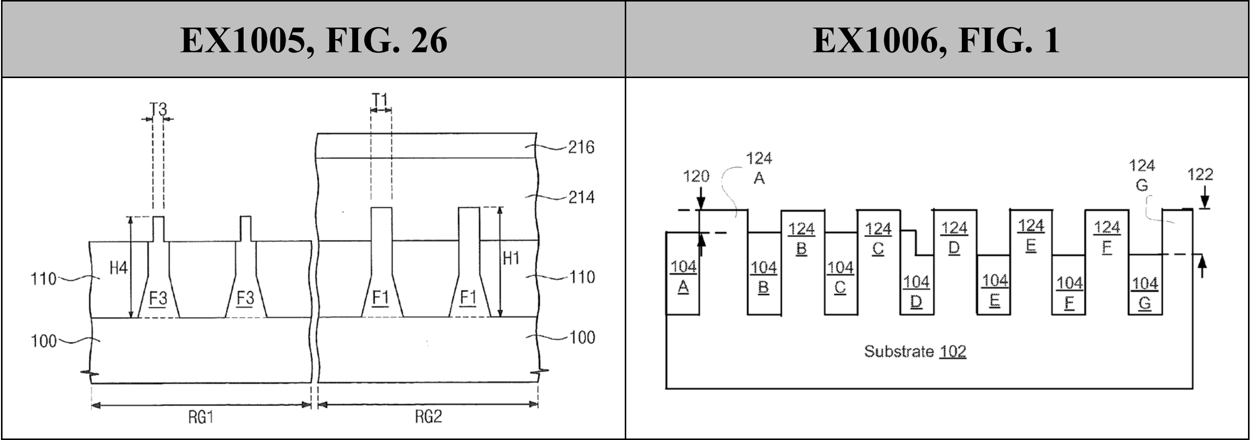
109. In my opinion, a POSA would have been motivated to modify Oh's fin-shaped structure by adjusting a height of a device isolation layer in Oh's transistors based on Rachmady's teachings to adjust drive current by adjusting fin heights above the device isolation layer.

110. In my opinion, Oh and Rachmady are both in the same field of endeavor: the formation of FinFETs based on desired device characteristics. In integrated circuit (IC) design, circuit designers specify certain transistor dimensions based on electrical properties, such as threshold voltage and drive

current, to meet circuit performance and size requirements: "[a] circuit designer specifies transistors in his design according to electrical properties for performing various functions." EX1007, ¶[0018]. For example, Oh adjusts fin widths to achieve desired transistor threshold voltages: "fin portions having widths different from each other … can enable the fabrication of transistors having threshold voltages different from each other." EX1005, ¶[0053]. Rachmady adjusts fin heights—without impact to transistor area—to achieve desired drive currents: "designers may independently select transistor height and area to achieve desired device characteristics". EX1006, ¶[0022]. Threshold voltage and drive current are among the key device characteristics to consider when designing ICs: "[e]lectrical properties to be considered include turn on voltage (threshold voltage), breakdown voltage, on-state current (I_{on}), leakage current, among others." EX1007, ¶[0018].

111. Additionally, as I discuss below, Oh and Rachmady both describe similar fin-shaped structures, including fin-shaped structures with varying fin heights formed on a substrate and an isolation structure disposed beside the fin-shaped structures. For example, Oh's Figure 26 (reproduced below with annotations) shows first fin portions F1 and third fin portions F3 with varying fin heights formed on a substrate 100. The varying fin heights of Oh's first fin portions F1 and third fin portions F3 can be relative to a device isolation layer 110 or a substrate 100. Device isolation layer 110 is disposed beside first fin portions F1

and third fin portions F3. Similarly, Rachmady's Figure 1 (reproduced below with annotations) shows fins 124 with varying fin heights formed on a substrate 102. The varying fin heights of Rachmady's fins 124 can be relative to an isolation region 104. Isolation region 104 is disposed beside fins 124.

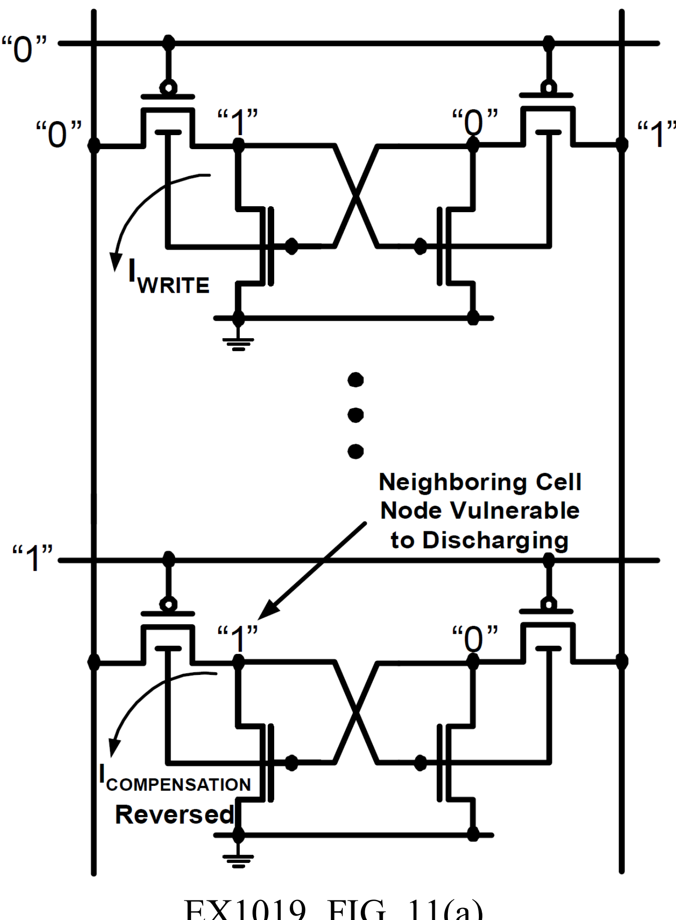


112. Whereas Oh does not explicitly disclose varying heights of device isolation layer 110 to adjust fin height above device isolation layer 110, Rachmady provides such teachings to adjust drive current, which is a key device characteristic in IC design as I discussed above. In my opinion, it would have been obvious to combine Oh's and Rachmady's teachings because a POSA would have (a) been motivated to apply Rachmady's selective fin height teachings to Oh's fin-shaped structure to adjust drive current and (b) reasonably expected to succeed in applying Rachmady's selective fin height teachings to Oh's fin-shaped structure for drive current adjustment.

a. A POSA would have been motivated to apply Rachmady's selective fin height teachings to Oh's fin-shaped structure to adjust drive current.

113. In my opinion, a POSA would have been motivated to modify Oh's fin-shaped structure based on Rachmady's teaching of forming fins with different heights above the device isolation layer to adjust drive current because such modifications provide further circuit design flexibility to Oh's transistors to meet certain circuit design requirements. In my opinion, a POSA would have understood that IC designs can vary based on circuit performance and size requirements. For example, in 4-transistor (4T) static random access memory (SRAM) designs, Guo describes the need for higher threshold voltages and higher drive currents in FinFET PMOS devices (shown in FIG. 11(a) below) to mitigate SRAM cell disturbances and to improve SRAM write margin. EX1019, p. 6 ("[N]eighboring cell write upset can be alleviated by employing high-V_{tp} PMOS and low-V_{tn} NMOS devices."). Guo states that "[s]ince high-V_{tp} PMOS devices tend to be relatively weak, PMOS drive current should be increased to improve the write margin." EX1019, p. 6. To address this issue, Guo proposes a negative wordline bias circuit solution to the increase drive currents of the FinFET PMOS devices with higher threshold voltages. EX1019, p. 6 ("This can be done by using a negative word-line bias voltage".) The negative wordline bias circuit (to generate the "negative word-line bias voltage") would require additional circuitry that can

impact SRAM circuit size. EX1019, p. 6. It is my opinion that the combination of Oh's and Rachmady's teachings provides another solution to meet the 4T SRAM design requirements in addition to the negative wordline bias circuit solution.

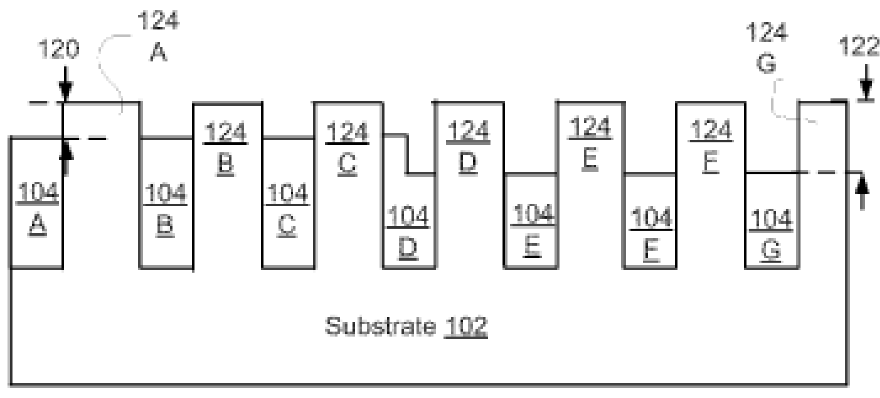


EX1019, FIG. 11(a).

114. Oh describes FinFETs with fin portions that have different widths for different threshold voltages. For example, Oh states that "fin portions having widths different from each other may be formed, which can enable the fabrication of transistors having threshold voltages different from each other." EX1005, ¶[0053]. Accordingly, Oh adjusts fin widths to enable transistor designs with

different threshold voltages.

115. Rachmady describes forming fin-shaped structures with different fin heights above isolation regions to adjust drive current and/or transistor areas in order to achieve desired device characteristics. EX1006, Abstract. Specifically, referring to Figure 1 (reproduced below), Rachmady explains how to adjust drive current with fin heights without increasing the transistor area: "[s]uch an ability to have fins 124 of different height allows multi-gate transistors to be made on the fins 124 with different desired properties. As the drive current of a transistor is dependent on the gate channel 'width' of a multi-gate transistor, and the 'width' may be made greater by use of a taller fin 124 without increasing the area of the transistor, selectable multi-height fins 124 allow the transistors with the same area to have selected drive currents based on the fin heights." EX1006, ¶[0022].



EX1006, FIG. 1.

116. In my opinion, applying Rachmady's teachings of adjusting drive current with different fin heights above the device isolation layer to Oh's fin-

shaped structure provides further improved drive current to Oh's transistors, which in turn can be used in a wider variety of circuit designs. For example, as discussed above in Guo, FinFET PMOS devices in 4T SRAM designs require higher threshold voltages and higher drive currents. EX1019, p. 6. Guo explains that the higher threshold voltages are needed to mitigate SRAM cell disturbances from neighboring SRAM cells during a write operation. EX1019, p. 6. However, the higher threshold voltages lead to lower drive currents in the FinFET PMOS devices, thus decreasing SRAM write margin. EX1019, p. 6. A POSA would have understood that FinFETs with narrower fin widths have higher threshold voltages. EX1018, ¶[0016], FIG. 2. In my opinion, to meet the higher threshold voltage/higher drive current requirements in 4T SRAM designs, a POSA would have been motivated to form FinFET PMOS devices with narrower fin widths based on Oh's teachings to achieve the higher threshold voltages, Additionally, to improve SRAM write margin, a POSA would have been further motivated to apply Rachmady's selective fin height teachings to Oh's FinFET PMOS devices to increase drive currents.

117. Because applying Rachmady's selective fin height teachings to Oh's fin-shaped structure extends the electrical properties of Oh's transistors—e.g., increases drive current of Oh's transistors formed with a minimum fin width—a POSA would have been motivated to combine Oh's fin-shaped structure with

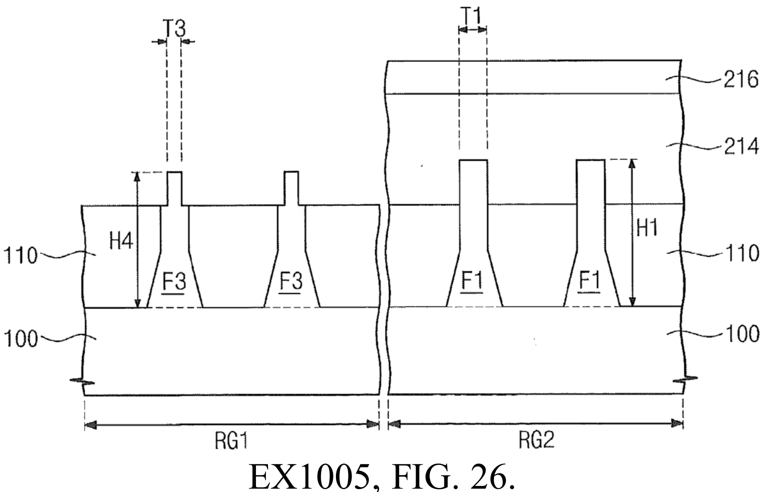
Rachmady's teachings.

b. A POSA would have reasonably expected to succeed in modifying Oh's fin-shaped structure based on Rachmady's selective fin height teachings.

118. In my opinion, Oh and Rachmady disclose well-known semiconductor fabrication processes to form fin structures, and thus a POSA would have reasonably expected that applying Rachmady's selective fin height teachings to adjust the fin height of Oh's transistors would successfully adjust the drive current of Oh's transistors.

119. Oh discloses etching exposed fin portion regions to shape fins with different widths, where a fin height relative to a device isolation layer is shortened due to the etching process. Specifically, referring to Figure 26 (reproduced below), Oh describes the etching process to form third fin portions F3 with a smaller fin width: "upper sidewalls of the first fin portions F1 with the first width T1 may be etched to form the third fin portions F3, whose upper portions have the third width T3," where "[t]he third width T3 may be smaller than the first width T1." EX1005, ¶[0070]. Oh further explains that the height H4 of fin portions F3 above substrate 100 is smaller after the etching process: "[a]s the result of the etching process, the third fin portions F3 may have a fourth height H4 smaller than the first height H1 of the first fin portions F1." EX1005, ¶[0070]. Oh discloses that "[the] etching process may be performed in a dry and/or wet etching manner" and "may include

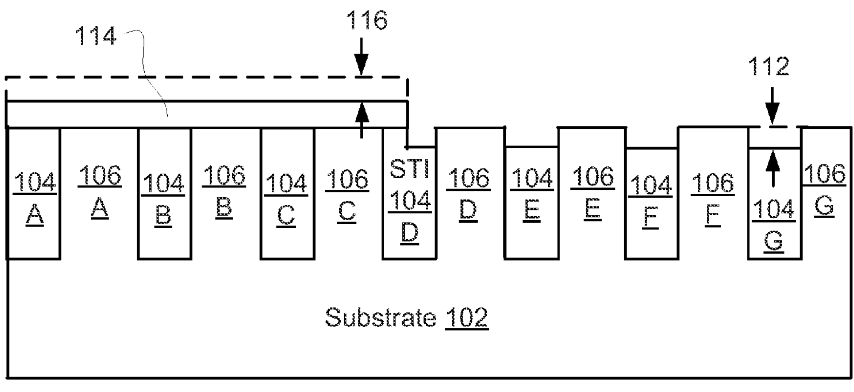
an isotropy etching process." EX1005, ¶[0070]. Oh does not disclose the etching process changes the device isolation layers 110 during etching upper sidewalls of the first fin portions F1. Therefore, top surfaces of device isolation layers 110 in first region RG1 and second region RG2 can remain at a same level after the etching process. With smaller fin height H4 above substrate 100 and the same level of the top surfaces of device isolation layers 110, a POSA would have understood that the fin height of fin portions F3 above device isolation layers 110 is shortened after the etching process.



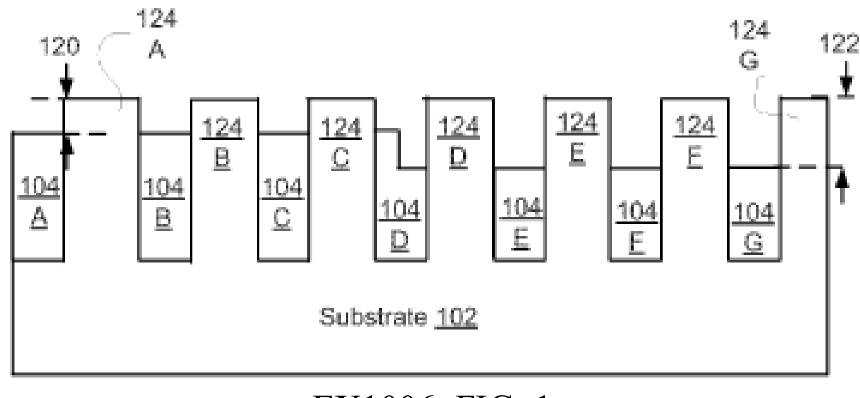
EX1005, FIG. 26.

120. Rachmady also discloses etching an exposed fin portion region, while its etching process removes portions of an isolation layer to increase fin heights above the isolation layer. Referring to Figure 6 (reproduced below, Rachmady uses a selective etching process to remove portions of isolation region 104 but not pre-fin regions 106: "[d]ifferent etchants and/or different materials may be used,

selected based on the desired etchant rate difference between the mask layer 108 and the isolation regions 104, and the etch selectivity to etch the mask layer 108 and isolation regions 104 while leaving the substrate 102 and pre-fin regions 106 substantially intact." EX1006, ¶[0029]. The structure shown in Rachmady's Figure 6 is a precursor structure to Rachmady's Figure 1 (reproduced below) with fins having different heights above isolation region 104: "FIGS. 2 through 9 are cross sectional side views that illustrate how fins 124 of different heights on the same substrate 102 [in FIG. 1] may be formed." EX1006, ¶[0023]. Rachmady provides well-known etchants and materials that can be used for its selective etching process: "[f]or example, spin-on dielectric films such as silicate or siloxane can be used as the mask layer 108 or the isolation regions 104, with HF or buffered HF as the etchant." EX1006, ¶[0029]. Thus, based on this etch selectivity, Rachmady can form fins with different fin heights above isolation region 104, as shown in Figure 1 (reproduced below), to adjust drive current.



EX1006, FIG. 6.



EX1006, FIG. 1.

121. After forming third fin portions F3 in Oh's Figure 26 (reproduced above) to achieve a desired threshold voltage, Rachmady's selective fin height process in Figure 6 (reproduced above) can be applied to Oh's third fin portions F3 to increase fin heights of third fin portions F3 protruding from the device isolation layer to increase drive current. Because Rachmady's selective fin height process can be controlled based on different etchants and materials, it is my opinion that a POSA would have reasonably expected to succeed in using Rachmady's selective fin height process to etch Oh's device isolation layer 110 in region RG1 to increase fin heights above device isolation layer 110—and thus drive currents—of third fin portions F3, while keeping these fins intact, similar to Rachmady's Figure 6 above.

c. Additional rationales for combining Oh's and Rachmady's teachings.

122. In addition to the above discussions on motivations to combine Oh's fin-shaped structure and Rachmady's selective fin height teachings and the reasonable expectation of success in combining Oh's and Rachmady's teachings,

below are additional rationales that would have led a POSA to combine the teachings from Oh and Rachmady.

123. *First*, in my opinion a POSA would have understood that the Oh-Rachmady combination combines known elements of Oh's fin-shaped structure and known elements of Rachmady's varying fin heights according to known methods of Rachmady's fin height process based on selective etching to yield the predictable results of varying fin heights in Oh's first region RG1 and second region RG2 to vary drive current based on circuit design requirements, such as those for FinFET PMOS devices in 4T SRAM designs.

124. *Second*, in my opinion a POSA would have understood that the Oh-Rachmady combination uses a known technique of Rachmady's fin height process based on selective etching to improve similar devices of Oh's fin-shaped structure in the same way by adjusting fin heights to vary drive current based on circuit design requirements, such as those for FinFET PMOS devices in 4T SRAM designs.

125. *Third*, in my opinion a POSA would have understood that the Oh-Rachmady combination applies a known technique of Rachmady's fin height process based on selective etching to a known device of Oh's fin-shaped structure ready for improvement to yield predictable results of varying fin heights in Oh's first region RG1 and second region RG2 to vary drive current based on circuit

design requirements, such as those for FinFET PMOS devices in 4T SRAM designs.

126. *Fourth*, in my opinion a POSA would have arrived at the Oh-Rachmady combination due to a teaching, suggestion or motivation that transistors with a wide array of electrical properties is necessary to enable different IC designs in the prior art, such as 4T SRAM designs, to arrive at the claimed invention.

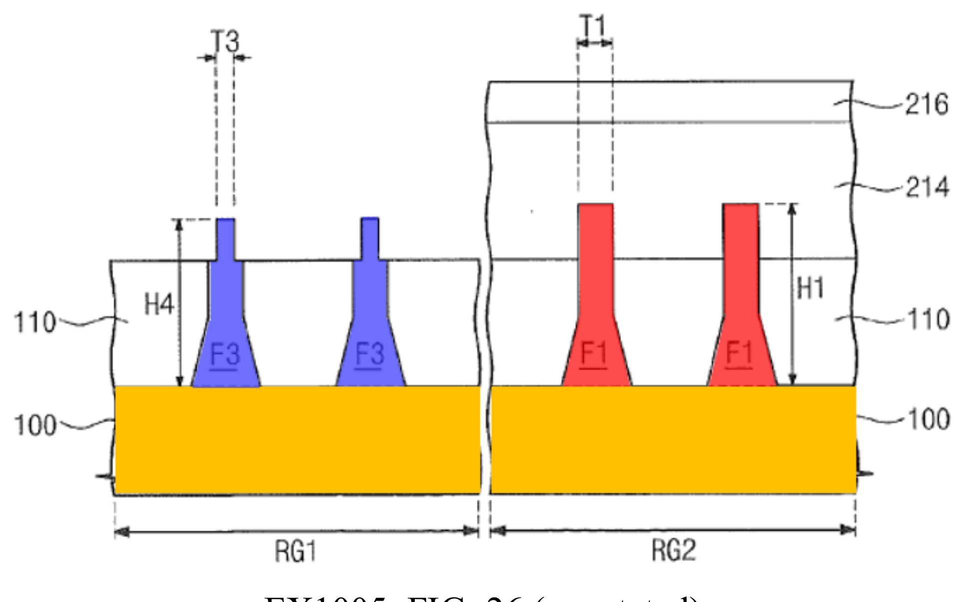
127. *Fifth*, in my opinion a POSA would have understood that the Oh-Rachmady combination is obvious to try since the combination is one of a finite number of identified, predictable solutions of Rachmady's fin height process based on selective etching, with a reasonable expectation of success in adjusting fin heights in Oh's first region RG1 and second region RG2 to vary drive current based on circuit design requirements, such as those for FinFET PMOS devices in 4T SRAM designs.

2. Dependent Claim 3

a. [3.a]: an isolation structure disposed beside the first fin-shaped structures and beside the second fin-shaped structures respectively,

128. Oh discloses an isolation structure beside the first fin portions F1 and beside the third fin portions F3. Specifically, referring to Oh's Figure 26 (reproduced below with annotations), device isolation layers 110 ("*an isolation structure*") is disposed beside **first fin portions F1** (red; "*first fin-shaped*

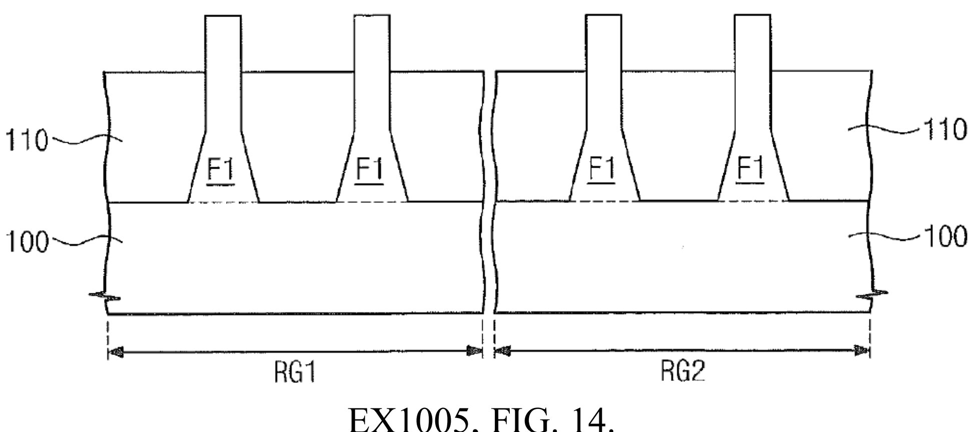
structures") and beside **third fin portions F3** (blue; "*second fin-shaped structures*") respectively.



EX1005, FIG. 26 (annotated).

129. As I discussed in Section VIII.A.1.b above, the structure in Oh's Figure 26 above is formed from a precursor structure shown in Oh's Figure 14 (reproduced below). Referring to Oh's Figure 14 below, Oh explains that the formation of the first fin portions F1 surrounded by device isolation layers 110: "[t]he device isolation layers 110 may be formed to cover lower sidewalls of the first fin portions F1," where "[t]he formation of the device isolation layers 110 may include forming a dielectric layer to cover the first and second regions RG1 and RG2, and then, etching the dielectric layer to expose upper portions of the first fin portions F1." EX1005, ¶[0059]. As shown in Oh's Figure 14 below, device isolation layers 110 beside the first fin portions F1 are formed in both the first

region RG1 and second region RG2.



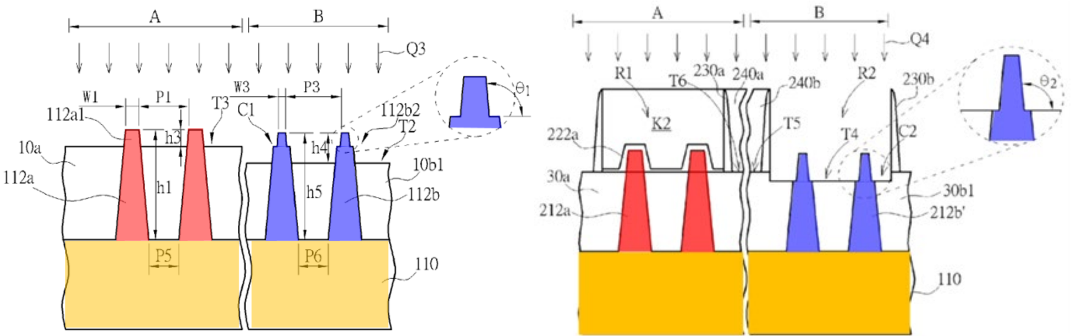
EX1005, FIG. 14.

130. After the formation of the first fin portions F1 surrounded by device isolation layers 110, Oh describes etching the first fin portions F1 in the first region RG1 to form **third fin portions F3**: "upper sidewalls of the first fin portions F1 with the first width T1 may be etched to form the third fin portions F3, whose upper portions have the third width T3." EX1005, ¶[0070]. After the formation of **first fin portions F1** (red) and **third fin portions F3** (blue), device isolation layers 110 remain disposed beside **first fin portions F1** (red) and beside **third fin portions F3** (blue), as shown in Oh's Figure 26 (reproduced above with annotations).

b. [3.b]: and ladder-shaped cross-sectional profile parts of the second fin-shaped structures are higher than a top surface of the isolation structure.

131. The Oh-Rachmady combination renders obvious ladder shaped cross-sectional profile parts of the third fin portions F3 that are higher than a top surface

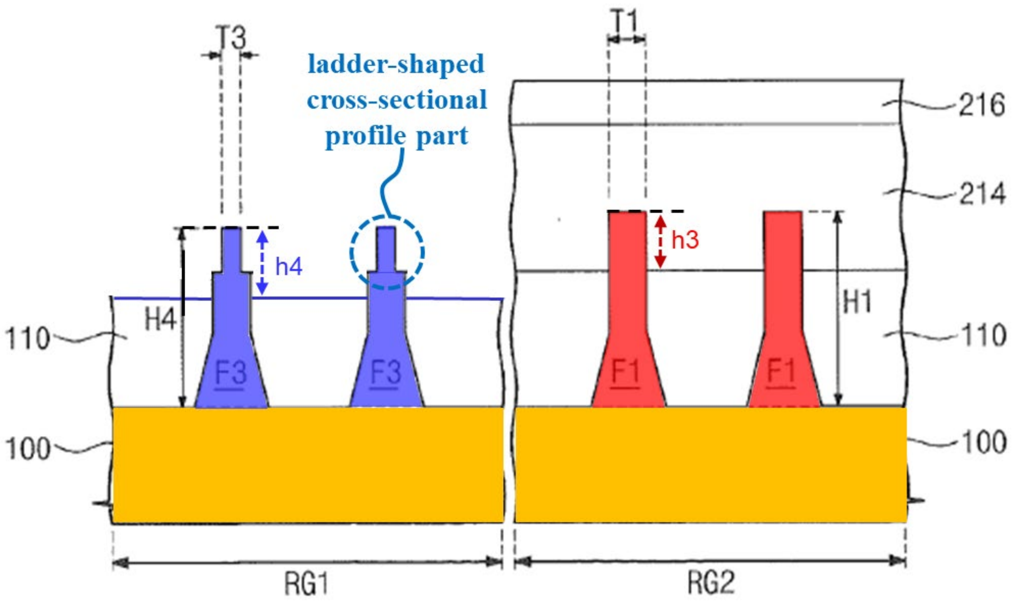
of the isolation structure. Figures 5 and 8 of the ’510 patent (reproduced below with annotations) show examples of ladder-shaped cross-sectional profile parts of **second fin-shaped structures 112b/212b’** (blue; shown in dashed line inset). The ’510 patent describes these structures as having a bending angle θ1 in Figure 5 and a bending angle θ2 in Figure 8 preferably larger than or equal to 90°. EX1001, 5:13-18, 7:14-21. It is my opinion that the Oh-Rachmady combination teaches this ladder shaped cross-sectional profile part.



EX1001, FIG. 5 (left; annotated) and 8 (right; annotated).

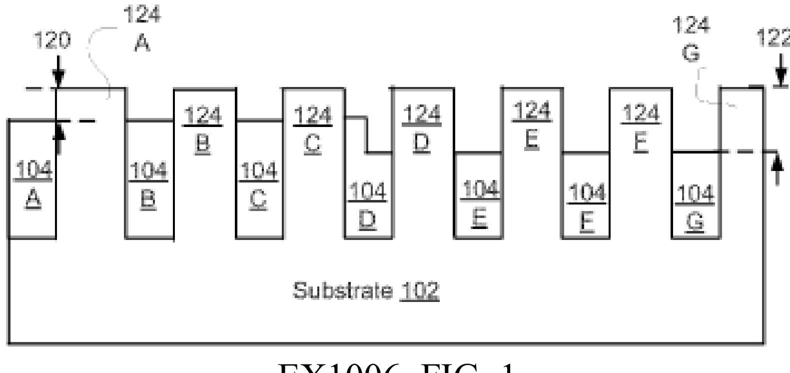
132. As I discussed in Section VIII.B.1 above, a POSA would have been motivated to combine Rachmady’s selective fin height process with Oh’s fin-shaped structure. Below, I present a modified version of Oh’s Figure 26 (with annotations), where a top surface of device isolation layer 110 in the first region RG1 is lower than a top surface of device isolation layer 110 in the second region RG2 due to Rachmady’s selective fin height process. Referring to the modified version of Oh’s Figure 26, a POSA would have understood that application of Rachmady’s selective fin height process to Oh’s fin-shaped structure would result

in ladder-shaped cross-sectional profile parts of **third fin portions F3** (blue; "*second fin-shaped structures*") being higher than a top surface of device isolation layer 110 ("*isolation structure*") for circuit designs that require Oh's transistors in first region RG1 to have higher drive currents (e.g., FinFET PMOS devices in 4T SRAM designs). Additionally, Oh explains that "upper sidewalls of the first fin portions F1 with the first width T2 may be etched to form the third fin portions F3," where "the etching process may include an isotropy etching process." EX1005, ¶[0070]. As shown in the modified version of Oh's Figure 26 below, Oh's ladder-shaped cross-sectional profile parts of **third fin portions F3** (blue; "*second fin-shaped structures*") are formed above device isolation layer 110—similar to the ladder-shaped cross-sectional profile parts of the **second fin-shaped structures** in Figure 5 of the '510 patent above (blue; see inset in dashed circle).



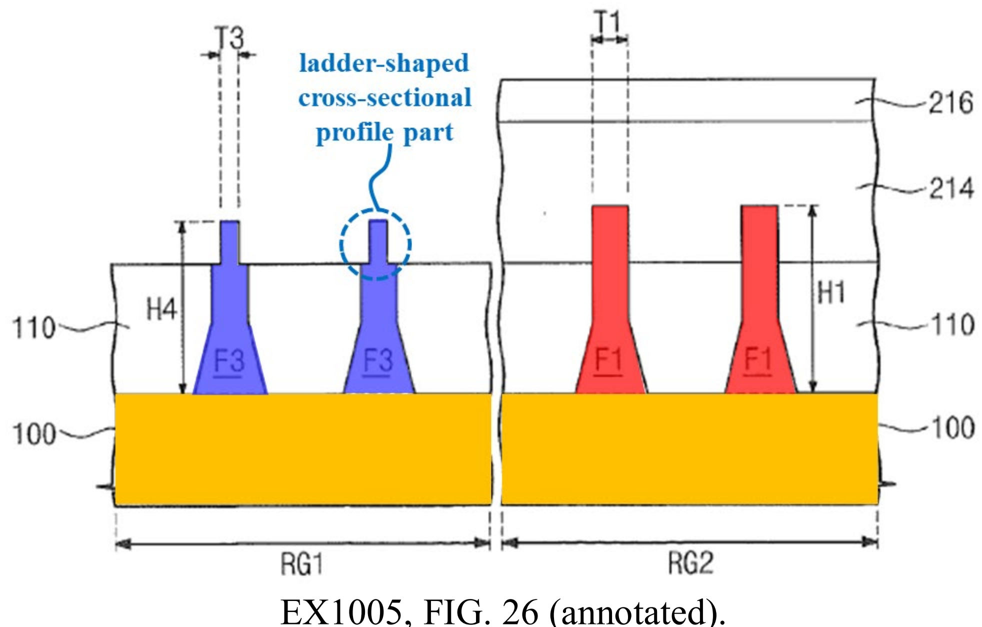
EX1005, FIG. 26 (modified and annotated).

133. As I discussed in Section VIII.B.1 above, Rachmady teaches etching down isolation regions to form fin-shaped structures with different fin heights above the isolation regions to adjust drive current and achieve desired device characteristics (e.g., higher drive currents for FinFET PMOS devices in 4T SRAM designs). EX1006, Abstract. For example, referring to Rachmady's Figure 1 (reproduced below), Rachmady states that "[f]ins 124A through 124C have a smaller height 120 while fins 124D through 124G have a larger height 122." EX1006, ¶[0021]. Rachmady explains that "[t]his difference between heights 120 and 122 is selectable by choosing materials and etchants." EX1006, ¶[0021]. Rachmady's Figures 2 through 9 describe a mask/etch process to remove portions of the isolation regions 104 to form fins of different heights above the isolation regions on the same substrate 102. EX1006, ¶¶[0023]-[0035]. By removing portions of the isolation region, fin heights can be increased, thus increasing drive current without increasing transistor area. EX1006, ¶[0038].



EX1006, FIG. 1.

134. As I discussed in Section VIII.B.1 above, a POSA would have been motivated to combine Rachmady's selective fin height process with Oh's fin-shaped structure. Referring to the modified version of Oh's Figure 26 above, applying Rachmady's selective removal of the isolation regions to increase drive current of Oh's transistors in first region RG1 would result in the ladder-shaped cross-sectional profile parts of the **third fin portions F3** (blue) being higher than a top surface of device isolation layer 110, thus increasing a **height h4 of third fin portions F3** (blue) from an original fin height in Oh's Figure 26 (reproduced below with annotations). As device isolation layer 110 is etched to increase **height h4 of third fin portions F3** (blue), the ladder-shaped cross-sectional profile parts would be modified to be at a level above device isolation layer 110 in the first region RG1. Accordingly, the fin height of **third fin portions F3** (blue) in Oh's modified Figure 26 relative to device isolation layer 110 is increased, thus increasing drive currents in Oh's transistors in the first region RG1 without increasing transistor area.



EX1005, FIG. 26 (annotated).

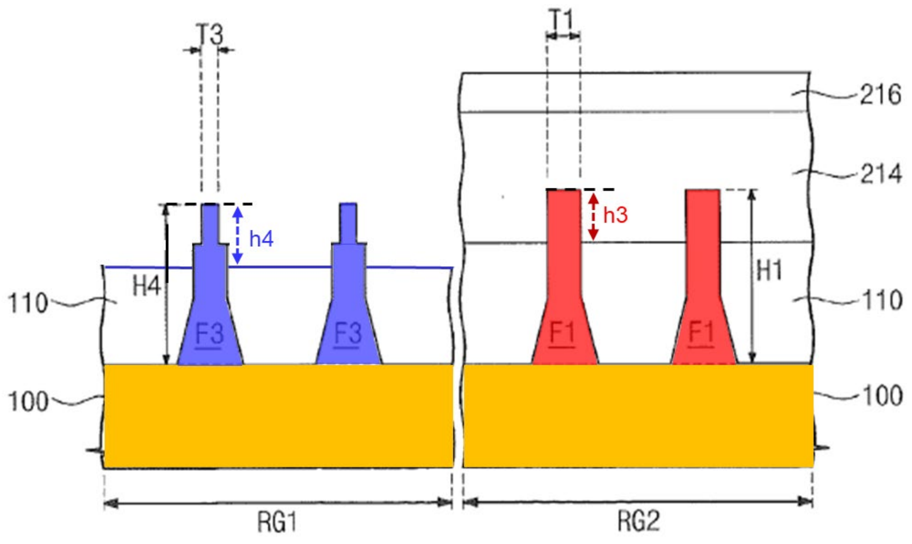
135. As I discussed in Section VIII.B.1 above, a POSA would have (a) been motivated to apply Rachmady's selective fin height teachings to Oh's fin-shaped structure to increase drive current (e.g., for FinFET PMOS devices in 4T SRAM designs) and (b) reasonably expected to succeed in doing so.

136. Thus, in view of the above, the Oh-Rachmady combination renders obvious claim 3.

3. Dependent Claim 4: wherein a top surface of the isolation structure of a first area is higher a top surface of the isolation structure of a second area.

137. The Oh-Rachmady combination renders obvious that a top surface of the isolation structure of the second region RG2 is higher than a top surface of the isolation structure of the first region RG1. Again, I present the modified version of Oh's Figure 26 (with annotations) below, where a top surface of device isolation

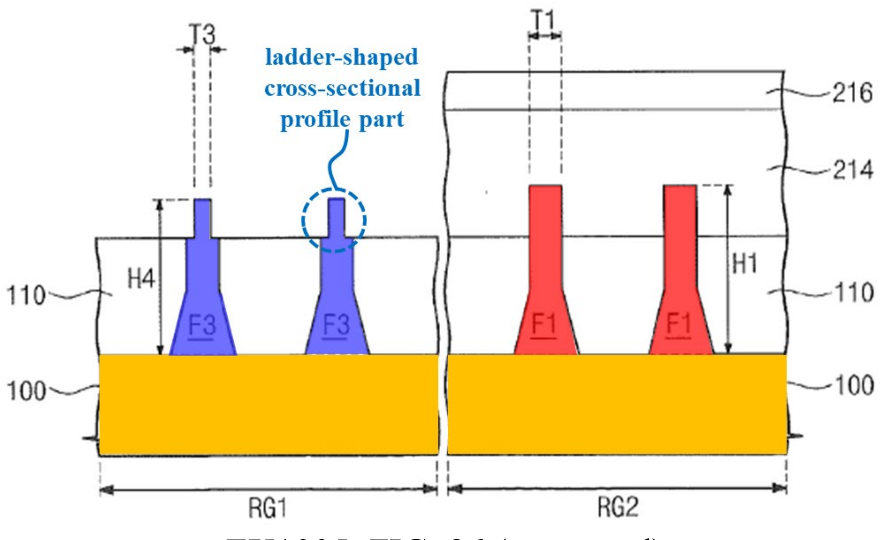
layer 110 in the first region RG1 is lower than a top surface of device isolation layer 110 in the second region RG2 due to Rachmady's selective fin height process. Referring to the modified version of Oh's Figure 26 (reproduced below with annotations)—and as I discussed above in dependent claim 3 (Section VIII.B.2.b) from which claim 4 depends—it would have been obvious for a top surface of device isolation layer 110 in the second region RG2 ("*the isolation structure of a first area*") to be higher than a top surface of device isolation layer 110 in the first region RG1 ("*the isolation structure of a second area*").



EX1005, FIG. 26 (modified and annotated).

138. As I discussed above in dependent claim 3 (Section VIII.B.2.b), applying Rachmady's selective fin height process to Oh's transistors in the first region RG1 would decrease the height of device isolation layer 110 and increase fin height h4 above device isolation layer 110 in the first region RG1. The height

of device isolation layer 110 in the second region RG2 would not change because device isolation layer 110 in the second region RG2 is covered by mask patterns 214 and 216 when etching device isolation layer 110 in the first region RG1 and thus not etched. EX1005, ¶[0069]. Accordingly, a POSA would have understood that the decrease in the height of device isolation layer 110 in the first region RG1 would result in a top surface of device isolation layer 110 in the second region RG2 being higher than a top surface of device isolation layer 100 in the first region RG1. Based on the original location of device isolation layer 110 in the first region RG1 in Oh's Figure 26 (reproduced below with annotations), the top surface of device isolation layer 110 in the first region RG1 would be below the top surface of device isolation layer 110 in the second region RG2 after device isolation layer 110 in the first region RG1 is etched, as shown in the modified version of Oh's Figure 26 (reproduced above with annotations).



EX1005, FIG. 26 (annotated).

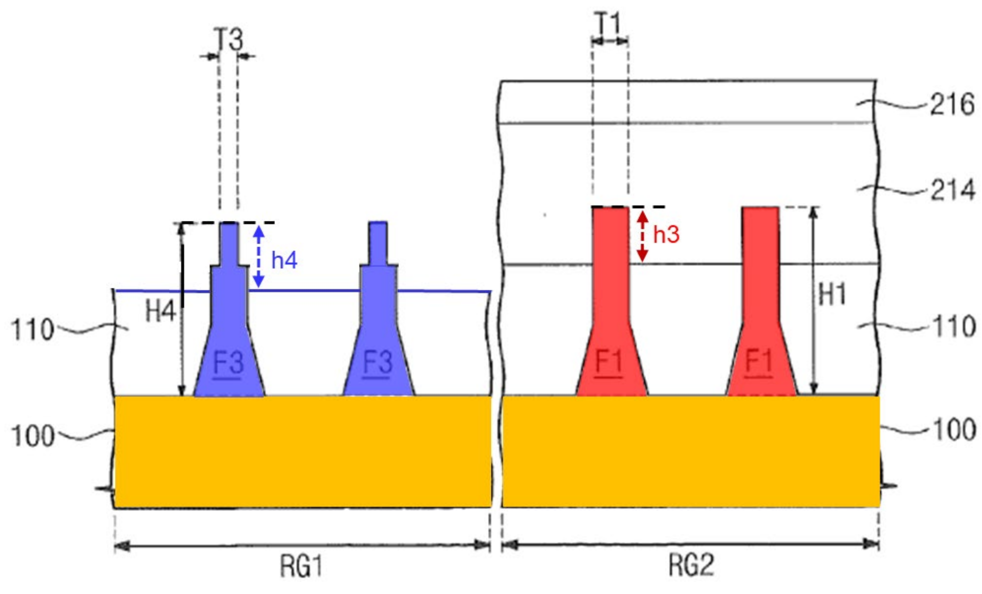
139. As I discussed in Section VIII.B.1 above, a POSA would have (a) been motivated to apply Rachmady's selective fin height teachings to Oh's fin-shaped structure to increase drive current (e.g., for FinFET PMOS devices in 4T SRAM designs) and (b) reasonably expected to succeed in doing so.

140. Thus, in view of the above, the Oh-Rachmady combination renders obvious claim 4.

4. Dependent Claim 5: wherein a height of the first fin-shaped structures protruding from the isolation structure is lower than a height of the second fin-shaped structures protruding from the isolation structure.

141. The Oh-Rachmady combination renders obvious that a height of first fin portions F1 protruding from the isolation structure is lower than a height of third fin portions F3 protruding from the isolation structure. I note that "*the* isolation structure" recited in claim 5 is not supported by independent claim 1 (from which claim 5 depends from) because independent claim 1 does not recite this term. For the purposes of my analysis in this proceeding, I assume "*the* isolation structure" recited in claim 5 is "*an* isolation structure." Again, I present the modified version of Oh's Figure 26 (with annotations) below, where a top surface of device isolation layer 110 in the first region RG1 is lower than a top surface of device isolation layer 110 in the second region RG2 due to Rachmady's selective fin height process. Referring to the modified version of Oh's Figure 26

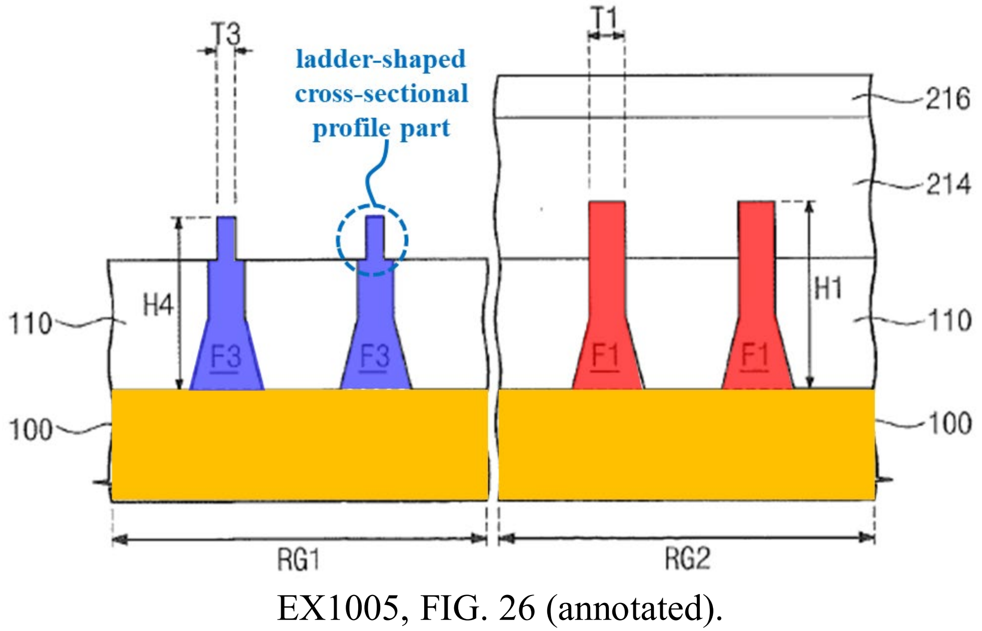
(reproduced below with annotations), a height of **first fin portions F1** (red; "*a height of the first fin-shaped structures*") protruding from device isolation layer 110 ("*the isolation structure*") is lower than a height of **third fin portions F3** (blue; "*a height of the second fin-shaped structures*") protruding from device isolation layer 110 ("*the isolation structure*").



EX1005, FIG. 26 (modified and annotated).

142. As I discussed above in dependent claim 3 (Section VIII.B.2.b), Rachmady teaches forming fin-shaped structures with different fin heights above isolation regions to adjust drive current and achieve desired device characteristics. EX1006, Abstract. Applying Rachmady's selective fin height teachings to Oh's fin-shaped structure in Figure 26 (reproduced below with annotations) would etch device isolation layer 110 in the first region RG1 and increase the fin height of **third fin portions F3** (blue) relative to device isolation layer 110. Referring to the

modified version of Oh's Figure 26 (reproduced above with annotations), the **fin height h3** (red) above device isolation layer 110 in the second region RG2 does not change because the first fin portions F1 and device isolation layer 110 are covered by mask patterns 214 and 216 and thus not etched. EX1005, ¶[0069]. As a result, to meet circuit design requirements of increased drive current (e.g., for FinFET PMOS devices in 4T SRAM designs), the height of **first fin portions F1** (red) protruding from device isolation layer 110 is made lower than the height of **third fin portions F3** (blue) protruding from device isolation layer 110.



EX1005, FIG. 26 (annotated).

143. Accordingly, a POSA would have understood that applying Rachmady's selective fin height teachings to Oh's fin-shaped structure would result in transistors in the first region RG1 and second region RG2 with different fin heights tuned to desired drive current characteristics. These fin heights are

relative to device isolation layer 110 as shown in the modified version of Oh's Figure 26 (reproduced above with annotations). For example, as I discussed above in Section VIII.B.1.a, to meet the 4T SRAM design requirements, a POSA would have been motivated to form FinFET PMOS devices with narrower fin widths based on Oh's teachings to achieve the higher threshold voltages. Referring to Oh's Figure 26 above, the FinFET PMOS devices with narrower fin widths can be the transistors in the first region RG1 having shaped **third fin portions F3** (blue). And to improve SRAM write margin, a POSA would have been further motivated to apply Rachmady's selective fin height teachings to Oh's FinFET PMOS devices to increase drive currents. Referring to the modified version of Oh's Figure 26 (above), the height of **third fin portions F3** (blue) protruding from device isolation layer 110 can be increased to be larger than the height of **first fin portions F1** (red) protruding from device isolation layer 110 to meet the desired drive current as shown in the modified version of Oh's Figure 26 (reproduced above with annotations), while maintaining particular threshold voltages for transistors in the first region RG1 and second region RG2.

144. Based on Rachmady's selective fin height teachings, to increase drive current in Oh's transistors in the first region RG1, device isolation layer 110 in the first region RG1 can be etched and thus the height of **third fin portions F3** (blue) protruding from device isolation layer 110 can be increased, as shown in the

modified version of Oh's Figure 26 above. Accordingly, to meet certain circuit design requirements of increased drive current for first fin portions F1 (e.g., for FinFET PMOS devices in 4T SRAM designs), the height of **first fin portions F1** (red) protruding from device isolation layer 110 can be lower than the height of **third fin portions F3** (blue) protruding from device isolation layer 110.

145. As I discussed in Section VIII.B.1 above, a POSA would have (a) been motivated to apply Rachmady's selective fin height teachings to Oh's fin-shaped structure to increase drive current and (b) reasonably expected to succeed in doing so.

146. Thus, in view of the above, the Oh-Rachmady combination renders obvious claim 5.

C. Ground 3: The combination of Wann and Lin renders obvious claims 1-6.

147. My discussion below is on the combination of Wann and Lin and how this combination renders obvious claims 1-6 of the '510 patent.

1. A POSA would have been motivated to combine Wann and Lin.

148. It is my opinion that Wann and Lin are both in the same field of endeavor: the formation of FinFETs to increase performance and decrease die size in semiconductor devices. EX1007, ¶¶[0002]-[0003]; EX1008, ¶¶[0002]-[0004]. Wann and Lin recognize that these FinFET benefits are advantageous to IC designs

as semiconductor devices continue to be manufactured in smaller technology nodes. EX1007, ¶¶[0002]-[0003]; EX1008, ¶¶[0002]-[0004]. For example, Wann states that "[t]he increased surface area of the channel and source/drain regions in a FinFET results in faster, more reliable and better-controlled semiconductor transistor devices," and that "devices designed using planar transistors can also reap benefits by manufacturing using FinFETs." EX1007, ¶¶[0002]-[0003]. Similarly, Lin states that "[t]he introduction of FinFETs has the advantageous feature of increasing drive current without the cost of occupying more chip area." EX1008, ¶[0004].

149. Wann and Lin both disclose mandrel/spacer processes to form fin structures. For example, Wann discloses forming mandrels over a substrate, conformally depositing a spacer material around the mandrels, removing the mandrels to leave behind spacers, and using the spacers as a mask to etch underlying layers to form fin structures. EX1007, ¶[0015]. Wann also discloses that "thinner fins that are closer together can be formed" using the mandrel/spacer process. EX1007, ¶[0015]. Wann's mandrel/spacer process form fins "hav[ing] the same height and width dimension." EX1007, ¶[0015].

150. Lin discloses a similar mandrel/spacer process, including details on the spacer formation and mandrel removal processes. EX1008, ¶¶[0039]-[0054]. Lin states that in its mandrel/spacer process "the spacing and depth between the

fins [] are better controlled and may be substantially equal between all of the fins []." EX1008, ¶[0062]. Lin also states that, with regard to a wet etch process used in its mandrel/spacer process, "the wet etch process is a lower cost and allows a higher throughput (wafers per hour) than a dry etch process." EX1008, ¶[0063].

151. Whereas Wann describes its mandrel/spacer process without specific details on the processes of spacer formation and mandrel removal, Lin provides such teachings to improve fin reliability and manufacturability. In my opinion, it would have been obvious to combine Wann's and Lin's teachings because a POSA would have (a) been motivated to apply Lin's mandrel/spacer process to Wann's fin-shaped structures to improve fin reliability and manufacturability and (b) reasonably expected to succeed in doing so.

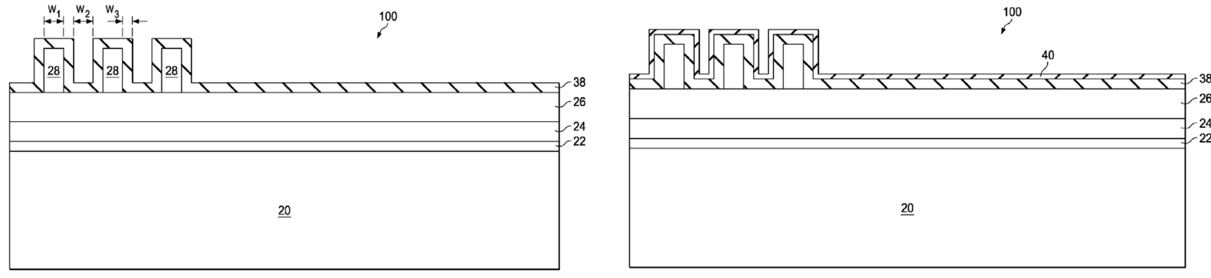
a. A POSA would have been motivated to apply Lin's mandrel/spacer process to Wann's fin-shaped structures.

152. In my opinion, a POSA would have been motivated to apply Lin's mandrel/spacer process to Wann's fin-shaped structures to improve fin reliability and manufacturability conferred by Lin's mandrel/spacer process. Wann states its goal of "improved methods for automatically converting older planar structure layouts to FinFET structure layouts." EX1007, ¶[0003]. To meet this goal, Wann describes "a selective fin-shaping process to allow individual fin width and fin height control." EX1007, ¶[0019]. Based on Wann's selective fin-shaping process,

"[b]enefits may include improved circuit design flexibility and FinFET process margin for designers and foundries that are transferring from a planar-based design to a FinFET-based design." EX1007, ¶[0019].

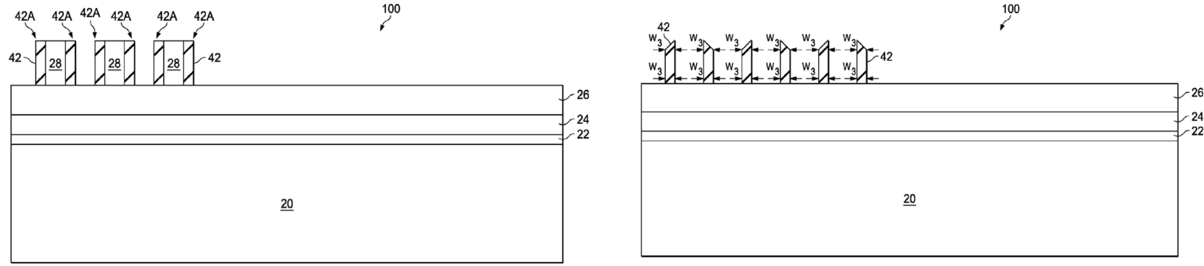
153. In my opinion, a POSA would have understood that Lin's mandrel/spacer process can be used to form Wann's regular fins with uniform dimensions and spacing for its fin-shaping process. For example, Wann states that "[t]hese fins are referred to herein as regular fins because they all have the same height and width dimensions". EX1007, ¶[0015]. In Wann's fin-shaped structures, the regular fins before Wann's fin-shaping process would have uniform dimensions and spacing after formed with Lin's mandrel/spacer process.

154. Lin describes details of a mandrel/spacer process that forms fins with uniform dimensions and uniform spacing from one another. EX1008, ¶[0062]. For example, referring to Lin's Figure 5 (reproduced below), Lin discloses a "fourth dielectric layer 38 may be conformally deposited over the third dielectric layer 26 and the first hardmask portions 28 such that the thickness of the fourth dielectric layer 38 on the top surface of the third dielectric layer 26 and the sidewalls of the first hardmask portions 28 is substantially a same thickness." EX1008, ¶[0039]. Next, referring to Lin's Figure 6 (reproduced below), Lin discloses "the formation of a fifth dielectric layer 40 on the fourth dielectric layer 38." EX1008, ¶[0040].



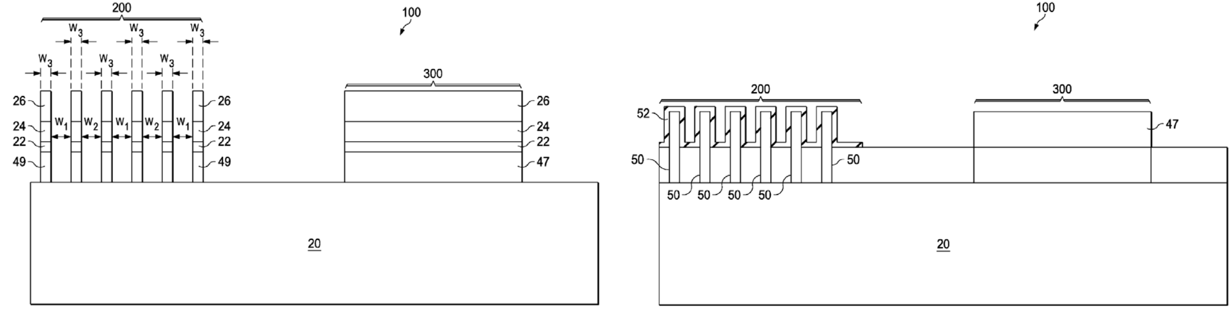
EX1008, FIGs. 5 (left) and 6 (right).

155. Following the formation of fifth dielectric layer 40, referring to Lin's Figure 7 (reproduced below), Lin discloses that "the etching of the fifth dielectric layer 40 and horizontal portions of the fourth dielectric layer 38 (step 522) to expose the first hardmask portions 28 and form fin spacers 42." EX1008, ¶[0042]. Lin states that "[t]he presence of the fourth [*sic*] dielectric layer 40 on the fourth dielectric layer 38 keeps the corners 42A (shoulders) of the fin spacers 42 to be substantially square." EX1008, ¶[0042]. Lin also states that "[t]he first hardmask portions 28 form a mandrel to support the fin spacers 42 and may help to prevent deformation of the fin spacers 42 during this etching step." EX1008, ¶[0042]. Next, referring to Lin's Figure 8 (reproduced below), "the first hardmask portions 28 may be removed," where "the removal of the first hardmask portions 28 may be a multiple etch process." EX1008, ¶[0043]. The multiple etch process includes a dry etch followed by a wet etch. EX1008, ¶[0043].



EX1008, FIGs. 7 (left) and 8 (right).

156. Based on fin spacers 42 in Lin's Figure 8 and after further processing, a pattern is transferred to substrate 20 to form semiconductor strips 49 as shown in Lin's Figure 13 (reproduced below). EX1008, ¶¶[0045]-[0051]. Lin explains that "[t]he spacing between the semiconductor strips 49 W_1 and W_2 are defined by the widths W_1 and W_2 between the fin spacers 42 (see FIGS. 5 and 8)." EX1008, ¶[0051]. Lin further explains that "the width W_1 is substantially equal to the width W_2." EX1008, ¶[0051]. Based on semiconductor strips 49 and after further processing, fins 50 are formed as shown in Lin's Figure 15 (reproduced below). EX1008, ¶¶[0052]-[0059].



EX1008, FIGs. 13 (left) and 15 (right).

157. As a result, Lin's mandrel/spacer process uses uniform pattern and uniform etching to form fins with uniform dimensions and uniform spacing from

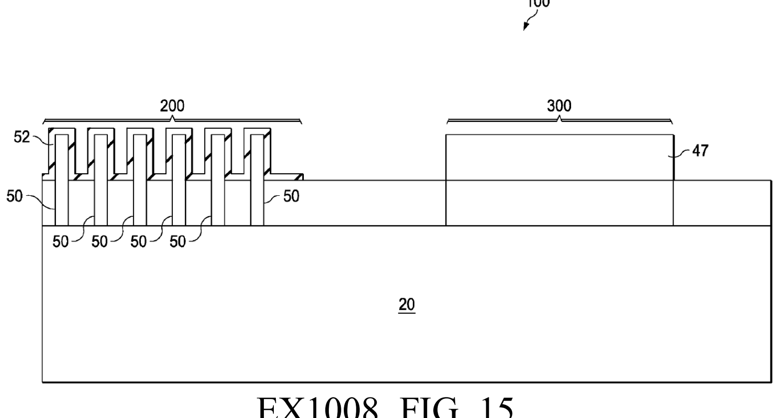
one another (the width W_1 is substantially equal to the width W_2). Lin explains that "the spacing and depth between the fins 50 are better controlled and may be substantially equal between all of the fins 50." EX1008, ¶[0062]. An additional benefit of Lin's mandrel/spacer process is its mandrel removal process, which includes a "wet etch process [that] is a lower cost and allows a higher throughput (wafers per hour) than a dry etch process." EX1008, ¶[0063].

158. In view of the above benefits of Lin's mandrel/spacer process, a POSA would have been motivated to combine Wann's fin-shaped structures and Lin's mandrel/spacer process teachings. A POSA would have understood that Lin's mandrel/spacer process improves the manufacturability of Wann's fins—e.g., from reliability, controllability, and cost points of views—thus improving the circuit design flexibility of Wann's fin-shaping process.

b. A POSA would have reasonably expected to succeed in applying Lin's mandrel/spacer process to Wann's fin-shaped structures.

159. Wann and Lin disclose well-known semiconductor fabrication processes—the mandrel/spacer process—to form fin structures, and thus a POSA would have reasonably expected that applying Lin's mandrel/spacer process teachings to form Wann's fin-shaped structures would successfully form fin-shaped structures with uniform spacing between lower parts of adjacent regular fins and between lower parts of adjacent shaped fins.

160. While Wann does not explicitly disclose details on spacer formation and mandrel formation and removal in its mandrel/spacer process to form its regular fins, Lin fills this gap by providing details on a mandrel/spacer process that can be used to form any number of regular fins prior to Wann's fin-shaping process on the regular fins, for example, with a similar fin structure as fins 50 shown in Lin's Figure 15 (reproduced below). In my opinion, a POSA would have reasonably expected to succeed in forming Wann's fin-shaped structures, where a distance between lower parts of adjacent regular fins is the same as a distance between lower parts of adjacent shaped fins. This is because Lin's mandrel/spacer process can be used to form Wann's regular fins, in which one or more of the regular fins can be further shaped by Wann's fin-shaping process.



EX1008, FIG. 15.

2. The Wann-Lin five-fin FinFET structure.

161. Below I describe Wann's five-fin FinFET embodiment, which has "2 regular fins, 2 fins shaped a particular way, and 1 fin shaped a different way."

EX1007, ¶[0042]. Wann's five-fin FinFET embodiment is disclosed, but it is not illustrated by Wann. For example purposes, Wann's selective fin-shaping process in Figure 2 is described in the context of a three-fin FinFET embodiment. But Wann's selective fin-shaping process is applicable to a wide variety of FinFETs with fins arranged in many different ways. EX1007, ¶¶[0041], [0042]. In fact, I calculate the number of fin permutations in Wann's five-fin FinFET embodiment to be 30 based on the following: $5! / (2! \times 2!) = 30$. This calculation takes into account that 2 of the fins are regular fins, 2 of the fins are shaped a particular way, and 1 of the fins is shaped in a different way. From these 30 fin permutations, I calculate 6 fin arrangements with 2 regular fins adjacent to one another and 2 shaped fins adjacent to one another.

162. Below, I describe combining Wann's five-fin FinFET embodiment with the teachings of Lin to form a FinFET structure, where a distance between lower parts of a pair of adjacent regular fins is the same as a distance between lower parts of a pair of adjacent shaped fins. A POSA would have found it obvious to apply Lin's spacer/mandrel process to any one of the 30 fin permutations of the Wann five-fin FinFET embodiment to improve fin reliability and manufacturability, which includes the 6 fin arrangements (with 2 regular fins adjacent to one another and 2 shaped fins adjacent to one another) that I discussed above. I apply one of these 6 permutations below and refer to this combination of

Wann's and Lin's teachings as the "Wann-Lin five-fin FinFET structure." A POSA would have understood that this fin permutation is obvious to try since it is merely one fin arrangement from a finite number of identified, predictable solutions, with a reasonable expectation of success. Additionally, the arrangement of the regular and shaped fins would not affect Wann's fin-shaping process goal: to vary the channel width of a FinFET "beyond an integer multiple of a single fin dimension." EX1007, ¶[0019].

a. Wann's disclosure applies to a wide variety of FinFETs with various fin arrangements.

163. Wann states that its "semiconductor apparatus includes fin field-effect transistor (FinFETs) having shaped fins and regular fins," where the "[s]haped fins have top portions that may be smaller, larger, thinner, or shorter than top portions of regular fins." EX1007, Abstract. Wann also states that "[t]he bottom portions of shaped fins and regular fins are the same." EX1007, Abstract.

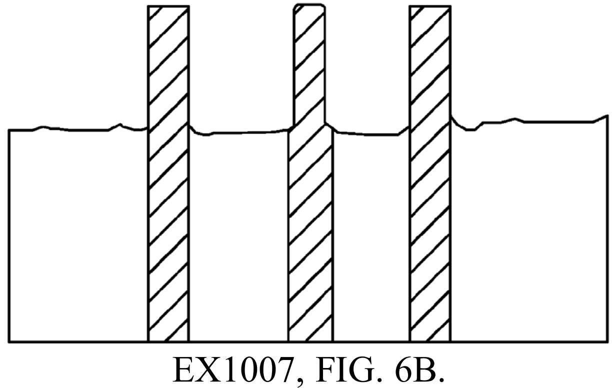
164. In the rapidly evolving semiconductor technology, the conversion of planar transistors to three-dimensional transistors, such as FinFETs, can offer improved transistor performance. For example, Wann recognized that the increased channel and source/drain surface areas in the fin-based structure of a FinFET improves device performance: "[t]he increase surface area of the channel and source/drain regions in a FinFET result in faster, more reliable, and better-

controlled semiconductor transistor devices." EX1007, ¶[0002]. Wann also recognized that semiconductor devices originally designed using planar transistors can benefit from manufacturing these devices with FinFETs, "such as increase performance and efficiencies and decreased die size." EX1007, ¶[0003]. To improve the conversion of planar transistors to FinFETs, Wann discloses a semiconductor manufacturing method to form FinFETs with equivalent electrical characteristics as their planar transistor counterparts. EX1007, ¶[0003].

165. To manufacture FinFETs with particular electrical characteristics, Wann discloses a selective fin-shaping process with individual fin width and fin height control: "the present disclosure pertain to a selective fin-shaping process to allow individual fin width and fin height control." EX1007, ¶[0019]. Wann explains the channel width control by the fin-shaping process: "[b]y shaping one or more fins in a FinFET, the channel width of a FinFET may vary beyond an integer multiple of a single fin dimension." EX1007, ¶[0019]. Wann's fin-shaping process envisages FinFETs with a wide variety of fin arrangements, where the "selective fin-shaping may enlarge one or more fins, shorten one or more fins, thin one or more fins, reduce all fin dimensions at the same time, or change the shape of one or more fins some other way to create shaped fins while other regular fins remain unchanged." EX1007, ¶[0019]. With these fin arrangement variations, Wann states that "[b]enefits may include improved circuit design flexibility and FinFET

process margin for designers and foundries that are transferring from a planar-based design to a FinFET-based design." EX1007, ¶[0019].

166. Wann describes its selective fin-shaping process in the context of a three-fin FinFET structure, such as the FinFET structure shown in Wann's Figure 6B (reproduced below). Figure 6B shows a three-fin FinFET structure with 2 regular fins (outer fins) and 1 shaped fin (middle fin). EX1007, ¶[0035]. As shown in Wann's Figure 6B, though a top portion of the middle fin has been shaped, Wann states that "[t]he bottom portions of all three fins are substantially the same, because the bottom portions are not shaped." EX1007, ¶[0035].



EX1007, FIG. 6B.

167. Wann's fin-shaping process is not limited to three-fin FinFET structures. In fact, Wann's selective fin-shaping process is applicable to FinFETs with any number of fins and any fin arrangement. EX1007, ¶[0041]. Wann states that "[t]he present disclosure is not limited [to] a FinFET having a particular number of fins," and that "[i]n reality a FinFET may have any number of fins from 1 to several or even hundreds." EX1007, ¶[0041]. With regard to fin arrangement,

Wann states that "[t]he apparatus may include many FinFETs of different sizes having different number of fins," where "[s]ome FinFETs may have shaped fins and some FinFETs may not." EX1007, ¶[0042]. Further, Wann is not limited to FinFETs with a particular fin arrangement, explaining that "FinFETs may have only one or more shaped fins, one or more regular fins, or a mixture of shaped fins and regular fins." EX1007, Abstract.

168. Though not illustrated in Wann's figures, Wann discloses "a five-fin FinFET [that] may have 2 regular fins, 2 fins shaped a particular way, and 1 fin shaped a different way." EX1007, ¶[0042]. As I describe below, this five-fin FinFET can be formed by Wann's selective fin-shaping process similar to Wann's three-fin FinFET (shown in figures 3B, 5A, 5B, 6A, and 6B).

b. Wann's fin-shaping process applies to various fin arrangements of FinFETs, including Wann's five-fin FinFET embodiment.

169. As I discussed above, Wann discloses a selective fin-shaping process to shape individual fin widths and fin heights for FinFETs with any number of fins to manufacture FinFETs with particular electrical characteristics. EX1007, ¶¶[0019], [0041]. One such example is Wann's five-fin FinFET embodiment, which has "2 regular fins, 2 fins shaped a particular way, and 1 fin shaped in a different way." EX1007, ¶[0042]. Wann states that "more than one fin may be shaped in the same opening" and "[a] FinFET may have more than one type of

shaped fins," as "the [fin-shaping] process may be repeated to shape fins any number of times." EX1007, ¶¶[0041], [0042]. Wann also states that "[w]hile the process may be repeated to shape fins any number of times, each time the fin-shaping process uses manufacturing resources including one photomask and one to several deposition and etching processes." EX1007, ¶[0042]. Accordingly, the 5 fins in Wann's five-fin FinFET embodiment can be arranged in any order since Wann discloses a fin-shaping process that can be repeated any number of times, in which the fin-shaping process uses photomask and etching operations for each iteration. EX1007, ¶[0042]. For example, Wann's five-fin FinFET embodiment can have the following sequence: 2 regular fins adjacent to one another, 2 fins shaped a particular way adjacent to one another, and 1 fin shaped in a different way. In my opinion, a POSA would have understood that this fin arrangement is one out of a finite number of predictable fin arrangements, with a reasonable expectation of success, as I describe below.

170. In regard of the finite number of fin arrangements for Wann's five-fin FinFET embodiment, as I discussed above, a POSA would have understood that 30 unique permutations are possible based on Wann's disclosure. Wann states that "more than one fin may be shaped in the same opening" and that "[a] FinFET may have more than one type of shaped fins." EX1007, ¶¶[0041], [0042]. Wann further states that "for FinFETs having more than 3 fins, the shaped fin may be spaced

apart from regular fins by 2 regular fins." EX1007, ¶[0041]. Therefore, for Wann's "five-fin FinFET [that] may have 2 regular fins, 2 fins shaped a particular way, and 1 fin shaped a different way," a POSA would have understood that there are 30 unique permutations to arrange the 2 regular fins, 2 particularly shaped fins, and 1 differently shaped fin. EX1007, ¶[0042]. And, 6 of these 30 unique permutations include the fin arrangement with 2 regular fins adjacent to one another and 2 fins shaped a particular way adjacent to one another. Based on Wann's fin-shaping process, a POSA would have understood that one of the many fin permutations of Wann's five-fin FinFET embodiment includes arranging the fins from left to right (i.e., in the same order as listed in Wann's paragraph 24): **2 regular fins adjacent to one another** (red) and **2 fins shaped a particular way adjacent to one another** (blue)—just like the claimed fin-shaped structure in the '510 patent—as shown in Illustration 8 below.

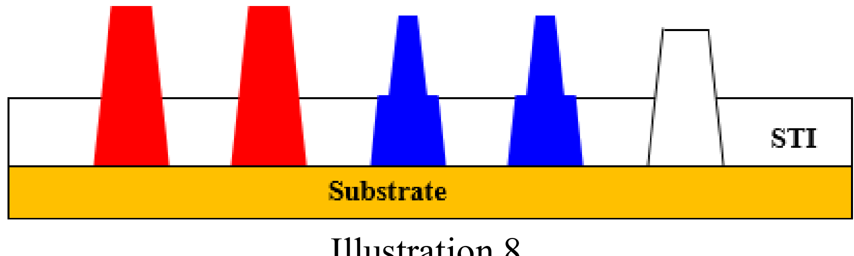
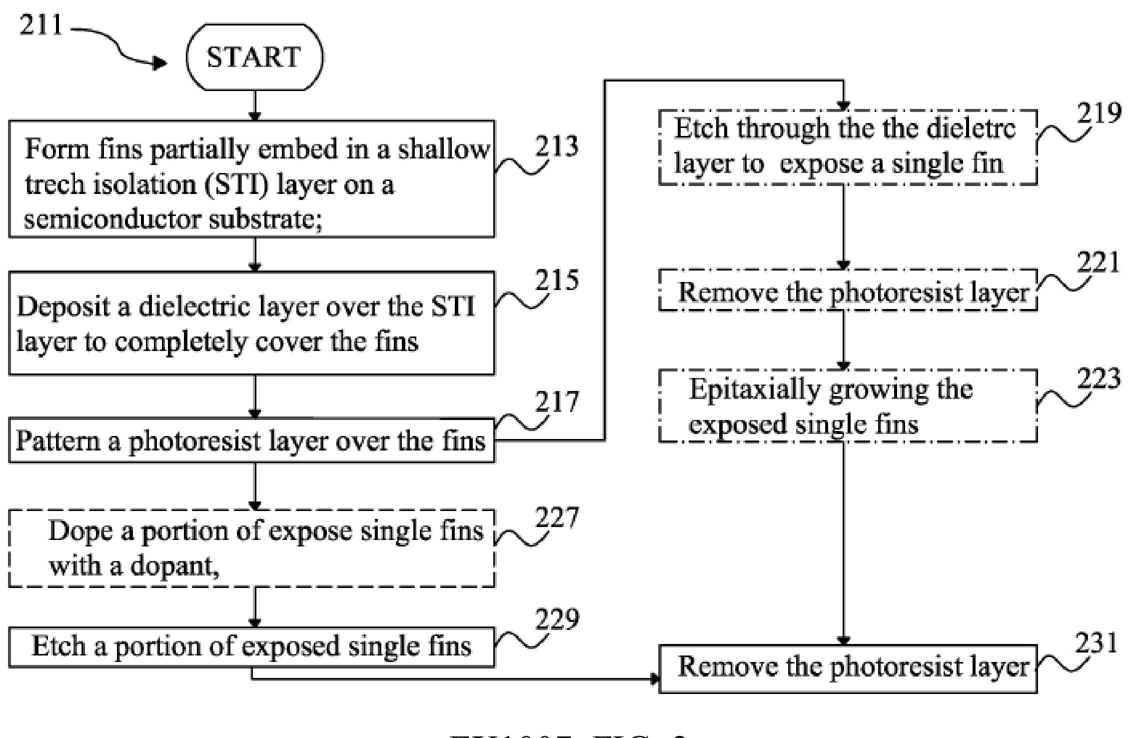


Illustration 8.

171. Referring to Wann's Figure 2 (reproduced below), Wann describes a process flow 211 for selective fin-shaping. EX1007, ¶[0020]. Wann illustrates the selective fin-shaping process flow with a three-fin FinFET embodiment as shown

in Figures 3B, 5A, 5B, 6A, and 6B.



EX1007, FIG. 2.

172. Wann describes that certain operations in process flow 211 are optional and may be omitted. For example, operation 215 can be omitted as "[t]he optional dielectric layer is used if the one or more fins are to be enlarged." EX1007, ¶[0021]. To form shorter and/or narrowly shaped fins, Wann's process flow 211 can perform operations 213, 217, 227, 229, and 231. EX1007, ¶¶[0022]-[0037]. Wann further discloses that operation 227 is optional: "in optional (broken line) operation 227 a portion of the exposed single fin is doped with a dopant." EX1007, ¶[0023]. As such, operation 227 may be omitted.

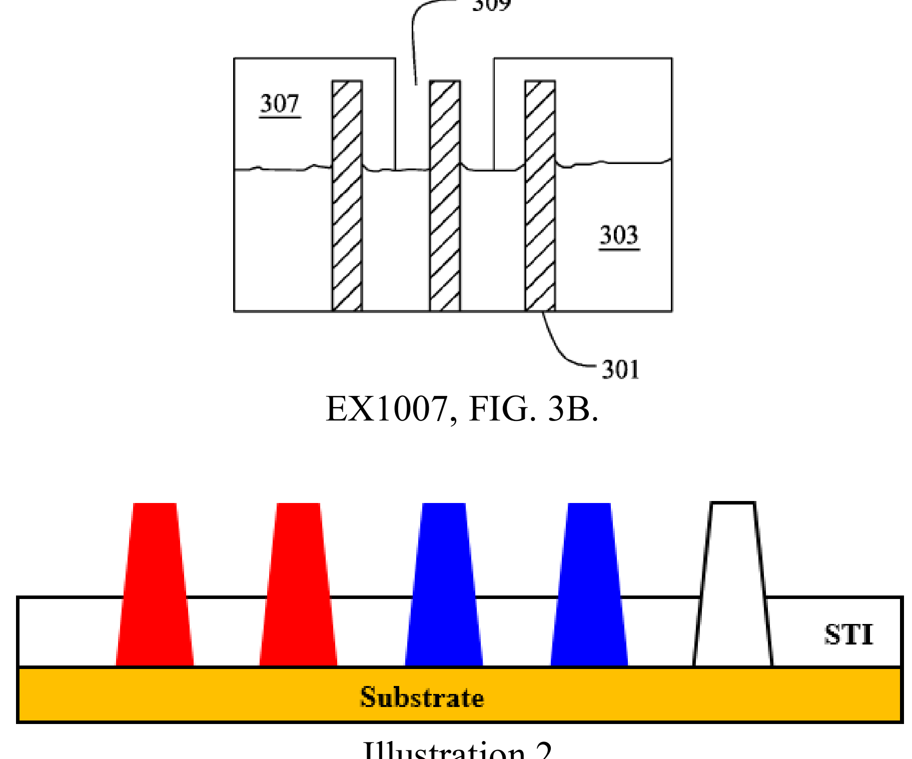
173. Accordingly, I provide Illustrations 2-9 below to pictorially depict the

formation process of Wann's five-fin FinFET embodiment described in Wann's textual disclosure. Illustrations 2-9 map operations 213, 217, 229, and 231 of Figure 2 to Wann's five-fin FinFET embodiment. For comparison, I use Wann's three-fin FinFET embodiment illustrated by Figures 3B, 5A, 5B, 6A, and 6B in my analysis of the formation of Wann's five-fin FinFET embodiment. Also, I provide Illustrations 10-15 below in my analysis of claims 1-6 of the '510 patent to pictorially depict Wann's and Lin's textual disclosure. As I discussed above in Section VIII.C.1.a, applying Lin's mandrel/spacer process, a POSA would have formed Wann's 5 regular fins with uniform dimensions and uniform spacing from one another to improve fin reliability and manufacturability.

174. Though Wann and Lin illustrate fins with ideal rectangle shapes, a POSA would have understood that these rectangle shapes are ideal and not the actual shape of manufactured fins. Due to variations in semiconductor processing, the manufactured fins are not rectangles. In Illustrations 2-15 that I provide below, I illustrate the fins in Wann's five-fin FinFET embodiment and the Wann-Lin five-fin FinFET structure as having a trapezoid shape, which in my opinion is a closer representation to manufactured fins (as compared to a rectangle shape).

175. Referring to operation 213 of Wann's selective fin-shaping process flow 211 in Figure 2, "fins partially embedded in shallow trench isolation (STI) layers are formed on a semiconductor substrate." EX1007, ¶[0020]. Wann also

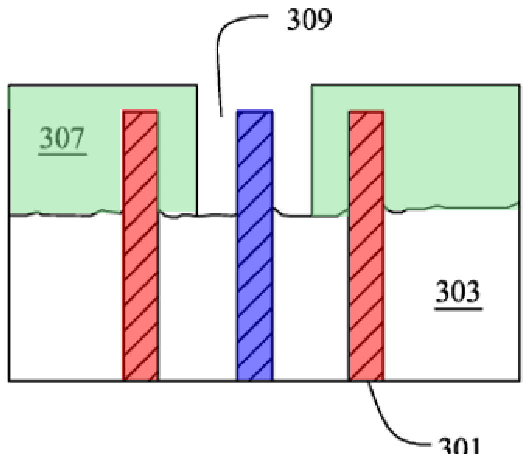
discloses forming the fins using a mandrel/spacer method by etching a semiconductor substrate. EX1007, ¶[0015]. Referring to Wann's Figure 3B (reproduced below), Wann illustrates a three-fin FinFET embodiment with 3 regular fins 301 formed by the mandrel/spacer method and partially embedded in STI layer 303 on a semiconductor substrate (not shown). EX1007, ¶[0020]. Similarly, 5 regular fins (red, blue, and white) of Wann's five-fin FinFET embodiment can be formed by the mandrel/spacer process and embedded in the STI layers on the semiconductor substrate, as shown in the Illustration 2 below. The red, blue, and white colors of the fins in Illustrations 2-15 and annotated Wann's figures below indicate different processes to be performed on these fins.



EX1007, FIG. 3B.

Illustration 2.

176. Referring to operation 217 of Wann's selective fin-shaping process flow 211 in Figure 2, Wann discloses that "[i]n operation 217 a photoresist layer is patterned over the fins" to expose particular fins to be shaped. EX1007, ¶[0022]. For example, after operation 217, the three-fin FinFET illustrated in Wann's Figure 3B (reproduced below with annotations) includes a photoresist layer 307 (green) formed over the two outer regular fins 301 (red) and patterned to create an opening 309 to expose the middle regular fin (blue). EX1007, ¶[0022]. Similarly, for Wann's five-fin FinFET embodiment having "2 regular fins, 2 fins shaped a particular way, and 1 fin shaped a different way," a photoresist layer (green) can be patterned over three fins (red and white) of the five-fin FinFET and two fins (blue) of the five-fin FinFET can be exposed for the fin-shaping process, as shown in Illustration 3 below.



EX1007, FIG. 3B (annotated).

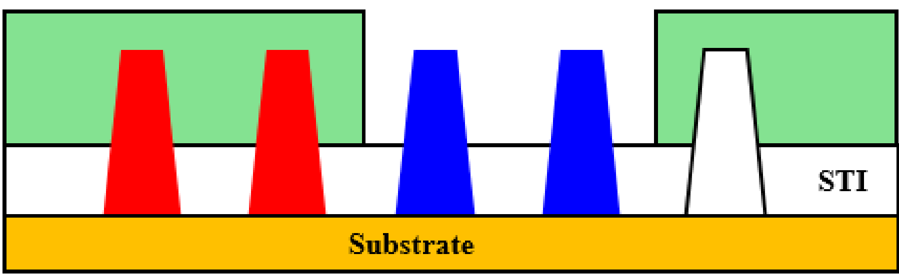
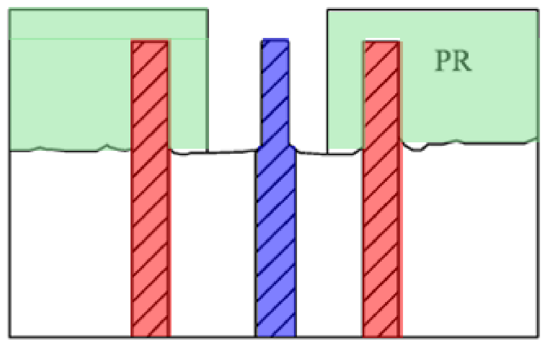


Illustration 3.

177. Referring to operation 229 of Wann's selective fin-shaping process flow 211 in Figure 2, "a portion of the exposed single fins is etched and removed." EX1007, ¶[0025]. For example, after etching in operation 229, the three-fin FinFET, having one shaped fin (blue) and two regular fins (red), is illustrated in Wann's Figure 5B (reproduced below with annotations). Similarly, the two exposed fins of the five-fin FinFET can be etched to have thinner top portions. Accordingly, the five-fin FinFET embodiment after the fin-shaping process can be shown in Illustration 4 below. Wann further discloses that the STI layer is also etched during Wann's fin-shaping process, though the etching of STI layer surrounding the shaped fin is not explicitly illustrated in Wann's Fig. 5B or Illustration 4 (both reproduced below). EX1007, ¶[0035]. I show the etched STI layer surrounding the shaped fin in Illustration 9 below.



EX1007, FIG. 5B (annotated).

178. Referring to operation 229 of Wann's selective fin-shaping process flow 211 in Figure 2, "a portion of the exposed single fins is etched and removed." EX1007, ¶[0025]. Here, "the exposed single fin is thinner and somewhat shorter than neighboring fins that are protected under the photoresist." EX1007, ¶[0029]. Wann discloses that "[v]arious etching methods may be applied directly to the silicon fin to change its shape," where the "[v]arious etching methods may be categorized into dry etch and wet etch, isotropic and anisotropic, and different combinations resulting in different shapes." EX1007, ¶[0030]. Wann also discloses that "while the shaped fin may be shorter than the regular fins, the top portion of the shaped fin may be the same length or longer than the top portion of regular fins because the STI layer is also etched and more of the top portion of the shaped fin may be exposed." EX1007, ¶[0035]. Similarly, the two exposed fins (blue) of Wann's five-fin FinFET embodiment can be etched, as shown in Illustration 4 below. Here, the exposed fins (blue) are thinner and shorter than neighboring fins (red and white) that are protected under the photoresist layer (green).

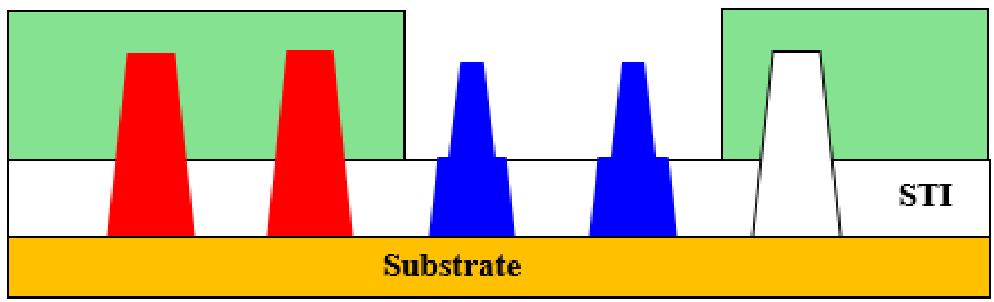
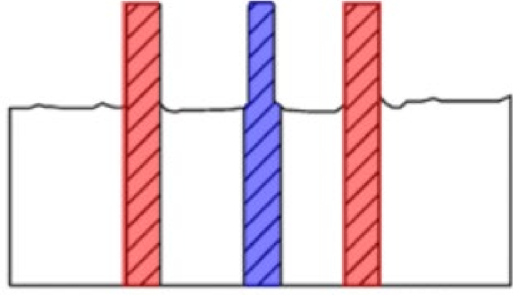


Illustration 4.

179. Referring to operation 231 of Wann's selective fin-shaping process flow 211 in Figure 2, Wann further discloses that "in operation 231 the photoresist layer is removed." EX1007, ¶[0040]. For example, after removal of the photoresist layer in operation 231, Wann's three-fin FinFET embodiment having one shaped fin (blue) and two regular fins (red) is shown in Wann's Figure 6B (reproduced below with annotations). Similarly, as shown in the Illustration 5 below, the photoresist layer (green) is removed in Wann's five-fin FinFET embodiment after operation 231.



EX1007, FIG. 6B (annotated).

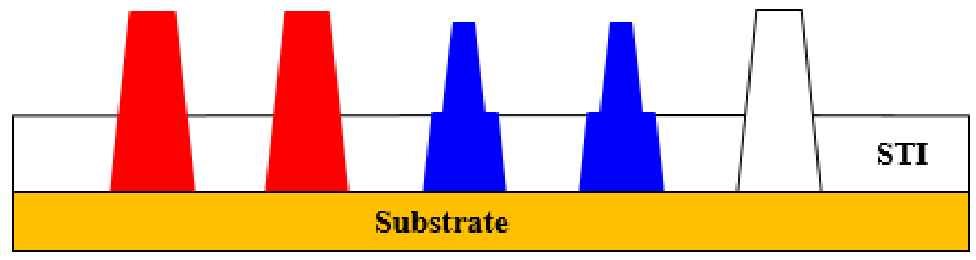


Illustration 5.

180. As I discussed above, Wann discloses that “the [fin-shaping] process may be repeated to shape fins any number of times” and “each time the fin-shaping process uses manufacturing resources including one photomask and one to several deposition and etching processes.” EX1007, ¶[0042]. Accordingly, for Wann’s five-fin FinFET embodiment having “2 regular fins, 2 fins shaped a particular way, and 1 fin shaped a different way,” the “1 fin shaped a different way” can be formed by repeating the sequence of operations 217, 229, and 231 of Figure 2, in a similar manner described above with respect to Wann’s three-fin FinFET embodiment.

181. Referring to operation 217 of Wann’s selective fin-shaping process flow 211 in Figure 2, additional photoresist layer (green) is formed over the 5 fins of Wann’s five-fin FinFET embodiment and patterned to create an opening to expose 1 regular fin (white), as shown in Illustration 6 below.

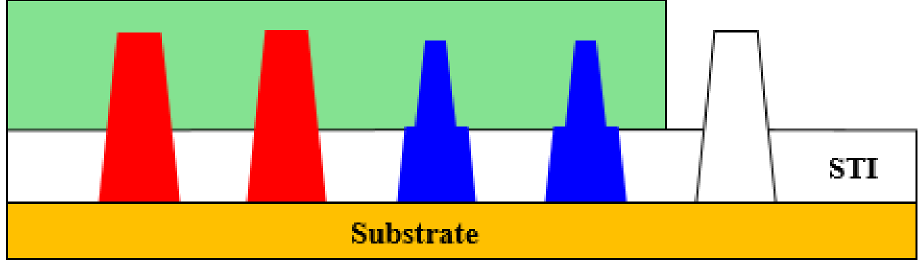
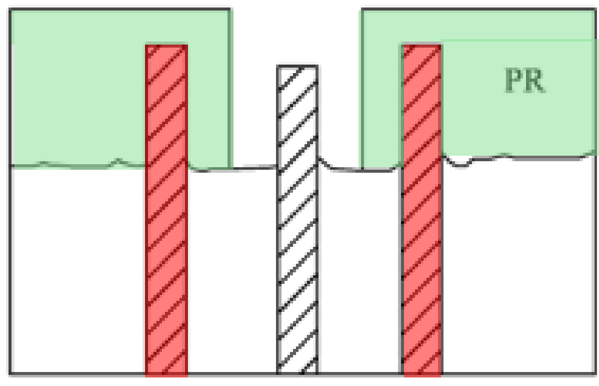


Illustration 6.

182. Referring to operation 229 of Wann's selective fin-shaping process flow 211 in Figure 2, a portion of the exposed regular fin (white) in Wann's five-fin FinFET embodiment is etched, as shown in Illustration 7 below. Here, the exposed regular fin (white) is shorter than neighboring fins that are protected under the photoresist layer (green). Wann states that "[t]he various etching methods may be categorized into dry etch and wet etch, isotropic and anisotropic, and different combinations resulting in different shapes." EX1007, ¶[0030]. Wann's Figure 5A (reproduced below with annotations) illustrates Wann's three-fin FinFET embodiment with the shaped fin (white) having a short top portion after repeated operation 229. Similarly, with two regular fins (red) and two shaped fins (blue) of Wann's five-fin FinFET embodiment covered by the additional photoresist layer (green), the exposed single fin (white) can be etched to have a shorter top portion, as shown in Illustration 7 below.



EX1007, FIG. 5A (annotated).

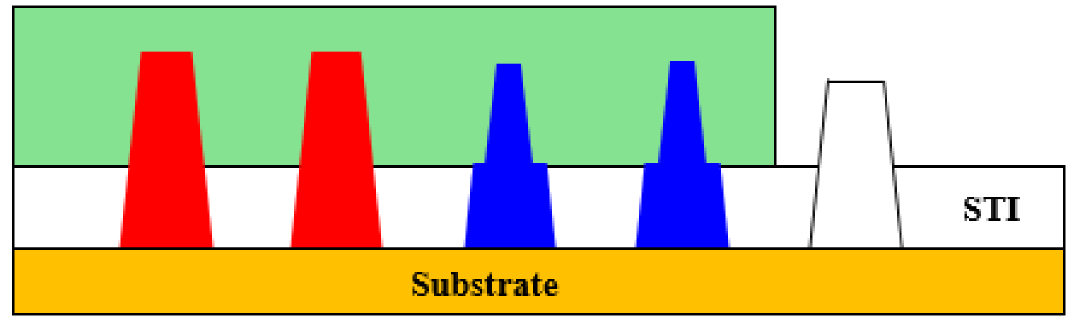
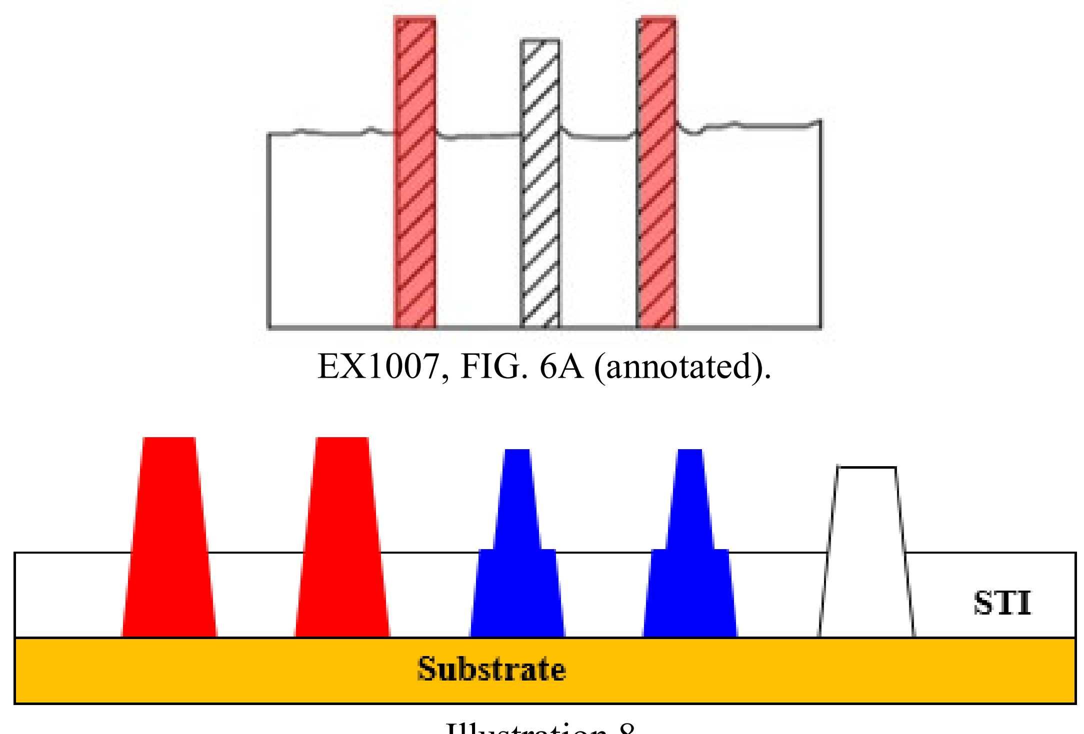


Illustration 7.

183. Referring to operation 231 of Wann's selective fin-shaping process flow 211 in Figure 2, the additional photoresist layer (green) in Wann's five-fin FinFET embodiment is removed, as shown in Illustration 8 below. After operation 231 of removing the photoresist layer (green), Wann's three-fin FinFET embodiment is illustrated in Wann's Figure 6A (reproduced below with annotations). EX1007, ¶[0035]. Similarly, as shown in Illustration 8 below, the additional photoresist layer (green) can be removed, to form the shaped fins and regular fins of Wann's five-fin FinFET embodiment having "2 regular fins, 2 fins shaped a particular way, and 1 fin shaped a different way" described in Wann.

EX1007, ¶[0042]. Referring to Illustration 8 below, Wann's five-fin FinFET embodiment can have 2 regular fins adjacent to one another (red), 2 fins shaped a particular way (blue) adjacent to one another, and 1 fin shaped in a different way (white).



EX1007, FIG. 6A (annotated).

Illustration 8.

184. Though Wann's Figures 6A and 6B do not appear to illustrate the removal of STI layer surrounding the shaped fin, Wann explicitly discloses that "the STI layer is also etched and more of the top portion of the shaped fin may be exposed." EX1007, ¶[0035]. Similarly, the exposed STI layer surrounding the two adjacent shaped fins and one differently-shaped fin of Wann's five-fin FinFET embodiment is also etched during the fin-shaping process. Accordingly, Wann's

five-fin FinFET embodiment with STI layer etched after the fin-shaping process can be shown in Illustration 9 below. Additionally, though the STI layer surrounding the two adjacent shaped fins and the STI layer surrounding the differently-shaped fin may not necessarily at a same level, the STI layer surrounding the two adjacent shaped fins (blue) and the differently-shaped fin (white) can be at a lower level than the STI layer surrounding the two adjacent regular fins (red).

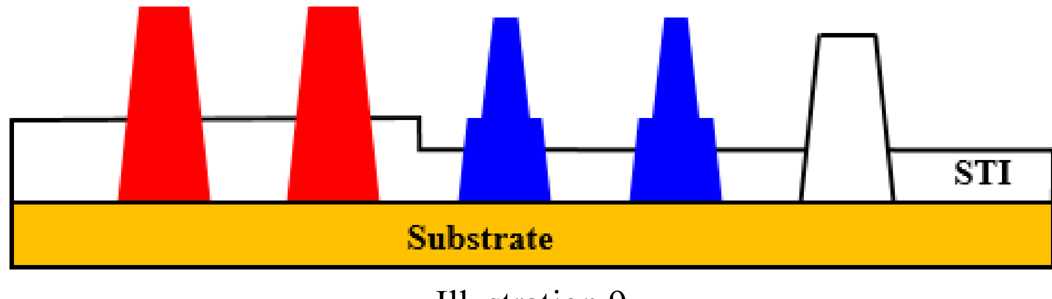


Illustration 9.

185. Additionally, the 2 regular fins, 2 particularly-shaped fins, and 1 differently-shaped fin of the five-fin FinFET disclosed in Wann can be arranged in a finite number of different ways. A POSA would have understood Illustration 8 above provides one possible arrangement of the "2 regular fins, 2 fins shaped a particular way, and 1 fin shaped a different way" in the five-fin FinFET embodiment disclosed by Wann. Consistent with Wann's disclosure, the five-fin FinFET embodiment may have the fin order shown above, where the **two regular fins** (red) are adjacent to one another and the **two shaped fins** (blue) are adjacent

to one another. Based on Wann's teachings, a POSA would have been motivated to form the above the five-fin FinFET embodiment with the fin arrangement and etched STI layer because they provide circuit flexibility to ease design constraints associated with planar-to-FinFET conversion when progressing to smaller technology nodes.

186. To summarize the above discussion, I map operations 213, 217, 229, and 231 of Figure 2 to Wann's three-fin FinFET embodiment (shown in Figures 3B, 5A, 5B, 6A, and 6B above) and to Wann's five-fin FinFET embodiment (shown in Illustrations 2-8 above) in Charts 1-7 below.

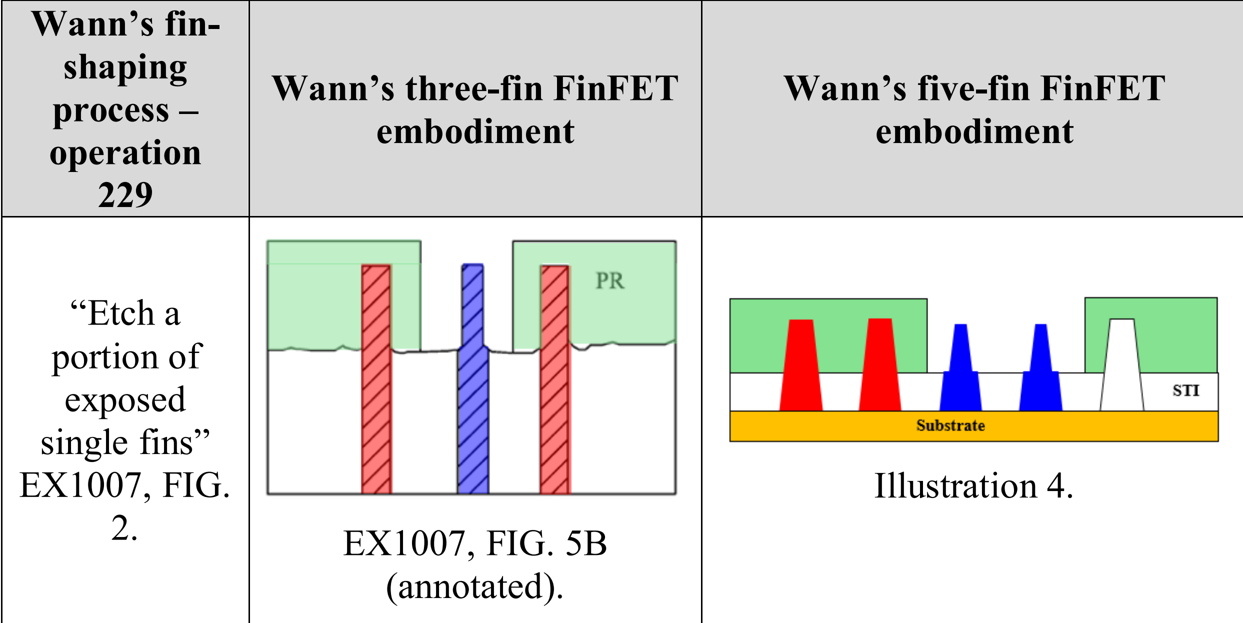
a. Chart 1: Operation 213

Wann's fin-shaping process – operation 213	**Wann's three-fin FinFET embodiment**	**Wann's five-fin FinFET embodiment**
"Form fins partially embed[ded] in a shallow trech [*sic*] isolation (STI) layer on a semiconductor substrate" EX1007, FIG. 2.	 EX1007, FIG. 3B (annotated).	 Illustration 2.

b. Chart 2: Operation 217

Wann's fin-shaping process – operation 217	Wann's three-fin FinFET embodiment	Wann's five-fin FinFET embodiment
"Pattern a photoresist layer over the fins" EX1007, FIG. 2.	309 307 303 301 EX1007, FIG. 3B (annotated).	STI Substrate Illustration 3.

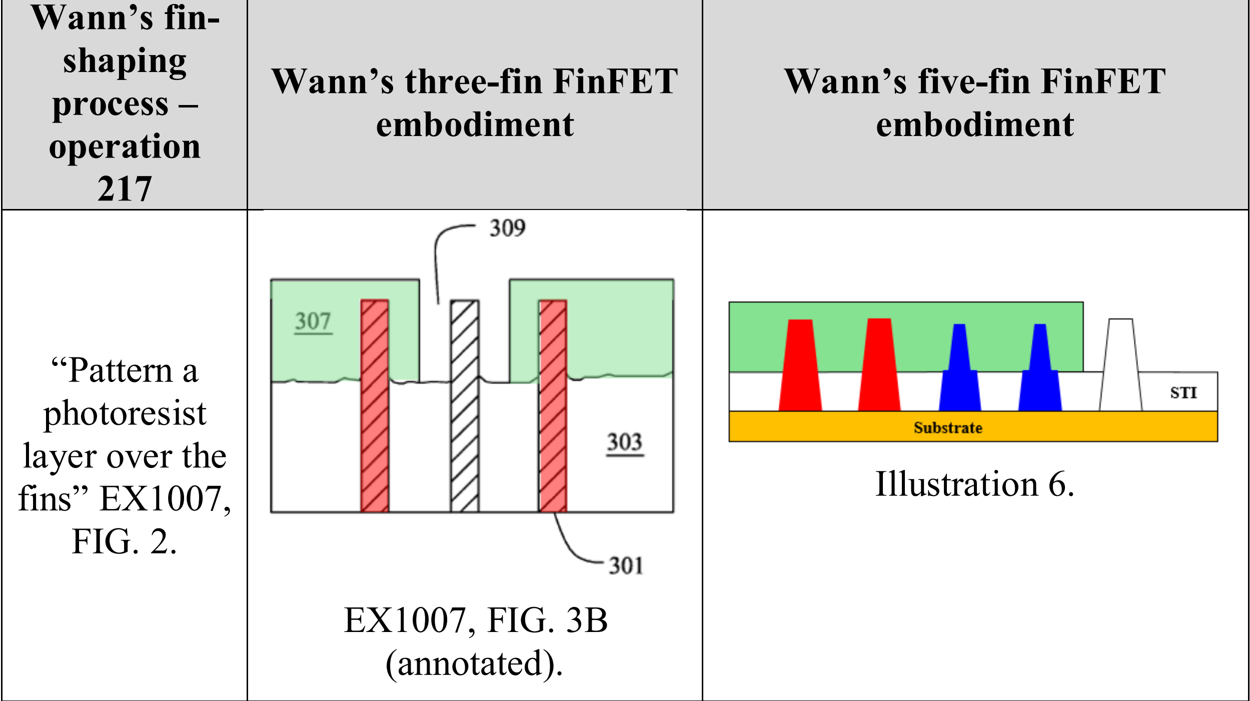
c. Chart 3: Operation 229

Wann's fin-shaping process – operation 229	Wann's three-fin FinFET embodiment	Wann's five-fin FinFET embodiment
"Etch a portion of exposed single fins" EX1007, FIG. 2.	 EX1007, FIG. 5B (annotated).	Illustration 4.

d. Chart 4: Operation 231

Wann's fin-shaping process – operation 231	Wann's three-fin FinFET embodiment	Wann's five-fin FinFET embodiment
"Remove the photoresist layer" EX1007.	EX1007, FIG. 6B (annotated).	STI Substrate Illustration 5.

e. Chart 5: Operation 217 (repeated)

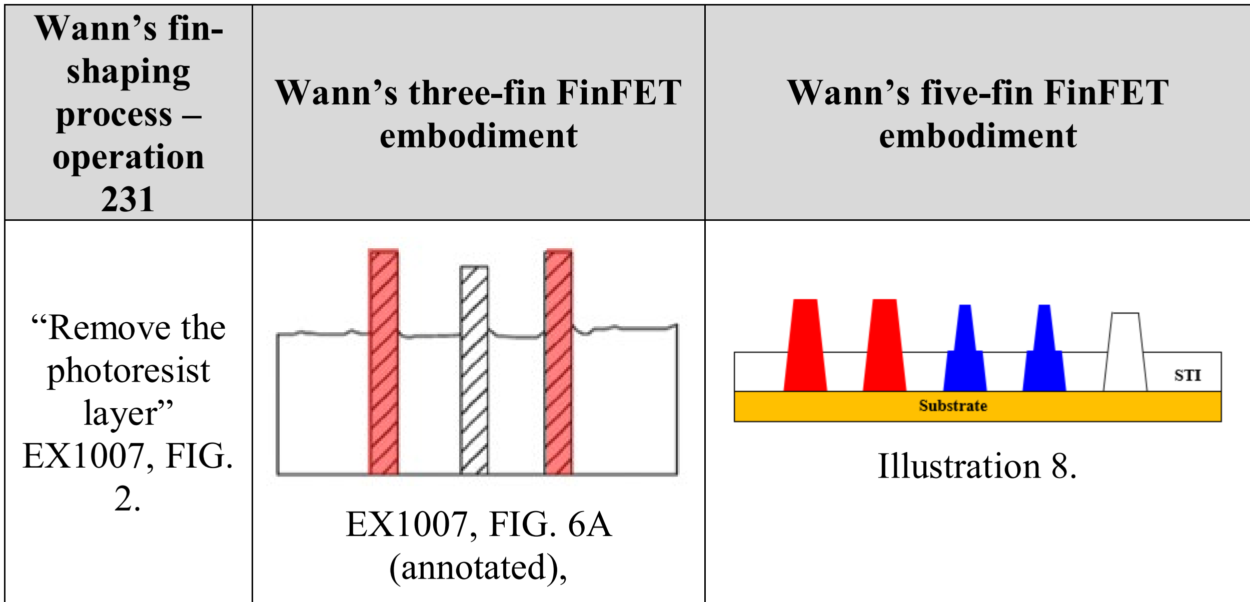


Wann's fin-shaping process – operation 217	Wann's three-fin FinFET embodiment	Wann's five-fin FinFET embodiment
"Pattern a photoresist layer over the fins" EX1007, FIG. 2.	309 307 303 301 EX1007, FIG. 3B (annotated).	STI Substrate Illustration 6.

f. Chart 6: Operation 229 (repeated)

Wann's fin-shaping process – operation 229	**Wann's three-fin FinFET embodiment**	**Wann's five-fin FinFET embodiment**
"Etch a portion of exposed single fins" EX1007, FIG. 2.	PR EX1007, FIG 5A (annotated).	STI Substrate Illustration 7.

g. Chart 7: Operation 231 (repeated)



Wann's fin-shaping process – operation 231	**Wann's three-fin FinFET embodiment**	**Wann's five-fin FinFET embodiment**
"Remove the photoresist layer" EX1007, FIG. 2.	EX1007, FIG. 6A (annotated),	STI Substrate Illustration 8.

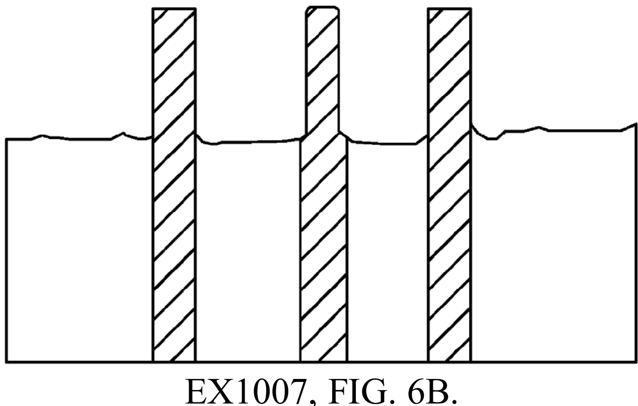
3. Independent Claim 1

a) [1.P]: A fin-shaped structure, comprising:

187. Wann and Lin disclose the fin-shaped structure. Wann "relates generally to integrated circuit devices, and more particularly to structure and methods for forming fin field-effect transistors (FinFETs)." EX1007, ¶[0001]. Wann states that "[v]arious embodiments of the present disclosure pertain to a selective fin-shaping process to allow individual fin width and fin height control." EX1007, ¶[0019]. Similarly, Lin is directed to "a method of forming a FinFET device." EX1008, Abstract. Lin discloses a mandrel/spacer process that forms fins with uniform dimensions and uniform spacing from one another. EX1008, ¶[0062].

188. The '510 patent claims can refer to a "*fin-shaped structure*" with a single FinFET or with multiple FinFETs. It is my opinion that Wann teaches both. In one of its embodiments, Wann discloses a three-fin FinFET with a shaped fin in the middle, as shown in Wann's Figure 6B (reproduced below). Wann recognized that "[i]n reality a FinFET may have any number of fins from 1 to several or even hundreds." EX1007, ¶[0041]. Wann further states that its "disclosure is not limited [to] a FinFET having a particular number of fins." EX1007, ¶[0041]. Wann explains that "more than one fin may be shaped in the same opening" and "[a] FinFET may have more than one type of shaped fins." EX1007, ¶¶[0041], [0042]. Wann also extends its teachings to devices with multiple FinFETs, where an

"apparatus may include many FinFETs of different sizes having different number of fins." EX1007, ¶[0042].



EX1007, FIG. 6B.

189. The Wann-Lin five-fin FinFET structure is another example of a single FinFET with a fin-shaped structure. As shown in Illustration 8 below, the Wann-Lin five-fin FinFET structure includes **two regular fins** (red) and **two shaped fins** (blue). As I discussed in Section VIII.C.1 above, it would have been obvious to combine Wann's and Lin's teachings because a POSA would have (a) been motivated to apply Lin's mandrel/spacer process to Wann's five-fin FinFET embodiment to improve fin reliability and manufacturability and (b) reasonably expected to succeed in doing so.

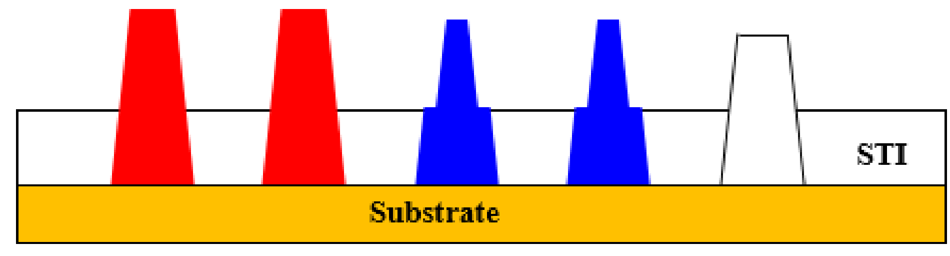


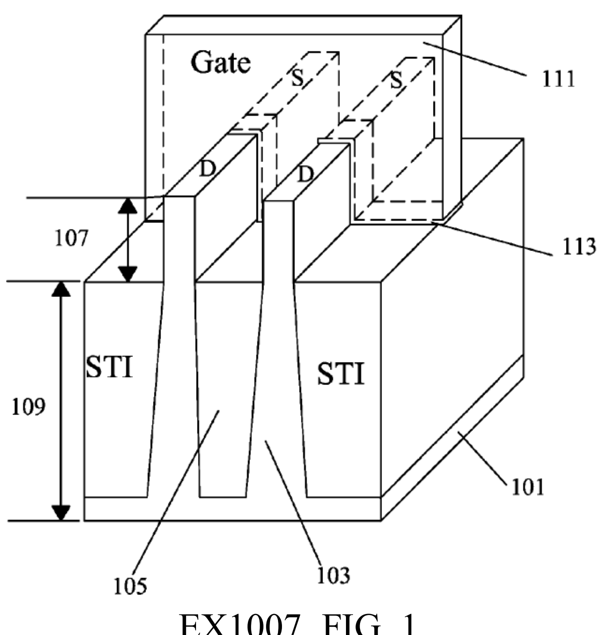
Illustration 8.

190. Thus, in view of the above, Wann and Lin disclose limitation [1.P].

b) [1.a]: a substrate having a plurality of first fin-shaped structures and a plurality [of] second fin-shaped structures, and the first fin-shaped structures comprising a first fin and a second fin, the second fin-shaped structures comprising a third fin and a fourth fin,

191. The Wann-Lin five-fin FinFET structure renders obvious a substrate having first fin-shaped structures including a first fin and a second fin and second fin-shaped structures including a third fin and a fourth fin.

192. Wann discloses a FinFET with a substrate 101 having a plurality of fins 103 in its Figure 1 (reproduced below). EX1007, ¶[0013]. Though a single FinFET with two fins is shown in Figure 1, Wann discloses that "[i]n reality a FinFET may have any number of fins from 1 to several or even hundreds." EX1007, ¶[0041].



EX1007, FIG. 1.

193. Referring to Wann-Lin five-fin FinFET structure in Illustration 8 below, a **substrate** (orange) has **two regular fins** (red; "*a plurality of first fin-shaped structures*") and **two shaped fins** (blue; "*a plurality of second fin-shaped structures*"). The **two regular fins** (red) include two fins ("*a first fin and a second fin*"). The **two shaped fins** (blue) include two fins ("*a third fin and a fourth fin*").

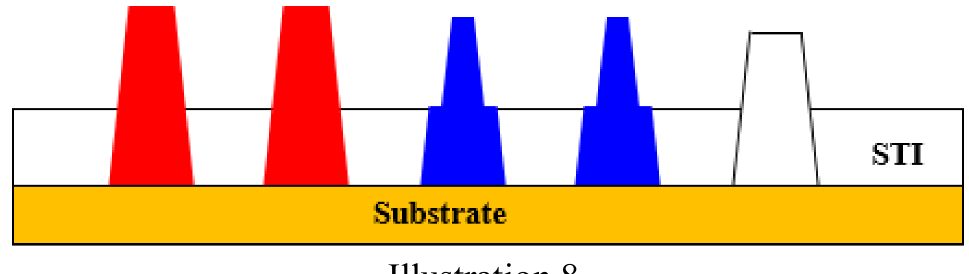


Illustration 8.

194. As I discussed above, Wann discloses that five fins of its five-fin FinFET embodiment can be formed on a **substrate** (orange). As I also discussed above in Section VIII.C.2, there are a finite number of fin arrangements that satisfy Wann's disclosure of 5 fins having two regular fins, two shaped fins, and one different fin. Accordingly, for the Wann-Lin five-fin FinFET structure shown in Illustration 8, a POSA would have found it obvious for the two fins on the left side of the **substrate** (orange) to be the **two regular fins** (red). EX1007, ¶[0020]. Next, as I discussed above in Section VIII.C.2 on Wann's fin-shaping process, it would have been obvious for the **two shaped fins** (blue) to be formed by a first selective fin-shaping process and for the one differently-shaped fin (white) to be shaped by repeating the selective fin-shaping process. The **two shaped fins** (blue) and one

differently-shaped fin (white) are thinner and/or shorter than the **two regular fins** (red). EX1007, ¶[0035]. Accordingly, a POSA would have understood that the Wann-Lin five-fin FinFET structure to have a plurality of first fin-shaped structures and a plurality second fin-shaped structures.

195. Thus, in view of the above, the Wann-Lin five-fin FinFET structure renders obvious limitation [1.a].

c) [1.b]: wherein a first distance between adjacent top corners of the first fin and the second fin of the first fin-shaped structures is less than a second distance between adjacent top corners of the third fin and the fourth fin of the second fin-shaped structures

196. The Wann-Lin five-fin FinFET structure renders obvious the fin-shaped structure where a first distance between adjacent top corners of the first fin and the second fin of the first fin-shaped structures is less than a second distance between adjacent top corners of the third fin and the fourth fin of the second fin-shaped structures. Referring to the Wann-Lin five-fin FinFET structure shown in Illustration 10 below, a **distance P1** (red; "*a first distance*") between adjacent top corners of the **two regular fins** (red; "*the first fin and the second fin of the first fin-shaped structures*") is less than a **distance P3** (blue; "*a second distance*") between adjacent top corners of the **two shaped fins** (blue; "*the third fin and the fourth fin of the second fin-shaped structures*").

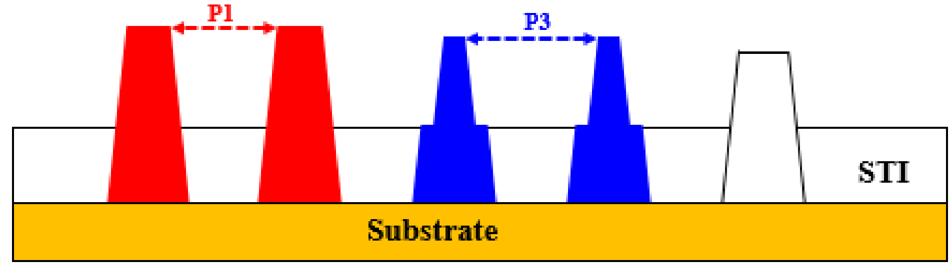
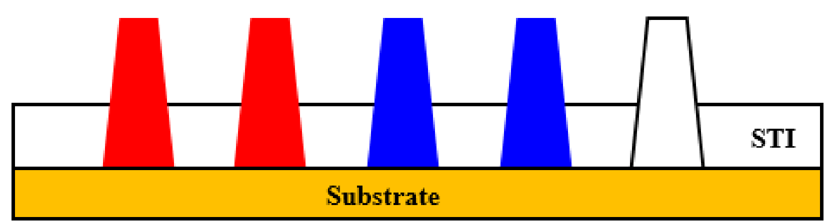


Illustration 10.

197. Due to the teachings of Wann and Lin and how this combination results in the Wann-Lin five-fin FinFET structure, the **first distance P1** (red) is shorter than the **second distance P3** (blue). To the extent Wann does not appear to disclose specific distances between the adjacent **two regular fins** (red) and between the adjacent **two shaped fins** (blue), based on Lin's mandrel/spacer process and Wann's fin-shaping process, a POSA would have understood that the combination of these teachings results in **first distance P1** (red) and **second distance P3** (blue).

198. As I discussed in Section VIII.C.2 above, 5 regular fins (red, blue, and white) in the Wann-Lin five-fin FinFET structure are formed as shown in Illustration 2 (below). Based on Lin's mandrel/spacer process that forms fins with uniform dimensions and uniform spacing from one another, these 5 regular fins are the same and the spacing between adjacent regular fins is also the same, as described in Section VIII.C.3.d below. EX1008, ¶[0062].



EX1003, Illustration 2.

199. After forming the 5 regular fins, as I discussed in Section VIII.C.2 above, a photoresist layer is formed over the 5 regular fins and an opening is formed to expose 2 regular fins (blue), which are etched as shown in Illustration 4 below. Additionally, referring to Wann's selective fin-shaping process for Wann's three-fin FinFET embodiment shown in Wann's Figure 5B (reproduced below), Wann discloses that "[t]he shaped fin has a narrower top portion that may be the same, slightly shorter, or longer than the neighboring regular fins." EX1007, ¶[0035]. As I discussed in Section VIII.C.2 above, Wann's selective fin-shaping process applies to Wann's five-fin FinFET embodiment. As a result of Wann's fin-shaping process, the exposed regular fins become the **two shaped fins** (blue). The **two shaped fins** (blue) are thinner and shorter than neighboring fins protected under a **photoresist layer** (green)—the 3 regular fins (red and white).

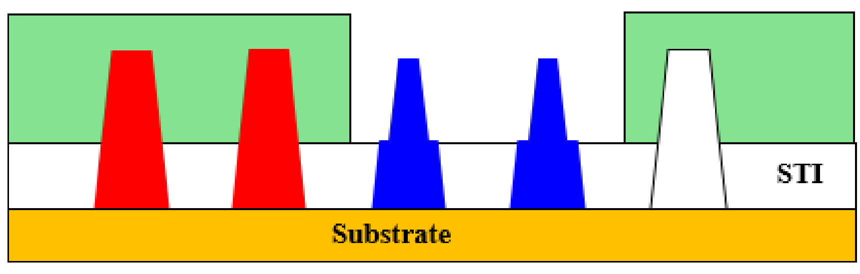
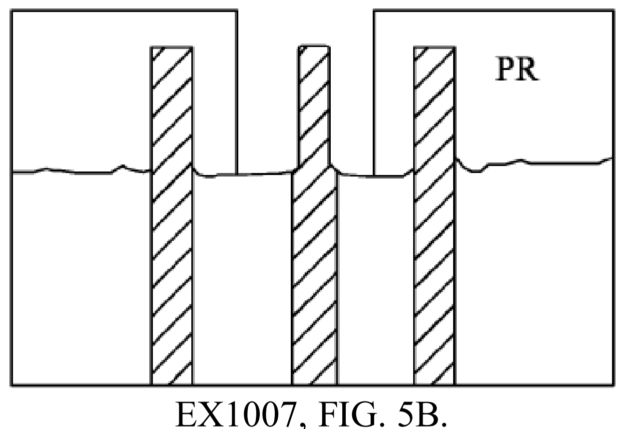


Illustration 4.



EX1007, FIG. 5B.

200. As I discuss below with respect to limitation [1.c] in Section VIII.C.3.d, a POSA would have understood that applying Lin's mandrel/spacer process to Wann's five-fin FinFET embodiment results in the formation of regular fins with uniform dimensions and uniform spacing from one another. Thereafter, Wann's selective fin-shaping process can be applied to the uniformly-shaped and uniformly-spaced regular fins to form the Wann-Lin five-fin FinFET structure. As Wann's selective fin-shaping process shapes top portions of the regular fins and the lower portions of the fins remain unchanged, a distance between lower parts of adjacent **two regular fins** (red) is the same as a distance between lower parts of adjacent **two shaped fins** (blue). Whereas, after Wann's selective fin-shaping process to narrow top portions of the adjacent **two shaped fins** (blue), a POSA would have understood that the distance between adjacent top corners of the adjacent **two shaped fins** (blue) is increased.

201. Accordingly, as shown in Illustration 10 above, a POSA would have

understood that the Wann-Lin five-fin FinFET structure has **first distance P1** (red) between adjacent top corners of the **two adjacent regular fins** (red) that is less than **second distance P3** (blue) between adjacent top corners of the **two adjacent shaped fins** (blue), because the top portions of the **two adjacent shaped fins** (blue) are narrower than the top portions of the **two adjacent regular fins** (red).

202. Thus, in view of the above, the Wann-Lin five-fin FinFET structure renders obvious limitation [1.b].

d) [1.c]: while a third distance between adjacent lower parts of the first fin and the second fin is the same as a fourth distance between adjacent lower parts of the third fin and the fourth fin;

203. The Wann-Lin five-fin FinFET structure renders obvious a fin-shaped structure where a third distance between adjacent lower parts of the first fin and the second fin is the same as a fourth distance between adjacent lower parts of the third fin and the fourth fin. Referring to the Wann-Lin five-fin FinFET structure in Illustration 11 below, a **distance P5** (red; "*a third distance*") between adjacent lower parts of the **two regular fins** (red; "*the first fin and the second fin*") is the same as a **distance P6** (green; "*a fourth distance*") between adjacent lower parts of the **two shaped fins** (blue; "*the third fin and the fourth fin*").

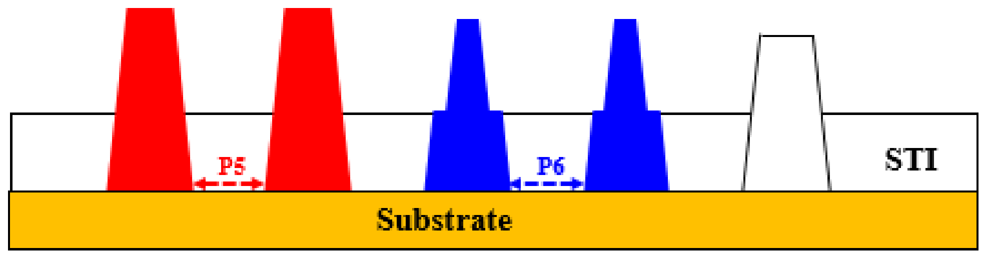


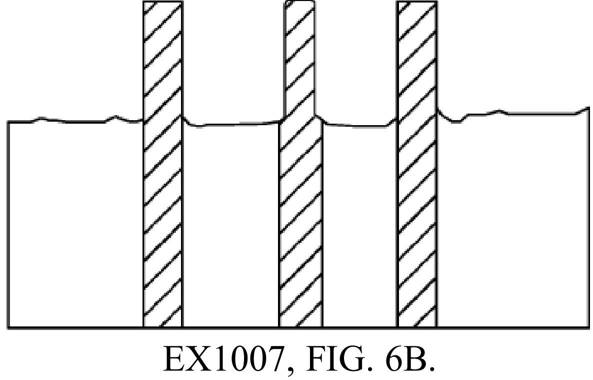
Illustration 11.

204. To the extent Wann does not appear to disclose specific distances between the adjacent **two regular fins** (red) and between the adjacent **two shaped fins** (blue), based on Lin's mandrel/spacer process and Wann's fin-shaping process, a POSA would have understood the combination of these teachings results in **third distance P5** (red) and **fourth distance P6** (blue). Additionally, a POSA would have understood that the **third distance P5** (red) and **fourth distance P6** (blue) are the same, as I discuss below.

205. Specifically, Lin describes a mandrel/spacer process that forms fins with uniform dimensions and uniform spacing from one another. EX1008, ¶[0062]. Lin states that "the spacing and depth between the fins [] are better controlled and may be substantially equal between all of the fins []." EX1008, ¶[0062]. As a result, applying Lin's mandrel/spacer process to Wann's five-fin FinFET embodiment, a POSA would have understood that distances between lower parts of adjacent regular fins in the Wann-Lin five-fin FinFET structure is the same.

206. Additionally, referring to Wann's selective fin-shaping process for Wann's three-fin FinFET embodiment shown in Wann's Figure 6B (reproduced

below), the top portion of the middle fin is shaped while the lower part of the middle fin is covered by the STI layer and remains unchanged. Wann states that "[t]he bottom portions of all three fins are substantially the same, because the bottom portions are not shaped." EX1007, ¶[0035]. As I discussed above in Section VIII.C.2.b, Wann's selective fin-shaping process applies to Wann's five-fin FinFET embodiment. Accordingly, after Wann's selective fin-shaping, a POSA would have understood distances between regular fins and shaped fins remain unchanged.



EX1007, FIG. 6B.

207. Based on the above teachings of Wann's five-fin FinFET embodiment and Lin's mandrel/spacer process, the Wann-Lin five-fin FinFET structure shown above in Illustration 11 renders obvious that **third distance P5** (red) between adjacent lower parts of the **two adjacent regular fins** (red) is the same as **fourth distance P6** (blue) between adjacent lower parts of the **two adjacent shaped fins** (blue), because the bottom portions of the **two adjacent regular fins** (red) and the **two adjacent shaped fins** (blue) were made at a uniform distance apart before

shaping, as described in Lin's mandrel/spacer process, and the bottom portions of the fins are substantially unchanged throughout Wann's fin-shaping process.

208. Thus, in view of the above, the Wann-Lin five-fin FinFET structure renders obvious limitation [1.c].

e) [1.d]: and wherein the adjacent top corners are directly opposite each other.

209. The Wann-Lin five-fin FinFET structure renders a fin-shaped structure where the adjacent top corners are directly opposite each other. Since there are two "*adjacent top corners*" recited in limitation [1.b], the "*adjacent top corners*" in limitation [1.d] refers to "*adjacent top corners of the first fin and the second fin*" and/or to the "*adjacent top corners of the third fin and the fourth fin*" recited in limitation [1.b].

210. Referring to the Wann-Lin five-fin FinFET structure in Illustration 10 below, the top corners of the **two regular fins** (red) are directly opposite each other and thus adjacent, and the top corners of the **two shaped fins** (blue) are directly opposite each other and thus adjacent; therefore, the Wann-Lin five-fin FinFET structure teaches limitation [1.d]. These are the same top corners referred to above when addressing the measurement of **distance P1** (red) between adjacent top corners of the **two regular fins** (red) and **distance P3** (blue) between adjacent top corners of the **two shaped fins** (blue).

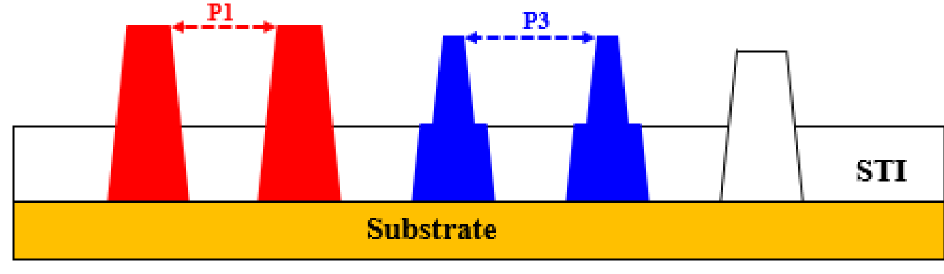


Illustration 10.

211. Thus, in view of the above, the Wann-Lin five-fin FinFET structure renders obvious limitation [1.d].

4. Dependent Claim 2: wherein the width of each top part of the first fin shaped structures is larger than the width of each top part of the second fin-shaped structures.

212. The Wann-Lin five-fin FinFET structure renders obvious that the width of each top part of the first fin shaped structures is larger than the width of each top part of the second fin-shaped structures. Referring to the Wann-Lin five-fin FinFET structure in Illustration 12 below, a **width W1** (red) of each top part of the **two regular fins** (red; "*first fin-shaped structures*) is larger than a **width W3** (blue) of each top part of **two shaped fins** (blue; "*second fin-shaped structures*").

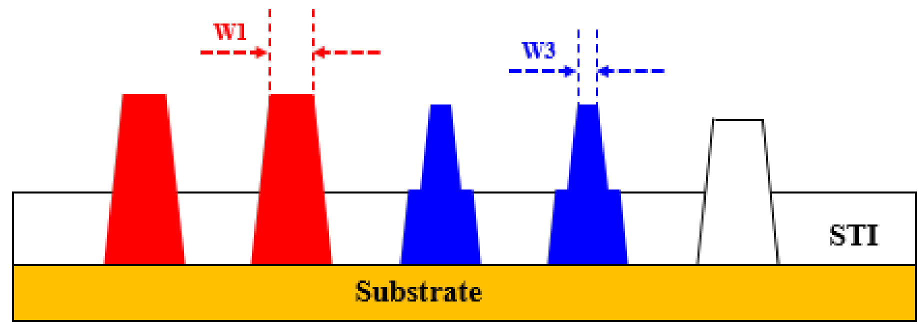
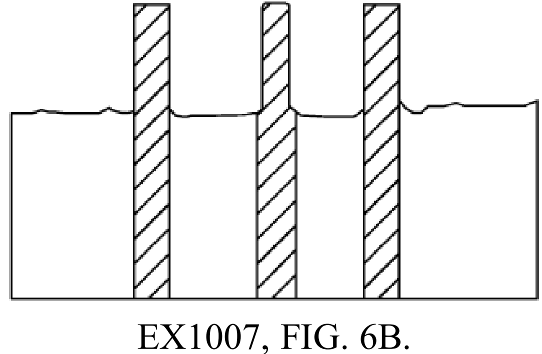


Illustration 12.

213. Referring to Wann's Figure 6B (reproduced below) where "the

FinFET also includes 3 fins, with 2 regular fins and 1 shaped fin," Wann explains that "[t]he shaped fin has a narrower top portion that may be the same, slightly shorter, or longer than the neighboring regular fins." EX1007, ¶[0035]. As I discussed above in Section VIII.C.2.b, Wann's selective fin-shaping process applies to Wann's five-fin FinFET embodiment. Similarly, in the Wann-Lin five-fin FinFET structure of Illustration 12 above, a POSA would have understood that a **width W3** (blue) of each top part of **two shaped fins** (blue) is narrower than a **width W1** (red) of each top part of the **two regular fins** (red).



EX1007, FIG. 6B.

214. Thus, in view of the above, the Wann-Lin five-fin FinFET structure renders obvious claim 2.

5. Dependent Claim 3

a) [3.a]: an isolation structure disposed beside the first fin-shaped structures and beside the second fin-shaped structures respectively,

215. The Wann-Lin five-fin FinFET structure renders obvious an isolation structure disposed beside the first fin-shaped structures and beside the second fin-

shaped structures respectively. Referring to the Wann-Lin five-fin FinFET structure in Illustration 9 below, an STI layer ("*an isolation structure*") is disposed beside the **two adjacent regular fins** ("*first fin-shaped structures*") and beside the **two adjacent shaped fins** ("*second fin-shaped structures*") respectively.

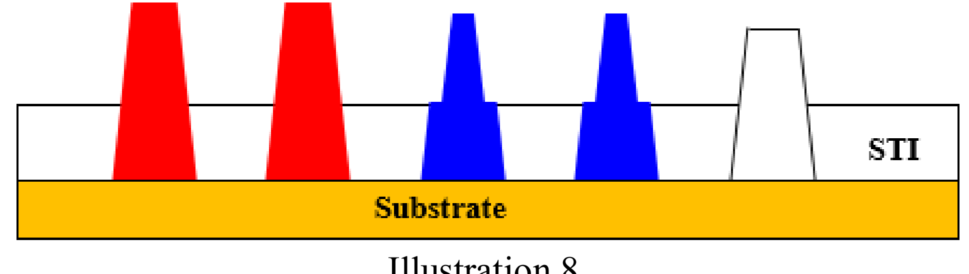
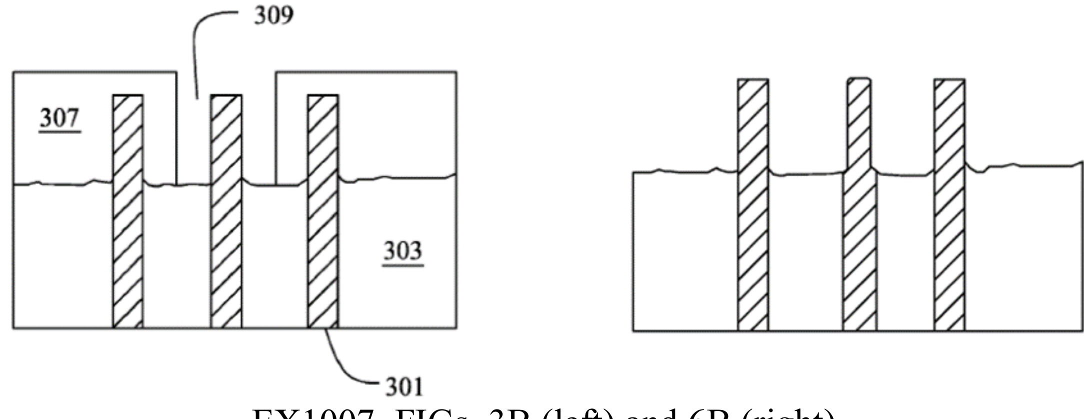


Illustration 8.

216. At the beginning of its fin-shaping process, as shown in Wann's Figure 3B (reproduced below), Wann states that "fins partially embedded in shallow trench isolation (STI) layers are formed on a semiconductor substrate." EX1007, ¶[0020]. While one or more top portions of the fins may be exposed to Wann's fin-shaping process, bottom portions of the fins remain embedded in the STI layer. EX1007, ¶[0035]. Referring to Wann's Figure 6B (reproduced below), Wann states that "[t]he bottom portions of all three fins are substantially the same, because the bottom portions are not shaped." EX1007, ¶[0035]. As I discussed above in Section VIII.C.2.b, Wann's selective fin-shaping process applies to Wann's five-fin FinFET embodiment. Similarly, in the Wann-Lin five-fin FinFET structure in Illustration 8 above, A POSA would have understood that the STI layer is disposed beside the **two adjacent regular fins** (red) and beside the **two**

adjacent shaped fins (blue), respectively.

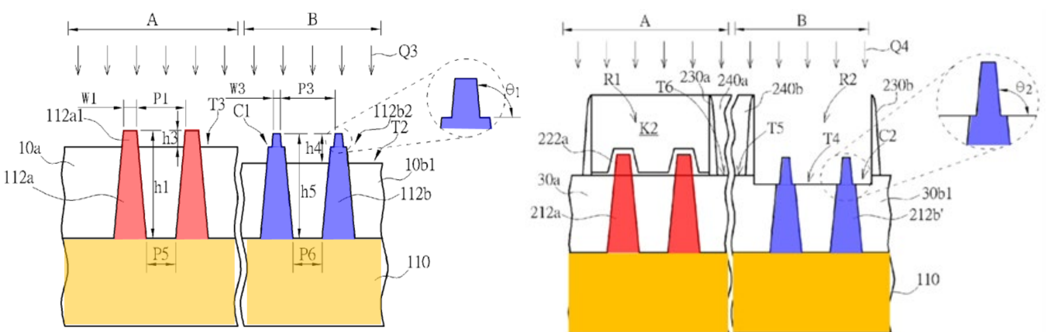


EX1007, FIGs. 3B (left) and 6B (right).

217. Thus, in view of the above, the Wann-Lin five-fin FinFET structure renders obvious limitation [3.a].

b) [3.b]: and ladder-shaped cross-sectional profile parts of the second fin-shaped structures are higher than a top surface of the isolation structure.

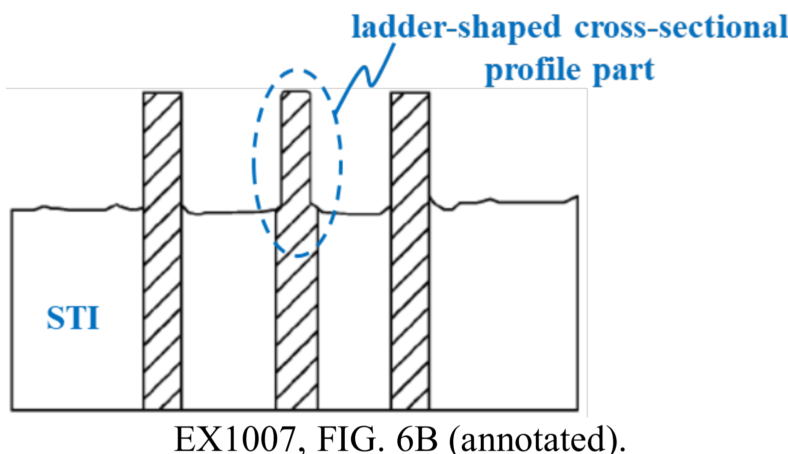
218. The Wann-Lin five-fin FinFET structure renders obvious that ladder-shaped cross-sectional profile parts of the second fin-shaped structures are higher than a top surface of the isolation structure. Figures 5 and 8 of the '510 patent (reproduced below with annotations) show examples of ladder-shaped cross-sectional profile parts of **second fin-shaped structures 112b/212b'** (blue; shown in dashed line inset). The '510 patent describes these structures as having a bending angle θ1 in Figure 5 and a bending angle θ2 in Figure 8 preferably larger than or equal to 90°. EX1001, 5:13-18, 7:14-21. It is my opinion that the Wann-Lin five-fin FinFET structure teaches this ladder shaped cross-sectional profile part.



EX1001, FIG. 5 (left; annotated) and 8 (right; annotated).

219. In Wann's selective fin-shaping process, referring to Wann's Figure 6B (reproduced below), Wann states that "while the shaped fin may be shorter than the regular fins, the top portion of the shaped fin may be the same length or longer than the top portion of regular fins because the STI layer is also etched and more of the top portion of the shaped fin may be exposed." EX1007, ¶[0035]. Wann discloses that the STI layer is also etched when the exposed fin is etched during the selective fin-shaping process: "the STI layer is also etched and more of the top portion of the shaped fin may be exposed." EX1007, ¶[0035]. Additionally, Wann discloses that the outer layer of the exposed fin is removed by "[a]ppropriate isotropic etching methods includ[ing] dry etching methods using plasma or wet etching methods," where the outer layer of the exposed fin can be etched at the same rate. Considering the loading effect of the etching process where corners are etched at a slower rate, a POSA would have understood that its bending angle can be at least 90°. Accordingly, though not explicitly shown in Wann's Figure 6B, a ladder-shaped cross-sectional profile part of the shaped fins is formed above the

STI layer and having a bending angle at least 90°—similar to the ladder-shaped cross-sectional profile parts of the second fin-shaped structures in Figure 5 of the ’510 patent above (blue; see inset in dashed circle).



EX1007, FIG. 6B (annotated).

220. Referring to the Wann-Lin five-fin FinFET structure in Illustration 13 below, ladder-shaped cross-sectional profile parts of the **two adjacent shaped fins** (“*second fin-shaped structures*”) are higher than a top surface of the STI layer (“*isolation structure*”). Wann explains that, during its fin-shaping process, “the STI layer is also etched and more of the top portion of the shaped fin may be exposed.” EX1007, ¶[0035].

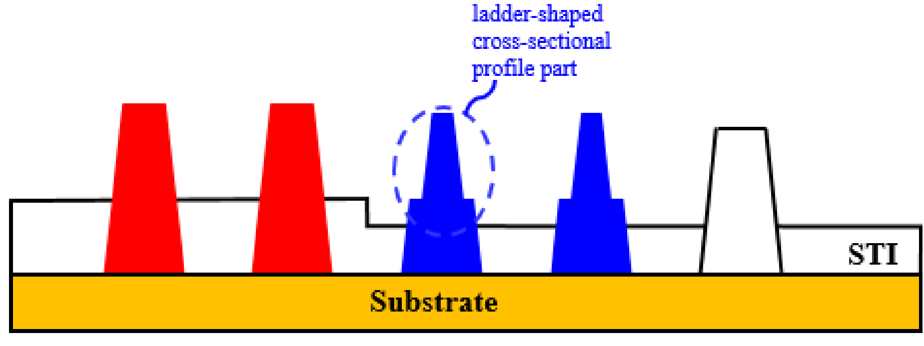


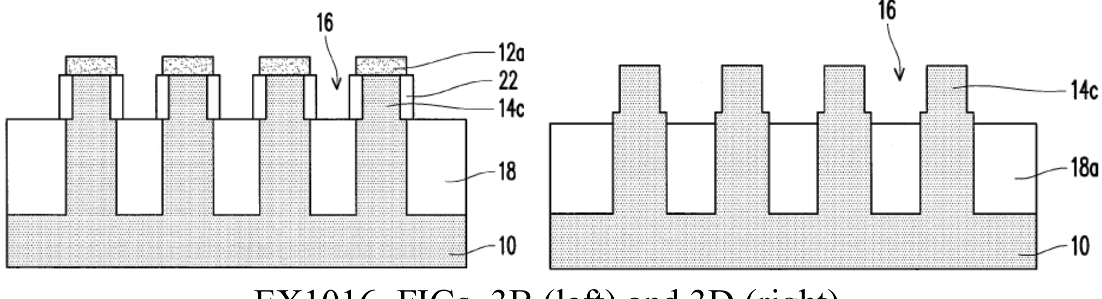
Illustration 13.

221. To the extent that an argument is made that Wann does not explicitly disclose limitation [3.b], in my opinion, a POSA would have understood that the height of the STI layer surrounding the shaped fin can vary for circuit design flexibility, based on a desired effective channel width. EX1007, ¶[0036]. Wann explains that, to achieve the desired effective channel width, "[t]he various etching methods discussed herein can shape the exposed fin a number of ways to create a profile that reduces the fin height and/or width." EX1007, ¶[0036]. For example, referring to Wann's Figure 6B (reproduced above with annotations), the STI layer around the shaped fin can be further etched to decrease the height of the STI layer surrounding the shaped fin such that the ladder-shaped cross-sectional profile part is higher than a top surface of the STI layer. Wann discloses that "the STI layer is also etched and more of the top portion of the shaped fin may be exposed." EX1007, ¶[0035].

222. Therefore, during the etching process, the ladder-shaped cross-sectional profile part maintains its shape because the etching process can be selective and remove outer layer 403 and the STI layer surrounding the shaped fin. EX1007, ¶[0035]. After the etching process, the STI layer surrounding the shaped fin can be removed to a level below the ladder-shaped cross-sectional profile part. Wann recognizes that "[t]he change in profile then allows a FinFET to have an effective channel width that is not an integer multiple of a regular fin." EX1007,

¶[0036].

223. Additionally, it was well known to form shaped fins with ladder-shaped cross-sectional profile parts higher than a top surface of an isolation structure. For example, as I discussed in Section VI.C above, Tung discloses a shaped fin with a ladder-shaped cross-sectional profile part higher than a top surface of an STI layer. As shown in Tung's Figure 3B (reproduced below), an oxide layer 22 is formed on sidewalls of fin 14c: "an oxidation process … oxidizes the sidewall of the upper portion of each fin 14 exposed by the hard mask layer 12a and the two neighboring two insulating layers 18 to form an oxide 22." EX1016, ¶[0041]. To form the ladder-shaped cross-sectional profile parts, Tung further discloses that "a portion of the insulating layers 18 are removed during the step of removing the oxides 22." EX1016, ¶[0041]. As shown in Tung's Figure 3D (reproduced below), the ladder-shaped cross-sectional profile parts of the shaped fins are higher than a top surface of insulating layer 18a.



EX1016, FIGs. 3B (left) and 3D (right).

224. Wann's teachings above are also applicable to the Wann-Lin five-fin

FinFET structure, where the heights of the STI layer surrounding the **two adjacent regular fins** (red) and the **two adjacent shaped fins** (blue) can vary based on a desired effective channel width, as shown above in Illustration 13. Accordingly, a POSA would have understood that the ladder-shaped cross-sectional profile parts of the **two adjacent shaped fins** (blue) in the Wann-Lin five-fin FinFET structure can be higher than a top surface of the STI layer.

225. Thus, in view of the above, the Wann-Lin five-fin FinFET structure renders obvious limitation [3.b].

6. Dependent Claim 4: wherein a top surface of the isolation structure of a first area is higher a top surface of the isolation structure of a second area.

226. The Wann-Lin five-fin FinFET structure renders obvious that a top surface of the isolation structure of a first area is higher a top surface of the isolation structure of a second area. Referring to the Wann-Lin five-fin FinFET structure in Illustration 13 below, a top surface of the STI layer surrounding the **two adjacent regular fins** (red; "*the isolation structure of a first area*") is higher than a top surface of the STI layer surrounding the **two adjacent shaped fins** (blue; "*the isolation structure of a second area*").

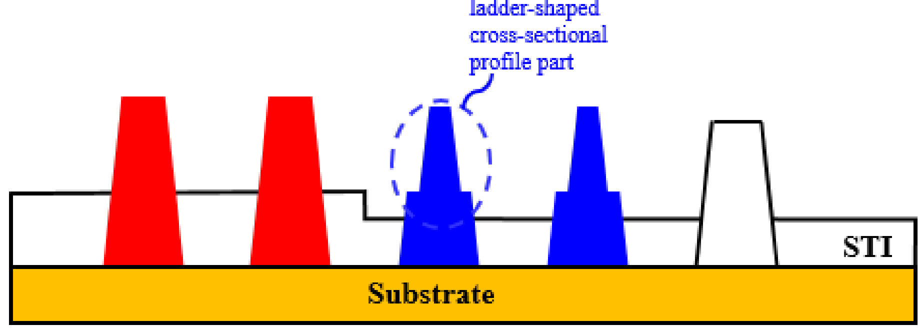
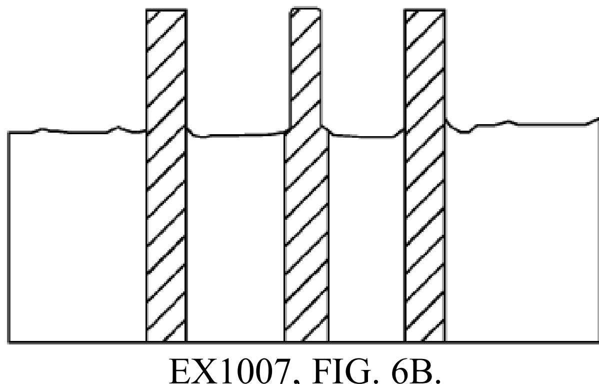


Illustration 13.

227. As I discussed in Section VIII.C.4 above with respect to dependent claim 3 from which claim 4 depends, the exposed fin and the STI layer are both etched during Wann's selective fin-shaping process. Though not explicitly shown in Wann's Figure 6B below, Wann recognizes that "while the shaped fin may be shorter than the regular fins, the top portion of the shaped fin may be the same length or longer than the top portion of regular fins because the STI layer is also etched and more of the top portion of the shaped fin may be exposed." EX1007, ¶[0035].



EX1007, FIG. 6B.

228. Thus, referring to the Wann-Lin five-fin FinFET structure in Illustration 13 above, a POSA would have understood that the top surface of the

STI layer surrounding the **two adjacent regular fins** (red) is higher than a top surface of the STI layer surrounding the **two adjacent shaped fins** (blue) because the STI layer surrounding the **two adjacent shaped fins** (blue) is also etched during Wann's fin-shaping process.

229. Thus, in view of the above, the Wann-Lin five-fin FinFET structure renders obvious claim 4.

7. Dependent Claim 5: wherein a height of the first fin-shaped structures protruding from the isolation structure is lower than a height of the second fin-shaped structures protruding from the isolation structure.

230. The Wann-Lin five-fin FinFET structure renders obvious that a height of the first fin-shaped structures protruding from the isolation structure is lower than a height of the second fin-shaped structures protruding from the isolation structure. I note that "*the* isolation structure" recited in claim 5 is not supported by independent claim 1 (from which claim 5 depends from) because independent claim 1 does not recite this term. For the purposes of my analysis in this proceeding, I assume "*the* isolation structure" recited in claim 5 is "*an* isolation structure." Referring to the Wann-Lin five-fin FinFET structure in Illustration 14 below, a **height h3 of the two regular fins** (red; "*a height of the first fin-shaped structures*") protruding from the STI layer ("*the isolation structure*") is lower than a **height h4 of the two shaped fins** (blue; "*a height of the second fin-shaped*

structures") protruding from the STI layer ("*the isolation structure*").

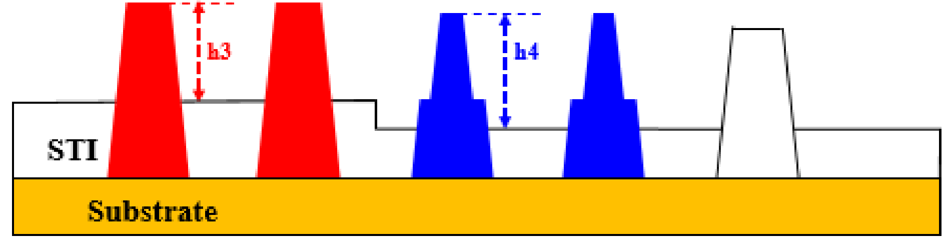
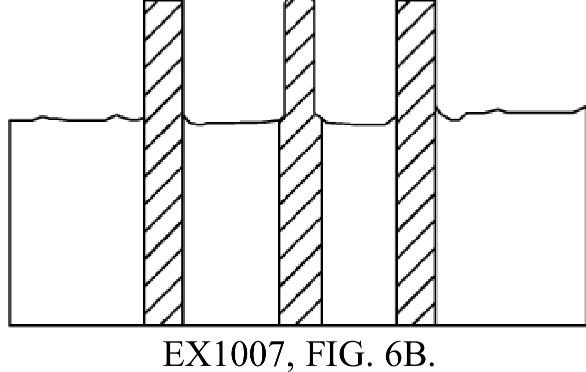


Illustration 14.

231. As I discussed in Section VIII.C.5 above, the STI layer is also etched during Wann's selective fin-shaping process. Though not explicitly shown in Wann's Figure 6B below, Wann recognizes that "while the shaped fin may be shorter than the regular fins, the top portion of the shaped fin may be the same length or longer than the top portion of regular fins because the STI layer is also etched and more of the top portion of the shaped fin may be exposed." EX1007, ¶[0035]. The etching of the STI layer will lower the top surface of the STI layer, thus increasing the height the shaped fin above the top surface of the STI layer. As a result, the top portion of the shaped fin can be longer than the top portion of regular fins, as explained in Wann. EX1007, ¶[0035].



EX1007, FIG. 6B.

232. Thus, referring to the Wann-Lin five-fin FinFET structure in Illustration 14 above, a POSA would have understood that **height h4 of the two shaped fins** (blue) protruding from the STI layer is higher than **height h3 of the two regular fins** (red) protruding from the STI layer because the STI layer surrounding the **two shaped fins** (blue) is etched during Wann's selective fin-shaping process, as I discussed above. In other words, **a height h3 of the two adjacent regular fins** ("*the first fin-shaped structures*") protruding from the STI layer ("*the isolation structure*") is lower than **a height h4 of the two adjacent shaped fins** ("*the second fin-shaped structures*") protruding from the STI layer ("*the isolation structure*").

233. Thus, in view of the above, the Wann-Lin five-fin FinFET structure renders obvious claim 5.

8. Dependent Claim 6: wherein a height of the first fin-shaped structures protruding from the substrate is higher than a height of the second fin-shaped structures protruding from the substrate.

234. The Wann-Lin five-fin FinFET structure renders obvious that a height of the first fin-shaped structures protruding from the substrate is higher than a height of the second fin-shaped structures protruding from the substrate. Referring to the Wann-Lin five-fin FinFET structure in Illustration 15 below, a **height h1 of the two regular fins** (red; "*first fin-shaped structures*") protruding from the

substrate (orange) is higher than a **height h5 of the two shaped fins** (blue; "*second fin-shaped structures*") protruding from the **substrate** (orange).

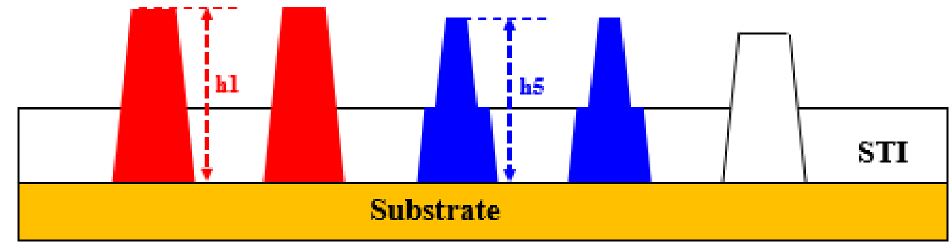
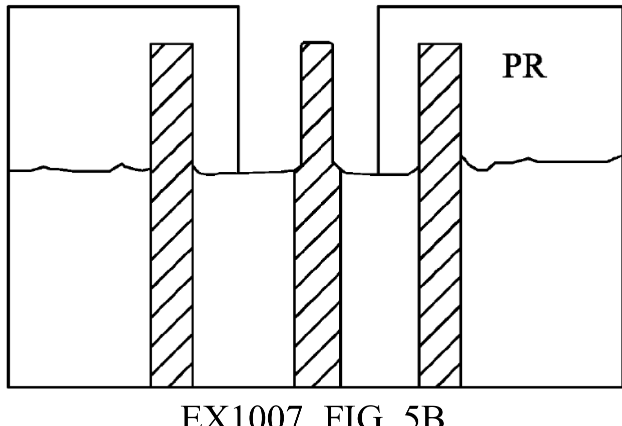


Illustration 15.

235. As I discussed in Section VIII.C.5 above, the exposed fin and the STI layer are both etched during Wann's selective fin-shaping process. Wann states that "while the shaped fin may be shorter than the regular fins, the top portion of the shaped fin may be the same length or longer than the top portion of regular fins because the STI layer is also etched and more of the top portion of the shaped fin may be exposed." EX1007, ¶[0035]. Further, with regard to Figure 5B below, Wann states "the exposed single fin is thinner and somewhat shorter than neighboring fins that are protected under the photoresist." EX1007, ¶[0029].



EX1007, FIG. 5B.

236. Thus, referring to the Wann-Lin five-fin FinFET structure in Illustration 15 above, a POSA would have understood that **height h5 of the two shaped fins** (blue) protruding from the substrate is lower than **height h1 of the two regular fins** (red) protruding from the substrate.

237. Thus, in view of the above, the Wann-Lin five-fin FinFET structure renders obvious claim 6.

IX. CLAIMS APPENDIX

1. **[1.P]** A fin-shaped structure, comprising:

[1.a] a substrate having a plurality of first fin-shaped structures and a plurality [of] second fin-shaped structures, and the first fin-shaped structures comprising a first fin and a second fin, the second fin-shaped structures comprising a third fin and a fourth fin,

[1.b] wherein a first distance between adjacent top corners of the first fin and the second fin of the first fin-shaped structures is less than a second distance between adjacent top corners of the third fin and the fourth fin of the second fin-shaped structures

[1.c] while a third distance between adjacent lower parts of the first fin and the second fin is the same as a fourth distance between adjacent lower parts of the third fin and the fourth fin;

[1.d] and wherein the adjacent top corners are directly opposite each other.

2. The fin-shaped structure according to claim 1, wherein the width of each top part of the first fin-shaped structures is larger than the width of each top part of the second fin-shaped structures.

3. The fin-shaped structure according to claim 1, further comprising:

[3.a] an isolation structure disposed beside the first fin-shaped structures and beside the second fin-shaped structures respectively,

[3.b] and ladder-shaped cross-sectional profile parts of the second fin-shaped structures are higher than a top surface of the isolation structure.

4. The fin-shaped structure according to claim 3, wherein a top surface of the isolation structure of a first area is higher a top surface of the isolation structure of a second area.

5. The fin-shaped structure according to claim 1, wherein a height of the first fin-shaped structures protruding from the isolation structure is lower than a height of the second fin-shaped structures protruding from the isolation structure.

6. The fin-shaped structure according to claim 1, wherein a height of the first fin-shaped structures protruding from the substrate is higher than a height of the second fin-shaped structures protruding from the substrate.

X. CONCLUSION

239. In signing this declaration, I recognize that the declaration will be filed as evidence in an *inter partes* review before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required, I will appear for cross-examination within the United States during the time allotted.

240. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on this 28th day of August 2025, in Lafayette, California.

Sayeef Salahuddin

Sayeef Salahuddin, Ph.D.