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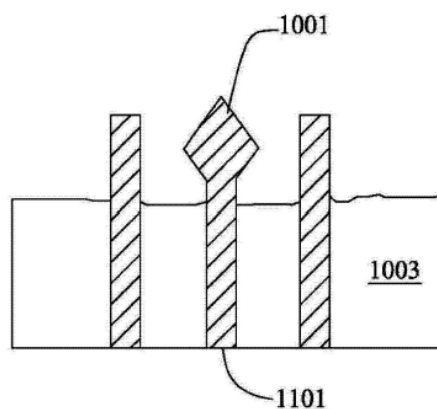
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(54) Title of the Invention

SELECTIVE FIN-SHAPING PROCESS USING PLASMA  
DOPING AND ETCHING FOR THREE-DIMENSIONAL  
TRANSISTOR APPLICATIONS

(57) Abstract

A semiconductor apparatus includes a fin field-effect transistor (FinFET) having shaped fins and regular fins. Top portions of the shaped fins may be smaller than, larger than, thinner than, or shorter than top portions of the regular fins. Bottom portions of the shaped fins are the same as bottom portions of the regular fins. The FinFET may have only one or more shaped fins, one or more regular fins, or a mixture of shaped fins and regular fins. A semiconductor manufacturing process for shaping one fin includes: forming a photolithographic opening in the one fin, optionally doping a portion of the fin, and etching a portion of the fin. The present invention further provides a selective fin-forming process using plasma doping and etching for three-dimensional transistor applications.



# SELECTIVE FIN-SHAPING PROCESS USING PLASMA DOPING AND ETCHING FOR THREE-DIMENSIONAL TRANSISTOR APPLICATIONS

## TECHNICAL FIELD

[0001] The present invention relates generally to integrated circuit devices, and more specifically to structures and methods for forming fin field-effect transistors (FinFETs).

## BACKGROUND ART

[0002] In the rapidly advancing semiconductor manufacturing industry, complementary metal oxide semiconductor (CMOS) FinFET devices may be used in many logic and other applications and are integrated into various different types of semiconductor devices. FinFET devices typically include semiconductor fins with high aspect ratios in which channels and source/drain regions for transistors are formed. Gates are formed along and on the sides of a portion of the semiconductor fins. The increased surface area of the channels and source/drain regions in the FinFET devices results in faster, more reliable and better-controlled semiconductor transistor devices.

[0003] New advanced designs are created with FinFET structures at the outset with computer-aided design (CAD) layers that define the boundary of each FinFET. As manufacturing process progresses into smaller and smaller technology nodes, devices originally designed in a larger technology node may benefit from manufacturing in a smaller technology node in ways such as increased performance and efficiencies and decreased die size. Similarly, devices that originally used planar transistor designs can also benefit from manufacturing them using FinFET devices. However, because different design rules apply to planar structure layouts and FinFET device layouts, manually converting portions of the device from a planar layout to a FinFET device layout is a highly resource-intensive process, and may be no different from creating a new design. For products already manufactured using planar transistors, a conversion method needs to be sought to form a FinFET device that is at least electrically equivalent to a planar transistor. Therefore, it is necessary to continue to seek an improved method for automatically converting an older planar structure layout to a FinFET structure layout.

## SUMMARY OF THE INVENTION

[0004] To address the problems existing in the prior art, according to one aspect of the present invention, there is provided an apparatus, comprising: a semiconductor substrate; and a plurality of fin field-effect transistors (FinFETs) located on the substrate, the FinFET having at least one fin; wherein at least one of the plurality of FinFETs comprises at least one shaped fin.

[0005] In the apparatus, the at least one shaped fin is smaller than other fins of the same FinFET.

[0006] In the apparatus, the at least one shaped fin is two or more fins arranged to be not adjacent to one another.

[0007] In the apparatus, a portion of the at least one shaped fin is thinner than other fins of the same FinFET.

[0008] In the apparatus, the at least one shaped fin is larger than other fins of the same FinFET.

[0009] In the apparatus, a portion of the at least one of the plurality of FinFETs is a single-fin FinFET.

[0010] In the apparatus, a portion of the at least one of the plurality of FinFETs comprises at least one shaped fin of a first shape, and another portion of the at least one of the plurality of FinFETs comprises at least one shaped fin of a second shape, wherein the first shape is different from the second shape.

[0011] In the apparatus, the at least one shaped fin has an inclined sidewall.

[0012] According to another aspect of the present invention, there is provided a fin field-effect transistor (FinFET), comprising: a semiconductor substrate; a plurality of fins located on the substrate, comprising one or more regular fins and one or more shaped fins, wherein the regular fins and the shaped fins have different top portion shapes; and an oxide layer located on the semiconductor substrate, embedding bottom portions of the plurality of fins, wherein the embedded bottom portions of the plurality of fins have substantially the same shape.

[0013] In the transistor, the one or more shaped fins comprise at least one shaped fin of a first shape and at least one shaped fin of a second shape.

[0014] In the transistor, the one or more shaped fins are smaller than the one or more regular fins.

[0015] In the transistor, the one or more shaped fins are larger than the one or more regular fins.

[0016] In the transistor, each of the one or more shaped fins is adjacent only to the one or more regular fins, so that the spacing between adjacent fins in the transistor is the same.

[0017] In the transistor, the plurality of fins and the semiconductor substrate are made of a same material.

[0018] According to still another aspect of the present invention, there is provided a method for forming a fin field-effect transistor (FinFET), the method comprising: forming a plurality of fins partially embedded in a shallow trench isolation (STI) layer on a semiconductor substrate; patterning a photoresist layer over the plurality of fins to form one or more openings to expose a single fin; and shaping the exposed single fin.

[0019] In the method, shaping the exposed single fin comprises: doping a portion of the exposed single fin with a dopant, and removing the doped portion of the exposed single fin.

[0020] In the method, shaping the exposed single fin comprises: etching a portion of the exposed single fin.

[0021] In the method, the removal step comprises etching.

[0022] According to still another aspect of the present invention, there is provided a method for forming a fin field-effect transistor (FinFET), the method comprising: forming a plurality of fins partially embedded in a shallow trench isolation (STI) layer on a semiconductor substrate; depositing a dielectric layer over the STI layer to completely cover the plurality of fins; patterning a photoresist layer over the dielectric layer to form one or more openings over a single fin; etching through the dielectric layer to expose the single fin; removing the photoresist layer; and shaping the exposed single fin.

[0023] In the method, shaping the exposed single fin comprises: epitaxially growing a fin material.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0024] Features of the present invention can be best understood from the following detailed description when read with reference to the drawings. It should be emphasized that, in accordance with the standard practice in the industry, various components are not drawn to scale and are for illustrative purposes only. In practice, the dimensions of the various components may be arbitrarily increased or reduced for clarity of discussion.

[0025] FIG. 1 shows a fin field-effect transistor (FinFET).

[0026] FIG. 2 shows a flowchart of a method for manufacturing a FinFET device according to various embodiments of the present invention.

[0027] FIGS. 3A and 3B show partially manufactured FinFET devices according to various embodiments of the present invention.

[0028] FIGS. 4A, 5A, and 6A show embodiments of fin shortening according to the present invention.

[0029] FIGS. 4B, 5B, and 6B show embodiments of fin thinning according to the present invention.

[0030] FIGS. 7, 8, and 10 show fin forming processes according to various embodiments of the present invention.

[0031] FIGS. 9A and 9B show fin shaping processes according to various embodiments of the present invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0032] The making and using of illustrative embodiments will be discussed in detail below. However, it should be understood that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. Specific examples of elements and arrangements will be described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first component on a second component in the following description may include embodiments in which the first component and the second component are formed in direct contact, and may also include embodiments in which an additional component is formed between the first component and the second component so that the first component and the second component are not be in direct contact. Certainly, the description may specifically state whether the components are directly in contact with each other. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. The specific embodiments discussed are merely illustrative and do not limit the scope of the present invention.

[0033] FinFET devices use a substantially rectangular fin structure formed generally in one of two ways. In one method, a shallow trench isolation (STI) component 105 is formed first on a bulk

silicon material, e.g., a substrate 101 shown in FIG. 1. Bulk silicon is exposed at the bottoms of trenches between the STI components. Silicon is then grown in the trenches to form fins 103 by using, for example, an epitaxial process. Once a desired fin height is reached, then the STI 105 is etched to a level below the top of the fin to expose a portion of the fin. The exposed portion of the fin is a top portion 107 and the embedded portion is a bottom portion 109. The bulk silicon material 101 may be a silicon substrate or a deposited silicon such as silicon-on-insulator (SOI) with a barrier oxide (BOX) layer between the SOI and the underlying silicon substrate. Using this method, the STI components define the size and shape of the fins. According to etching parameters used when the trenches are formed, the fins may have a variety of substantially rectangular shapes, including the slight angle at the bottom portion of the fin as shown in FIG. 1.

[0034] In another method, bulk silicon on a substrate is etched into a rectangular fin shape by first patterning and depositing a hardmask layer on the bulk silicon. The hardmask forms a pattern covering the tops of the fins. The bulk silicon is then etched to form trenches between the regions covered by the hardmask layer. The trenches are formed into shallow trench isolation (STI) components 105 by depositing a dielectric material (which is usually silicon oxide). The dielectric material is usually deposited in excess to completely cover the fins 103 and optionally the hardmask layer (if not yet removed). The dielectric material is planarized down to the top surface of the fin/hardmask, and then etched to a level below the top of the fin so that a portion of the fin protrudes above the STI. The protruded fin portion is a top portion 107 and the embedded fin portion is a bottom portion 109.

[0035] In a variation of the second method, the hardmask for etching the bulk silicon is formed by a process using mandrels. A photoresist pattern is formed and used to etch a mandrel pattern. A conformal spacer material is then deposited around the mandrel. The conformal spacer is usually formed of a hardmask, wherein a spacer sidewall formed by the hardmask is thinner than that of the mandrel. The mandrel material between the spacers is then removed in a subsequent etching operation to leave just the spacers behind. Some of the spacers are then used as a hardmask for etching the underlying silicon layers, thereby forming fin structures. Fins formed by using the mandrel/spacer method can be closer to each other and thinner than fins formed by using the first method or the unmodified second method. The exposed fin portion 107 has a height dimension (h), a width dimension (w) and a length dimension (l). Some electrical properties of the FinFET device can be defined according to these dimensions. For example, an effective channel width of

the transistor may be calculated using the dimensions of the fins under the gate. As shown in FIG. 1, the effective channel width is 2 fins, or  $2 \times (2h + w)$ . Note that the effective channel width does not include the distance between fins. These fins are referred to herein as regular fins because they all have the same height and width dimensions.

[0036] The remaining FinFET device forming process steps are described here to provide the context for the present invention. A gate dielectric layer 113 and a gate electrode layer 111 are deposited over the narrowed fins and the STI layer. The gate dielectric layer 113 is formed of a high dielectric constant (high-k) insulating material. Exemplary high-k materials may have k values greater than about 4.0, or even greater than about 7.0, and may include aluminum-containing dielectrics such as  $\text{Al}_2\text{O}_3$ ,  $\text{HfAlO}$ ,  $\text{HfAlON}$ , or  $\text{AlZrO}$ ; Hf-containing materials such as  $\text{HfO}_2$ ,  $\text{HfSiO}_x$ ,  $\text{HfAlO}_x$ ,  $\text{HfZrSiO}_x$ , or  $\text{HfSiON}$ ; and/or other materials such as  $\text{LaAlO}_3$  or  $\text{ZrO}_2$ . The gate electrode layer 111 is formed on the gate dielectric layer 113, and may be formed of a conductive material such as doped polysilicon, a metal, or a metal nitride.

[0037] The gate electrode layer 111 and the gate dielectric layer 113 are then patterned to form gate stacks over a middle portion of the fins. The fin portions not under the gate stacks are then optionally doped to form lightly doped drain (LDD) and source regions. The dopant used depends on the conductivity type of the transistor. The LDD regions may be doped by ion-implanting or by plasma doping where the dopant is deposited onto the fin and annealed. The source and drain regions are formed on the gate stacks. A source and drain region may be formed by ion-implanting the source/drain region or by removing a portion of the fin and epitaxially re-growing the removed portion under doping conditions to form the source/drain region.

[0038] A circuit designer specifies transistors in his design according to electrical properties for performing various functions. Electrical properties to be considered include an on voltage (threshold voltage), breakdown voltage, on-state current ( $I_{\text{on}}$ ), leakage current, etc. The on-state current is a current driven through the transistor when the gate voltage is equal to a threshold voltage. The on-state current is proportional the channel width. When a circuit is designed using a planar transistor, the channel width may be any value by just making the transistor wider or narrower. However, for a FinFET device, the channel width cannot be just any value—the channel width is an integer multiple of the dimension for a single fin. For example, the channel width of the FinFET device may equal to 2 fins or 3 fins, but cannot be 2.5 fins. When a planar transistor-

based design is converted to a FinFET device-based design, the planar transistor cannot be converted to a FinFET device having exactly the same on-state current. While usually a range of on-state currents may be acceptable according to the circuit functionality and application, the limitation on selecting the channel width for the FinFET reduces design flexibility and the accuracy of the conversion from planar transistors to FinFET devices.

[0039] Various embodiments of the present invention relate to a selective fin-shaping process to allow control over the width and height of a single fin. By shaping one or more fins in a FinFET device, the channel width of the FinFET device may vary beyond an integer multiple of the dimension of a single fin. The selective fin shaping may enlarge one or more fins, shorten one or more fins, thin one or more fins, reduce all fin dimensions at the same time, or change the shape of one or more fins in other ways to create shaped fins in the case that other regular fins remain unchanged. For example, the equivalent of a FinFET device having 2.5 fins may be designed by reducing the dimension of one fin. Its advantages may include improved circuit design flexibility and increased FinFET process margin for designers and foundries that perform the conversion from the planar transistor-based design to the FinFET device-based design.

[0040] Referring to FIG. 2, a process flow 211 for selective fin shaping is shown. In operation 213, fins partially embedded in a shallow trench isolation (STI) layer are formed on a semiconductor substrate. As discussed herein, a number of methods may be used to form the fins. The fins may be obtained by etching bulk silicon or by epitaxial growth.

[0041] In operation 215, an optional dielectric layer is deposited over the STI layer to completely cover the fins. If the one or more fins are to be enlarged, the optional dielectric layer will be used. If the one or more fins are to be reduced, then the optional dielectric layer is not necessary. The optional dielectric layer may be a silicon oxide, silicon nitride, or another dielectric layer that is easier to etch than the underlying STI layer. In some cases, an etch stop layer may be deposited before the dielectric layer. In such case, the dielectric layer may be the same material as the STI layer. FIG. 3A shows a partially manufactured FinFET device after operation 215. The fins 301 are partially embedded in the STI layer 303. The dielectric layer 305 is deposited over the STI layer 303 and completely covers the fins 301.

[0042] Referring back to FIG. 2, in operation 217, a photoresist layer is patterned over the fins. Lithographic dimensions limit minimum dimensions that a photoresist layer can protect and a

minimum size opening that the photoresist pattern may create. The minimum opening is smaller than the minimum region to be protected. In other words, an opening may be created with a dimension of one fin pitch, but conversely, a protective region covering one fin pitch may be too small. In FIGS. 3A and 3B, a photoresist layer 307 is deposited and patterned to create an opening 309. If the dielectric layer in operation 215 is deposited, the photoresist layer is deposited over the dielectric layer as shown in FIG. 3A. If the dielectric layer in operation 215 is not deposited, then the photoresist layer is deposited directly over the STI layer and the fins as shown in FIG. 3B.

[0043] Referring back to FIG. 2, in optional (broken line) operation 227, the exposed single fin is doped with a dopant. According to a portion to be doped, several doping processes may be used. In one embodiment, a small vertical portion at the topmost portion of the fin may be doped by using an ion implant process. Dopant ions are directed at the opening, but because of the aspect ratio of the opening, all the top portion of the fin is substantially doped, shown as the fin tip 401 in FIG. 4A. The dopant may be oxygen to form a silicon oxide fin tip. The dopant may be nitrogen, to form a silicon nitride tip. Other dopants that effectively change the chemical property of the fin tip 401 so that it can be easily removed in a subsequent etching procedure may also be used.

[0044] In other embodiments, a conformal plasma doping process may be used to convert an outer layer 403 of the fin to a different material, as shown in FIG. 4B. Plasma may be generated in situ or remotely. For example, oxygen plasma may be used to oxidize the outer layer portion of the fin. Plasmas including other dopants may also be used to effectively change the chemical property of the outer layer 403 of the fin so that the outer layer 403 can be easily removed in a subsequent etching procedure.

[0045] Referring back to FIG. 2, in operation 229, a portion of the exposed single fin is etched and removed. The removed portion may be a portion doped in operation 227. According to the type of doping processes and the etch selectivities of various materials, several etching processes may be used.

[0046] In some embodiments, the portion to be removed is substantially located at the tip of the fin. These embodiments may be used to shorten one or more of the fins in the FinFET device, but the width of the fins cannot be changed at all. Various types of plasma etching may be used to remove the doped portion from the fin tip. In one example of FIG. 4A where the portion to be removed is located at the fin tip, biased plasma may be used to remove the material at the fin tip.

According to the material to be removed, plasma may include active ions such as hydrogen and fluorine, for example, fluorocarbon plasma. Plasma may also optionally or additionally include relative inert species such as nitrogen, argon, krypton, or xenon. For example, if the fin tip is silicon oxide, anisotropic plasma etching may include a fluorine-based etchant. Note that the plasma etchant should have an etching preference for silicon oxide at the fin tip relative to silicon oxide in the underlying STI layer and for silicon in the fin, so as not to remove much of the STI layer and shape the fin in an undesirable way. Incidental etching of the STI layer may be minimized by biasing at a low power toward the substrate, by directing plasma toward the substrate at an angle so that plasma at most of incident angles is blocked, and also by selecting the dopant and the STI material to have different etch selectivities.

[0047] In another example, the fin tip may be silicon nitride if the dopant is nitrogen. Plasma etching of silicon nitride with relative high etch selectivity of silicon nitride over silicon oxide may include some fluorine-based plasma along with methane, nitrogen, and oxygen additive gas flows. One skilled in the art can adjust the gas mixture so that little or no STI layer is removed relative to silicon nitride at the fin tip. After the doped fin tip is etched away, the resulting structure may be that of FIG. 5A, where the exposed single fin is shorter than adjacent fins that are protected.

[0048] The doped fin tip may also be removed by a wet etching method. In the wet etching method, one or more substrates are bathed in an etchant container that may also be agitated to facilitate the contact of the etchant with the surface to be etched. The wet etchant generally attacks all exposed surfaces, so the wet etchant should have a relatively high etch selectivity for etching the fin tip material against other parts of the structure. For example, for the silicon oxide fin tip, the wet etchant may include hydrofluoric acid or a fluorocarbon etchant. For the silicon nitride fin tip, the wet etchant may include phosphoric acid.

[0049] In some embodiments, the portion to be removed is an outer layer of the fin as shown in FIG. 4B. Appropriate isotropic etching methods include dry etching methods using plasma or wet etching methods. For example, a silicon oxide outer layer may be removed by using buffered oxide etching or a mixture of ammonium fluoride and hydrofluoric acid in a wet etch. Plasma etching may involve non-biased plasma, including remotely generated plasma, to remove an outer layer. For example, a remotely generated SF<sub>6</sub> plasma with oxygen may be used. After the doped outer

layer portion is etched away, the resulting structure may be that of FIG. 5B, where the exposed single fin is thinner and somewhat shorter than adjacent fins that are protected by the photoresist.

[0050] In still other embodiments, a portion of the exposed single fin is etched without first doping a portion of the fin. Various etching methods may be applied directly to the silicon fin to change its shape. The various etching methods may be classified as dry etching and wet etching, isotropic etching and anisotropic etching, and different combinations resulting in different shapes.

[0051] In one example, plasma etching using various fluorine-based plasmas (such as  $\text{XeF}_2$  and  $\text{BrF}_3$ ) may be used to isotropically reshape the exposed fin. The effect would be similar to first oxidizing the fin using oxygen containing plasma and then etching the silicon oxide layer.

[0052] In another example, plasma etching using a polymerization technique allows for moderate anisotropic etching only on the tip portion of the fin. Polymer byproducts from etching deposition on the sidewalls form a protective layer. With this technique, the polymer residue must be removed in subsequent processing. Carbon-rich fluorocarbon or hydrofluorocarbon plasma may be used.

[0053] In another example, wet etching using an anisotropic etchant may shape the fin according to crystal orientation. Anisotropic wet etching that removes silicon at an orientation plane dependent rate includes using tetramethylammonium hydroxide (TMAH), potassium hydroxide (KOH) or another strong alkaline etchant ( $\text{pH} > 12$ ) to etch silicon. Because the bonding energy of silicon atoms is different for each crystal plane, these etchants therefore have high sensitivity between particular orientation planes in an etching rate limited (not diffusion limited) reaction. A TMAH wet etching forms a notch opening. The orientation dependence of KOH wet etching is similar to TMAH, but with different rates and ratios. In one example, the etchant includes TMAH and KOH with the TMAH at about 20% by weight.

[0054] In still another example, isotropic wet etching may, from all directions, uniformly remove silicon that is not protected. Isotropic silicon etching may use a combination of hydrofluoric acid (HF) with a number of additives such as nitric acid ( $\text{HNO}_3$ ), citric acid ( $\text{CH}_3\text{COOH}$ ), sodium chlorite ( $\text{NaClO}_2$ ), perchloric acid ( $\text{HClO}_4$ ), fresh potassium permanganate ( $\text{KMnO}_4$ ), or combinations of these additives. These chemical mixtures uniformly remove material, and are limited by the mass transport (diffusion limited) of chemical species to the crystal surface.

[0055] Referring back to FIG. 2, in operation 231, the photoresist layer is removed. The photoresist removal is accomplished using an ashing process known in the art. Examples of the resulting fin structure are shown in FIGS. 6A and 6B. In FIG. 6A, the FinFET device includes 3 fins, with 2 regular fins and 1 shaped fin. The shaped fin has a shorter top portion. In FIG. 6B, the FinFET device also includes 3 fins, with 2 regular fins and 1 shaped fin. The shaped fin has a narrower top portion that may be the same, slightly shorter, or longer than an adjacent regular fin. The bottom portions of all three fins are substantially the same, because the bottom portions are not shaped. Note that while the shaped fin may be shorter than the regular fins, the top portion of the shaped fin may have the same length as or be longer than the top portions of the regular fins because the STI layer is also etched and more of the top portion of the shaped fin may be exposed.

[0056] The various etching methods discussed herein can shape the exposed fin in a number of ways to form a profile that reduces the fin height and/or width. The change in profile enables the FinFET device to have an effective channel width that is not an integer multiple of a regular fin. According to the desired effective channel width, an etching method is selected to minimize processing and maximize process control.

[0057] In the embodiments where the fin width is reduced, an additional advantage is to increase the distance between adjacent fins. Increasing the distance between fins increases a process window for forming a gate. The FinFET device gate may include many layers of different materials deposited over a middle portion of the fins. Each layer increases the aspect ratio of the remaining space between the fins so that it may be difficult to fully deposit the last layer due to the lack of voids. Increasing the distance between fins decreases the initial aspect ratio so that the last deposition process window is larger.

[0058] Still referring to FIG. 2, an optional embodiment to shape the exposed single fin by enlarging the fin is shown in operations 219 to 223. In operation 219, the dielectric layer obtained from operation 215 is etched through to expose a single fin. The dielectric layer is used to protect regular fins while the exposed fin is enlarged. FIG. 7 shows the structure after the dielectric layer 705 is etched to a level below the STI layer 703, forming an opening 709 containing one single fin 701. The photoresist layer 707 is then removed in operation 221 of FIG. 2 as shown in FIG. 8. The photoresist is removed in operation 221 because the epitaxy temperature is very high, above a

temperature suitable for the photoresist material. Note that for epitaxial growth of the fin 801, the dielectric layer 805 may be a silicon oxide and in some cases silicon nitride.

[0059] In operation 223, silicon is grown on the exposed fin during an epitaxial growth process. No silicon is grown on surfaces covered by the dielectric layer 805. The photoresist is removed in operation 221 because the epitaxy temperature is very high, above a temperature suitable for the photoresist material. FIGS. 9A and 9B show different results obtained from operation 223. In FIG. 9A, single crystals are grown along the surface of the exposed fin according to crystal orientations, forming a shaped fin 901A. Various tip angles of the fin 901A depends on the crystal orientation of the fin. In some embodiments, the fin tip shape may be controlled to form a different shape, such as that of FIG. 9B. During epitaxial growth, additional gas that can etch a particular surface may be included to shape the growth. A bulb-tip shape such as that of the fin 901B may be formed by adjusting the epitaxial recipe with various hydrochloric acid gas flows.

[0060] Referring back to FIG. 2, in operation 231, the photoresist layer is removed. The photoresist removal is accomplished using an ashing process known in the art. An example of a resulting fin is shown in FIG. 10, showing the shaped fin 901A. In FIG. 10, the FinFET device includes 3 fins, with 2 regular fins and 1 shaped fin. The shaped fin has an angular face that corresponds to the crystal orientation of silicon. The effective channel width of the FinFET device of FIG. 10 is increased compared with the FinFET device having 3 regular fins.

[0061] The various embodiments of the present disclosure are discussed herein with respect to one FinFET device with 3 fins. In practice, a FinFET device may have any number of fins from 1 to several or even hundreds. The present disclosure is not limited a FinFET device having a particular number of fins. For a single-fin FinFET device, the only fin is the shaped fin. For a two-fin FinFET device, one or both of the fins may be shaped. For a three-fin FinFET device, the middle fin may be shaped. As discussed, while a single fin opening may be formed in the photoresist, only one fin may be too small for current photolithography processes with the photoresist protecting it. Therefore, for FinFET devices having more than 3 fins, the shaped fin may be spaced apart from regular fins by 2 regular fins. A four-fin FinFET device may include shaped fins at either end and two regular fins in the middle. Optionally, a plurality of fins may be shaped in the same opening. Therefore, a four-fin FinFET device may also include shaped fins in

the middle and regular fins at either end. Certainly, three fins may be shaped or three fins may be regular, or all of the fins may be shaped or may be regular.

[0062] An integrated circuit apparatus includes many transistors. The apparatus may include many FinFETs with different sizes having different number of fins. Some FinFETs may have shaped fins and some FinFETs may not. A FinFET may have multiple types of shaped fins, for example, a five-fin FinFET may have 2 regular fins, 2 fins shaped in a particular way, and 1 fin shaped in a different way. While the fin shaping process may be repeated any number of times, each time the fin-shaping process uses manufacturing resources including one photomask and one to several deposition and etching processes.

[0063] According to various embodiments, the present invention relates to an apparatus having several FinFETs on a semiconductor substrate, wherein some of the FinFETs have at least one shaped fin. The shaped fin may be smaller or larger than regular fins in the same FinFET or in other FinFETs. In some embodiments, the at least one shaped fin may be two or more fins. and are not placed adjacent to each other. In some embodiments, multiple types of shaped fins may be used in the same FinFET.

[0064] According to various embodiments, the present invention further relates to a FinFET device, including: a semiconductor substrate, several fins on the substrate including one or more regular fins and one or more shaped fins with different top portion shapes, and an oxide layer on the substrate embedding bottom portions of the fins, wherein the embedded bottom portions of the fins have substantially the same shape. While positioning effects may affect the bottom portion shapes for fins at the edge of the transistor to some extent, such variations are not significant, and the fins would have substantially the same shape if their only difference during manufacturing is the positioning of the small crown.

[0065] According to various embodiments, the present disclosure also relates to a method for forming a FinFET device, including: forming several fins partially embedded by a shallow trench isolation (STI) layer on a semiconductor substrate, patterning a photoresist layer over a plurality of fins to form one or more openings exposing a single fin, and shaping the exposed single fin.

[0066] Although the embodiments of the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the present invention as defined by

the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the processes, machines, manufacture, composition of materials, apparatuses, methods and steps described in the specification. As should be understood by those of ordinary skill in the art, with the disclosure of the present invention, processes, machines, manufacture, composition of materials, apparatuses, methods or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein, may be used according to the present invention. Therefore, the appended claims shall be included within the scope of such processes, machines, manufacture, composition of materials, apparatuses, methods or steps.

## CLAIMS

1. An apparatus, comprising:  
  
a semiconductor substrate; and  
  
a plurality of fin field-effect transistors (FinFETs) located on the substrate, the FinFET having at least one fin;  
  
wherein at least one of the plurality of FinFETs comprises at least one shaped fin.
2. The apparatus according to claim 1, wherein the at least one shaped fin is smaller than other fins of the same FinFET.
3. The apparatus according to claim 2, wherein the at least one shaped fin is two or more fins arranged to be not adjacent to one another.
4. The apparatus according to claim 1, wherein a portion of the at least one shaped fin is thinner than other fins of the same FinFET.
5. The apparatus according to claim 1, wherein the at least one shaped fin is larger than other fins of the same FinFET.
6. The apparatus according to claim 1, wherein a portion of the at least one of the plurality of FinFETs is a single-fin FinFET.
7. The apparatus according to claim 1, wherein a portion of the at least one of the plurality of FinFETs comprises at least one shaped fin of a first shape, and another portion of the at least one of the plurality of FinFETs comprises at least one shaped fin of a second shape, and wherein the first shape is different from the second shape.

8. The apparatus according to claim 1, wherein the at least one shaped fin has an inclined sidewall.

9. A fin field-effect transistor (FinFET), comprising:

a semiconductor substrate;

a plurality of fins located on the substrate, comprising one or more regular fins and one or more shaped fins, wherein the regular fins and the shaped fins have different top portion shapes; and

an oxide layer located on the semiconductor substrate, embedding bottom portions of the plurality of fins,

wherein the embedded bottom portions of the plurality of fins have substantially the same shape.

10. A method for forming a fin field-effect transistor (FinFET), the method comprising:

forming a plurality of fins partially embedded in a shallow trench isolation (STI) layer on a semiconductor substrate;

depositing a dielectric layer over the STI layer to completely cover the plurality of fins;

patterning a photoresist layer over the dielectric layer to form one or more openings over a single fin;

etching through the dielectric layer to expose the single fin;

removing the photoresist layer; and

shaping the exposed single fin.

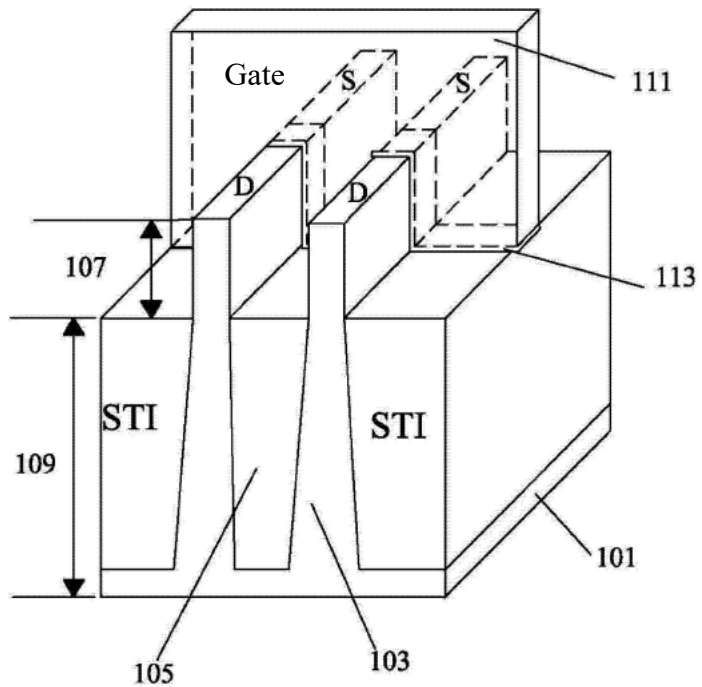


FIG. 1

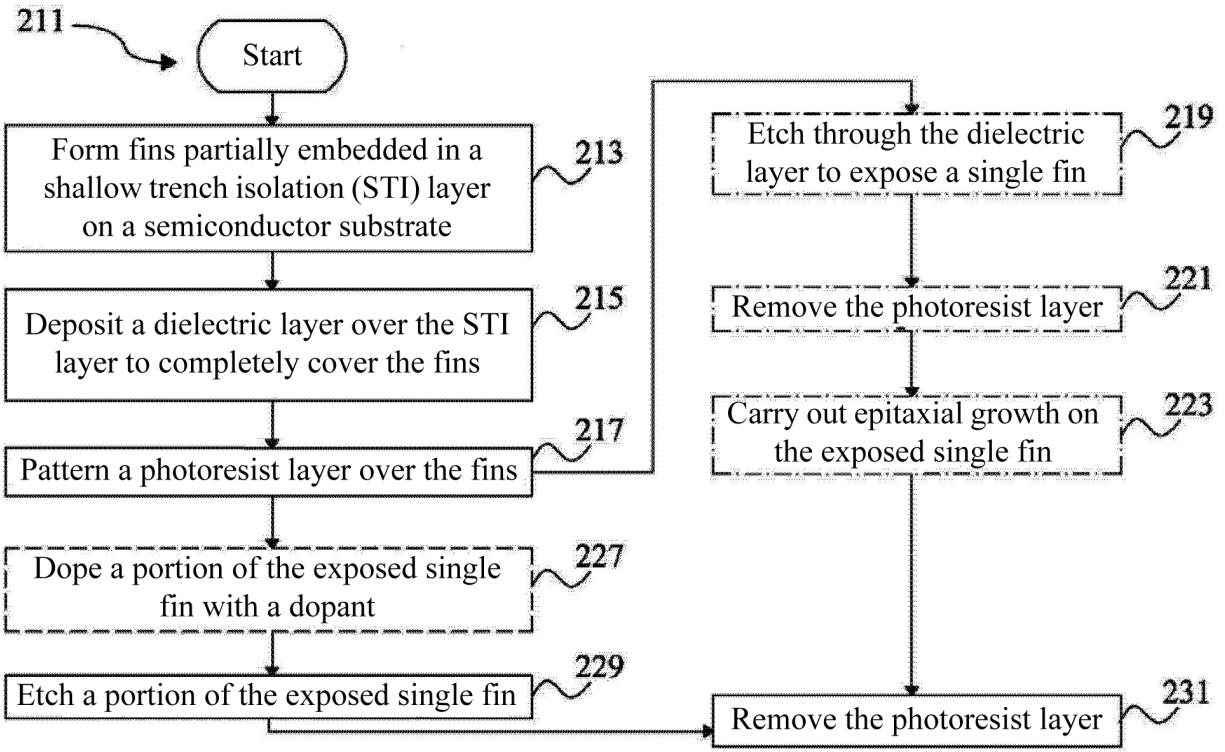


FIG. 2

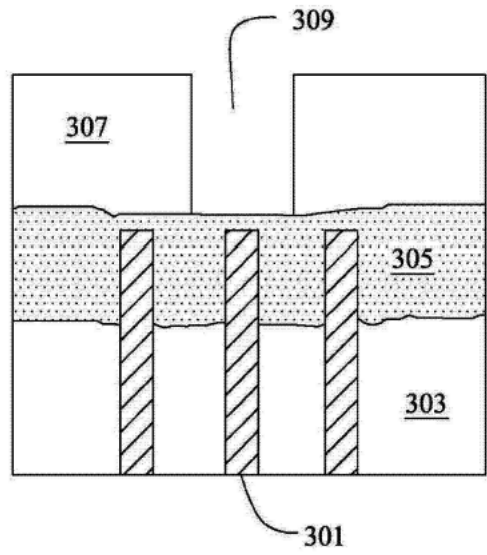


FIG. 3A

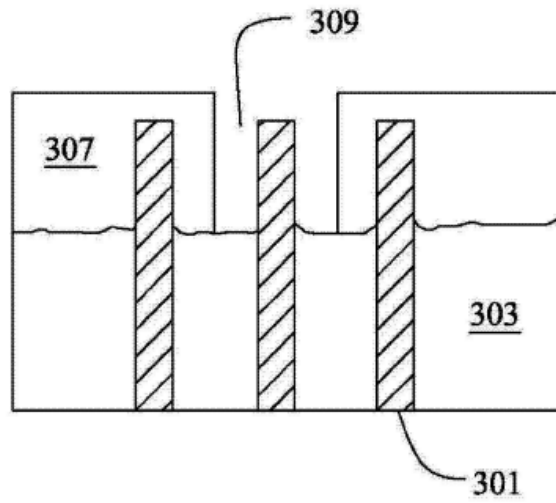


FIG. 3B

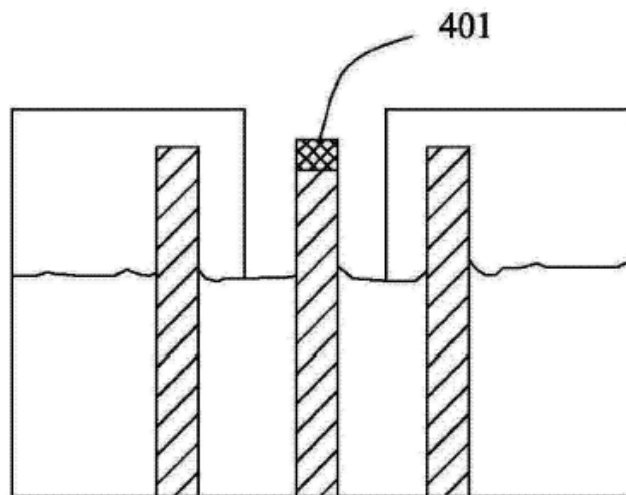


FIG. 4A

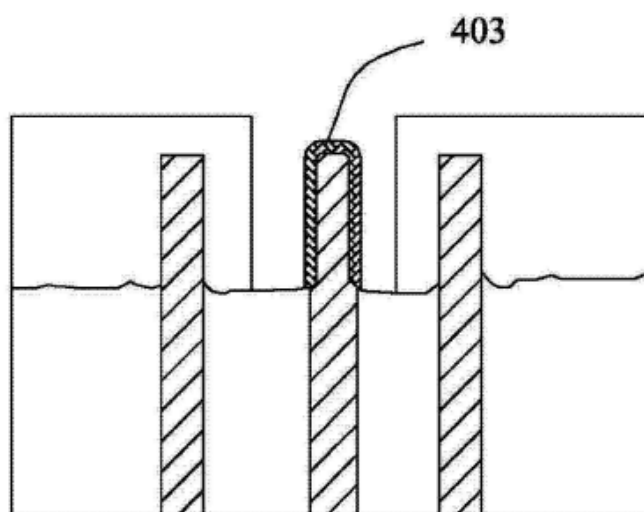


FIG. 4B

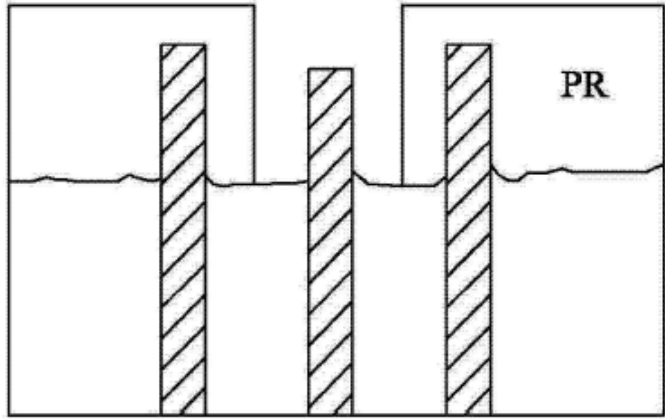


FIG. 5A

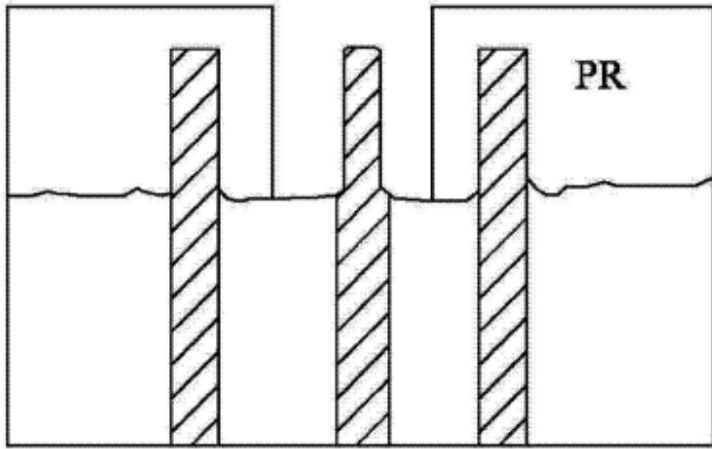


FIG. 5B

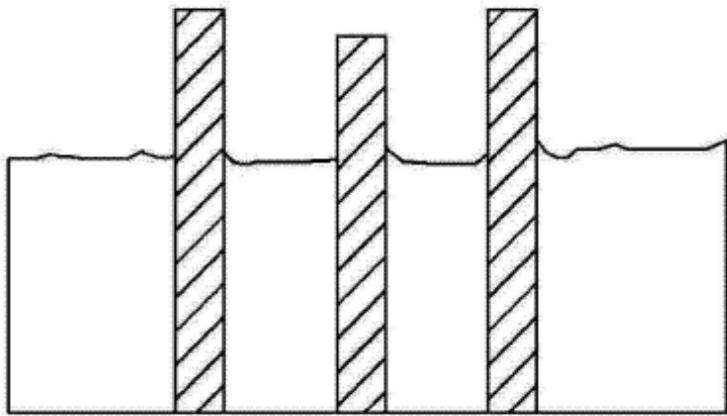


FIG. 6A

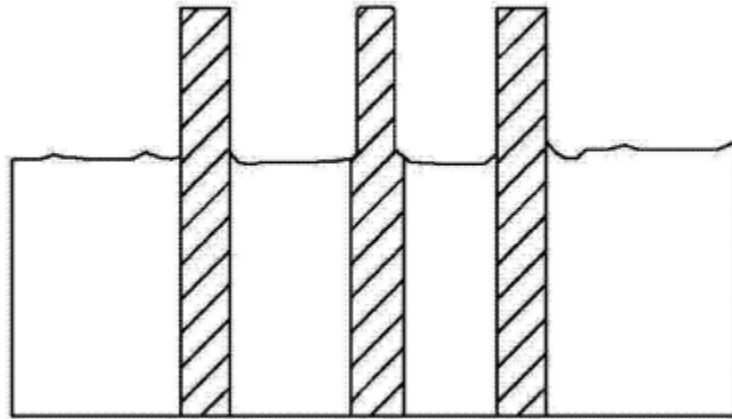


FIG. 6B

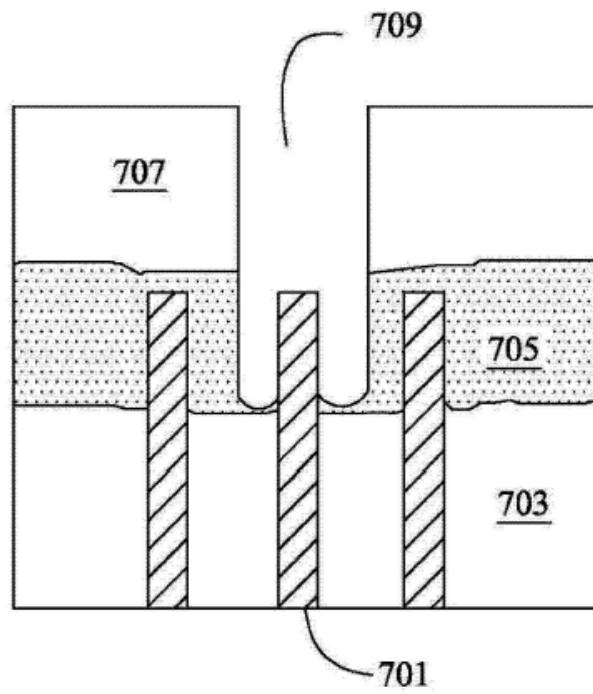


FIG. 7

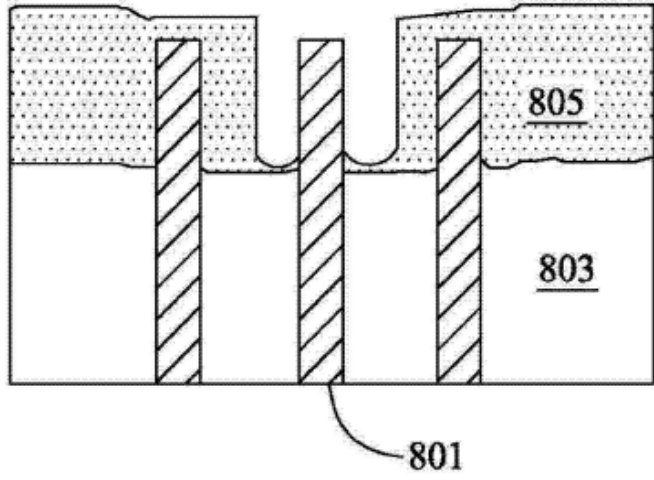


FIG. 8

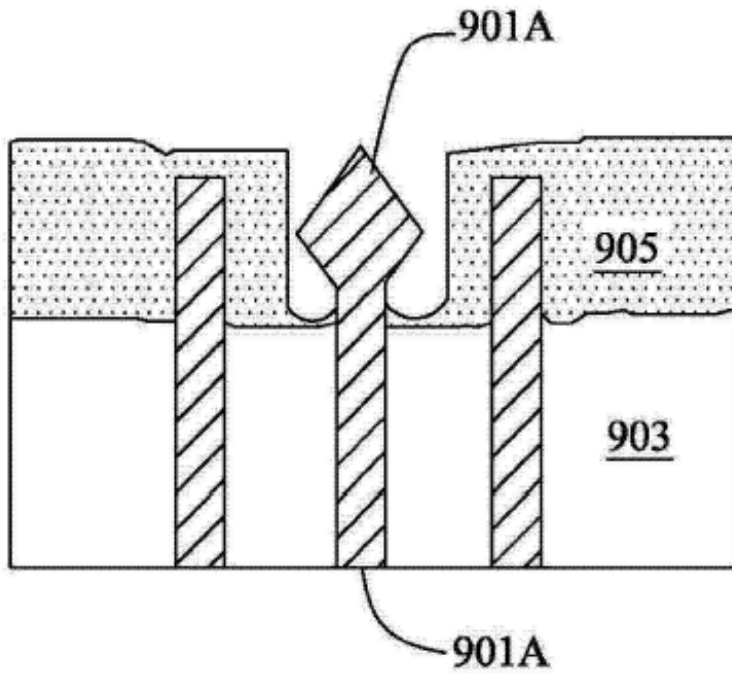


FIG. 9A

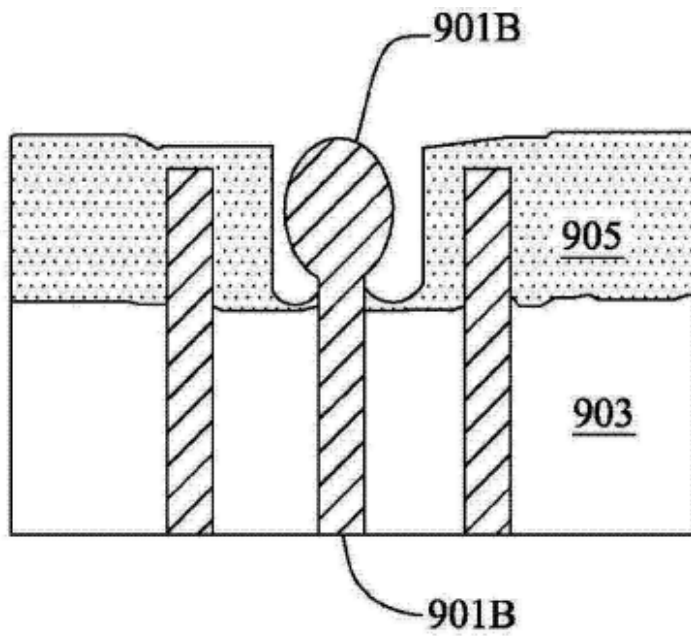


FIG. 9B

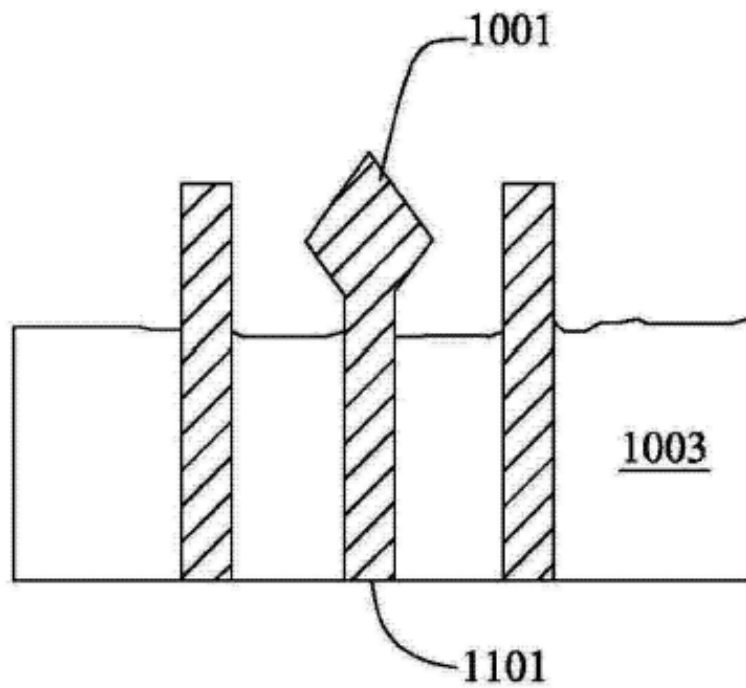


FIG. 10



## CERTIFICATE OF TRANSLATION

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Title: Project Manager



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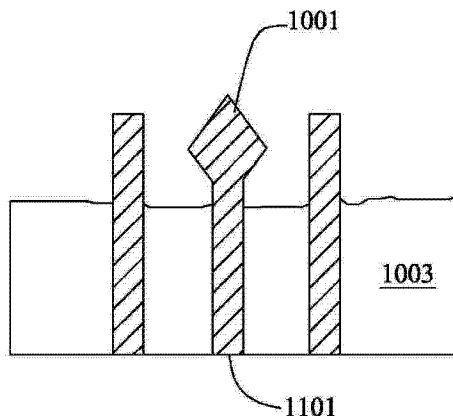
权利要求书 1 页 说明书 8 页 附图 8 页

(54) 发明名称

用于三维晶体管应用的采用等离子体掺杂和蚀刻的选择性鳍成形工艺

(57) 摘要

一种半导体装置,包括:具有成型鳍和规则鳍的鳍式场效晶体管 (FinFET)。成型鳍的顶部可以小于、大于、薄于、或短于规则鳍的顶部。成型鳍的底部和规则鳍的底部相同。FinFET 可以具有仅一个或多个成型鳍、一个或多个规则鳍、或成型鳍和规则鳍的混合。将一个鳍成型的半导体制造工艺包括:形成一个鳍的光刻开口,可选地掺杂鳍的一部分,以及蚀刻鳍的一部分。本发明还提供了一种用于三维晶体管应用的采用等离子体掺杂和蚀刻的选择性鳍成形工艺。



1. 一种装置,包括:  
半导体衬底;以及  
多个鳍式场效晶体管 (FinFET),位于所述衬底上,所述 FinFET 具有至少一个鳍;  
其中,所述多个 FinFET 中的至少一个包括至少一个成型鳍。
2. 根据权利要求 1 所述的装置,其中,所述至少一个成型鳍小于相同 FinFET 的其他鳍。
3. 根据权利要求 2 所述的装置,其中,所述至少一个成型鳍是不邻近设置的两个或多个鳍。
4. 根据权利要求 1 所述的装置,其中,所述至少一个成型鳍的一部分比相同 FinFET 的其他鳍更薄。
5. 根据权利要求 1 所述的装置,其中,所述至少一个成型鳍大于相同 FinFET 的其他鳍。
6. 根据权利要求 1 所述的装置,其中,所述多个 FinFET 中的至少一个的一部分是单鳍 FinFET。
7. 根据权利要求 1 所述的装置,其中,所述多个 FinFET 中的至少一个的一部分包括至少一个第一形状的成型鳍,所述多个 FinFET 的至少一个的另一部分包括至少一个第二形状的成型鳍,并且其中,所述第一形状和所述第二形状不同。
8. 根据权利要求 1 所述的装置,其中,所述至少一个成型鳍具有倾斜侧壁。
9. 一种鳍式场效晶体管 (FinFET),包括:  
半导体衬底;  
多个鳍,位于所述衬底上,包括一个或多个规则鳍和一个或多个成型鳍,其中,所述规则鳍和所述成型鳍的顶部形状不同;以及  
氧化层,位于所述半导体衬底上,嵌入所述多个鳍的底部,  
其中,所述多个鳍的嵌入底部具有基本上相同的形状。
10. 一种形成鳍式场效晶体管 (FinFET) 的方法,所述方法包括:  
在半导体衬底上形成多个部分地嵌入在浅沟槽隔离 (STI) 层中的鳍;  
在所述 STI 层上方沉积介电层,以完全覆盖所述多个鳍;  
图案化所述介电层上方的光刻胶层,以在单个鳍上方形成一个或多个开口;  
蚀刻穿透所述介电层,以暴露出单个鳍;  
去除所述光刻胶层;以及  
将暴露出的所述单个鳍成型。

## 用于三维晶体管应用的采用等离子体掺杂和蚀刻的选择性 鳍成形工艺

### 技术领域

[0001] 本发明一般地涉及集成电路器件,更具体地来说,涉及形成鳍式场效晶体管(fin field-effect transistors, FinFET)的结构和方法。

### 背景技术

[0002] 在快速发展的半导体制造业,互补金属氧化物半导体(complementary metal oxide semiconductor, CMOS) FinFET 器件可用于很多逻辑和其他应用中,并且集成为各种不同类型的半导体器件。FinFET 器件通常包括高纵横比的半导体鳍,在该半导体鳍中形成有晶体管的沟道和源极/漏极区域。沿着半导体鳍的一部分的侧面并在其上形成栅极。在 FinFET 器件内,沟道和源极/漏极区域的表面积增加使得半导体晶体管器件更快、更可靠并且更好控制。

[0003] 通过计算机辅助设计(computer-aided design, CAD)层来限定每个 FinFET 的边界开始应用于 FinFET 结构,新式的先进设计应运而生。由于制造工艺发展,出现越来越小的技术节点,原本采用较大技术节点设计的器件可以从采用较小技术节点制造中受益,如提高了性能和效率,并且减小了管芯的尺寸。同样,原本采用平面晶体管设计的器件也可以通过采用 FinFET 器件制造获益。然而,因为应用于平面结构布局的设计规则和应用于 FinFET 器件布局的设计规则不同,所以手工实现器件由平面布局到 FinFET 器件布局的转换部分是资源高度密集的过程,可能无异于创建新设计。对于已经使用平面晶体管制造的产品,要寻求形成至少与平面晶体管电气等效的 FinFET 器件的转换方法。因此,要继续寻求自动将旧的平面结构布局转换为 FinFET 结构布局的改进方法。

### 发明内容

[0004] 为了解决现有技术中所存在的问题,根据本发明的一个方面,提供了一种装置,包括:半导体衬底;以及多个鳍式场效晶体管(FinFET),位于所述衬底上,所述 FinFET 具有至少一个鳍;其中,所述多个 FinFET 中的至少一个包括至少一个成型鳍。

[0005] 在该装置中,所述至少一个成型鳍小于相同 FinFET 的其他鳍。

[0006] 在该装置中,所述至少一个成型鳍是不邻近设置的两个或多个鳍。

[0007] 在该装置中,所述至少一个成型鳍的一部分比相同 FinFET 的其他鳍更薄。

[0008] 在该装置中,所述至少一个成型鳍大于相同 FinFET 的其他鳍。

[0009] 在该装置中,所述多个 FinFET 中的至少一个的一部分是单鳍 FinFET。

[0010] 在该装置中,所述多个 FinFET 中的至少一个的一部分包括至少一个第一形状的成型鳍,所述多个 FinFET 的至少一个的另一部分包括至少一个第二形状的成型鳍,并且其中,所述第一形状和所述第二形状不同。

[0011] 在该装置中,所述至少一个成型鳍具有倾斜侧壁。

[0012] 根据本发明的另一方面,提供了一种鳍式场效晶体管(FinFET),包括:半导体衬

底；多个鳍，位于所述衬底上，包括一个或多个规则鳍和一个或多个成型鳍，其中，所述规则鳍和所述成型鳍的顶部形状不同；以及氧化层，位于所述半导体衬底上，嵌入所述多个鳍的底部，其中，所述多个鳍的嵌入底部具有基本上相同的形状。

[0013] 在该晶体管中，所述一个或多个成型鳍包括至少一个第一形状的成型鳍和至少一个第二形状的成型鳍。

[0014] 在该晶体管中，所述一个或多个成型鳍小于所述一个或多个规则鳍。

[0015] 在该晶体管中，所述一个或多个成型鳍大于所述一个或多个规则鳍。

[0016] 在该晶体管中，所述一个或多个成型鳍中的每一个均只邻近于所述一个或多个规则鳍，使晶体管中邻近的鳍之间的间隔相同。

[0017] 在该晶体管中，所述多个鳍和所述半导体衬底的材料相同。

[0018] 根据本发明的又一方面，提供了一种形成鳍式场效晶体管 (FinFET) 的方法，所述方法包括：在半导体衬底上形成多个部分地嵌入在浅沟槽隔离 (STI) 层中的鳍；图案化所述多个鳍上方的光刻胶层，以形成一个或多个暴露出单个鳍的开口；以及将暴露出的所述单个鳍成型。

[0019] 在该方法中，将暴露出的所述单个鳍成型包括：利用掺杂剂掺杂暴露出的所述单个鳍的一部分，以及去除暴露出的所述单个鳍的掺杂部分。

[0020] 在该方法中，将暴露出的所述单个鳍成型包括：蚀刻暴露出的所述单个鳍的一部分。

[0021] 在该方法中，所述去除步骤包括蚀刻。

[0022] 根据本发明的又一方面，提供了一种形成鳍式场效晶体管 (FinFET) 的方法，所述方法包括：在半导体衬底上形成多个部分地嵌入在浅沟槽隔离 (STI) 层中的鳍；在所述 STI 层上方沉积介电层，以完全覆盖所述多个鳍；图案化所述介电层上方的光刻胶层，以在单个鳍上方形成一个或多个开口；蚀刻穿透所述介电层，以暴露出单个鳍；去除所述光刻胶层；以及将暴露出的所述单个鳍成型。

[0023] 在该方法中，将暴露出的所述单个鳍成型包括：外延生长鳍材料。

## 附图说明

[0024] 当结合附图进行阅读时，根据下面详细的描述可以最好地理解本发明的特征。应该强调的是，根据工业中的标准实践，各种部件没有被按比例绘制并且仅仅用于说明的目的。实际上，为了清楚的讨论，各种部件的尺寸可以被任意增加或减少。

[0025] 图 1 示出了鳍式场效晶体管 (FinFET)。

[0026] 图 2 示出了根据本发明的各个实施例的制造 FinFET 器件的方法的流程图。

[0027] 图 3A 和图 3B 示出了根据本发明的各个实施例的部分制造完成的 FinFET 器件。

[0028] 图 4A、图 5A 和图 6A 示出了根据本发明的鳍短化的实施例。

[0029] 图 4B、图 5B 和图 6B 示出了根据本发明的鳍薄化的实施例。

[0030] 图 7、图 8 和图 10 示出了根据本发明的各个实施例的鳍形成工艺。

[0031] 图 9A 和图 9B 示出了根据本发明的各个实施例的鳍成形工艺。

## 具体实施方式

[0032] 以下详细讨论了说明性的实施例的制造和使用。然而,应该理解,本发明提供了许多可以在各种具体环境中实现的可应用的创造性概念。以下描述元件和布置的特定示例以简化本公开。当然这些仅仅是示例并不打算限定。例如,以下描述中第一部件形成在第二部件上可包括其中第一部件和第二部件以直接接触形成的实施例,并且也可包括其中额外的部件形成在第一部件和第二部件之间的实施例,使得第一和第二部件不直接接触。当然描述会具体阐述部件是否互相直接接触。另外,本公开可能在各个例子中重复参考数字和/或字母。所讨论的具体实施例仅仅是说明性的且并不限定本发明的范围。

[0033] FinFET 器件采用大致为矩形的鳍结构,通常用两种方法中的一种形成。在一种方法中,浅沟槽隔离 (shallow trench isolation, STI) 部件 105 首先形成在体硅材料上,如图 1 所示的衬底 101。STI 部件之间的沟槽底部暴露出体硅。然后,通过采用例如外延工艺,在沟槽里生长硅,以形成鳍 103。一旦达到所需的鳍高度,蚀刻 STI 105 至低于鳍顶部的水平面,以暴露出部分鳍。鳍的暴露部分是顶部 107,内嵌部分是底部 109。体硅材料 101 可以是硅衬底或者沉积硅,如绝缘体上硅 (silicon-on-insulator, SOI),在 SOI 和下面的硅衬底之间有阻挡氧化物 (barrier oxide, BOX) 层。采用此种方法,STI 部件限定了鳍的尺寸和形状。根据沟槽形成时所使用的蚀刻参数,鳍可能具有多种大致为矩形的形状,包括如图 1 所示的底部有微小的角度的鳍。

[0034] 在另一种方法中,通过首先对体硅进行图案化并且在该体硅上沉积硬掩模层,从而把衬底上的体硅蚀刻成矩形鳍形状。硬掩模形成了覆盖在鳍顶部的图案。然后,蚀刻体硅,在覆盖着硬掩模层的区域之间形成沟槽。通过沉积绝缘材料(通常是氧化硅),沟槽形成浅沟槽隔离 (STI) 部件 105。绝缘材料通常过量沉积以完全覆盖鳍 103 和可选的硬掩模层(如果尚未去除)。将绝缘材料平坦化至鳍/硬掩模层的顶部表面以下,然后将该绝缘材料蚀刻至低于鳍顶部的水平面,以使部分鳍突出到 STI 之上。突出的鳍的部分是顶部 107,内嵌的鳍部分是底部 109。

[0035] 在第二种方法的变形中,通过使用了金属心的工艺形成用于蚀刻体硅的硬掩模。形成和使用光刻胶图案蚀刻金属心图案。然后,围绕金属心沉积共形隔离件材料。共形隔离件通常由硬掩模形成,该硬掩模所形成的隔离件侧壁比金属心的隔离件侧壁更薄。然后,在随后的蚀刻操作中去除隔离件之间的金属心材料,只留下后面的隔离件。然后,一些隔离件用作硬掩模,以蚀刻下面的硅层,从而形成鳍结构。采用金属心/隔离件方法所形成的鳍,可以比采用第一种方法或采用未修正的第二种方法所形成的鳍相互更接近、更薄。暴露出的鳍部分 107 具有高度尺寸 (h)、宽度尺寸 (w) 和长度尺寸 (l)。根据这些尺寸可以限定 FinFET 器件的一些电气特性。例如,晶体管的有效沟道的宽度可以利用栅极下面的鳍尺寸计算出来。如图 1 所示,有效沟道宽度是 2 个鳍,或者  $2 \times (2h+w)$ 。注意,有效沟道的宽度不包括鳍之间的距离。因为在本文中的鳍都具有相同的高度尺寸和宽度尺寸,所以这些鳍被称为规则鳍。

[0036] 此处描述的剩余的形成 FinFET 器件的工艺步骤为本发明提供语境。栅极介电层 113 和栅极电极层 111 沉积在变窄的鳍上和 STI 层上方。栅极介电层 113 由高介电常数 (高 k) 绝缘材料形成。示例性的高 k 材料的 k 值可以大于约 4.0,甚至大于约 7.0,可能包括含铝电介质,如  $Al_2O_3$ 、 $HfAlO$ 、 $HfAlON$ 、或  $AlZrO$ ;也可以包括含铪的电介质,如  $HfO_2$ 、 $HfSiO_x$ 、 $HfAlO_x$ 、 $HfZrSiO_x$ 、或  $HfSiON$ ;和/或其他材料,如  $LaAlO_3$  或  $ZrO_2$ 。栅极电极层 111 形成在

栅极介电层 113 上,并由导电材料形成,如掺杂多晶硅、金属、或金属氮化物。

[0037] 然后,将栅极电极层 111 和栅极介电层 113 图案化,以在鳍的中部上方形成栅极堆叠件。然后,将不位于栅极堆叠件以下的鳍部分可选地掺杂,以形成轻掺杂漏极 (lightly doped drain, LDD) 和源极区域。使用的掺杂剂取决于晶体管的导电类型。可以通过离子注入或等离子体掺杂对 LDD 区域掺杂,其中,将掺杂剂沉积在鳍上并退火。在栅极堆叠件上形成源极和漏极区域。可以通过以下步骤形成源极和漏极区域:离子注入源极/漏极区域,或去除部分鳍并在掺杂条件下将去除的部分外延再生长以形成源极/漏极区域。

[0038] 电路设计者根据所要实现的各种功能的电气特性在其设计中指定晶体管。要考虑的电气特性包括开启电压(阈值电压)、击穿电压、导通电流(on-state current,  $I_{on}$ )、漏电流、等等。导通电流是栅极电压等于阈值电压时驱动穿过晶体管的电流。导通电流与沟道宽度成正比。当采用平面晶体管设计电路时,仅通过让晶体管更宽些或更窄些,沟道宽度就可以是任意值。然而,对于 FinFET 器件,沟道宽度不能是任意值——沟道宽度是单个鳍尺寸的整数倍。例如,FinFET 器件的沟道宽度可以等于 2 个鳍或 3 个鳍,但不能是 2.5 个鳍。当基于平面晶体管的设计转换成基于 FinFET 器件的设计的时候,平面晶体管不能转换成具有完全相同的导通电流的 FinFET 器件。虽然根据电路的功能和应用,通常在一定范围内的导通电流都是可接收的,但是 FinFET 的沟道宽度的选择限制降低了设计的灵活性和平面晶体管到 FinFET 器件转换的精度。

[0039] 本发明的各个实施例关于选择性鳍成形工艺,以允许单个鳍宽度和鳍高度控制。通过将 FinFET 器件中的一个或多个鳍成型,FinFET 器件的沟道宽度可以变化为超过了单个鳍尺寸的整数倍。选择性鳍成形可以扩大一个或多个鳍,缩小一个或多个鳍,薄化一个或多个鳍,同时减小所有鳍尺寸,或在其他规则鳍保持不变的情况下,用其他方式改变一个或多个鳍的形状以创建成型的鳍。例如,通过减小一个鳍的尺寸可设计相当于有 2.5 个鳍的 FinFET 器件。优点可包括提高了电路设计的灵活性,增加了从事基于平面晶体管的设计到基于 FinFET 器件设计的转换的设计者和铸造厂的 FinFET 工艺裕度。

[0040] 参考图 2,示出了选择性鳍成形的工艺流程 211。在操作 213 中,在半导体衬底上形成部分嵌入浅沟槽隔离(STI)层的鳍。如本文所论述,可采用多种方法形成鳍。鳍可以通过蚀刻体硅得到,或外延生长得到。

[0041] 在操作 215 中,在 STI 层上方沉积可选介电层以完全覆盖鳍。如果要扩大一个或多个鳍,则要用到可选介电层。如果要减小一个或多个鳍,则可选介电层是不必要的。可选介电层可以是氧化硅、氮化硅、或其他较下面的 STI 层更容易蚀刻的介电层。在一些情况下,可在介电层之前沉积蚀刻停止层。在这种情况下,介电层的材料与 STI 层的材料可以相同。图 3A 示出了经过操作 215 后部分制造完成的 FinFET 器件。鳍 301 部分地嵌入 STI 层 303。介电层 305 沉积在 STI 层 303 上方,并且完全覆盖鳍 301。

[0042] 再次参考图 2,在操作 217 中,在鳍上方图案化光刻胶层。光刻尺寸限制了光刻胶层可以保护的最小尺寸以及光刻胶图案可以创建的最小尺寸开口。最小开口小于要保护的最小区域。换句话说,可以用一个鳍间距的尺寸创建开口,但相反,覆盖一个鳍间距的保护区域可能会太小。在图 3A 和图 3B 中,沉积并图案化光刻胶层 307,以创建开口 309。如果沉积了操作 215 中的介电层,则如图 3A 中所示,在介电层上方沉积光刻胶层。如果没有沉积操作 215 中的介电层,那么如图 3B 所示,直接在 STI 层和鳍上方沉积光刻胶层。

[0043] 再次参考图 2,在可选(虚线)操作 227 中,对暴露的单个鳍用掺杂剂掺杂。根据将要掺杂的部分,可以采用若干掺杂工艺。在一个实施例中,可采用离子注入工艺对鳍最顶部的小的垂直部分进行掺杂。掺杂离子对准开口,但由于开口的纵横比,基本上鳍的顶部都将被掺杂,如图 4A 中的鳍顶端 401 所示。掺杂剂可能是氧,以形成氧化硅鳍顶端。掺杂剂可能是氮,以形成氮化硅顶端。也可以采用可有效地改变鳍顶端 401 的化学特性以使其可以在后续的蚀刻程序中被简单地去除的其他掺杂剂。

[0044] 在其他实施例中,如图 4B 所示,可采用共形等离子体掺杂工艺将鳍外层 403 转换为不同的材料。等离子体可以在现场或远程产生。例如,可用氧等离子体来氧化鳍的外层部分。也可以采用包括其他掺杂剂的等离子体,有效地改变鳍外层 403 的化学特性,以使外层 403 可以在后续的蚀刻程序中被简单地去除。

[0045] 再次参考图 2,在操作 229 中,蚀刻和去除暴露出的单个鳍的部分。去除部分可以是操作 207 中被掺杂的部分。根据掺杂工艺的类型和各种材料的蚀刻选择性,可以采用若干式蚀刻工艺。

[0046] 在一些实施例中,将要去除的部分基本上位于鳍的顶端。采用这些实施例可以缩短 FinFET 器件中的一个或多个鳍,但丝毫不能改变鳍的宽度。可采用各个类型的等离子体蚀刻去除鳍顶端的掺杂部分。在图 4A 的一个示例中,将要去除的部分位于鳍的顶端,可以采用偏等离子体去除鳍顶端的材料。根据要去除的材料,等离子体可以包括活性离子,如氢和氟,例如氟碳等离子体。等离子体也可以可选地或额外地包括相对惰性类物质(relative inert species),如氮、氩、氦或氙。例如,如果鳍顶端是氧化硅,则各向异性等离子体蚀刻可以包括氟基蚀刻剂。注意,相对于下面 STI 层里的氧化硅和鳍里的硅,等离子体蚀刻剂应该对于鳍顶端的氧化硅具有蚀刻偏好(etching preference),以免以不期望的方式去除了许多 STI 层并且对鳍定型。可以通过以下方式将 STI 层的意外蚀刻最小化:以朝向衬底的较低功率进行偏置,将等离子体以一个角度朝向衬底使得大部分入射角都被阻挡,并且还通过选择蚀刻剂和 STI 材料来具有不同的蚀刻选择性。

[0047] 在另一个示例中,如果掺杂剂是氮,则鳍顶端可以是氮化硅。比氧化硅具有氮化硅相对高蚀刻选择性的氮化硅等离子体蚀刻可以随着甲烷、氮和氧助剂气流而包括一些氟基等离子体。本领域技术人员可以调整气体混合物,以使相对于鳍顶端的氮化硅,很少或没有 STI 层被去除。蚀刻掉掺杂的鳍顶端后,由此产生的结构可能是图 5A 中的那样,其中,暴露的单个鳍短于邻近的受保护的鳍。

[0048] 还可以采用湿式蚀刻方法去除掺杂的鳍顶端。在湿式蚀刻方法中,一个或多个衬底浸(bathed)在蚀刻剂容器里,还可以进行搅动,以促进蚀刻剂接触要被蚀刻的表面。湿式蚀刻剂通常会腐蚀(attack)所有暴露的表面,因此,相对于结构的其他部分,湿式蚀刻剂应具有用于蚀刻鳍顶端材料的高蚀刻选择性。例如,对于氧化硅鳍顶端,湿式蚀刻剂可以包括氢氟酸或氟碳蚀刻剂。对于氮化硅鳍顶端,湿式蚀刻剂可以包括磷酸。

[0049] 在一些实施例中,如图 4B 所示,鳍外层是将被去除的部分。适当的各向同性蚀刻方法包括使用等离子体的干式蚀刻方法和湿式蚀刻方法。例如,可通过采用湿式蚀刻中的缓冲氧化蚀刻或氟化铵和氢氟酸的混合物去除氧化硅外层。等离子体蚀刻可涉及无偏等离子体,包括远程产生等离子体,去除外层。例如,可以采用带有氧的远程产生的 SF<sub>6</sub> 等离子体。蚀刻掉掺杂的外层部分后,由此产生的结构可能是图 5B 中的那样,其中,暴露的单个鳍

薄于、并且有些短于邻近的受光刻胶保护的鳍。

[0050] 仍有其他的实施例中，不采用首先掺杂鳍部分的方法蚀刻暴露的单个鳍的部分。各种蚀刻方法直接应用于硅鳍以改变其形状。可以将各种蚀刻方法分类为：干式蚀刻和湿式蚀刻、各向同性和各向异性、和产生不同形状的不同组合。

[0051] 在一个示例中，可能采用使用各种氟基等离子体（如  $\text{XeF}_2$  和  $\text{BrF}_3$ ）的等离子体蚀刻来各向同性地对暴露的鳍重新成型。效果类似于首先采用含等离子体的氧气氧化鳍、然后蚀刻氧化硅层。

[0052] 在另一个示例中，采用聚合技术的等离子体蚀刻可以使得仅针对鳍的顶端部分进行适度的各向异性蚀刻。侧壁上的来自蚀刻沉积的聚合物副产品形成保护层。使用此技术，在后续的处理中必须去除聚合物残留物。可采用富含碳的氟碳或氢氟碳等离子体。

[0053] 在另一个示例中，采用各向异性蚀刻剂的湿式蚀刻可以根据晶体定向将鳍成型。以定向面从属速率去除硅的各向异性湿式蚀刻包括采用四甲基氢氧化铵（tetramethylammonium hydroxide, TMAH）、氢氧化钾（potassium hydroxide, KOH）或其他强碱性蚀刻剂（ $\text{pH} > 12$ ）去蚀刻硅。因为每个晶面硅原子的结合能（bonding energy）不同，所以在蚀刻率限制（而非扩散限制）的反应中，这些蚀刻剂在特定的定向面间具有高灵敏度。TMAH 湿式蚀刻形成凹口（notch）开口。KOH 湿式蚀刻的定向依赖性类似于 TMAH，但有不同的速率和比例。在一个示例中，蚀刻剂包括 TMAH 和 KOH，其中 TMAH 约占重量的 20%。

[0054] 在又一个示例中，各向同性湿式蚀刻可以均匀地从所有方向去除未受保护的硅。各向同性硅蚀刻可以采用氢氟酸（hydrofluoric, HF）的组合，添加若干添加物，如硝酸（ $\text{HNO}_3$ ）、柠檬酸（ $\text{CH}_3\text{COOH}$ ）、亚氯酸钠（ $\text{NaClO}_2$ ）、高氯酸（ $\text{HClO}_4$ ）、新鲜的高锰酸钾（ $\text{KMnO}_4$ ）、或这些添加物的组合。这些化学混合物均匀地去除材料，并且受化学物类（chemical species）在晶体表面的质量传输（扩散限制）的限制。

[0055] 再次参考图 2，在操作 231 中，去除了光刻胶层。采用本领域公知的灰化工艺完成光刻胶的去除。图 6A 和图 6B 示出了由此产生的鳍结构的示例。在图 6A 中，FinFET 器件包括 3 个鳍，其中 2 个规则鳍和 1 个成型鳍。成型鳍具有较短的顶部。在图 6B 中，FinFET 器件也包括 3 个鳍，其中 2 个规则鳍和 1 个成型鳍。成型鳍具有较窄的顶部，该较窄的顶部可以相同于、略短于、或略长于相邻的规则鳍。因为底部没有成型，所以三个鳍的底部都大致相同。注意，虽然成型鳍可能短于规则鳍，但是因为 STI 层也被蚀刻，并且成型鳍的顶部可以更多地暴露出来，所以成型鳍的顶部可以与规则鳍的顶部长度相同或者长于规则鳍。

[0056] 本文讨论的各种蚀刻方法可以多种方式将暴露的鳍成型，以形成减小鳍高度和/或宽度的轮廓。轮廓变化使得 FinFET 器件能够具有非规则鳍整数倍的有效沟道宽度。根据期望的有效沟道宽度选择蚀刻方法来最小化处理和最大化工工艺控制。

[0057] 在减小鳍宽度的实施例中，额外的优点是增加了邻近鳍间的距离。增加鳍间的距离增大了用于形成栅极的工艺窗口。FinFET 器件可以包括沉积在鳍中部上方的不同材料的许多层。每层都增加了鳍间的剩余空间的纵横比，使得最后的层可能由于没有空隙而难以充分沉积。增加鳍间距离减少了最初的纵横比，使得最后沉积工艺窗口较大。

[0058] 仍然再次参考图 2，操作 219 至操作 223 示出了通过增大鳍成型暴露出的单个鳍的可选实施例。在操作 219 中，蚀刻穿透由操作 215 得到的介电层以暴露单个鳍。当增大暴露的鳍时，介电层用来保护规则鳍。图 7 示出了将介电层 705 蚀刻到 STI 层 703 以下，形成

包含一个单个鳍 701 的开口 709 之后的结构。然后,如图 8 所示,用图 2 中的操作 221 去除光刻胶层 707。因为外延温度非常高,高于适合光刻胶材料的温度,所以在操作 221 中去除了光刻胶。注意,为了鳍 801 的外延生长,介电层 805 可以是氧化硅,且某些情况下可以是氮化硅。

[0059] 在操作 223 中,在外延生长工艺期间,硅在暴露出的鳍上生长。没有硅在被介电层 805 覆盖的表面上生长。因为外延温度非常高,高于适合光刻胶材料的温度,所以在操作 221 中去除了光刻胶。图 9A 和图 9B 示出了由操作 223 得到的不同的结果。在图 9A 中,根据晶体定向,沿着暴露的鳍的表面单晶生长,形成了成型鳍 901A。鳍 901A 的各种顶端角度取决于鳍的晶体定向。在一些实施例中,可控制鳍的顶端形状以形成不同的形状,如图 9B 中示出的那样。在外延生长期间,可包括能蚀刻特定表面的额外气体以将生长成型。可以通过调整具有各种盐酸气流的外延配方 (epitaxial recipe) 形成如鳍 901B 的形状的球状顶端形状。

[0060] 再次参考图 2,在操作 231 中,去除光刻胶层。采用本领域公知的灰化工艺完成光刻胶的去除。图 10 中示出了由此产生的鳍的示例,展示了成型鳍 901A。在图 10 中,FinFET 器件包括 3 个鳍,其中 2 个规则鳍和 1 个成型鳍。成型鳍有对应硅晶定向的有角的表面 (angular face)。与有 3 个规则鳍的 FinFET 器件相比,图 10 中的 FinFET 器件的有效沟道宽度增加。

[0061] 本文中关于一个有三个鳍的 FinFET 器件论述了本公开的各个实施例。实际上,FinFET 器件可能有任意数量的鳍,从一个至多个、甚至上百个。本公开并不限制 FinFET 器件具体的鳍个数。对于单鳍 FinFET 器件,唯一的鳍是成型鳍。对于两鳍 FinFET 器件,可以将一个或两个鳍成型。对于三鳍 FinFET 器件,可以将中间的鳍成型。如所述,尽管可在光刻胶中形成单个鳍开口,但是有光刻胶保护,仅一个鳍对于当前光刻工艺来说可能太小。因此,对于有超过 3 个鳍的 FinFET 器件,成型鳍可以通过 2 个规则鳍与规则鳍间隔开。四鳍 FinFET 器件可以包括位于两端的成型鳍和位于中间的两个规则鳍。可选地,可在同一开口中成型多个鳍。因此,四鳍 FinFET 器件也可包括位于中间的成型鳍和在两端的规则鳍。当然,可能三个鳍是成型的或三个鳍是规则的,或者可能所有鳍都是成型的或所有鳍都是规则的。

[0062] 一种集成电路装置包括很多晶体管。该装置可能包括很多具有不同数量鳍的不同尺寸的 FinFET。一些 FinFET 可能具有成型鳍,而一些 FinFET 可能不具有成型鳍。FinFET 可以具有多种类型的成型鳍,例如,五鳍 FinFET 可以具有 2 个规则鳍、2 个通过特定方式成型的鳍和 1 个通过不同方式成型的鳍。虽然成型鳍的工艺可能重复任意次,但是每次鳍成形工艺使用的生产资源都包括一个光掩模和一次至多次沉积和蚀刻工艺。

[0063] 根据各个实施例,本发明涉及一种装置,该装置具有位于半导体衬底上的若干个 FinFET,其中,一些 FinFET 具有至少一个成型鳍。该成型鳍可以小于或大于相同 FinFET 中的或其他 FinFET 中的规则鳍。在一些实施例中,至少一个成型鳍可以是两个或多个鳍,并且不相互邻接放置。在一些实施例中,多种成型鳍可以用在相同的 FinFET 中。

[0064] 根据各种实施例,本发明还涉及一种 FinFET 器件,包括:半导体衬底、在衬底上的包括一个至多个规则鳍和具有不同顶部形状的一个至多个成型鳍的若干个鳍、在衬底上的嵌入了鳍底部的氧化层,其中,所嵌入的鳍底部具有大致相同的形状。然而定位效果可能在

一定程度上影响晶体管边缘上的鳍的底部形状,但是这种变形并不明显,并且如果在制造的时候其唯一的不同是定位小欧冠,那么鳍将有大致相同的形状。

[0065] 根据各种实施例,本公开也关于形成 FinFET 器件的方法,包括:在半导体衬底上形成若干个通过浅沟槽隔离(STI)层部分地内嵌的鳍、在多个鳍上图案化光刻胶层以形成一个或多个暴露单个鳍的开口、和成型暴露的单个鳍。

[0066] 尽管已经详细地描述了本发明的实施例及其优势,但应该理解,可以在不背离所附权利要求限定的本发明主旨和范围的情况下,做各种不同的改变、替换和更改。而且,本申请的范围并不仅限于本说明书中描述的工艺、机器、制造、材料组分、装置、方法和步骤的特定实施例。作为本领域普通技术人员应理解,通过本发明的公开,现有的或今后开发的用于执行与本文所述相应实施例基本相同的功能或获得基本相同结果的工艺、机器、制造,材料组分、装置、方法或步骤根据本发明可以被使用。因此,所附权利要求应该包括在这样的工艺、机器、制造、材料组分、装置、方法或步骤的范围内。

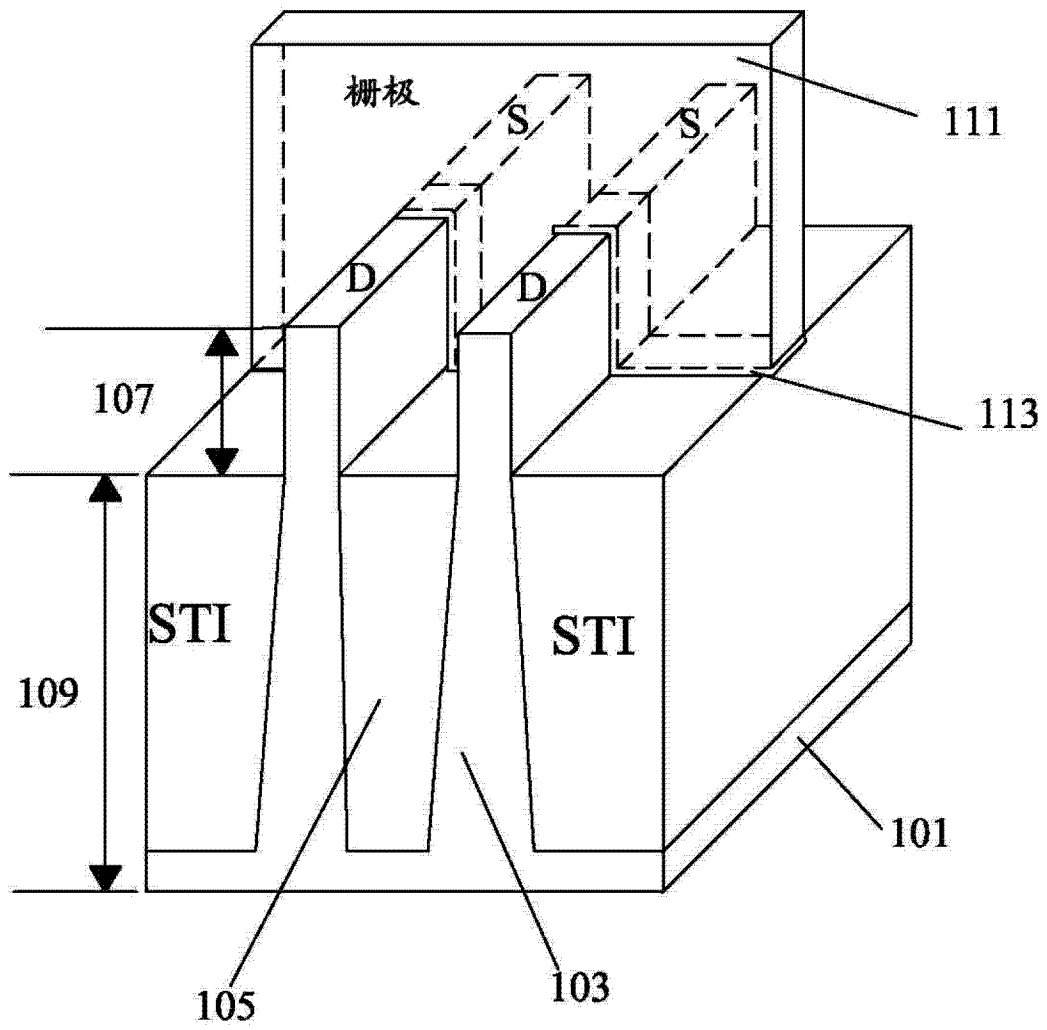


图 1

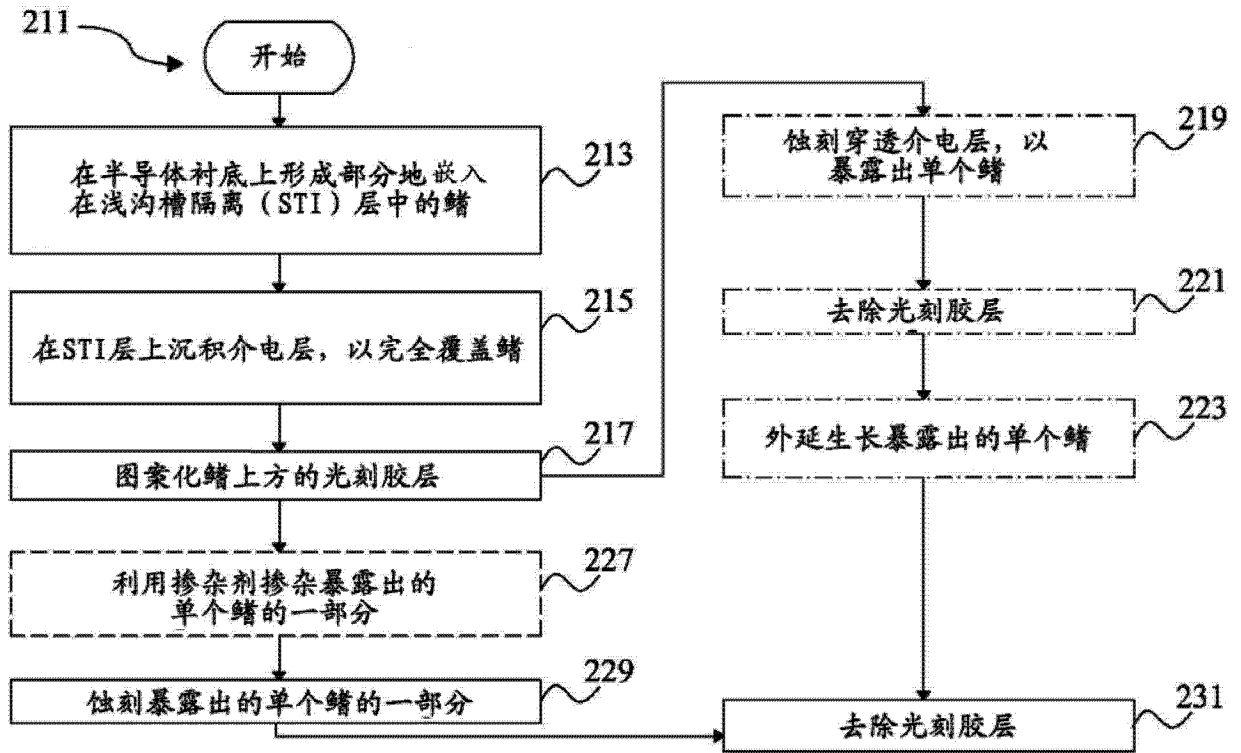


图 2

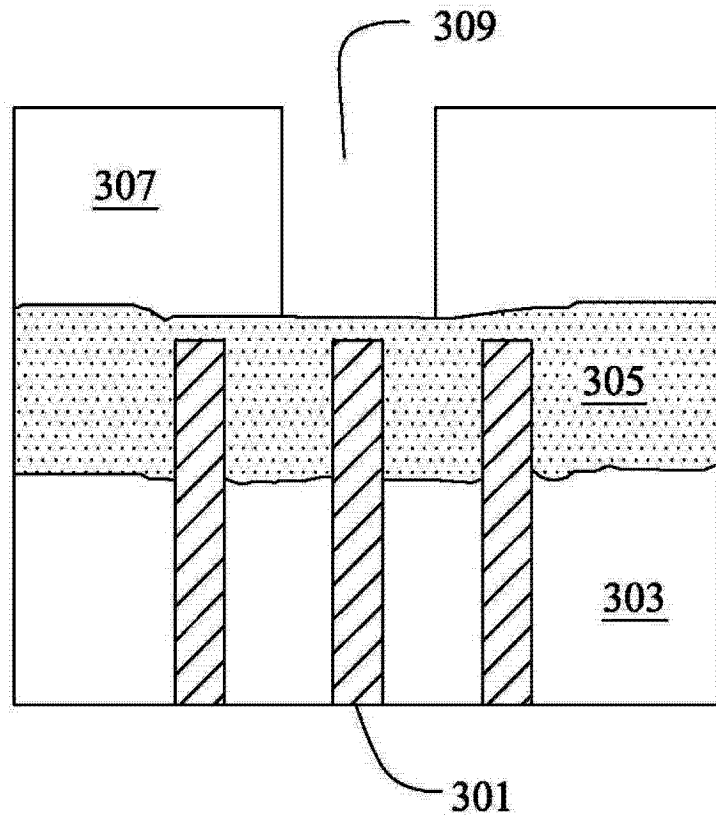


图 3A

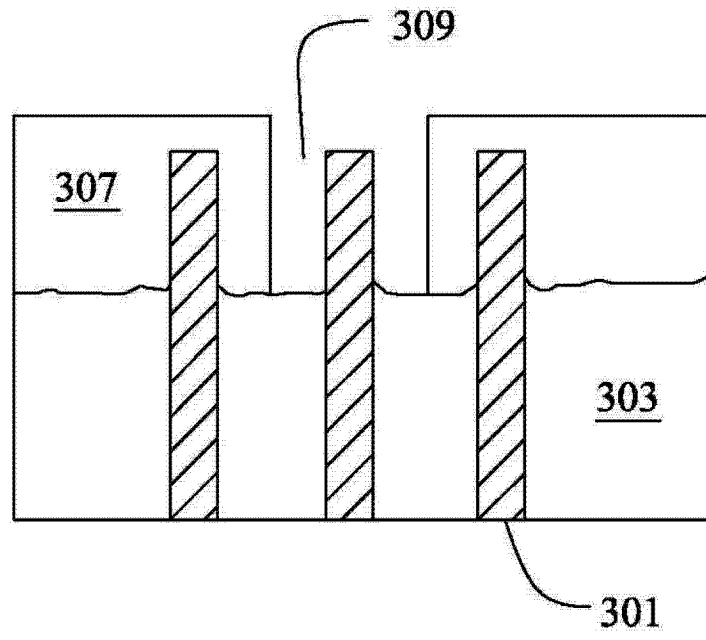


图 3B

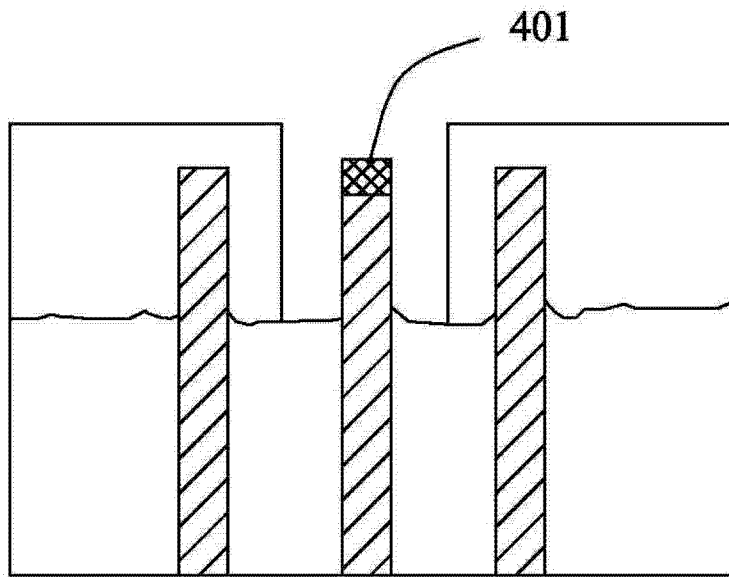


图 4A

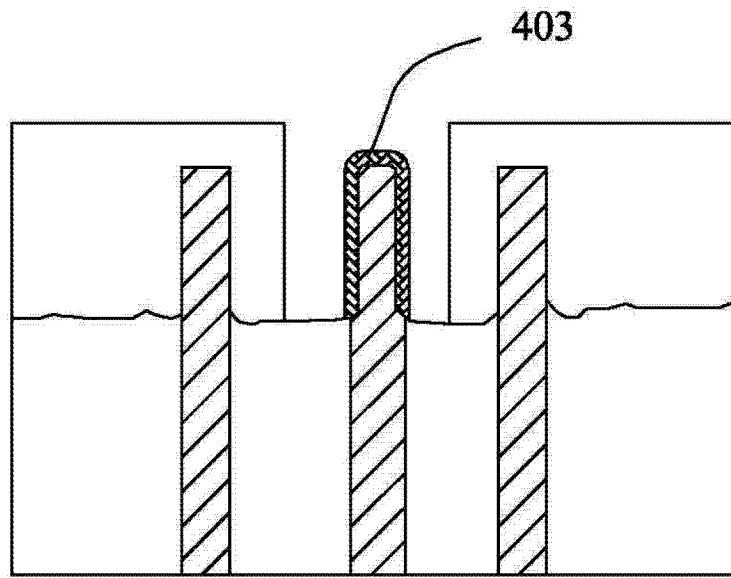


图 4B

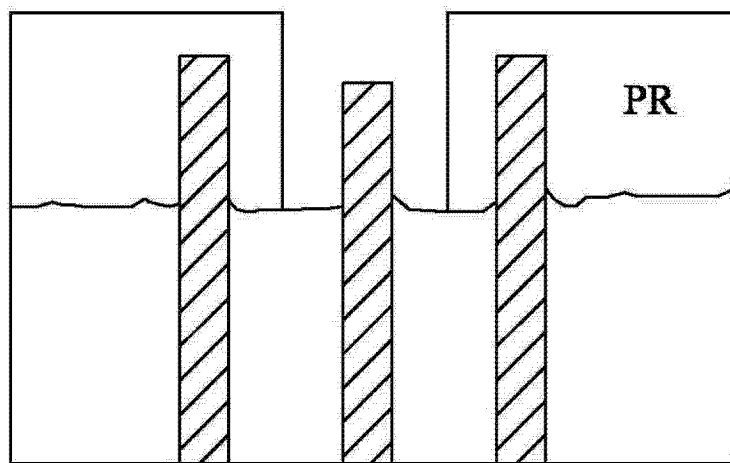


图 5A

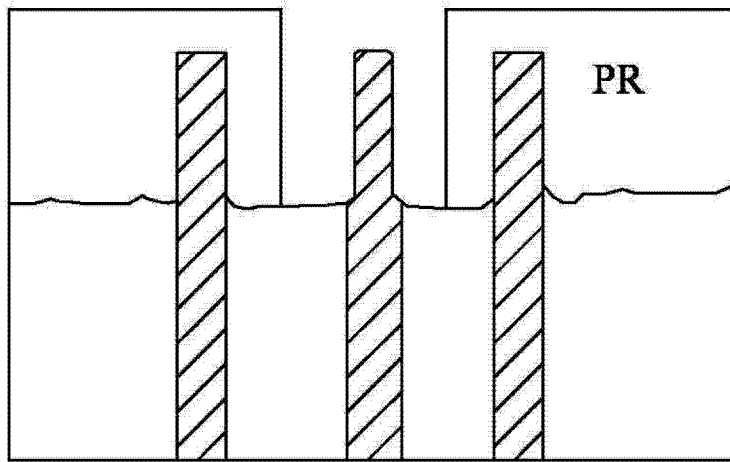


图 5B

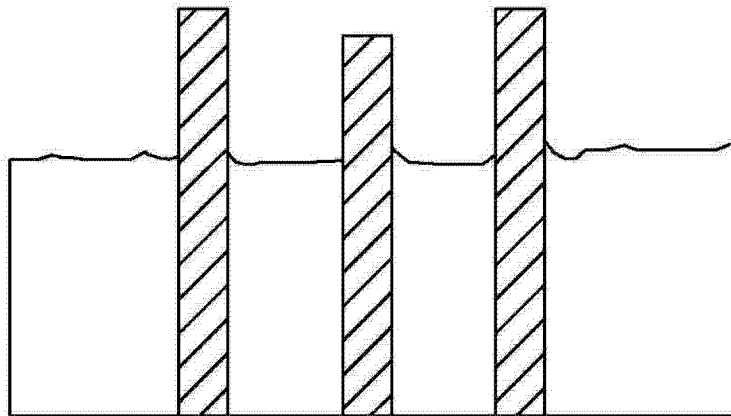


图 6A

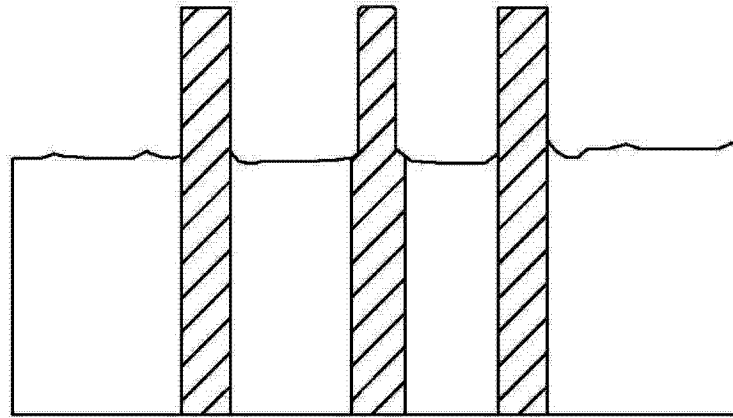


图 6B

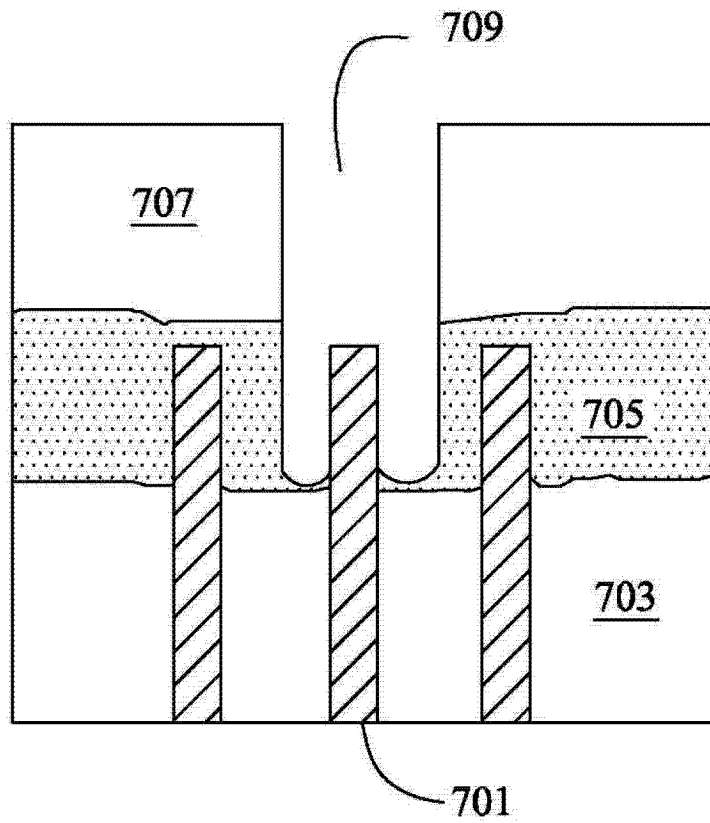


图 7

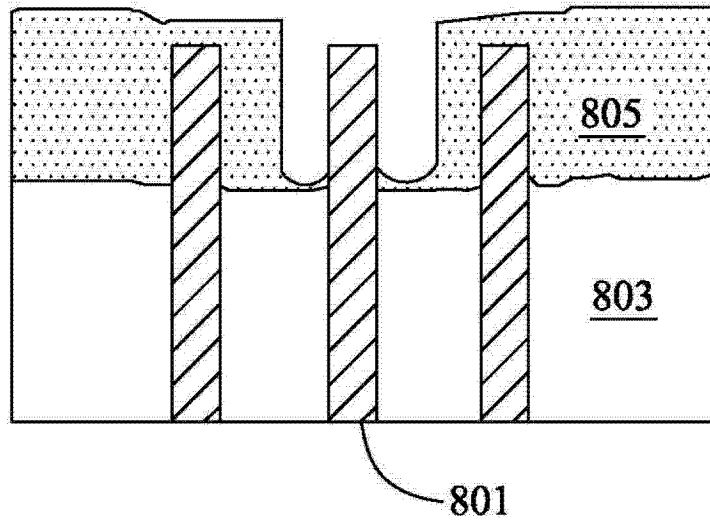


图 8

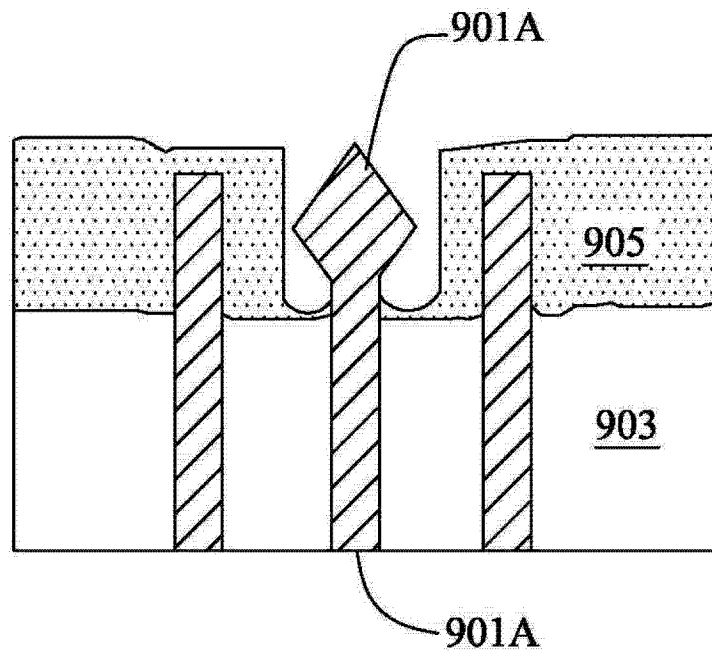


图 9A

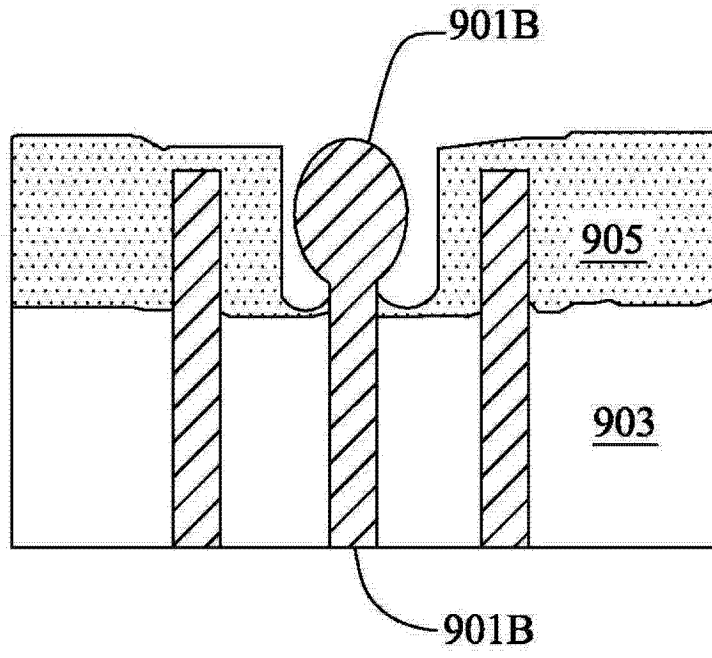


图 9B

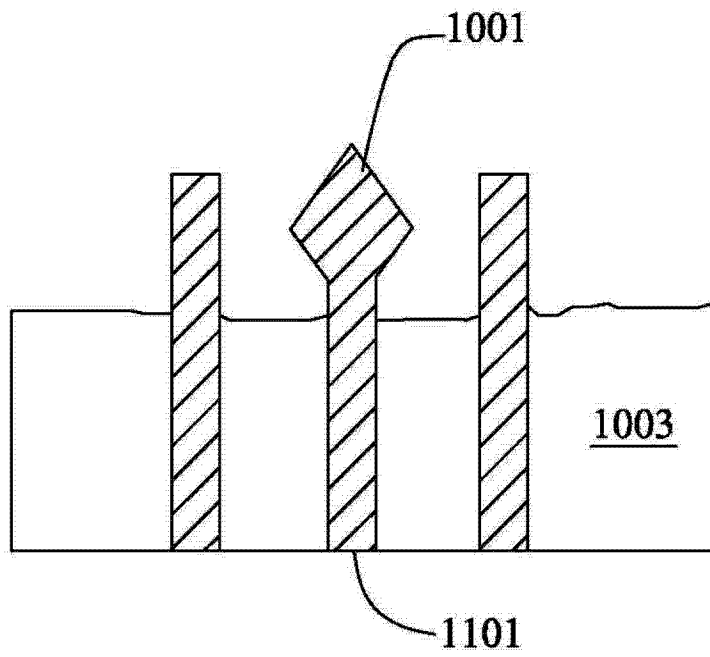


图 10