UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

Petitioner,

v.

MARLIN SEMICONDUCTOR LIMITED,

Patent Owner.

Case No. IPR2025-01484

U.S. Patent No. 9,786,510 B2

DECLARATION OF JOSEPH MCALEXANDER

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"A Third Distance Between Adjacent Lower Parts Of The First Fin And The Second Fin Is The Same As A Fourth Distance Between Adjacent Lower Parts Of The Third Fin And The Fourth Fin" 27

TABLE OF EXHIBITS

Exhibit	Description
2002	Peter Van Zant, *Microchip Fabrication, A Practical Guide to Semiconductor Processing*, (4th ed. 2000)
2003	*Curriculum Vitae* of Joseph C. McAlexander III

I. QUALIFICATIONS

1. I am a Registered Professional Engineer (#79454) and the President of M^c^Alexander Sound, Inc. I hold a Bachelor of Science degree in Electrical Engineering from North Carolina State University. I have been associated with the integrated circuit and electronics industry as a designer and consultant for the past 53 years and am a named inventor on 31 U.S. patents and a number of foreign patents, many of which are directly related to the design and operation of transistors and circuits incorporating transistors, including control, addressing, comparing and sensing, and fabrication.

2. My skills and experience are in areas of circuit design and analysis, device and board fabrication and assembly, testing, marketing, control system design and analysis, manufacturing operations, and respective areas of quality, reliability, and defect/failure analysis. Specifically, I have:

- designed memories, including Dynamic Random Access Memories (DRAMs), Static Random Access Memories (SRAMs), Charge Coupled Devices (CCDs), Shift Registers (SRs), and functional circuits including I/O buffers for address and data, decoders, clocks, sense amplifiers, fault tolerant (incorporating both non-volatile EPROM and random access memory components), parallel-to-serial data paths for video applications, level shifters, converters, pumps, and logic, as well as wireless communication systems and MEMs;
- managed operations including engineering, training, and quality assurance for device fabrication, assembly, test, analysis, and reliability assessment, as well as manufacturing control, each of which involved both volatile and non-volatile memory; testing, analysis, and control involved use of mechanical calibration and

measuring equipment, including optical, scanning e-beam, IR, capacitive, and laser using phase contrast and FFT for HARI applications;

- taught courses in solid-state device physics, integrated circuit design, integrated circuit fabrication, and statistical control;
- provided expert services, investigating both process and design technologies of various devices (microprocessor and controller, volatile and non-volatile memory, programmable logic, card, tag, module, mixed signal, custom, and other), systems (PC and peripheral, computer, control, laser measurement, switch, architecture, software, and other), and consumer products (medical, TV, telephone, VCR, facsimile, copier, lighting, game, and other); and
- designed and managed development, testing, and evaluation of memory devices and systems incorporating such devices, including simulation of operation. I have also had experience in programming, erasing, and wearout of electrically programmable and erasable non-volatile memories.

3. Because of my background, training, and experience, I am qualified as an expert to opine on the challenged patent. A more detailed account of my work experience and other qualifications is listed in my Curriculum Vitae, which is submitted as Exhibit 2003.

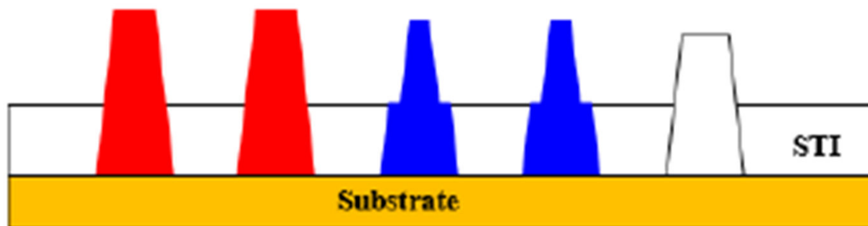
II. OVERVIEW

4. Each of the three asserted grounds fails to disclose all of the limitations of each challenged claim of U.S. Patent Number 9,786,510 (“the ’510 patent”).

5. With respect to Grounds 1 and 2, the Oh reference (Ex. 1005) does not disclose or render obvious “a third distance between adjacent lower parts of the first

fin and the second fin is the same as a fourth distance between adjacent lower parts of the third fin and the fourth fin," as required by all challenged claims. The Petition argues that Oh renders obvious that the spacing between adjacent fins is uniform, but this interpretation is conclusory and unsupported by Oh's disclosure.

6. With respect to Ground 3, the Petition fails to set forth any motivation to combine the Wann (Ex. 1007) and Lin (Ex. 1008) references in the manner suggested by the Petition. The Petition proposes a very specific combination that allegedly meets all of the challenged claim elements, as alleged to be depicted in the illustration below:



EX1003, Illustration 8.

7. However, this above illustration is not found in either of the Wann or Lin alleged prior art, and based only on Wann's brief mention of a five-fin FinFET embodiment having "2 regular fins, 2 fins shaped a particular way, and 1 fin shaped a different way." As such, the proposed combination is wholly speculative and fabricated using impermissible hindsight; and the Petition fails to set forth any rationale for why a POSA would combine the Wann and Lin references in this specific manner.

III. MATERIALS CONSIDERED

8. In preparing this declaration, I have reviewed the Petition and the declaration of Petitioner's expert, as well as the materials that they cite, including the asserted prior art.

IV. UNDERSTANDING OF THE LAW

9. In preparing and expressing my opinions and considering the subject matter of the challenged patent, I am relying on certain basic legal principles that counsel have explained to me. These principles are discussed below.

A. Claim Construction

10. I understand that the scope of a patent is defined by its claims. I understand that a claim can be:

a. a method claim, which covers a process/activity, or

b. an apparatus claim, which covers a physical machine, etc.

11. I understand that the first step in determining the validity of a claim is for the claim to be properly construed. I have been further advised that, in an inter partes review proceeding, the claims of a patent are typically given their ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the claims and the patent disclosure (specification).

12. I further understand that an inventor can provide special definitions for specific claim term(s) within the patent. However, any special definition for a claim term must be set forth in the specification with reasonable clarity and precision.

B. Invalidity

13. I have been informed that a claim may be invalid as obvious if the subject matter described by the claim, as a whole, would have been obvious to a POSITA at the time the claimed invention was made. I understand that the standard for obviousness in an inter partes review proceeding is by a preponderance of the evidence.

14. I have also been informed that a determination of obviousness involves an analysis of the scope and content of the prior art, the similarities between the claimed invention and the prior art, and the level of ordinary skill in the art. I have been informed and understand that a prior art reference should be viewed as a whole.

15. I have been informed that, in considering whether an invention for a claimed combination would have been obvious, I may assess whether there are apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the market place, and/or the background knowledge possessed by a POSITA. I also understand that other

principles may be relied on in evaluating whether a claimed invention would have been obvious.

16. I have been informed that, in making a determination as to whether or not the claimed invention would have been obvious to a POSITA, one is to consider certain objective indicators of non-obviousness if they are present, such as: commercial success of product(s) practicing the claimed invention; long-felt but unsolved need; teaching away; unexpected results; copying; and praise by others in the field. I understand that, for such objective evidence to be relevant to the non-obviousness of claim, there must be a causal relationship (called a "nexus") between the claim and the evidence. I also understand that this nexus must be based on a novel element of the claim rather than something available in the prior art.

17. I have also been informed and understand that, when considering the obviousness of a patent claim, one should consider whether a reason or motivation existed for combining the elements of the references in the manner claimed, and that the prior art must create a reasonable expectation of success in producing the claimed subject matter.

V. SEMICONDUCTOR TRANSISTOR TECHNOLOGY PRIMER

18. The following is a brief primer of semiconductor transistors to establish a foundation of common terms and concepts that can be used in addressing the defects in the Petition. These terms and concepts focus on: (1) the basic components

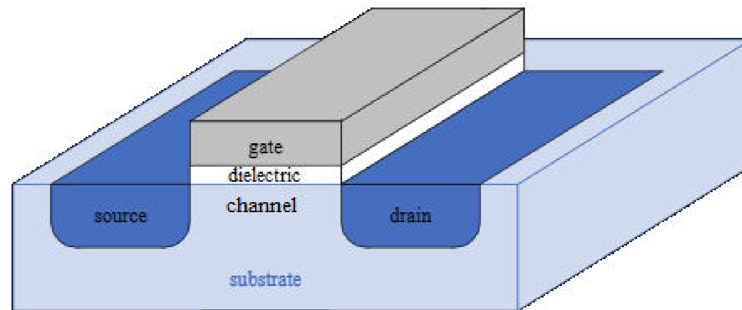
of transistors; (2) the difference between planar and three-dimensional (*e.g.*, fin) transistors; and (3) common process steps for creating transistors.

A. Basic Transistor Components

19. Today's semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical functions: switching (*i.e.*, turning access to electrical current on and off) and amplification (*i.e.*, increasing the amplitude of a signal while retaining its electrical characteristics). Ex. 2002 at 1-2. Where earlier tube devices used a vacuum tube to control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors. Ex. 2002 at 3.

20. One type of transistor typically used in an integrated circuit (or "chip") is a "field effect transistor," or FET. Materials used to build such transistors are divided into three categories based on their ability to conduct electrical current: conductors, dielectrics, and semiconductors. Ex. 2002 at 29-34. In a conductor (*e.g.*, a metal), electric current can flow freely. Ex. 2002 at 29. A dielectric (*e.g.*, silicon dioxide) is an insulative material at the opposite end of the conductivity spectrum and has a high resistance to the flow of current. Ex. 2002 at 30. Semiconductors (*e.g.*, silicon) fall between conductors and dielectrics and have some conducting and some resisting ability. Ex. 2002 at 31-34.

21. The simplified FET below illustrates how these materials may be used to create a semiconductor transistor device. As shown, the transistor is built on a semiconductor substrate and comprises a source, a drain, a gate, and a channel. *See*, *e.g.*, Ex. 2002 at 510-511. The source, drain and channel comprise semiconductor material, the gate comprises a conductor, and the gate and channel are separated by a thin dielectric layer.



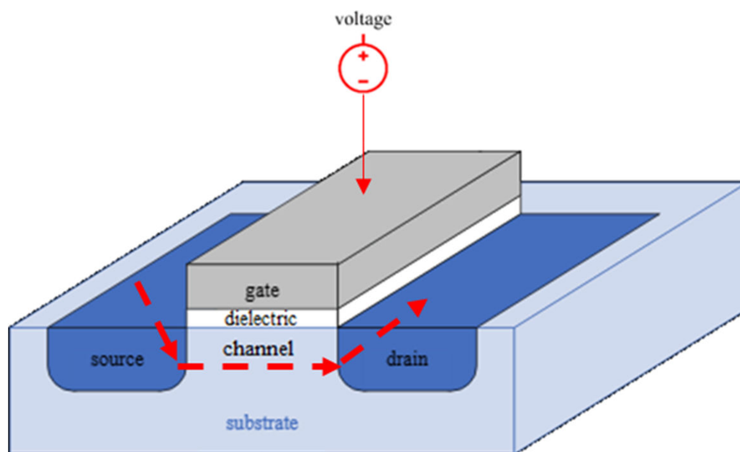
See, *e.g.*, Ex. 2002 at 510-511.

22. The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in holes (a positive, or p-type, region). Ex. 2002 at 26-28, 427-28. The channel is a region under the gate and between the source and drain, and is of the opposite type to that of the source and drain. In other words, if the source and drain are n-type regions, then the channel will be a p-type region (and vice versa). Ex. 2002 at 510-511.

23. The gate is a conductor (or semiconductor) located above the channel. In this simplified version of a FET, there is a dielectric between the channel and the gate. Ex. 2002 at 510-511. When a voltage is applied to the gate, the dielectric

prevents the "flow of charge" (current) between the gate and the channel, but the applied voltage results in the creation of a "field effect" in the channel. Ex. 2002 at 510-511. This "field effect" either builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). Ex. 2002 at 510-511.

24. As illustrated below, this field effect allows charge to flow from the source, through the channel, to the drain. Thus, selectively applying voltage to the gate switches the transistor on and off, starting and stopping drain-to-source or source-to-drain current.



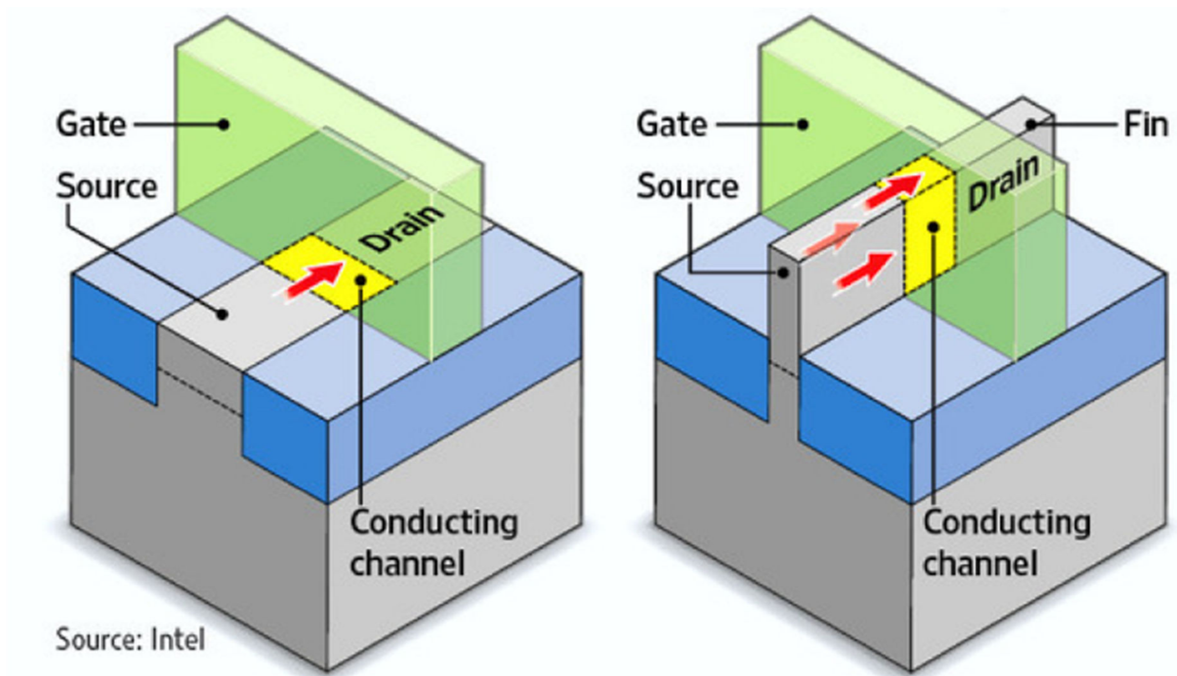
B. Planar vs. Three-Dimensional Transistors

25. Integrated circuit chips in modern computer systems are typically composed of millions and even billions of transistors. The first transistor prototypes in 1947 were several inches in size, and implementing even the simplest early computers required tens of thousands of gates or transistors. Given those numbers, and the correlation between an increased number of transistors and increased

computing power, the desire to shrink transistor sizes to fit more transistors on a chip has been consistent and widespread in industry. This desire led to the development of a new type of transistor, a "FinFET."

26. The simplified illustrative FET transistors illustrated in the previous section all feature a gate structure built on a flat semiconductor substrate; in other words, a "planar" FET. In the early 2010s, however, commercial gates evolved from such two-dimensional (2D) planar transistors to three-dimensional (3D) FinFET transistors.

27. In the below image, the figure on the left illustrates a 2D planar transistor built on a flat silicon substrate. In this traditional 2D planar transistor, the transistor forms a conducting channel in the silicon region under the gate.



28. In contrast, as illustrated above in the right figure, an exemplary 3D fin transistor design features a vertical semiconductor fin structure above the substrate that acts as a channel between the source and drain regions. In the resulting fin field effect transistor ("FinFET"), the source and drain regions are formed at opposing regions of the fin, and the gate is wrapped over the fin surrounding the fin on the top and two sides.

29. Thus, where a planar gate has only a horizontal dimension, the FinFET gate has both horizontal and vertical dimensions, thereby allowing a FinFET transistor to take up less surface area than a planar transistor. This alone means that more FinFET transistors may fit on an integrated circuit chip compared to that of the planar transistor. In addition, because FinFETs typically leak less current than planar FET transistors, FinFETs may be more tightly packed on an integrated circuit chip. This, too, increases the number of FinFET transistors that may fit onto a single chip.

C. Processes For Manufacturing Integrated Circuits And Transistors

1. The Four Stages Of Fabricating Integrated Circuits

30. The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging.

31. In the first stage, the semiconductor material itself is created. Ex. 2002 at 13. For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. Ex. 2002 at 13.

32. In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and it is then sliced into thin disks called "wafers." Ex. 2002 at 13-14. A wafer acts as a semiconductor substrate on and in which transistors may be formed.

33. The third stage is wafer fabrication, during which individual integrated circuits are formed in and on the wafer semiconductor substrate. Ex. 2002 at 14. Thousands of integrated circuits can be formed on the substrate of a single wafer. Ex. 2002 at 14.

34. In the packaging stage, the wafer is separated into individual chips. Ex. 2002 at 14-15.

2. The Wafer Fabrication Stage

35. The third manufacturing stage, wafer fabrication, is the one most relevant here, and it can take several thousand steps, during which transistors and other devices are formed in and on the wafer's substrate. Ex. 2002 at 14. These steps are generally performed using three categories of materials (conductors, semiconductors, and dielectrics) in four basic operations (layering, patterning, doping, and heat treatments). *See* Ex. 2002 at 29-31, 71. For purposes of

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understanding the Petition and its deficiencies, the two most important basic operations are layering and patterning.

36. **Layering** is the operation used to add thin layers to the semiconductor substrate. Ex. 2002 at 72. The layers may be conductors, semiconductors, or dielectrics; and they can have a variety of functions and be made in a variety of ways. Ex. 2002 at 72.

37. For example, one way of adding a layer of material is to deposit that material onto the semiconductor substrate. Another way of adding a layer of material is to grow the material on the semiconductor substrate. After an initial layer is added to the semiconductor substrate, additional layers may be added to the earlier layers using similar growth or deposition processes. To illustrate, the transistor structure shown below shows a number of layers that have been added to the wafer's semiconductor substrate, some deposited, some grown. Ex. 2002 at 72.

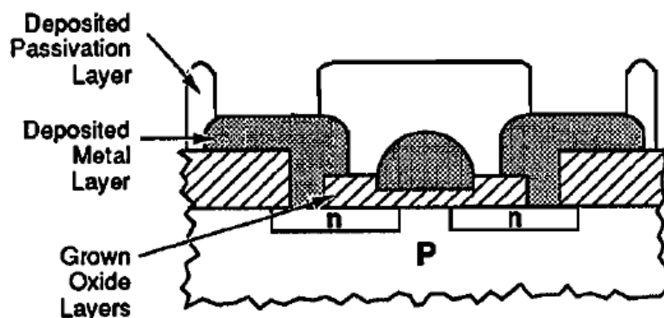


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

38. **Patterning** is the series of steps to remove (etch away) selected portions of the semiconductor substrate or one or more layers of materials that were added during one or more prior layering operations. Ex. 2002 at 72-73. This creates a pattern on the wafer surface. Ex. 2002 at 72-73.

39. The patterning may result in one or more holes in the layered material or one or more remaining islands of material. Ex. 2002 at 72-73. For example, the following figures illustrate the use of patterning to make (1) a hole in a previously formed layer: and (2) an island from a previously formed layer:

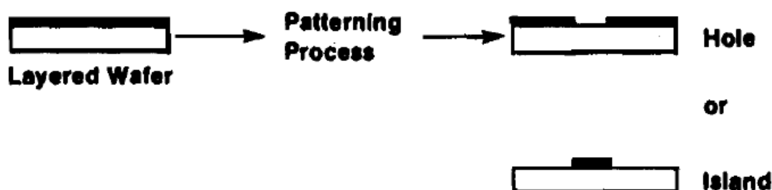


Figure 4.7 Patterning.

40. The repeated combination of layering and patterning in different sequences and variations is critical to the formation of transistors in and on the semiconductor wafer:

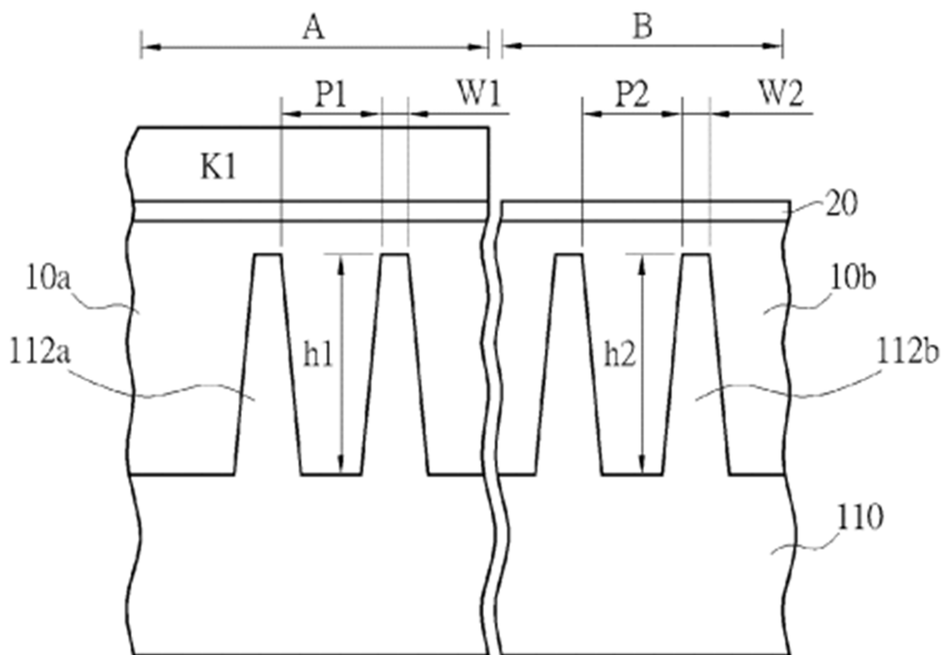
> These parts are created one layer at a time by the combination of putting a layer on the surface and removing a portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts.

Ex. 2002 at 73.

VI. THE CHALLENGED '510 PATENT

41. The '510 patent "relates generally to a fin-shaped structure and method thereof, and more specifically to a fin-shaped structure which has a ladder-shaped cross-sectional profile, and a method thereof." Ex. 1001, 1:7-10. Specifically, the patent states that the invention involves "cover[ing] a mask in a first area, and then remov[ing] an external surface of a top part of a second fin-shaped structure of a second area, so that the second fin-shaped structure is formed." *Id.*, 2:18-23. "Hence, fin-shaped structures of different heights and critical dimensions can be formed, and thus transistors for each area can achieve required electrical requirements." *Id.*, 2:24-26.

42. The patent describes an embodiment in which "two first fin-shaped structures 112a are formed in the first area A and two second fin-shaped structures 112b are formed in the second area B." *Id.*, 3:1-4. The above-described structure is illustrated in Figure 1:



Id., Fig. 1. In this embodiment:

> [T]he first fin-shaped structures 112a and the second fin-shaped structures 112b have the same structure. A height h1 of each of the first fin-shaped structures 112a is common to a height h2 of each of the second fin-shaped structures 112b; a width w1 of a top part of each of the first fin-shaped structures 112a is the same as a width w2 of a top part of each of second fin-shaped structures 112b; and a first distance p1 between a top part of each of the first fin-shaped structures 112a is the same as a distance p2 between a top part of each of the second fin-shaped structures 112b. Therefore, when a selective treatment process is performed on one single area or on a plurality

> of areas, symmetric structures in these areas will receive the same influence and uniform structures can be formed.

Id., 3:6-20.

43. Subsequently, "[a]s shown in FIG. 4, a treatment process Q2 is performed to modify an external surface R1 of a first top part 112b1 of each of the second fin-shaped structures 112b, thereby a modified part 120 covering the first top part 112b1 of each of the second fin-shaped structures 112b is formed." *Id.*, 4:53-57.

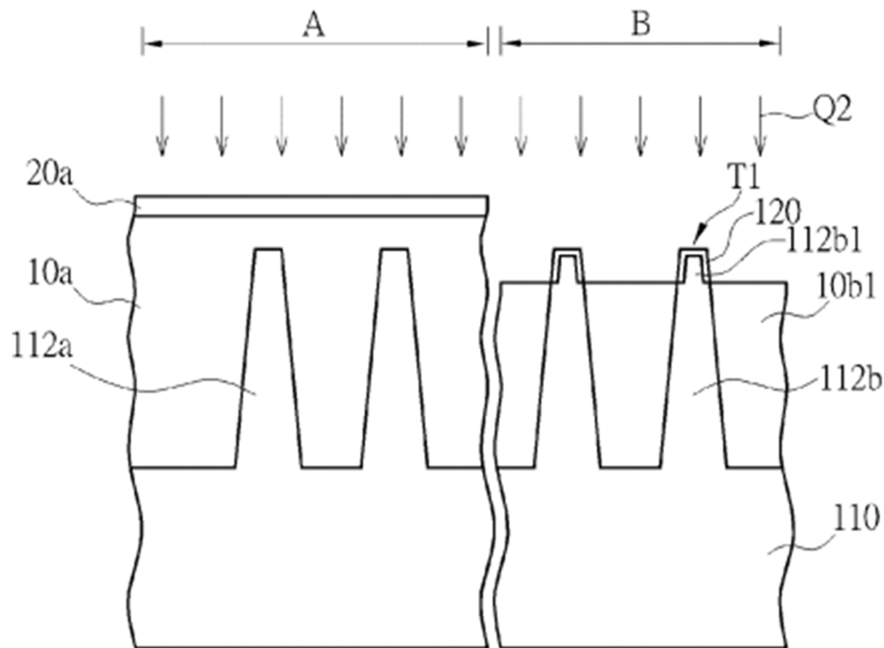


FIG. 4

Id., Fig. 4.

44. Then, "[a]fter the modified parts 120 are formed, the patterned mask 20a is removed, as shown in FIG. 5."

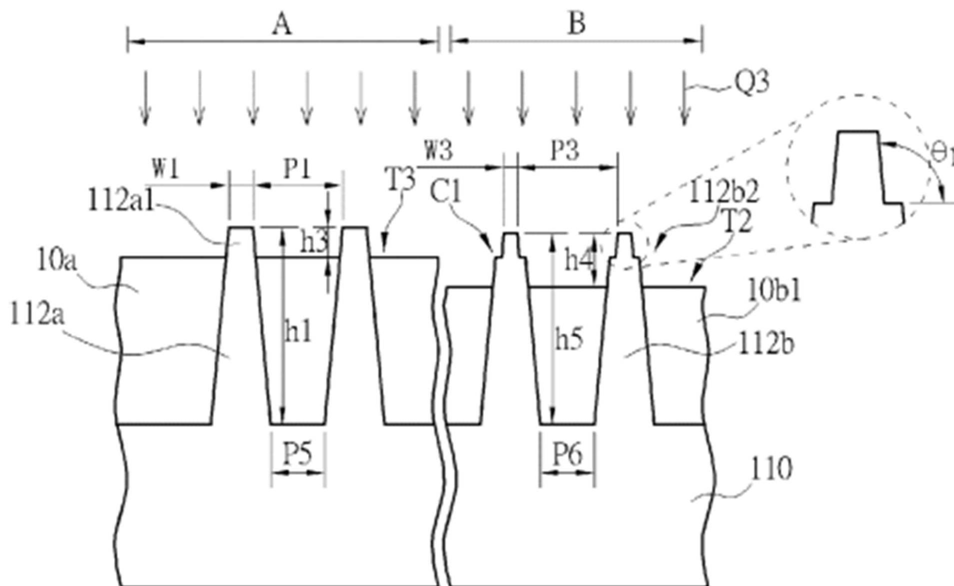


FIG. 5

Id., Fig. 5. As shown above in Figure 5, in the resulting structure, "[t]he first distance p1 between adjacent top corners of the first fin and the second fin of the first fin-shaped structures 112a is less than a second distance p3 between adjacent top corners of the third fin and the fourth fin of the second fin-shaped structures 112b while a third distance p5 between adjacent lower parts of the first fin and the second fin is the same as a fourth distance p6 between adjacent lower parts of the third fin and the fourth fin." *Id.*, 5:24-32.

45. The above-described innovative aspects of the invention are embodied in all challenged claims via independent claim 1, which recites:

1. A fin-shaped structure, comprising:

[1.a] a substrate having a plurality of first fin-shaped structures and a plurality second fin-shaped structures, and the first fin-shaped structures comprising a first fin and a second fin, the second fin-shaped structures comprising a third fin and a fourth fin,

[1.b] ***wherein a first distance between adjacent top corners of the first fin and the second fin of the first fin-shaped structures is less than a second distance between adjacent top corners of the third fin and the fourth fin of the second fin-shaped structures***

[1.c] ***while a third distance between adjacent lower parts of the first fin and the second fin is the same as a fourth distance between adjacent lower parts of the third fin and the fourth fin***; and

[1.d] wherein the adjacent top corners are directly opposite each other.

Ex. 1001, claim 1 (annotated to identify claim elements)

VII. THE PETITION FAILS TO ESTABLISH THE REQUIRED LIKELIHOOD OF SUCCESS

A. Grounds 1 and 2: Oh Does Not Disclose Or Render Obvious "A Third Distance Between Adjacent Lower Parts Of The First Fin And The Second Fin Is The Same As A Fourth Distance Between Adjacent Lower Parts Of The Third Fin And The Fourth Fin"

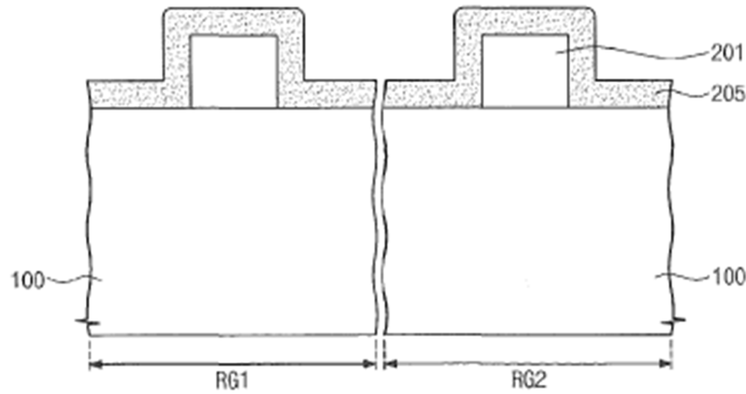
46. Claim Element [1.c] recites: "while a third distance between adjacent lower parts of the first fin and the second fin is the same as a fourth distance between adjacent lower parts of the third fin and the fourth fin." Oh does not disclose or render obvious this claim element.

47. The Petition alleges that Oh discloses or renders obvious [1.c] because "Oh discloses or renders obvious uniform spacing between fins when forming its fin-shaped structure." Pet., 19. But Oh never mentions the distances between adjacent fins, nor any comparison of distances between two sets of fins, nor such distances measured from the "adjacent lower parts" of the fin. *See generally* Ex. 1005.

48. The Petition alleges that Oh's Figures 2, 4, 6, and 14 show that Oh's initial fin formation process for both regions RG1 and RG2 are the same, so the distance between the two sets of fins are allegedly also the same. Pet., 19-21. But Oh never states that the two sets of fins are formed using identical processes. For example, with respect to Oh's Figure 2, the Petition alleges that "first mask patterns

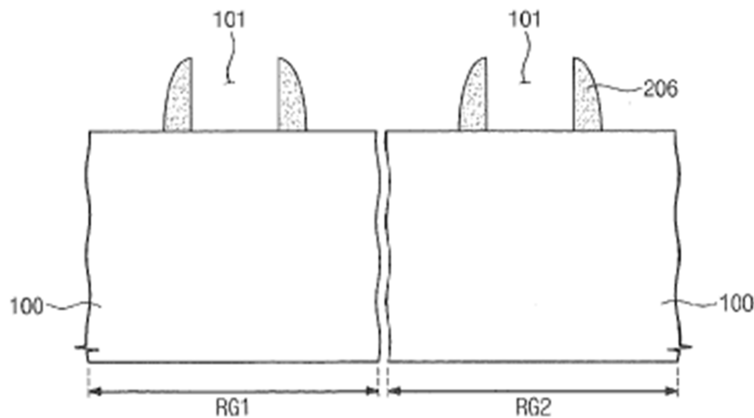
201 and a conformal second mask layer 205 are formed on a substrate 100." Pet., 19.

Fig. 2

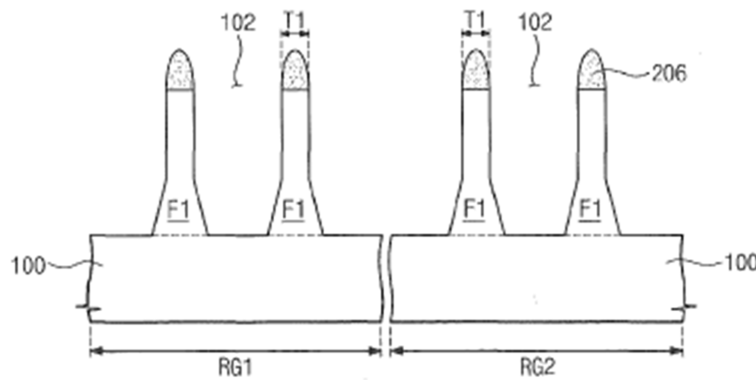


Ex. 1005, Fig. 2. Similarly, with respect to Oh's Figure 4, the Petition alleges that "second mask patterns 206 are spaced apart from one another in the first region RG1 and second region RG2 by first trenches 101." Pet., 19.

Fig. 4



Ex. 1005, Fig. 4. With respect to Oh's Figure 6, the Petition alleges that "an etching process using mask patterns 206 results in the formation of first fin portions F1 separated by second trenches 102." Pet., 20.



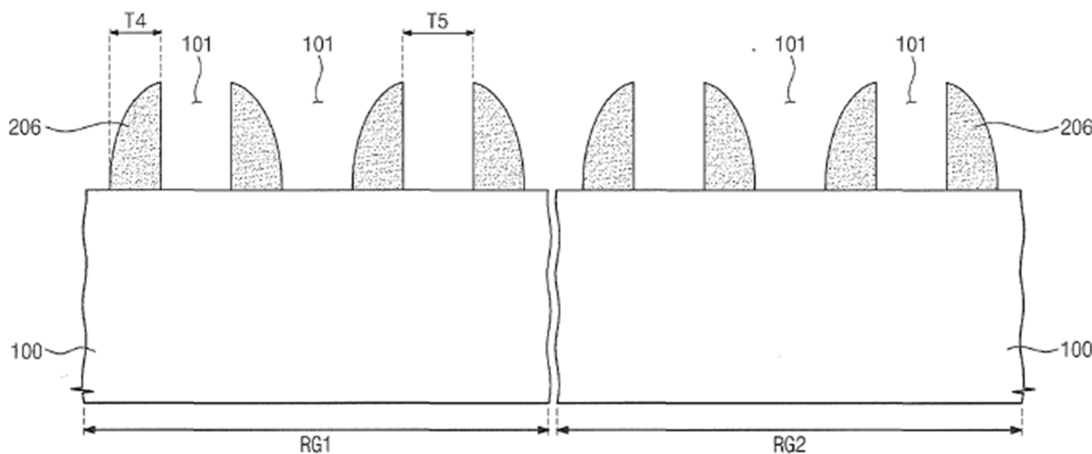
Ex. 1005, Fig. 6.

49. Based on the above-described figures, the Petition alleges that "[a]ccordingly, a POSA would have understood that Oh teaches that the distance between the first fin portions F1 in the first region RG1 and second region RG2 are identical, because it teaches that the two first mask patterns 201 in Figure 2 are identical, as was first trenches 101 in Figure 4 and second trenches 102 in Figure 6." Pet., 21. But Oh does not state that the mask pattern and mask layer on both regions in Figure 2, or the trenches in Figures 4 and 6, are the same. *See* Ex. 1005, ¶¶ [0047]-[0050].

50. Next, the Petition alleges that "when the same etching process is performed on exposed trenches having the same properties and size, then the resulting trenches will be the same." Pet., 21. But Oh never discloses that the same etching process is performed on both regions, nor that the trenches have the same properties and size.

51. Finally, the Petition alleges that "if Oh does not expressly disclose that the spacing/distance between the fins in Figure 14 is the same, a POSA would have found it obvious to apply the teachings from Figure 30 to render such a property obvious." Pet., 23. But Oh's Figure 30 also does not disclose that each of the trenches between fins has the same width.

Fig. 30



Ex. 1005, Fig. 30. In its description of Fig. 30, Oh only states that "[t]he fourth width T4 of the second mask pattern 206 may be different from the lower width T5

of the first trench 101." Ex. 1005, ¶ [0073]. That is, Oh only discloses that T4 is different than T5, not that each of the trenches all have the same width T5. Thus, Oh's Figure 30 also fails to disclose "a third distance between adjacent lower parts of the first fin and the second fin is the same as a fourth distance between adjacent lower parts of the third fin and the fourth fin."

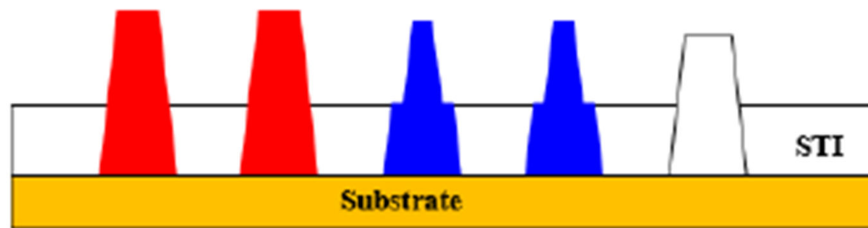
52. In short, the Petition fails to identify any disclosure in Oh from which a POSA could determine relative distances between adjacent fins in both regions. As such, Oh does not disclose or render obvious element [1.c].

B. Ground 3

53. Ground 3 fails because it is based on a wholly speculative combination of Wann and Lin; and the Petition fails to offer any rationale for why a POSA would combine Wann and Lin in the manner proposed by the Petition.

1. The Petition Offers No Motivation Or Basis For The Concocted "Wann-Lin five-fin FinFET structure"

54. The Petition alleges that because Wann briefly mentions a five-fin FinFET embodiment having "2 regular fins, 2 fins shaped a particular way, and 1 fin shaped a different way," a POSA would have been motivated to implement such an embodiment according to the illustration below.



EX1003, Illustration 8.

Pet., 51-52 (citing Ex. 1003, Illustration 8). This combination is wholly speculative, because Wann provides no details on this embodiment other than that it "may have 2 regular fins, 2 fins shaped a particular way, and 1 fin shaped in a different way." Ex. 1007, ¶ [0042]. Wann does not disclose any particular shapes or arrangements of the fins in this embodiment. *See id*.

55. The Petition argues that "[a] POSA would have understood that this fin permutation is obvious to try since it is merely one fin arrangement from a finite number of identified, predictable solutions, with a reasonable expectation of success." Pet., 51. This is incorrect—the number of fin arrangements and shapes is not finite, because fins can be shaped in an infinite number of ways. For example, Wann discloses numerous fin shapes, including diamond-shaped and oval-shaped fins:

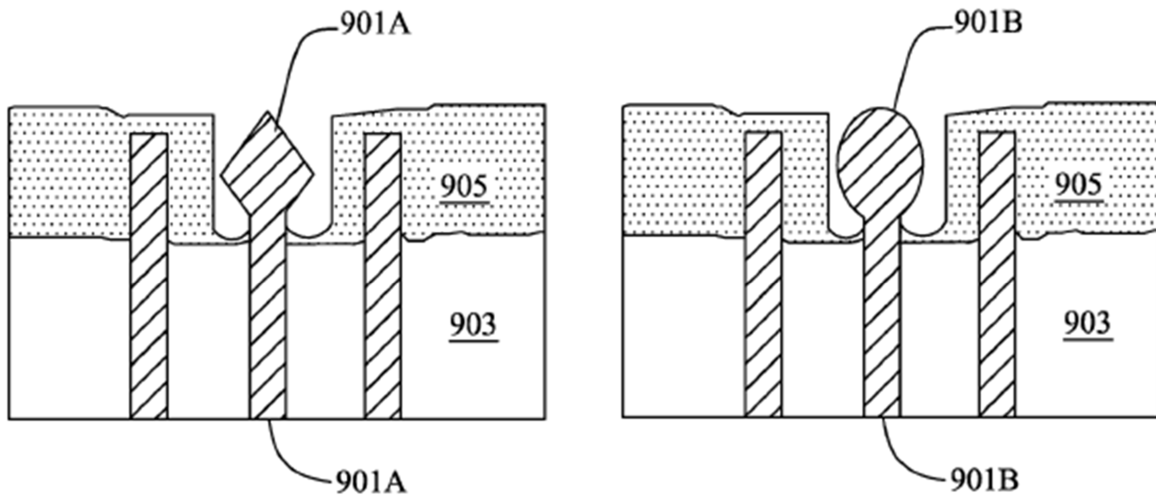


Figure 9A Figure 9B

Ex. 1008, Figs. 9A and 9B. The Petition offers no rationale for choosing the particular fin shape shown in "Illustration 8" over any other fin shape. *See* Pet., 51-56. Moreover, the Petition identifies no disclosure in Wann or Lin, or any other rationale, for why a POSA would have been motivated to arrange the fins in the order illustrated in Illustration 8—that is, the "2 regular fins adjacent to one another" and the "2 fins shaped a particular way adjacent to one another." Pet., 56. Every embodiment disclosed by Wann that includes fins of different shapes orients the fins such that the particularly-shaped fin is between two regular fins, rather than having two fins of the same shape adjacent to one another. See Ex. 1007, Figs. 4-10.

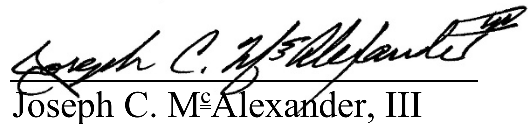
2. The Petition Offers No Motivation To Combine Wann and Lin In A Manner That Discloses Or Renders Obvious "A Third Distance Between Adjacent Lower Parts Of The First Fin And The Second Fin Is The Same As A Fourth Distance Between Adjacent Lower Parts Of The Third Fin And The Fourth Fin"

56. Similarly, the Petition fails to establish any motivation to combine Wann and Lin such that "a third distance between adjacent lower parts of the first fin and the second fin is the same as a fourth distance between adjacent lower parts of the third fin and the fourth fin," as required by element [1.c].

57. The Petition alleges that "a POSA would have reasonably expected to succeed in forming Wann's fin-shaped structures, where a distance between lower parts of adjacent regular fins is the same as a distance between lower parts of adjacent shaped fins" "because Lin's mandrel/spacer process can be used to form Wann's regular fins, in which one or more of the regular fins can be further shaped by Wann's fin-shaping process." Pet., 50. But even if this were true, it does not explain ***why*** a POSA would want to use Lin's mandrel/spacer process (which results in "substantially equal" spacing between fins) over any other process. The Petition alleges that "[a]dvantageously, Lin's mandrel/spacer process provides substantially uniform fins, in which 'the spacing and depth between the fins 50 are better controlled and may be substantially equal between all of the fins 50.'" Pet., 49 (citing Ex. 1008, ¶ [0062]). But this does not provide a motivation for why a POSA would

want uniform spacing in the first place. The Petition also alleges that "[a]n additional benefit of Lin's mandrel/spacer process is its mandrel removal process, which includes a 'wet etch process [that] is a lower cost and allows a higher throughput (Wafers per hour) than a dry etch process.'" Pet., 49 (citing Ex. 1008, ¶ [0063]). But such a mandrel removal process including a wet etch process could be performed regardless of whether the fins are uniformly spaced.

Dated: December 10, 2025



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