

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
Petitioner

v.

MARLIN SEMICONDUCTOR LIMITED,
Patent Owner

Case IPR2025-01484
U.S. Patent No. 9,786,510

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 9,786,510**

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EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 9,786,510 to Shen et al. (“’510 patent”)
1002	Prosecution History of U.S. Patent No. 9,786,510 (“’510 File History”)
1003	Declaration of Dr. Salahuddin
1004	Curriculum Vitae of Dr. Salahuddin
1005	U.S. Patent Application Publication No. 2013/0244392 A1 to Oh et al. (“Oh”)
1006	U.S. Patent Application Publication No. 2010/0276756 A1 to Rachmady et al. (“Rachmady”)
1007	U.S. Patent Application Publication No. 2013/0093026 A1 to Wann et al. (“Wann”)
1008	U.S. Patent Application Publication No. 2014/0256093 A1 to Lin et al. (“Lin”)
1009	Colinge et. al., <i>FinFETs and Other Multi-Gate Transistors</i> , 2008 (“Colinge”)
1010	Hu, C., “MOSFETs in ICs – Scaling, Leakage, and Other Topics,” Chapter 7 of <i>Modern Semiconductor Devices for Integrated Circuits</i> , 1st ed., 2009 (“Hu”)
1011	Choi et al., “A Spacer Patterning Technology for Nanoscale CMOS,” <i>IEEE Transactions on Electron Devices</i> , Vol. 49, No. 3, pp. 436-441, March 2002 (“Choi”)
1012	U.S. Patent Application Publication No. 2013/0277759 A1 to Chen et al. (“Chen”)
1013	U.S. Patent Application Publication No. 2016/0027895 A1 to Akarvardar et al. (“Akarvardar”)

Exhibit No.	Description
1014	U.S. Patent Application Publication No. 2012/0068264 A1 to Cheng et al. (“Cheng”)
1015	Chang et al., “Scaling of SOI FinFETs down to Fin Width of 4 nm for the 10 nm technology node,” <i>IEEE Transactions on Electron Devices</i> , 2011 Symposium on VLSI Technology - Digest of Technical Papers, Kyoto, Japan, 2011, pp. 12-13 (“Chang”)
1016	U.S. Patent Application Publication No. 2013/0200483 A1 to Tung (“Tung”)
1017	U.S. Patent Application Publication No. 2013/0149826 A1 to Lee et al. (“Lee”)
1018	U.S. Patent Application Publication No. 2008/0303095 A1 to Xiong et al. (“Xiong”)
1019	Guo et al., “FinFET-Based SRAM Design,” ISLPED ’05, Proceedings of the 2005 International Symposium on Low Power Electronics and Design, San Diego, CA, USA, August 2005, pp. 2-7 (“Guo”)

I. RELIEF REQUESTED

Applying the following grounds, Taiwan Semiconductor Manufacturing Company Ltd. (“Petitioner”) requests *inter partes* review of claims 1-6 of U.S. Patent No. 9,786,510 to Shen et al. (“the ’510 patent”; EX1001) and cancellation of claims 1-6:

Ground	Claims Challenged	35 U.S.C. §	Reference(s)
1	1, 2, and 6	§ 103	Oh
2	3-5	§ 103	Oh in view of Rachmady
3	1-6	§ 103	Wann in view of Lin

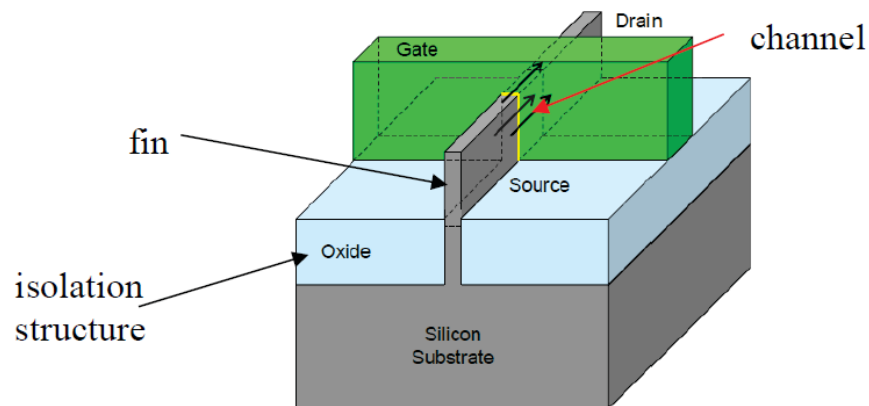
II. STATE OF THE ART

The ’510 patent discloses “fin-shaped structures having ladder-shaped cross-sectional profile parts in some areas, so that fin-shaped structures of different heights and critical dimensions (CD) can be formed, in order to form transistors for each area that meet each area’s specific electrical demands.” EX1001, 1:34-40. As demonstrated by this Petition—which is supported by the Declaration of Dr. Salahuddin (EX1003)—the claimed fin-shaped structures and arrangements were known before the ’510 patent.

As discussed below, the shaping of fins in FinFETs was well known before the ’510 patent.

A. FinFET Characteristics

At the time of the '510 patent, FinFET technology was well known in the semiconductor art. EX1009, 8-17; EX1010, 280-282; EX1003, ¶42. The term “FinFET” refers to a three-dimensional, non-planar field-effect transistor (FET). EX1009, 11; EX1010, 280-282; EX1003, ¶42. A representative FinFET is shown below. EX1003, ¶42.



EX1003, FIG. 1.

The FinFET includes a semiconductor structure (commonly called a “fin”) protruding from a substrate (e.g., a silicon substrate). EX1009, 66; EX1010, 282; EX1003, ¶43. The FinFET also includes a gate structure surrounding the fin and source/drain regions on opposite sides of the gate structure. EX1003, ¶43. A top portion of the fin under the gate structure acts as a channel of the FinFET for current flow between the source and drain regions. EX1003, ¶43. The isolation structure on the substrate surrounding a bottom portion of the fin electrically isolates the fin from adjacent fins. EX1003, ¶43.

B. Fin Shaping Techniques

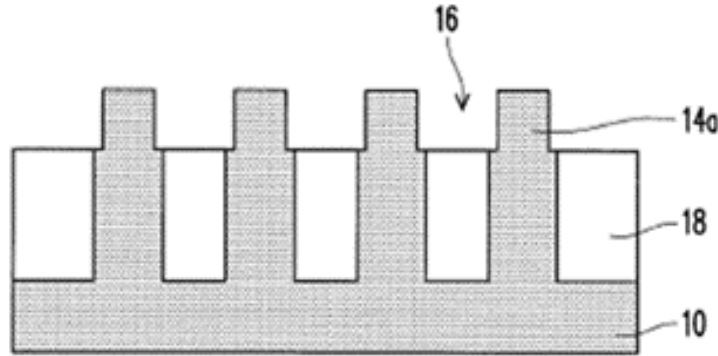
It was well known before the '510 patent that different fin shapes can affect the electrical characteristics of FinFETs. EX1003, ¶¶50-54. For example, FinFETs with fins having different widths provide different threshold voltages. EX1005, ¶[0053]; EX1003, ¶50. In another example, FinFETs with fins having different heights provide different drive currents. EX1017, ¶¶[0003], [0024]; EX1003, ¶50. Accordingly, depending on circuit design requirements, fin width and height can be adjusted to achieve desired FinFET electrical characteristics. EX1003, ¶50.

Before the '510 patent, Tung described a method of adjusting fin widths. EX1016, Abstract; EX1003, ¶51. The method included forming a hard mask material layer on a substrate, patterning the hard mask material layer to form a first hard mask layer, and removing a portion of the substrate to form two trenches and a fin between the trenches. EX1016, ¶[0008]. Afterwards, an insulating layer is formed in each trench to expose an upper portion of the fin, and the upper portion of the fin is trimmed so that the trimmed upper portion is narrower than a lower portion of the fin. EX1016, ¶[0008].

For example, as shown in Figure 1E below, the trimmed upper portion of each fin 14a is narrower than the fin's lower portion. EX1016, ¶[0039]. In addition to setting a threshold voltage of the subsequently-formed FinFET, the trimmed upper portion of each fin 14a provides a fin structure to prevent epitaxial layers

around neighboring fin structures from undesirably contacting one another.

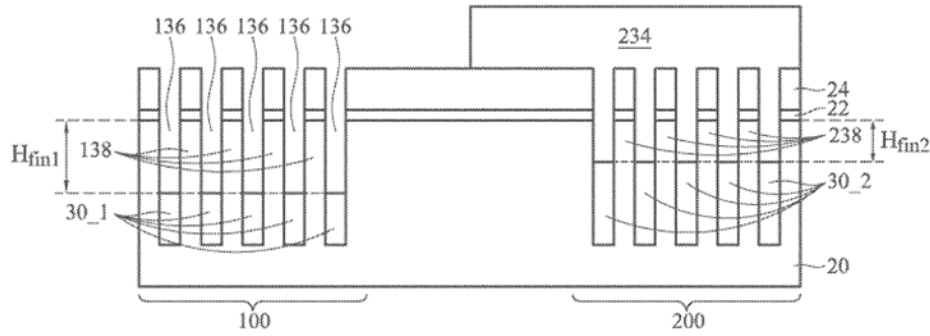
EX1016, ¶[0007]; EX1003, ¶¶52-53.



EX1016, FIG. 1E.

Also before the '510 patent, Lee described a method of forming fins with different heights. EX1017, ¶[0012]; EX1003, ¶54. Lee's method included forming shallow trench isolation (STI) regions in a substrate and recessing top surfaces of the STI regions in different device areas to different depths. EX1017, ¶¶[0016]-[0019]; EX1003, ¶54. As a result, portions of the substrate between the recesses became fins with different heights. EX1017, ¶¶[0017]-[0018]; EX1003, ¶54.

For example, as shown in Figure 5 below, fins 138 in device region 100 have a fin height H_{fin1} greater than a fin height H_{fin2} of fins 238 in device region 200. EX1003, ¶54; EX1017, ¶¶[0017]-[0018]. Lee explained that “[w]ith the FinFETs in different device regions having different fin heights, it is easier to tune the performance of devices in different device regions.” EX1017, ¶[0024].



EX1017, FIG. 5.

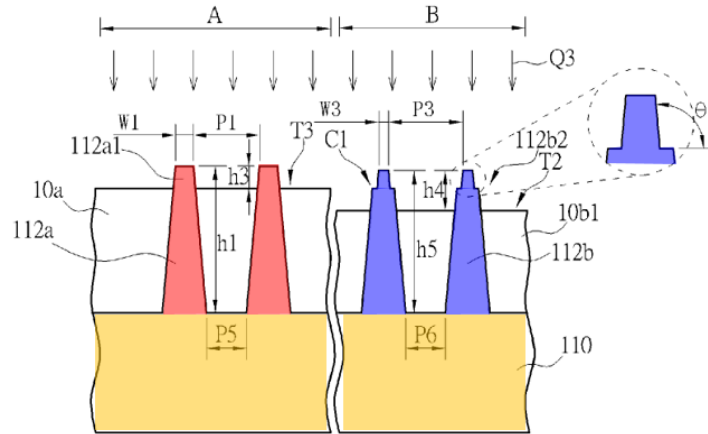
III. THE '510 PATENT

A. Overview of the '510 Patent

The '510 patent describes and claims a substrate having first fin-shaped structures (including a first fin and a second fin) and second fin-shaped structures (including a third fin and a fourth fin). The first and second fin-shaped structures are formed such that a distance between directly opposite top corners of adjacent first fin-shaped structures is less than a distance between directly opposite top corners of adjacent second fin-shaped structures, while a distance between lower parts of adjacent first fin-shaped structures is the same as a distance between lower parts of adjacent second fin-shaped structures. EX1001, 1:34-40. Figures 5 and 8 show two embodiments of the '510 patent's fin-shaped structures. EX1001, 2:43-48; EX1003, ¶¶28-29.

Figure 5 (below) shows the first embodiment in which **first fin-shaped structures 112a** (red) and **second fin-shaped structures 112b** (blue) are formed on a **substrate 110** (orange). EX1001, 4:65-5:12; EX1003, ¶¶30-31. Each of the

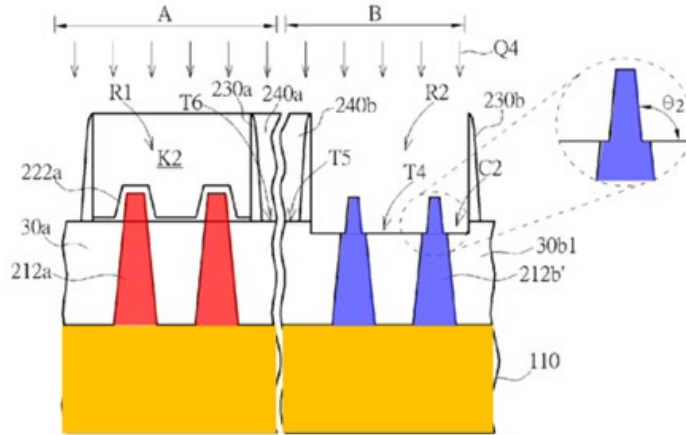
second fin-shaped structures 112b has a “ladder-shaped” cross-sectional profile part C1, where “[t]he ladder-shaped cross-sectional profile part C1 has a bending angle θ_1 , which is preferably larger than or equal to 90° .” EX1001, 5:13-18. In this embodiment, “[t]he ladder-shaped cross-sectional profile part C1 of each of the **second fin-shaped structures 112b** is higher than a top surface T2 of the isolation structure 10b1.” EX1001, 5:32-44. The ’510 patent also states that “[t]he width w_1 of the top part of each of the **first fin-shaped structures 112a** ... is larger than a width w_3 of a top part of each of the **second fin-shaped structures 112b**.” EX1001, 5:20-24. The ’510 patent further states that “[t]he first distance p_1 between adjacent top corners of the first fin and the second fin of the **first fin-shaped structures 112a** is less than a second distance P_3 between adjacent top corners of the third fin and the fourth fin of the **second fin-shaped structures 112b**, while a third distance P_5 between adjacent lower parts of the first fin and the second fin is the same as a fourth distance P_6 between adjacent lower parts of the third fin and the fourth fin.” EX1001, 5:24-32.



EX1001, FIG. 5 (annotated).

Figure 8 (below) shows a second embodiment in which **first fin-shaped structures 212a** (red) and **second fin-shaped structures 212b'** (blue) are formed on **substrate 110** (orange). EX1001, 5:62-6:5; EX1003, ¶32. The '510 patent states that “a removing process Q4 [is] performed to remove an external surface S1 of a top part of each of the second fin-shaped structures 212b ... to form **second fin-shaped structures 212b'** having ladder-shaped cross-sectional profile parts C2, wherein the ladder-shaped cross-sectional profile parts C2 have a bending angle θ_2 , and the bending angle θ_2 is preferably larger than or equal to 90° .” EX1001, 7:14-21. The '510 patent also states that “[a]n isolation structure 30b1 is formed, and a top surface T4 of the isolation structure 30b1 at the bottom of the recess R2 is lower than a top surface T5 of isolation structure 30b1 beside the recess R2, and even lower than a top surface T6 of the isolation structure 30a in the first area A,

depending upon the etchants of the removing process Q4 and a desired formed structure.” EX1001, 7:25-32.



EX1001, FIG. 8 (annotated).

B. Level of Ordinary Skill in the Art

A person of ordinary skill in the art (“POSA”) would have a Master’s degree in electrical engineering, physics, chemistry, materials science, or a related field, and at least three years of work experience in semiconductor design and manufacturing, including FinFETs. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education. EX1003, ¶¶36-38.

C. Claim Construction

In an *inter partes* review, claims are “construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b). All claim terms must be given their ordinary and customary meaning as understood by a POSA at the time of the

invention, in light of the specification and the prosecution history of the patent. *Id.*

Solely for the purposes of this Petition, Petitioner submits that all claim terms should receive their plain and ordinary meaning in the context of the '510 patent specification. EX1003, ¶40.

IV. OVERVIEW OF THE APPLIED REFERENCES

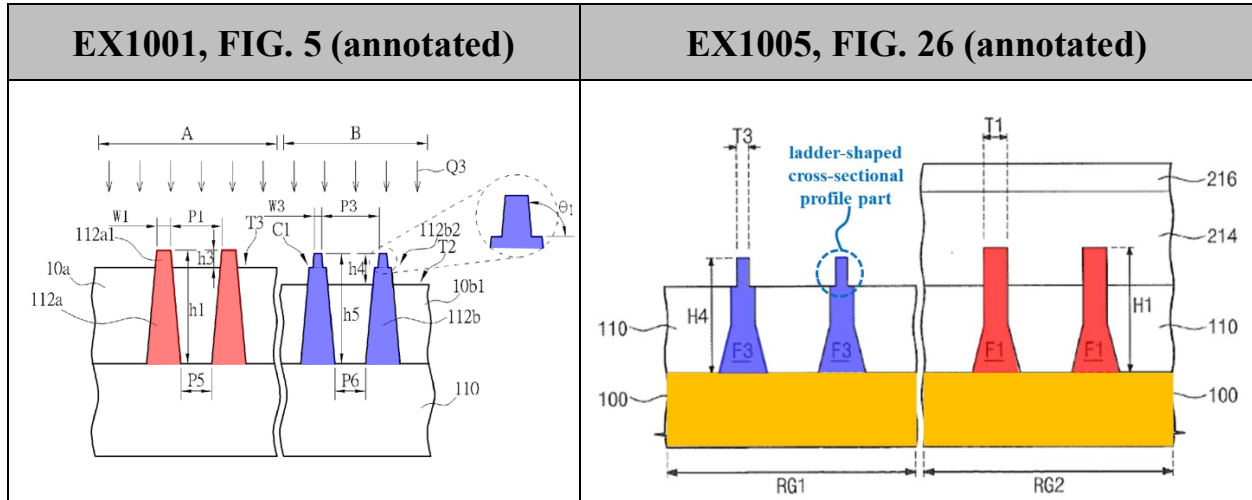
The '510 patent's earliest possible priority date is September 9, 2014. EX1001, (30). Without conceding that this is the correct priority date, all references relied upon herein are prior art as of September 9, 2014.

A. Oh

Oh (EX1005) was filed in the United States on February 28, 2013 and published on September 19, 2013. Oh claims priority to Korean Patent Appl. No. 10-2012-0027735, which was filed on March 19, 2012. Therefore, Oh is prior art at least under 35 U.S.C. § 102(a)(1) based on its U.S. publication date and under 35 U.S.C. § 102(a)(2) based on its U.S. and Korean filing dates.

Oh teaches the same fin-shaped structure described in the '510 patent. EX1003, ¶¶55-57. The fin-shaped structures from Oh and the '510 patent are shown below, which both have a **substrate** (orange; 100 and 110) with **first fin-shaped structures** (red; first fin portions F1 and 112a) and **second fin-shaped structures** (blue; third fin portions F3 and 112b). EX1003, ¶¶56-57. Similar to the '510 patent's two adjacent **first fin-shaped structures 112a** (red) in a first area A

and two adjacent **second fin-shaped structures 112b** (blue) in a second area B, Oh has two adjacent **first fin portions F1** (red) in a second region RG2 and two adjacent **third fin portions F3** (blue) in a first region RG1, respectively. EX1003, ¶¶56-57.

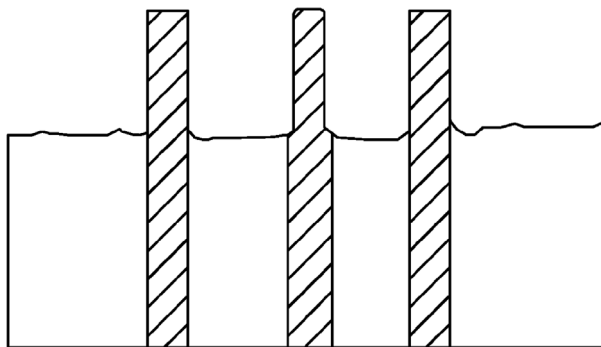


Also, similar to the '510 patent's ladder-shaped cross-sectional profile parts of **second fin-shaped structures 112b** (blue; shown in dashed line inset in Figure 5 above), Oh's **third fin portions F3** (blue) are also shaped to include ladder-shaped cross-sectional profile parts, as shown in Figure 26 above. Compare EX1005, ¶[0070], with EX1001, 5:13-44; EX1003, ¶58. The '510 patent states that the bending angle θ_1 in its ladder-shaped cross-sectional profile part can be larger than or equal to 90° , which is similar to the 90° bending angle in Oh's ladder-shaped cross-sectional profile part. Compare EX1005, ¶[0070], with EX1001, 5:16-18; EX1003, ¶58.

B. Wann

Wann (EX1007) was filed on October 14, 2011 and published on April 18, 2013. Therefore, Wann is prior art at least under 35 U.S.C. § 102(a)(1).

Wann is directed to a selective fin-shaping process to allow individual fin width and fin height control. EX1007, ¶¶0019]. An example of Wann’s fin-shaped structure is shown in a three-fin FinFET of Figure 6B below. EX1003, ¶¶63-66. Figure 6B shows a FinFET structure with 3 fins, where 2 fins have a regular shape (outer fins) and 1 fin is shaped (middle fin). EX1007, ¶¶0035]; EX1003, ¶66.



EX1007, FIG. 6B.

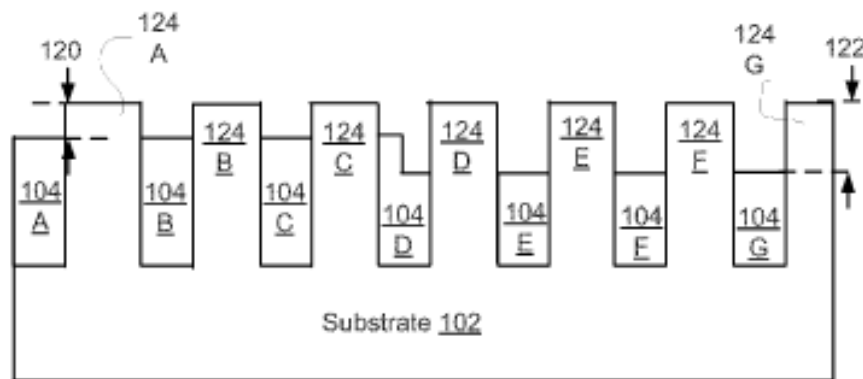
But Wann’s fin-shaping process is not limited to three-fin FinFET structures. EX1003, ¶67. In fact, Wann states that “[i]n reality a FinFET may have any number of fins from 1 to several or even hundreds.” EX1007, ¶¶0041]. With regard to fin arrangement, Wann states that “[t]he apparatus may include many FinFETs of different sizes having different number of fins,” where “[s]ome FinFETs may have shaped fins and some FinFETs may not.” EX1007, ¶¶0042]. For example,

Wann discloses “a five-fin FinFET [that] may have 2 regular fins, 2 fins shaped a particular way, and 1 fin shaped a different way.” EX1007, ¶[0042].

C. Rachmady

Rachmady (EX1006) was filed on July 15, 2010 and published on November 4, 2010. Therefore, Rachmady is prior art at least under 35 U.S.C. § 102(a)(1).

Rachmady discloses a selective fin height process to adjust drive current in FinFETs. EX1006, Abstract; EX1003, ¶¶60-61. Referring to Figure 1 below, Rachmady discloses that “[s]uch an ability to have fins 124 of different height allows multi-gate transistors to be made on the fins 124 with different desired properties.” EX1006, ¶[0022]. Using a selective etching and mask process, Rachmady discloses removing portions of isolation regions 104 while keeping adjacent fin portions intact. EX1006, ¶[0029]; EX1003, ¶¶61-62.

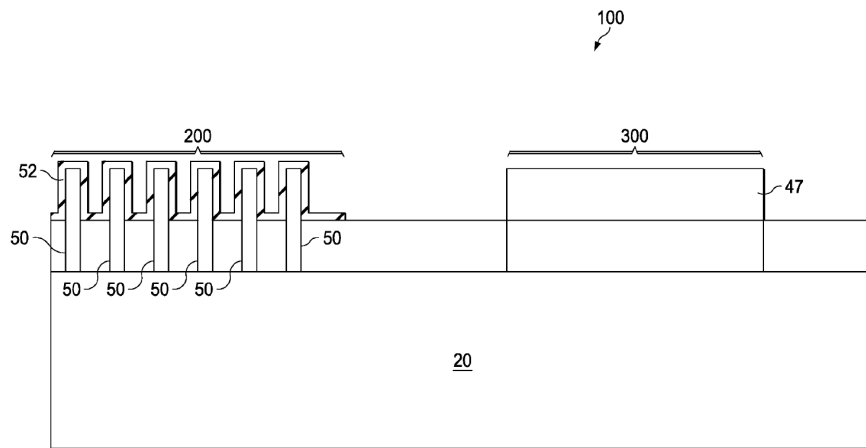


EX1006, FIG. 1.

D. Lin

Lin (EX1008) was filed on March 14, 2013 and published on September 11, 2014. Therefore, Lin is prior art at least under 35 U.S.C. § 102(a)(2).

Lin discloses a mandrel/spacer process that forms fins with uniform dimensions and uniform spacing from one another. EX1008, ¶¶[0062]; EX1003, ¶¶68-69. Referring to Figure 15 below, Lin states that its mandrel/spacer process “the spacing and depth between the fins 50 are better controlled and may be substantially equal between all of the fins 50.” EX1008, ¶[0062]. As a result, a POSA would have understood that a distance between adjacent fins 50 is the same among all fins 50. EX1003, ¶70.



EX1008, FIG. 15.

V. GROUNDS OF UNPATENTABILITY

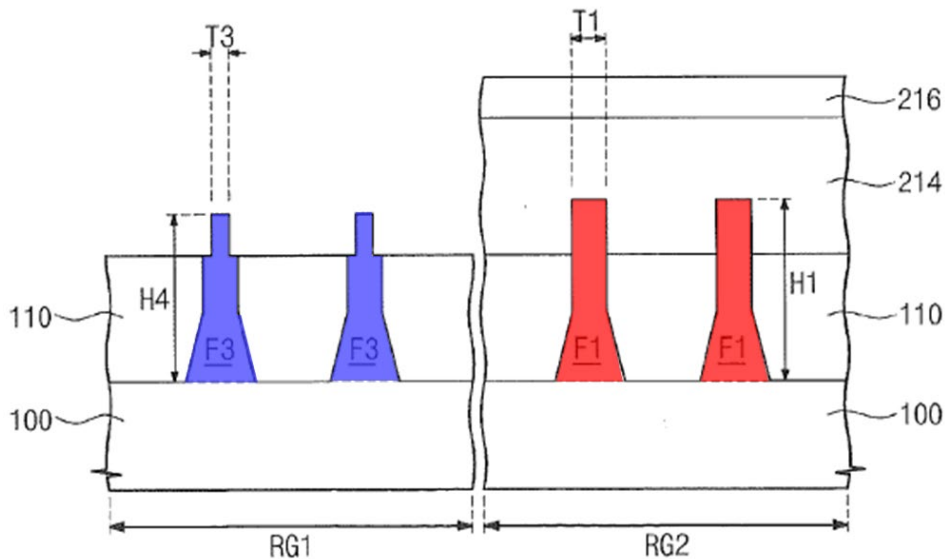
Claims 1-6 of the '510 patent are unpatentable for at least the reasons below.

A. Ground 1: Oh renders obvious claims 1, 2, and 6.

1. Independent Claim 1

a. [1.P]: A fin-shaped structure, comprising:

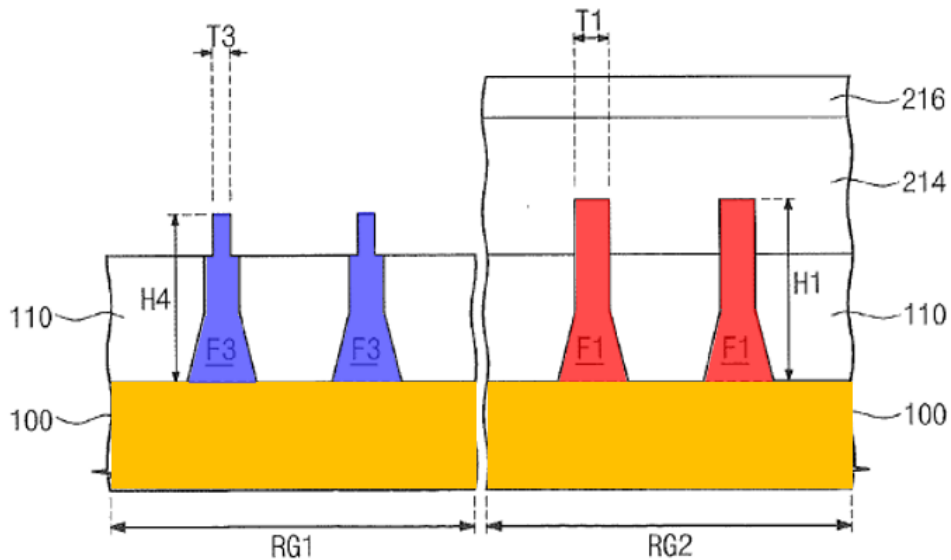
Oh discloses the preamble. EX1003, ¶¶72-74. Oh “relate[s] to field effect transistors, and in particular, to methods of fabricating fin field effect transistors,” where “some of the field effect transistors are formed to include fin portions having different widths from each other.” EX1005, ¶¶[0002], [0004]. An example of Oh’s “*fin-shaped structure*” is shown in Figure 26 below—with **first fin portions F1** (red) and **third fin portions F3** (blue). EX1005, ¶[0070]; EX1003, ¶¶72-73.



EX1005, FIG. 26 (annotated).

- b. [1.a]: a substrate having a plurality of first fin-shaped structures and a plurality [of] second fin-shaped structures, and the first fin-shaped structures comprising a first fin and a second fin, the second fin-shaped structures comprising a third fin and a fourth fin,

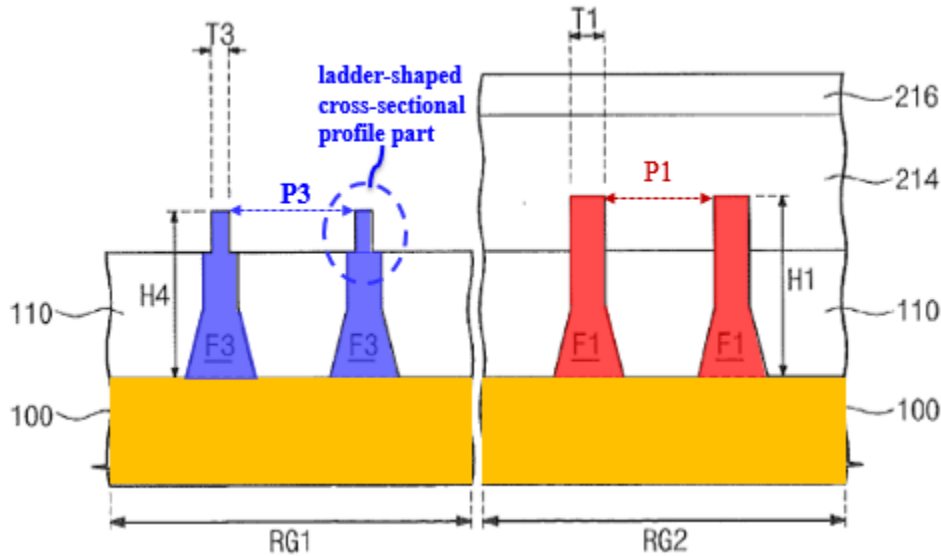
Oh discloses this limitation. EX1003, ¶¶75-80. Referring to Oh's Figure 26 below, a **substrate 100** ("substrate") has **first fin portions F1** (red; "a plurality of first fin-shaped structures") and **third fin portions F3** (blue; "a plurality [of] second fin-shaped structures"). **Substrate 100** (orange) includes a first region RG1 with **third fin portions F3** (blue) thereon and a second region RG2 with **first fin portions F1** (red). EX1005, ¶[0047]; EX1003, ¶75. As shown in Oh's Figure 26, **first fin portions F1** (red) include two fins ("a first fin and a second fin") and **third fin portions F3** (blue) include two fins ("a third fin and a fourth fin"). EX1003, ¶75.



EX1005, FIG. 26 (annotated).

- c. [1.b]: wherein a first distance between adjacent top corners of the first fin and the second fin of the first fin-shaped structures is less than a second distance between adjacent top corners of the third fin and the fourth fin of the second fin-shaped structures

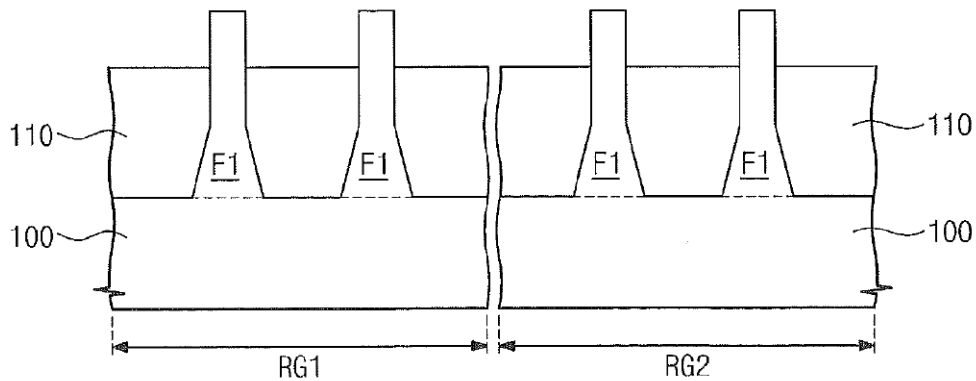
Oh discloses or renders obvious this limitation. EX1003, ¶¶81-85. Referring to Oh's Figure 26 below, a POSA would have understood that a **distance P1** (red; "a first distance") between adjacent top corners of the two fins in **first fin portions F1** (red; "the first fin and the second fin of the first fin-shaped structures") is less than a **distance P3** (blue; "a second distance") between adjacent top corners of the two fins in **third fin portions F3** (blue; "the third fin and the fourth fin of the second fin-shaped structures"). EX1003, ¶81.



EX1005, FIG. 26 (annotated).

The **first distance P1** (red) is shorter than the **second distance P3** (blue) due to how the fins are formed using the Oh's fin-shaping process. EX1003, ¶82.

Initially, the fins in both first region RG1 and second region RG2 are formed as shown in Oh's Figure 14 below (a precursor structure to Figure 26). EX1005, ¶¶[0059], [0069]; EX1003, ¶82. First fin portions F1 are the same and, as described in Section V.A.1.d below, the spacing (i.e., distance) between adjacent first fin portions F1 is also the same or it would have been obvious to make it so. EX1003, ¶82.



EX1005, FIG. 14.

After forming the first fin portions F1 in Oh's Figure 14, third fin portions F3 in first region RG1 are formed by etching upper parts of the two fins in the first region RG1. EX1005, ¶[0070]; EX1003, ¶83. Referring to Oh's Figure 26 above, while the second region RG2 is covered with an etching mask pattern 214 and a fourth mask pattern 216, Oh explains that the "upper sidewalls of the first fin portions F1 [in the first region RG1] with the first width T1 may be etched to form the third fin portions F3, whose upper portions have the third width T3," where

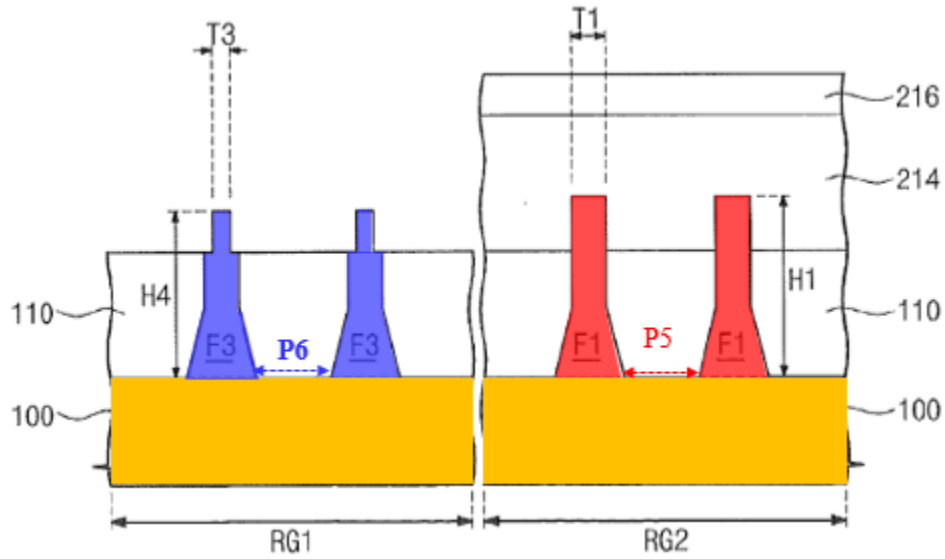
“[t]he third width T3 may be smaller than the first width T1.” EX1005, ¶¶ [0069]-[0070].

Because Oh’s fin-shaping process affects the upper parts of fins where an upper part width of a shaped fin (e.g., width T3) is less than an upper part width of a non-shaped fin (e.g., width T1), a POSA would have understood that Oh’s fin-shaping process for forming **third fin portions F3** (blue) results in a **distance P1** (red) being less than **distance P3** (blue). EX1003, ¶84.

- d. **[1.c]: while a third distance between adjacent lower parts of the first fin and the second fin is the same as a fourth distance between adjacent lower parts of the third fin and the fourth fin;**

Oh discloses or renders obvious this limitation. EX1003, ¶¶86-101.

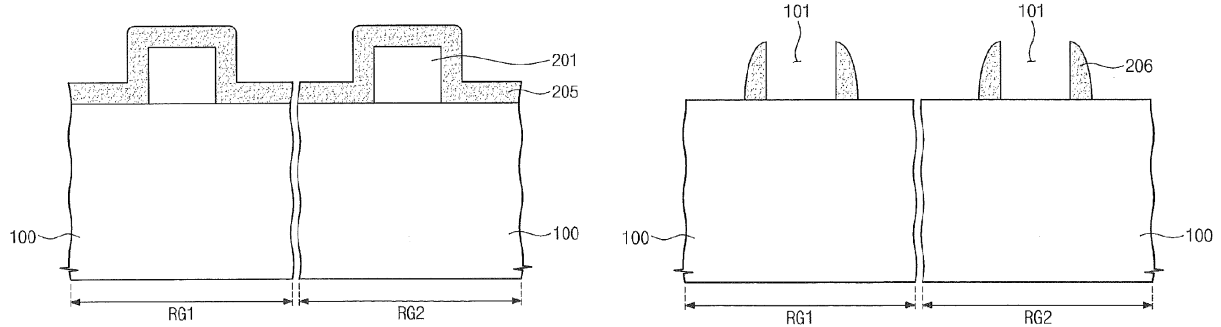
Referring to Oh’s Figure 26 below, a POSA would have understood that a **distance P5** (red; “*a third distance*”) between adjacent lower parts of the two fins in **first fin portions F1** (red; “*the first fin and the second fin*”) is the same as a **distance P6** (blue; “*a fourth distance*”) between adjacent lower parts of the two fins in **third fin portions F3** (blue; “*the third fin and the fourth fin*”). EX1003, ¶86.



EX1005, FIG. 26 (annotated).

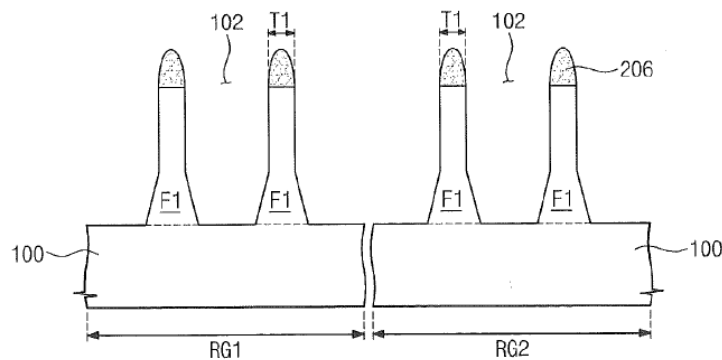
Oh discloses or renders obvious uniform spacing between fins when forming its fin-shaped structure. EX1003, ¶87. Oh's Figures 2, 4, 6, and 14—all precursor structures to Oh's Figure 26—show portions of Oh's initial fin formation process. EX1003, ¶87.

In Oh's Figure 2 below, first mask patterns 201 and a conformal second mask layer 205 are formed on a substrate 100. EX1005, ¶[0048]; EX1003, ¶88. After an etching process, referring to Oh's Figure 4 below, second mask patterns 206 are spaced apart from one another in the first region RG1 and second region RG2 by first trenches 101. EX1005, ¶[0049]; EX1003, ¶89.



EX1005, FIGS. 2 (left) and 4 (right).

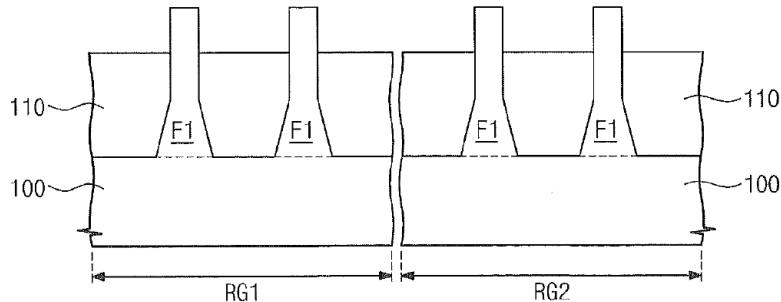
Following this step, an etching process using mask patterns 206 results in the formation of first fin portions F1 separated by second trenches 102, as shown in Oh's Figure 6 below. EX1005, ¶[0050]; EX1003, ¶90. The structure in Oh's Figure 6 is a precursor to the structure in Oh's Figure 14. EX1005, ¶[0059] ("Referring to FIGS. 13 and 14 . . . the first fin portions F1 may be formed by the method described with reference to FIGS. 1 through 6.")



EX1005, FIG. 6.

Thereafter, as shown in Oh's Figure 14 below, device isolation layers 110 are formed in second trenches 102 to cover lower parts of first fin portions F1. EX1001, ¶[0059]; EX1003, ¶91. A POSA would have understood that, based on Oh's teachings, the resulting distance between the first fin portions F1 in the first

region RG1 and between the first fin portions F1 in the second region RG2 is the same. EX1003, ¶91.

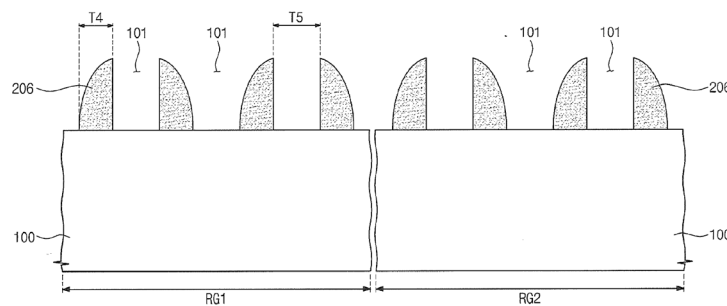


EX1005, FIG. 14.

As shown above for Oh's Figures 2, 4, and 6, a direct path exists from first mask patterns 201 (Figure 2, ¶[0048]) to first trenches 101 (Figure 4, ¶[0049]) to second trenches 102 (Figure 6, ¶[0050]), to device isolation layers 110 in Figure 14. EX1003 ¶92. Oh discloses that its "use of similar or identical reference numbers in the various drawings is intended to **indicate the presence of a similar or identical element** or feature." EX1005, ¶[0038] (emphasis added).

Accordingly, a POSA would have understood that Oh teaches that the distance between the first fin portions F1 in the first region RG1 and second region RG2 are identical, because it teaches that the two first mask patterns 201 in Figure 2 are identical, as was first trenches 101 in Figure 4 and second trenches 102 in Figure 6. EX1003 ¶92. As Dr. Salahuddin explains, when the same etching process is performed on exposed trenches having the same properties and size, then the resulting trenches will be the same. EX1003 ¶92.

Oh also renders obvious uniform spacing between fins. For example, Oh's Figure 30 below applies the same initial fin formation process as Oh's Figure 4. EX1005, ¶[0073] (“Referring to FIGS. 29 and 30 . . . [t]he second mask patterns 206 may be formed by the process described with reference to FIGS. 1 through 4.”) Oh further discloses that, referring to Figure 30, “[t]he second mask patterns 206 may be spaced apart from each other by the first trenches 101” and that there exists “the width T5 of the first trench 101.” EX1005 ¶[0073]. Oh accordingly discloses that its Figure 30 embodiment, which was formed by the same Figure 1 through 4 process as is used by Oh Figure 14, has first trenches 101 that are separated by width T5. EX1003, ¶93. It would have accordingly been obvious to a POSA to adapt this teaching of first trenches 101 having the same width T5 to Oh's Figure 14 embodiment. EX1003, ¶93; *Bos. Sci. Scimed, Inc. v. Cordis Corp.*, 554 F.3d 982, 991 (Fed. Cir. 2009) (“Combining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness.”)

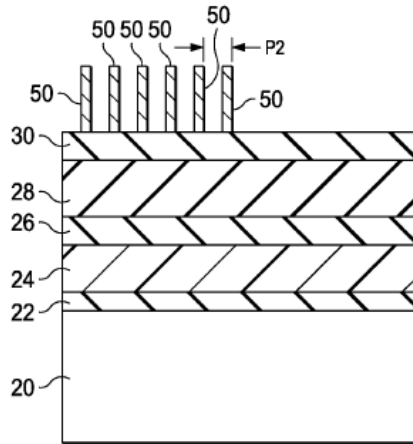


EX1005, FIG. 30.

Put differently, if Oh does not expressly disclose that the spacing/distance between the fins in Figure 14 is the same, a POSA would have found it obvious to apply the teachings from Figure 30 to render such a property obvious. EX1003, ¶94. This is because it is simply an application of a known technique (e.g., Oh's spacer process with trenches 101 having the same width T5, as shown in Oh's Figure 30) to a known structure (e.g., second mask patterns 206 and first trenches 101 in Oh's Figure 4) to yield predictable results (e.g., uniformly-spaced second mask patterns 206 and first trenches 101, which would lead to uniformly-spaced fins in Oh's Figure 14). EX1003, ¶94. Accordingly, Oh discloses or renders obvious that first trenches 101 in Oh's Figure 4 would have the same width. EX1003, ¶94.

Further, uniform spacing between first fin portions F1 would have been familiar to a POSA given well-known techniques and design objectives. EX1003, ¶96. For example, referring to Figure 5 below, Chen (EX1012) discloses a process to form spacers with uniform spacing P2 between adjacent spacers 50. EX1012, ¶[0013]; EX1003, ¶96. Based on the uniform spacing P2, Chen's process forms fins with uniform dimensions and uniform spacing. EX1012, ¶[0023]; EX1003, ¶96. A POSA would have understood that the benefits of Chen's process—similar to Oh's spacer process in Figure 30—include the manufacturing of smaller integrated circuits, mitigation of etch-loading effects during fin formation, and

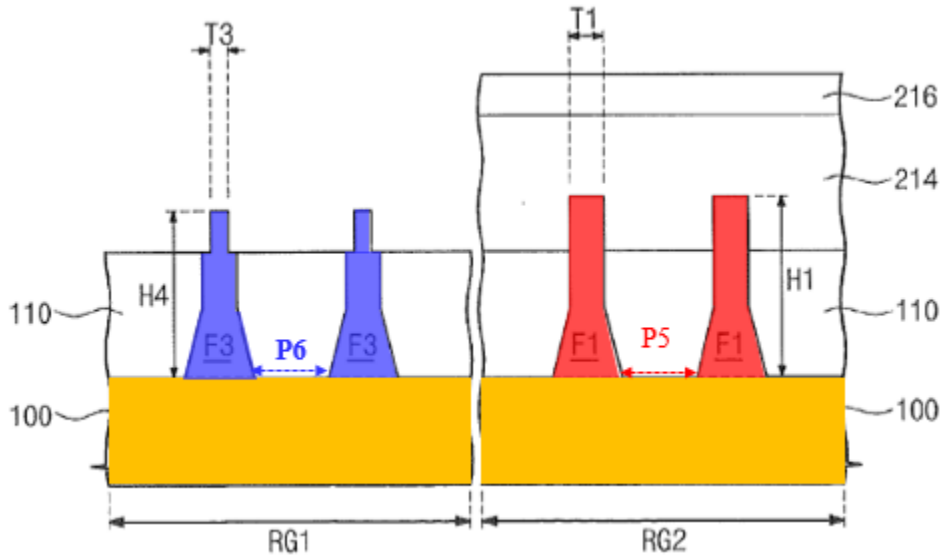
facilitation of epitaxial fin merging in multi-fin FinFETs. EX1013, ¶[0013]; EX1014, ¶[0005]; EX1003, ¶97. Further, a POSA would have reasonably expected to succeed applying such teachings to second mask patterns 206 in Oh's Figure 4. EX1003, ¶97.



EX1012, FIG. 5.

Referring to Oh's Figure 14 above, after a device isolation layer 110 is formed to cover lower parts of the first fin portions F1 in the first region RG1 and second region RG2, the two fins in the first region RG1 are shaped as discussed above in Section V.A.1.c. EX1003, ¶98. Specifically, the upper sidewalls of the first fin portions F1 in the first region RG1 are etched, while lower parts of these fins are unchanged because they are surrounded by device isolation layer 110. EX1005, ¶[0070]; EX1003, ¶99. As a result, Oh's fin-shaping process does not affect the uniformly-spaced lower parts of the fins in the first region RG1 and second region RG2. EX1003, ¶99.

In view of the above, referring to Oh's Figure 26 below, a POSA would have understood that **distance P6** (blue) between adjacent lower parts of the two fins in **third fin portions F3** (blue) is the same as **distance P5** (red) between adjacent lower parts of the two fins in **first fin portions F1** (red). EX1003, ¶100.



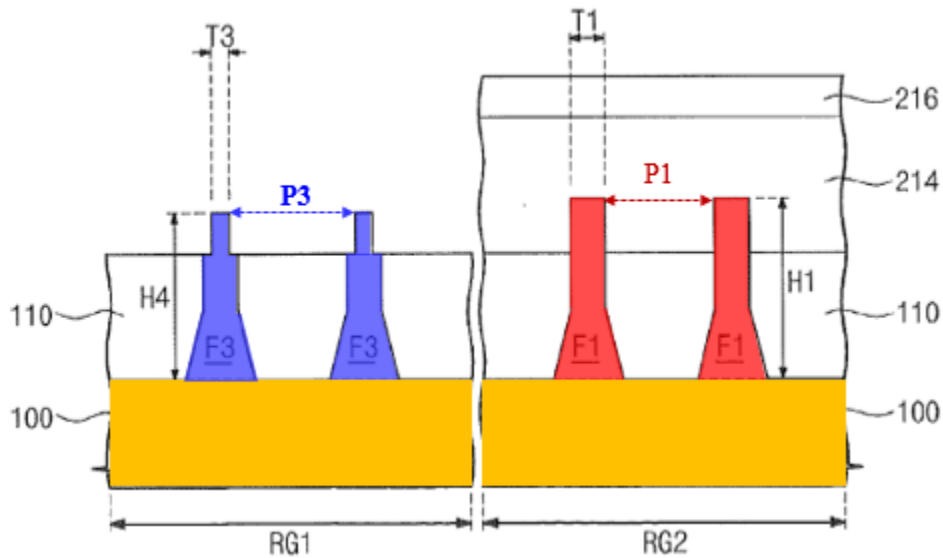
EX1005, FIG. 26 (annotated).

- e. **[1.d]: and wherein the adjacent top corners are directly opposite each other.**

Oh discloses this limitation. EX1003, ¶¶102-104. Since there are two “*adjacent top corners*” recited in limitation [1.b], the “*adjacent top corners*” in limitation [1.d] refers to “*adjacent top corners of the first fin and the second fin*” and/or to the “*adjacent top corners of the third fin and the fourth fin*” recited in limitation [1.b]. EX1003, ¶102.

Referring to Oh's Figure 26 below, the top corners of the two fins in **first fin portions F1** (red) are directly opposite each other and thus adjacent, and the top

corners of the two fins in **third fin portions F3** (blue) are directly opposite each other and thus adjacent; therefore Oh discloses limitation [1.d]. These are the same top corners referred to above when addressing the measurement of **distance P1** (red) between adjacent top corners of the two fins in **first fin portions F1** (red) and **distance P3** (blue) between adjacent top corners of the two fins in **third fin portions F3** (blue). EX1003, ¶103.

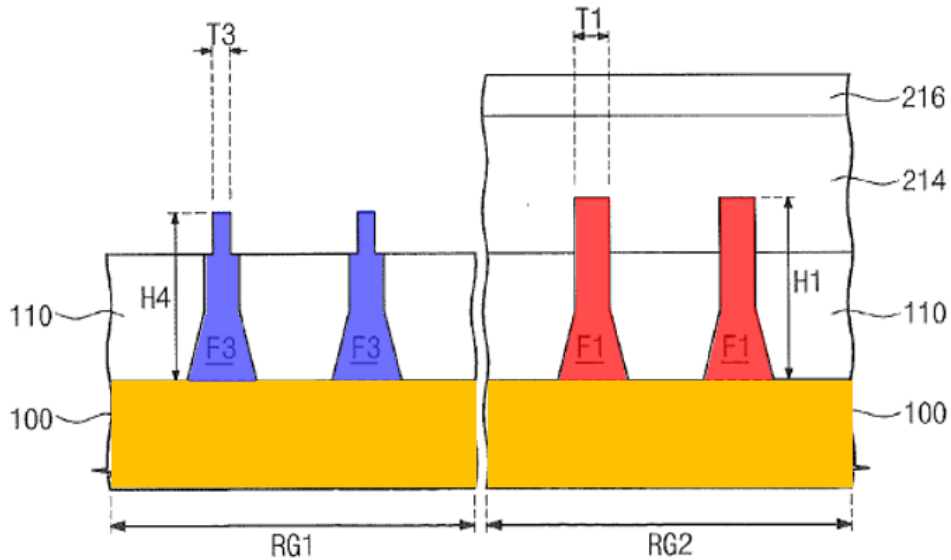


EX1005, FIG. 26 (annotated).

- 2. Dependent Claim 2: wherein the width of each top part of the first fin-shaped structures is larger than the width of each top part of the second fin-shaped structures.**

Oh discloses claim 2. EX1003, ¶¶105-106. Referring to Oh's Figure 26 below, a width T1 of each top part of **first fin portions F1** (red; "*first fin-shaped structures*") is larger than a width T3 of each top part of **third fin portions F3**

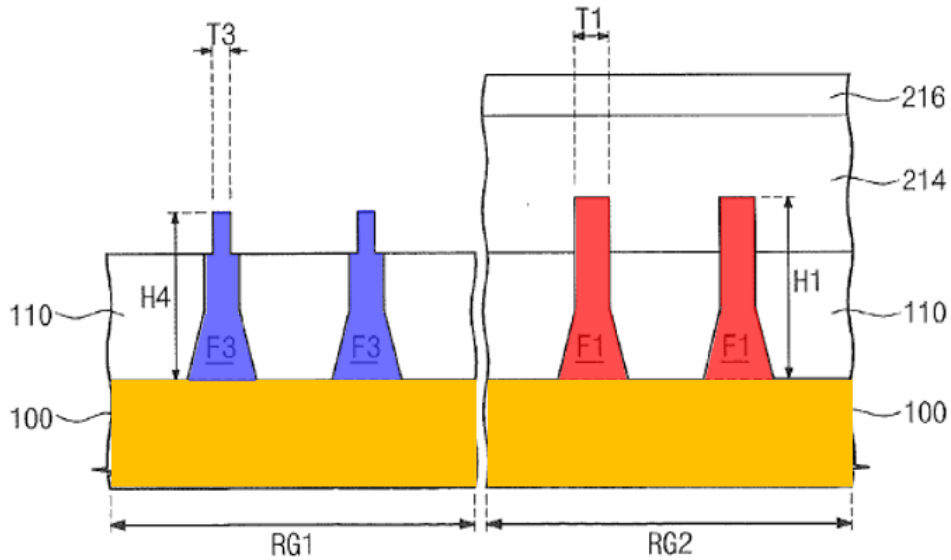
(blue; “*second fin-shaped structures*”). EX1003, ¶105. Oh explains that “[t]he third width T3 may be smaller than the first width T1.” EX1005, ¶[0070].



EX1005, FIG. 26 (annotated).

- 3. Dependent Claim 6: wherein a height of the first fin-shaped structures protruding from the substrate is higher than a height of the second fin-shaped structures protruding from the substrate.**

Oh discloses claim 6. EX1003, ¶¶107-108. Referring to the Oh’s Figure 26 below, a height H1 of **first fin portions F1** (red; “*first fin-shaped structures*”) protruding from **substrate 100** (orange) is higher than a height H4 of **third fin portions F3** (blue; “*second fin-shaped structures*”) protruding from **substrate 100** (orange). EX1003, ¶107. Oh explains that “[a]s the result of the etching process, the third fin portions F3 may have a fourth height H4 smaller than the first height H1 of the first fin portions F1.” EX1005, ¶[0070].



EX1005, FIG. 26 (annotated).

B. Ground 2: The combination of Oh and Rachmady renders obvious claims 3-5.

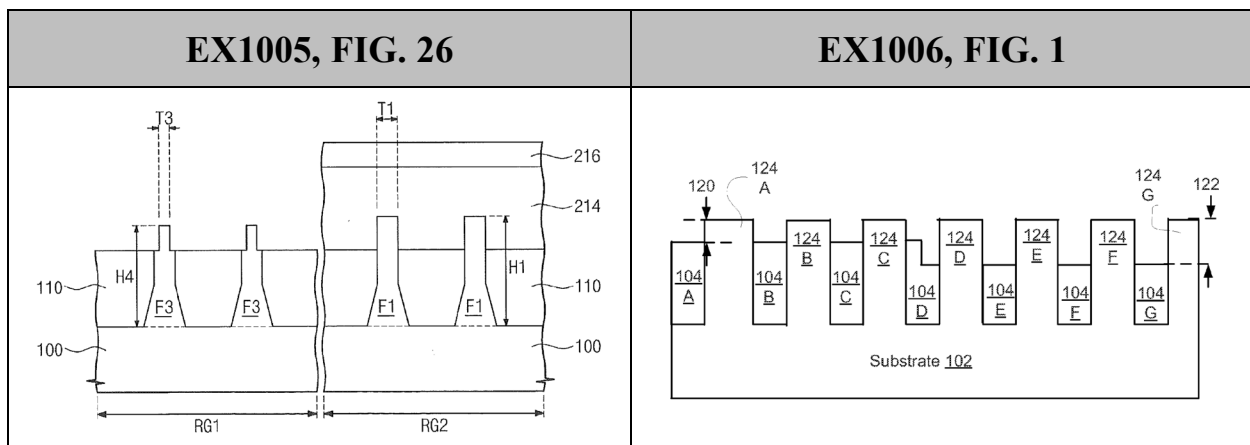
1. A POSA would have been motivated to combine Oh and Rachmady.

A POSA would have been motivated to modify Oh's fin-shaped structure by adjusting a height of a device isolation layer based on Rachmady's teachings to adjust drive current in Oh's transistors. EX1003, ¶¶109-127.

Oh and Rachmady are both in the same field of endeavor: the formation of FinFETs based on desired device characteristics. EX1003, ¶110. In integrated circuit (IC) design, circuit designers specify certain transistor dimensions based on electrical properties to meet circuit performance and size requirements. EX1007, ¶¶0018]; EX1003, ¶110. For example, Oh adjusts fin widths to achieve desired transistor threshold voltages. EX1005, ¶¶0053]. Rachmady adjusts fin heights—without impact to transistor area—to achieve desired drive currents. EX1006,

¶[0022]. Threshold voltage and drive current are among the key device characteristics to consider when designing ICs. EX1003, ¶110.

Also, Oh and Rachmady both describe similar fin-shaped structures, including fin-shaped structures with varying fin heights relative to an isolation structure. EX1003, ¶111. For example, Oh's Figure 26 (below) shows first fin portions F1 and third fin portions F3 with varying fin heights relative to a device isolation layer 110. EX1003, ¶111. Similarly, Rachmady's Figure 1 (below) shows fins 124 with varying fin heights relative to an isolation region 104. EX1003, ¶111.



Whereas Oh does not explicitly disclose varying heights of device isolation layer 110 to adjust fin height, Rachmady provides such teachings to adjust drive current—again, a key device characteristic in IC design. EX1003, ¶112. It would have been obvious to combine Oh's and Rachmady's teachings because a POSA would have (a) been motivated to apply Rachmady's selective fin height teachings to Oh's fin-shaped structure to adjust drive current and (b) reasonably expected to succeed in doing so. EX1003, ¶112.

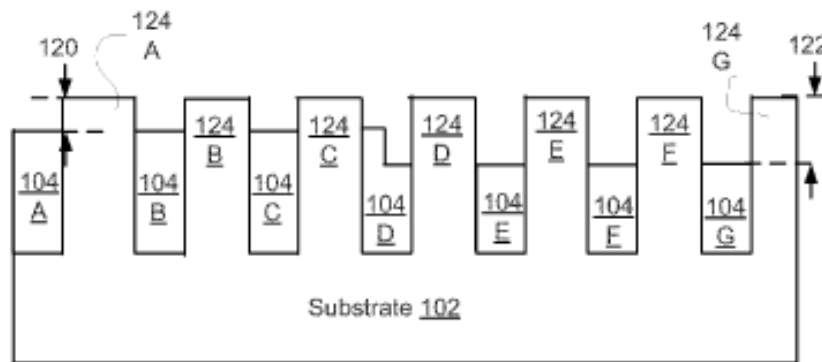
a. A POSA would have been motivated to apply Rachmady's selective fin height teachings to Oh's fin-shaped structure to adjust drive current.

A POSA would have been motivated to modify Oh's fin-shaped structure based on Rachmady's teaching of forming fins with different heights to adjust drive current because such modifications provide further circuit design flexibility to Oh's transistors to meet certain circuit design requirements. EX1003, ¶113. A POSA would have understood that circuit designs can vary based on circuit performance and size requirements. EX1003, ¶113. For example, Guo describes the need for higher threshold voltages and higher drive currents in FinFET PMOS devices in 4-transistor (4T) static random access memory (SRAM) designs to mitigate SRAM cell disturbances and to improve SRAM write margin. EX1019, p. 6; EX1003, ¶113. In addition to the negative wordline bias circuit solution proposed by Guo, the combination of Oh's and Rachmady's teachings provides another solution—which does not require additional circuitry that can impact SRAM circuit size—to meet the 4T SRAM design requirements: to form FinFET PMOS devices with higher threshold voltages and higher drive currents. EX1003, ¶113.

Oh describes FinFETs with fin portions that have different widths for different threshold voltages, stating that “fin portions having widths different from each other may be formed, which can enable the fabrication of transistors having

threshold voltages different from each other.” EX1005, ¶[0053]; EX1003, ¶114.

Rachmady provides additional circuit design flexibility and describes forming fin-shaped structures with different fin heights above isolation regions to adjust drive current (which is based on a transistor’s threshold voltage). EX1006, Abstract; EX1003, ¶115. Referring to Figure 1 below, Rachmady explains that “as the drive current of a transistor is dependent on the gate channel ‘width’ of a multi-gate transistor, and the ‘width’ may be made greater by use of a taller fin 124 without increasing the area of the transistor, selectable multi-height fins 124 allow the transistors with the same area to have selected drive currents based on the fin heights.” EX1006, ¶[0022].



EX1006, FIG. 1.

Applying Rachmady’s teachings to Oh’s fin-shaped structure provides improved drive current to Oh’s transistors, which in turn can be used in a wider variety of circuit designs. EX1003, ¶116. For example, as described above, FinFET PMOS devices in 4T SRAM designs require higher threshold voltages and higher drive currents. EX1019, p. 6; EX1003, ¶116. The higher threshold voltages are

needed to mitigate SRAM cell disturbances from neighboring SRAM cells during a write operation. EX1019, p. 6; EX1003, ¶116. Consequently, the higher threshold voltages lead to lower drive currents in the FinFET PMOS devices, thus decreasing SRAM write margin. EX1019, p. 6; EX1003, ¶116.

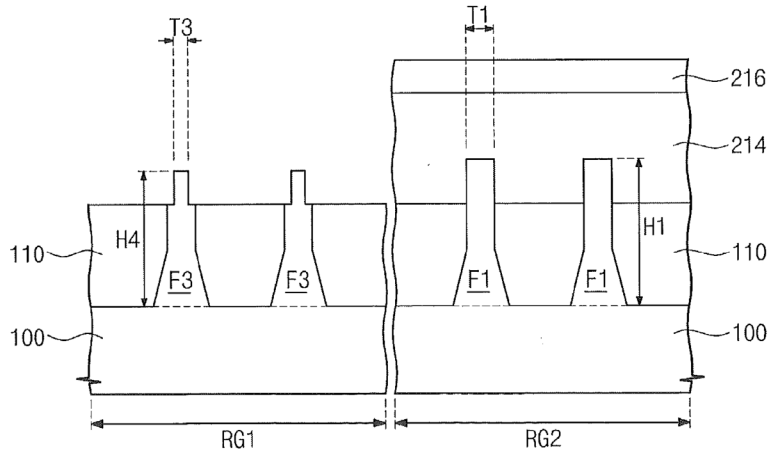
A POSA would have understood that FinFET with narrower fin widths have higher threshold voltages. EX1018, ¶[0016], Figure 2; EX1003, ¶116. To meet the higher threshold voltage/higher drive current requirements in 4T SRAM designs, a POSA would have been motivated to form FinFET PMOS devices with narrower fin widths to achieve the higher threshold voltages based on Oh's teachings. EX1003, ¶116. And to improve SRAM write margin, a POSA would have been further motivated to apply Rachmady's selective fin height teachings to Oh's FinFET PMOS devices to increase drive currents. EX1003, ¶¶116-117.

b. A POSA would have reasonably expected to succeed in modifying Oh's fin-shaped structure based on Rachmady's selective fin height teachings.

Oh and Rachmady disclose well-known semiconductor fabrication processes to form fin structures, and thus a POSA would have reasonably expected that applying Rachmady's teachings to adjust the height of Oh's fins would successfully adjust drive current. EX1003, ¶118.

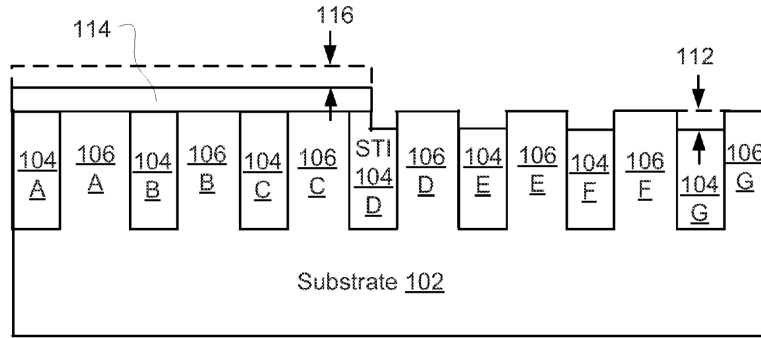
Oh discloses etching exposed fin portion regions to shape fins, where a fin height relative to a device isolation layer is shortened due to the etching process.

EX1003, ¶119. Referring to Figure 26 below, Oh explains that “upper sidewalls of the first fin portions F1 with the first width T1 may be etched to form the third fin portions F3, whose upper portions have the third width T3,” where “[t]he third width T3 may be smaller than the first width T1.” EX1005, ¶[0070]. Oh further explains that “[a]s the result of the etching process, the third fin portions F3 may have a fourth height H4 smaller than the first height H1 of the first fin portions F1.” EX1005, ¶[0070].



EX1005, FIG. 26.

Rachmady also discloses etching an exposed fin portion region, where its etching process removes portions of an isolation layer to increase fin heights. EX1003, ¶120. Referring to Figure 6 below (a precursor structure to Figure 1), Rachmady uses a selective etching process to remove portions of isolation region 104 but not pre-fin regions 106. EX1006, ¶[0029]. Thus, based on this etch selectivity, Rachmady’s fin heights can be varied to adjust drive current. EX1003, ¶120.



EX1006, FIG. 6.

After forming third fin portions F3 in Oh’s Figure 26 (above) and to achieve a desired threshold voltage, Rachmady’s selective fin height process can be applied to increase fin heights of third fin portions F3 protruding from the device isolation layer. EX1003, ¶121. Because Rachmady’s selective fin height process can be controlled based on different etchants and materials, a POSA would have reasonably expected to succeed in etching Oh’s device isolation layer 110 in region RG1 to increase fin heights—and thus drive currents—of third fin portions F3, while keeping these fins intact. EX1003, ¶121.

c. Additional rationales for combining Oh’s and Rachmady’s teachings

Additional rationales that would have led a POSA to combine the teachings Oh and Rachmady are below. EX1003, ¶¶122-127.

First, a POSA would have understood that the Oh-Rachmady combination combines known elements (Oh’s fin-shaped structure and Rachmady’s varying fin heights) according to known methods (Rachmady’s fin height process based on

selective etching) to yield predictable results (varying fin heights in Oh's first region RG1 and second region RG2 to vary drive current based on circuit design requirements, such as those for FinFET PMOS devices in 4T SRAM designs). EX1003, ¶123.

Second, a POSA would have understood that the Oh-Rachmady combination uses a known technique (Rachmady's fin height process based on selective etching) to improve similar devices (Oh's fin-shaped structure) in the same way (by adjusting fin heights to vary drive current based on circuit design requirements, such as those for FinFET PMOS devices in 4T SRAM designs). EX1003, ¶124.

Third, a POSA would have understood that the Oh-Rachmady combination applies a known technique (Rachmady's fin height process based on selective etching) to a known device ready for improvement (Oh's fin-shaped structure) to yield predictable results (varying fin heights in Oh's first region RG1 and second region RG2 to vary drive current based on circuit design requirements, such as those for FinFET PMOS devices in 4T SRAM designs). EX1003, ¶125.

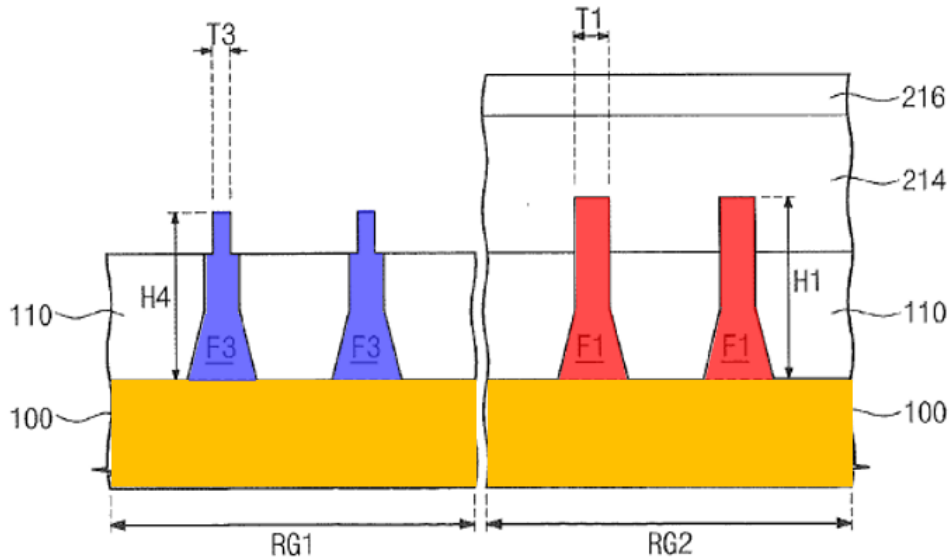
Fourth, a POSA would have arrived at the Oh-Rachmady combination due to a teaching, suggestion or motivation in the prior art (necessity of transistors with a wide array of electrical properties to enable different IC designs, such as 4T SRAM designs) to arrive at the claimed invention. EX1003, ¶126.

Fifth, a POSA would have understood that the Oh-Rachmady combination is obvious to try since it is merely choosing from a finite number of identified, predictable solutions (Rachmady's fin height process based on selective etching), with a reasonable expectation of success (adjust fin heights in Oh's first region RG1 and second region RG2 to vary drive current based on circuit design requirements, such as those for FinFET PMOS devices in 4T SRAM designs). EX1003, ¶127.

2. Dependent Claim 3

- a. [3.a]: an isolation structure disposed beside the first fin-shaped structures and beside the second fin-shaped structures respectively,**

Oh discloses this limitation. EX1003, ¶¶128-130. Referring to Oh's Figure 26 below, device isolation layers 110 ("*an isolation structure*") is disposed beside **first fin portions F1** (red; "*first fin-shaped structures*") and beside **third fin portions F3** (blue; "*second fin-shaped structures*") respectively. EX1003, ¶128.

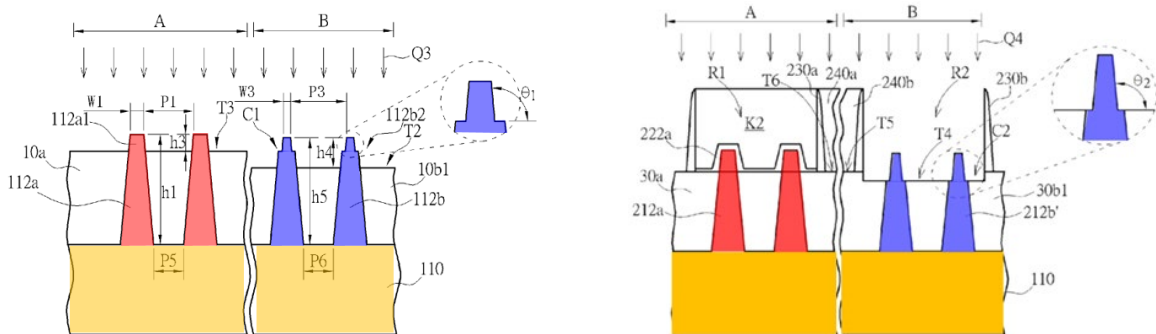


EX1005, FIG. 26 (annotated).

Oh explains that “[t]he device isolation layers 110 may be formed to cover lower sidewalls of the first fin portions F1. The formation of the device isolation layers 110 may include forming a dielectric layer to cover the first and second regions RG1 and RG2, and then, etching the dielectric layer to expose upper portions of the first fin portions F1.” EX1005, ¶[0059]. After, to form **third fin portions F3**, Oh explains that “upper sidewalls of the first fin portions F1 with the first width T1 may be etched to form the third fin portions F3, whose upper portions have the third width T3.” EX1005, ¶[0070]. After the formation of **first fin portions F1** (red) and **third fin portions F3** (blue), device isolation layers 110 remain disposed beside **first fin portions F1** (red) and beside **third fin portions F3** (blue), as shown in Oh’s Figure 26. EX1003, ¶¶129-130.

- b. [3.b]: and ladder-shaped cross-sectional profile parts of the second fin-shaped structures are higher than a top surface of the isolation structure.

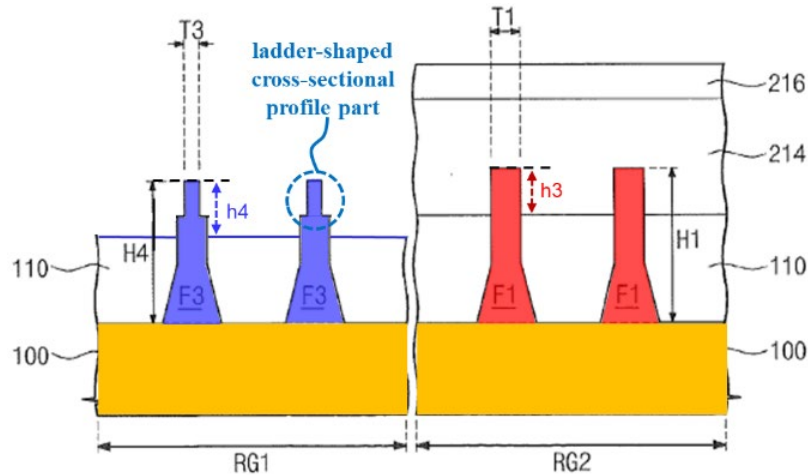
The Oh-Rachmady combination renders obvious this limitation. EX1003, ¶¶131-136. Figures 5 and 8 of the '510 patent (below) show examples of ladder-shaped cross-sectional profile parts of **second fin-shaped structures 112b/212b'** (blue; shown in dashed line inset). EX1003, ¶131. The Oh-Rachmady combination teaches this structure. EX1003, ¶131.



EX1001, FIG. 5 (left; annotated) and 8 (right; annotated).

Referring to the modified version of Oh's Figure 26 below, as would be understood by a POSA, application of Rachmady's selectable fin height process to Oh's fin-shaped structure would result in ladder-shaped cross-sectional profile parts of **third fin portions F3** (blue; "second fin-shaped structures") being higher than a top surface of device isolation layer 110 ("isolation structure") for circuit designs that require Oh's transistors in first region RG1 to have higher drive currents (e.g., FinFET PMOS devices in 4T SRAM designs). EX1003, ¶132. As shown below, Oh's ladder-shaped cross-sectional profile parts of **third fin**

portions **F3** (blue; “*second fin-shaped structures*”) are formed above device isolation layer 110—similar to the ladder-shaped cross-sectional profile parts of the **second fin-shaped structures** in Figure 5 of the ’510 patent (blue; see inset in dashed circle). EX1003, ¶132.

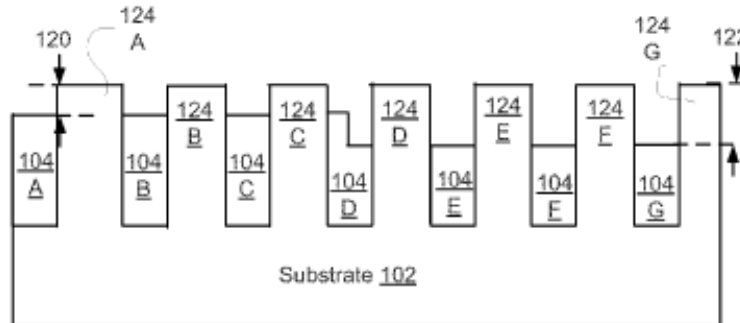


EX1005, FIG. 26 (modified and annotated).

Rachmady teaches etching down isolation regions to form fin-shaped structures with different fin heights above the isolation regions to adjust drive current and achieve desired device characteristics (e.g., higher drive currents for FinFET PMOS devices in 4T SRAM designs). EX1006, Abstract, ¶¶[0023]-[0035]; EX1003, ¶133. For example, referring to Figure 1 below, Rachmady states that “[f]ins 124A through 124C have a smaller height 120 while fins 124D through 124G have a larger height 122,” where the “difference between heights 120 and 122 is selectable by choosing materials and etchants.” EX1006, ¶[0021]. As a result, portions of the isolation region can be removed to increase fin heights and to

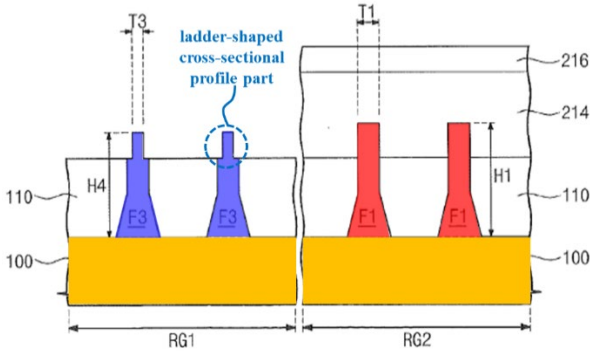
increase drive current without increasing transistor area. EX1006, ¶[0038];

EX1003, ¶133.

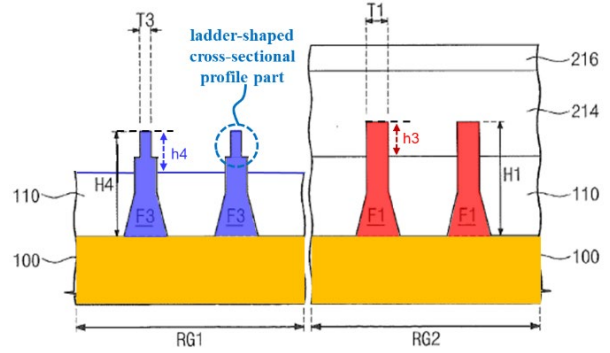


EX1006, FIG. 1.

Referring to the modified version of Oh's Figure 26 below, applying Rachmady's selective removal of the isolation regions to increase drive current of Oh's transistors in first region RG1 would result in the ladder-shaped cross-sectional profile parts of the **third fin portions F3** (blue) being higher than a top surface of device isolation layer 110 (original third fin portions F3 in the original Figure 26 (left) and modified third fin portions F3 in the modified Figure 26 (right)). EX1003, ¶134. Put differently, based on the original location of the ladder-shaped cross-sectional profile parts of **third fin portions F3** (blue) in Oh's Figure 26, the ladder-shaped cross-sectional profile parts would be above device isolation layer 110 in first region RG1 when device isolation layer 110 is etched to increase **height h4 of third fin portions F3** (blue). EX1003, ¶134. As a result, drive currents are increased in Oh's transistors in first region RG1 without increasing transistor area. EX1003, ¶134.



EX1005, FIG. 26 (annotated).

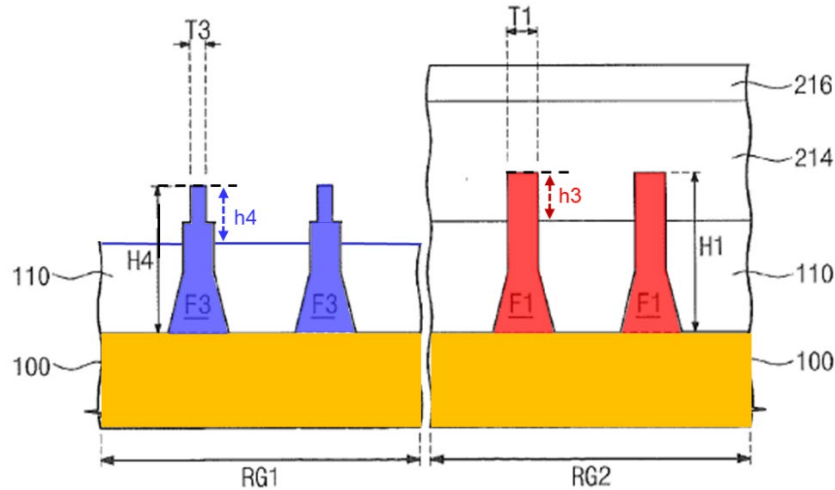


EX1005, FIG. 26 (modified and annotated).

It would have been obvious to combine Oh's and Rachmady's teachings because a POSA would have (a) been motivated to apply Rachmady's selective fin height teachings to Oh's fin-shaped structure to increase drive current (e.g., for FinFET PMOS devices in 4T SRAM designs) and (b) reasonably expected to succeed in doing so, as discussed above in Section V.B.1. EX1003, ¶135.

3. Dependent Claim 4: wherein a top surface of the isolation structure of a first area is higher a top surface of the isolation structure of a second area.

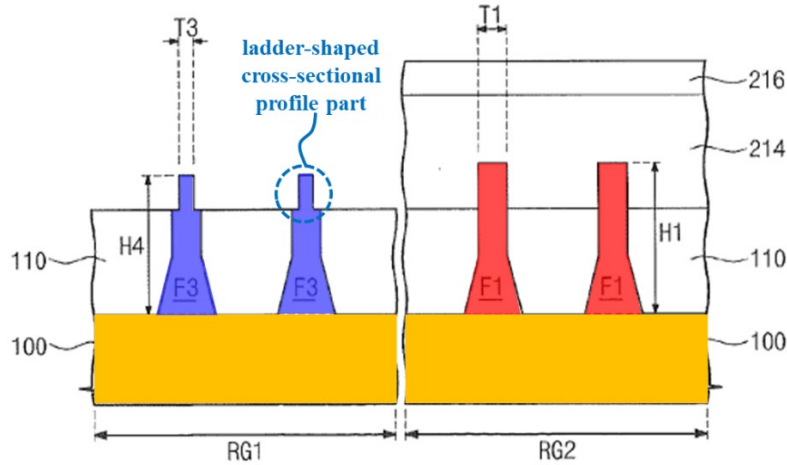
The Oh-Rachmady combination renders obvious claim 4 (which depends from claim 3). EX1003, ¶¶137-140. Referring to the modified version of Oh's Figure 26 below—and as discussed above in dependent claim 3 (Section V.B.2.b) from which claim 4 depends—it would have been obvious for a top surface of device isolation layer 110 in the second region RG2 (*“the isolation structure of a first area”*) to be higher than a top surface of device isolation layer 110 in the first region RG1 (*“the isolation structure of a second area”*). EX1003, ¶137.



EX1005, FIG. 26 (modified and annotated).

Referring to the modified version of Oh's Figure 26 above, applying Rachmady's selective fin height process to Oh's transistors in the first region RG1 would result in a top surface of device isolation layer 110 in the second region RG2 being higher than a top surface of device isolation layer 110 in the first region RG1, because device isolation layer 110 in the second region RG2 is protected by mask patterns 214 and 216 when etching device isolation layer 110 in the first region RG1. EX1003, ¶138. Put differently, based on the original location of device isolation layer 110 in the first region RG1 in Oh's Figure 26 below, the top surface of device isolation layer 110 in the first region RG1 would be below the top surface of device isolation layer 110 in the second region RG2 after device isolation layer 110 in the first region RG1 is etched, as shown in the modified version of Oh's Figure 26 above. EX1003, ¶138. Device isolation layer 110 in the

second region RG2 would not be etched because it is covered by mask patterns 214 and 216. EX1005, ¶[0069].



EX1005, FIG. 26 (annotated).

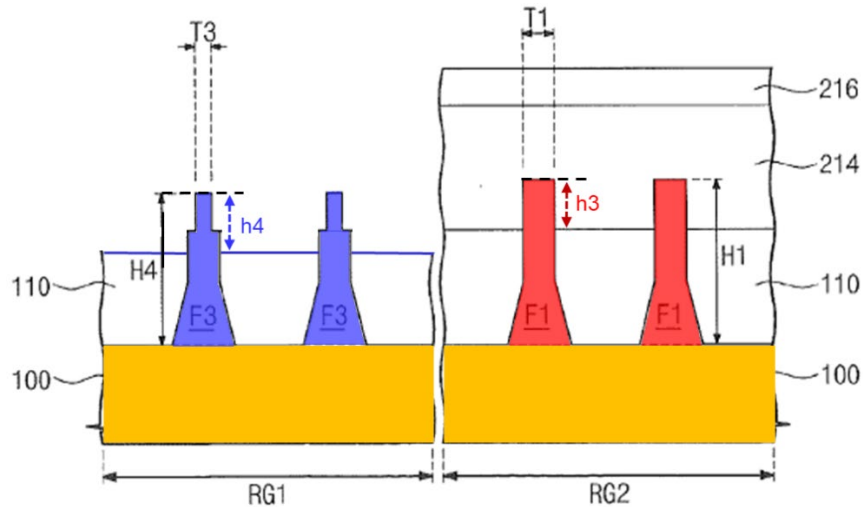
It would have been obvious to combine Oh's and Rachmady's teachings because a POSA would have (a) been motivated to apply Rachmady's selective fin height teachings to Oh's fin-shaped structure to increase drive current (e.g., for FinFET PMOS devices in 4T SRAM designs) and (b) reasonably expected to succeed in doing so, as discussed above in Section V.B.1. EX1003, ¶139.

- 4. Dependent Claim 5: wherein a height of the first fin-shaped structures protruding from the isolation structure is lower than a height of the second fin-shaped structures protruding from the isolation structure.**

The Oh-Rachmady combination renders obvious claim 5. EX1003, ¶¶141-146.¹ Referring to the modified version of Oh's Figure 26 below, a height of **first**

¹ For purposes of this IPR proceeding, "the isolation structure" recited in

fin portions F1 (red; “a height of the first fin-shaped structures”) protruding from device isolation layer 110 (“the isolation structure”) is lower than a height of **third fin portions F3** (blue; “a height of the second fin-shaped structures”) protruding from device isolation layer 110 (“the isolation structure”). EX1003, ¶141.



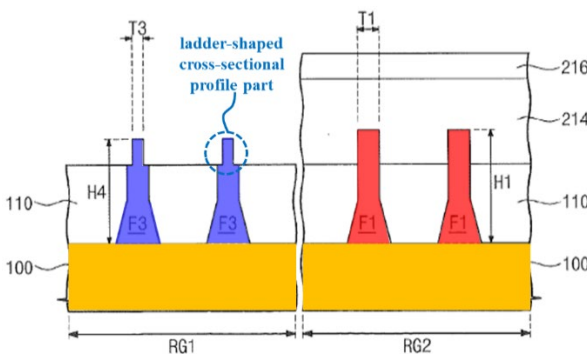
EX1005, FIG. 26 (modified and annotated).

Based on Rachmady’s teachings of adjusting fin heights to adjust transistor drive current, Oh’s device isolation layer 110 in the first region RG1 can be etched to increase the height of **third fin portions F3** (blue) protruding from device isolation layer 110, as shown in the modified version of Oh’s Figure 26 above, and thus increase Oh’s transistor drive current. As a result, to meet circuit design requirements of increased drive current (e.g., for FinFET PMOS devices in 4T

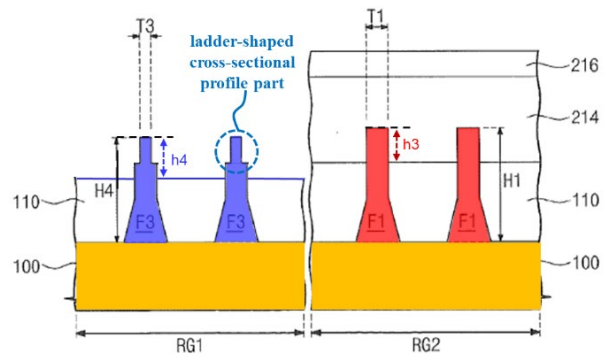
claim 5 is assumed to be “an isolation structure,” since the term “isolation structure” is not recited in independent claim 1, from which claim 5 depends.

SRAM designs), the height of **first fin portions F1** (red) protruding from device isolation layer 110 is made lower than the height of **third fin portions F3** (blue) protruding from device isolation layer 110. EX1003, ¶142.

Applying Rachmady's teachings to Oh's Figure 26 (below) would result in transistors in the first region RG1 and second region RG2 with different fin heights (relative to device isolation layer 110, as shown in the modified version of Oh's Figure 26 below) tuned to desired drive current characteristics. EX1003, ¶¶142-143. For example, as discussed above in Section V.B.1.a, to meet the higher threshold voltage/higher drive current requirements in 4T SRAM designs, a POSA would have been motivated to form FinFET PMOS devices with narrower fin widths to achieve the higher threshold voltages based on Oh's teachings. EX1003, ¶143. Referring to Oh's Figure 26 (below), the FinFET PMOS devices with narrower fin widths can be the transistors in the first region RG1 having shaped **third fin portions F3** (blue). EX1003, ¶143.



EX1005, FIG. 26 (annotated).



EX1005, FIG. 26 (modified and annotated).

And to improve SRAM write margin, a POSA would have been further motivated to apply Rachmady's selective fin height teachings to Oh's FinFET PMOS devices to increase drive currents. EX1003, ¶143. Referring to the modified version of Oh's Figure 26 (above), the height of **third fin portions F3** (blue) above device isolation layer 110 can be increased, such that the height of **third fin portions F3** (blue) protruding from device isolation layer 110 is larger than the height of **first fin portions F1** (red) protruding from device isolation layer 110. EX1003, ¶¶143-144.

It would have been obvious to combine Oh's and Rachmady's teachings because a POSA would have (a) been motivated to apply Rachmady's selective fin height teachings to Oh's fin-shaped structure to increase drive current and (b) reasonably expected to succeed in doing so, as discussed above in Section V.B.1. EX1003, ¶145.

C. Ground 3: The combination of Wann and Lin renders obvious claims 1-6.

Ground 3 concerns the combination of Wann and Lin. Both Wann and Lin are FinFET references. The combination of the teachings from these references renders obvious claims 1-6. The combination is as follows.

First, Wann provides fundamental teachings regarding the formation of FinFETs, including the use of multiple fin arrangements which would have all but one of the properties claimed by the '510 patent. In particular, Wann discloses a

five-fin embodiment, but does not disclose the exact ordering of the fins in this embodiment (which is a requirement of the '510 patent). But, as Dr. Salahuddin explains, there are only 30 possible arrangements for Wann's five-fin embodiment, in which 6 of those 30 arrangements—in combination with Lin's teachings—read on claims 1-6. There are thus a finite number of known arrangements of Wann's five-fin embodiment. As explained below, a POSA would have found it obvious to try any of those 6 arrangements in combination with Lin's teachings (also referred to herein as “the Wann-Lin five-fin FinFET structure”), with a reasonable expectation of success.

Second, the limitation missing from Wann is that the fins should be uniformly spaced apart when they are created. Lin discloses such a teaching.

1. A POSA would have been motivated to combine Wann and Lin.

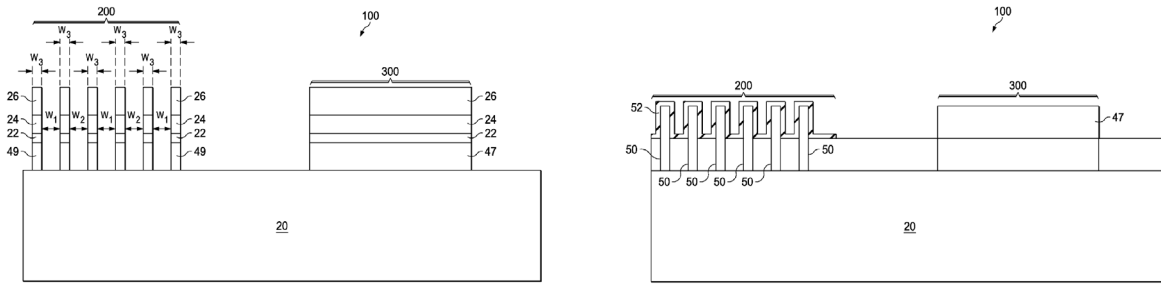
Wann and Lin both disclose mandrel/spacer processes to form fin structures. EX1003, ¶¶148-149. Whereas Wann does not explicitly disclose details on spacer formation and mandrel removal in its mandrel/spacer process, Lin provides such teachings. EX1003, ¶¶149-150. It would have been obvious to combine Wann's and Lin's teachings because a POSA would have (a) been motivated to apply Lin's mandrel/spacer process to Wann's fin-shaped structures to improve fin reliability and manufacturability and (b) reasonably expected to succeed in doing so.

EX1003, ¶151.

a. A POSA would have been motivated to apply Lin's mandrel/spacer process to Wann's fin-shaped structures.

Fin reliability and manufacturability improvements conferred by Lin's teachings would have motivated a POSA to apply Lin's mandrel/spacer process to Wann's fin-shaped structures. EX1003, ¶¶152-158. A goal of Wann is for "improved methods for automatically converting older planar structure layouts to FinFET structure layouts." EX1007, ¶[0003]. To meet this goal, Wann discloses a selective fin-shaping process to allow individual fin width and fin height control. EX1007, ¶[0019].

Lin describes a mandrel/spacer process that forms fins with uniform dimensions and uniform spacing from one another. EX1008, ¶[0062]; EX1003, ¶¶154-156. For example, referring to Figure 13 below, Lin explains that "[t]he spacing between the semiconductor strips 49 W_1 and W_2 are defined by the widths W_1 and W_2 between the fin spacers 42," where "the width W_1 is substantially equal to the width W_2 ." EX1008, ¶[0051]. Based on semiconductor strips 49 and after further processing, fins 50—with uniform dimensions and uniform spacing—are formed as shown in Lin's Figure 15 below. EX1008, ¶¶[0052]-[0059]; EX1003, ¶156.



EX1008, FIGs. 13 (left) and 15 (right).

Advantageously, Lin’s mandrel/spacer process provides substantially uniform fins, in which “the spacing and depth between the fins 50 are better controlled and may be substantially equal between all of the fins 50.” EX1008, ¶[0062]; EX1003, ¶157. An additional benefit of Lin’s mandrel/spacer process is its mandrel removal process, which includes a “wet etch process [that] is a lower cost and allows a higher throughput (wafers per hour) than a dry etch process.” EX1008, ¶[0063].

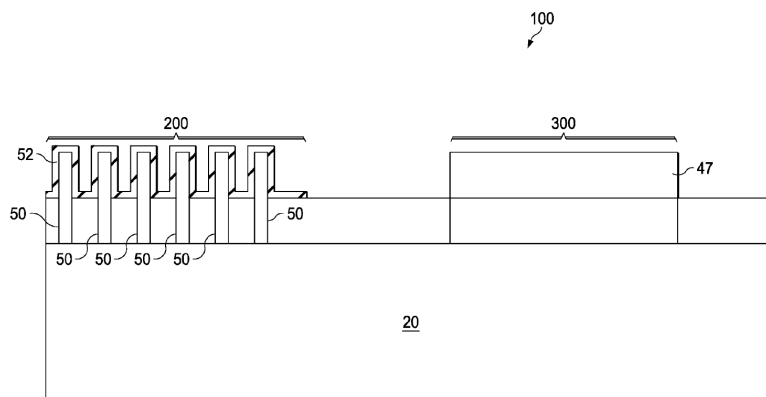
In view of the above, a POSA would have been motivated to combine Wann’s and Lin’s teachings. EX1003, ¶158. A POSA would have understood that Lin’s mandrel/spacer process improves the manufacturing of Wann’s fins—e.g., from reliability, controllability, and cost points of views—thus improving the circuit design flexibility of Wann’s fin-shaping process. EX1003, ¶158.

b. A POSA would have reasonably expected to succeed in applying Lin’s mandrel/spacer process to Wann’s fin-shaped structures.

Wann and Lin disclose well-known semiconductor fabrication processes to form fin structures, and thus a POSA would have reasonably expected that

applying Lin's teachings to form Wann's fin-shaped structures would successfully form fin structures with uniform spacing between lower parts of adjacent regular fins and between lower parts of adjacent shaped fins. EX1003, ¶159.

While Wann does not explicitly disclose details on spacer formation and mandrel formation and removal in its mandrel/spacer process to form its regular fins, Lin fills this gap by providing details on a mandrel/spacer process that can be used to form any number of regular fins (prior to Wann's fin-shaping process)—with a similar fin structure as fins 50 shown in Lin's Figure 15 below. EX1003, ¶160. A POSA would have reasonably expected to succeed in forming Wann's fin-shaped structures, where a distance between lower parts of adjacent regular fins is the same as a distance between lower parts of adjacent shaped fins. EX1003, ¶160. This is because Lin's mandrel/spacer process can be used to form Wann's regular fins, in which one or more of the regular fins can be further shaped by Wann's fin-shaping process. EX1003, ¶160.



EX1008, FIG. 15.

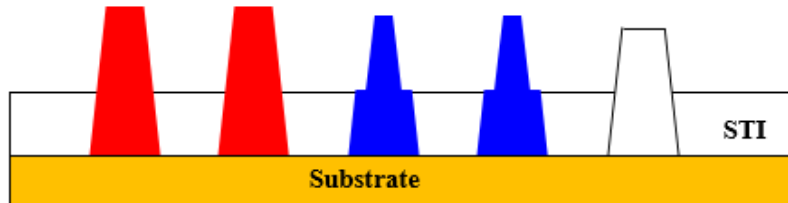
2. The Wann-Lin five-fin FinFET structure.

Though Wann discloses a five-fin FinFET embodiment having “2 regular fins, 2 fins shaped a particular way, and 1 fin shaped a different way,” it does not provide illustrations of the five-fin structure. EX1007, ¶[0042]; EX1003, ¶161. But, based on Wann’s fin-shaping process, a POSA would have understood that one of the many fin permutations of Wann’s five-fin FinFET embodiment includes arranging the fins from left to right in the same order as listed in Wann’s paragraph 24; that is, an arrangement of **2 regular fins adjacent to one another** (red) and **2 fins shaped a particular way adjacent to one another** (blue)—just like the claimed fin-shaped structure in the ’510 patent—as shown in Illustration 8 provided by Dr. Salahuddin (below).² A POSA would have understood that this fin permutation is obvious to try since it is merely one fin arrangement from a finite number of identified, predictable solutions, with a reasonable expectation of success.³ *KSR Int’l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1742 (2007); EX1003,

² Dr. Salahuddin provides Illustrations 2-5 and 8 to pictorially depict Wann’s textual disclosure.

³ Dr. Salahuddin explains that Wann’s disclosure of a five-fin embodiment, with “2 regular fins, 2 fins shaped a particular way, and 1 fin shaped a different way,” describes 30 possible different arrangements of fins, 6 of which have the

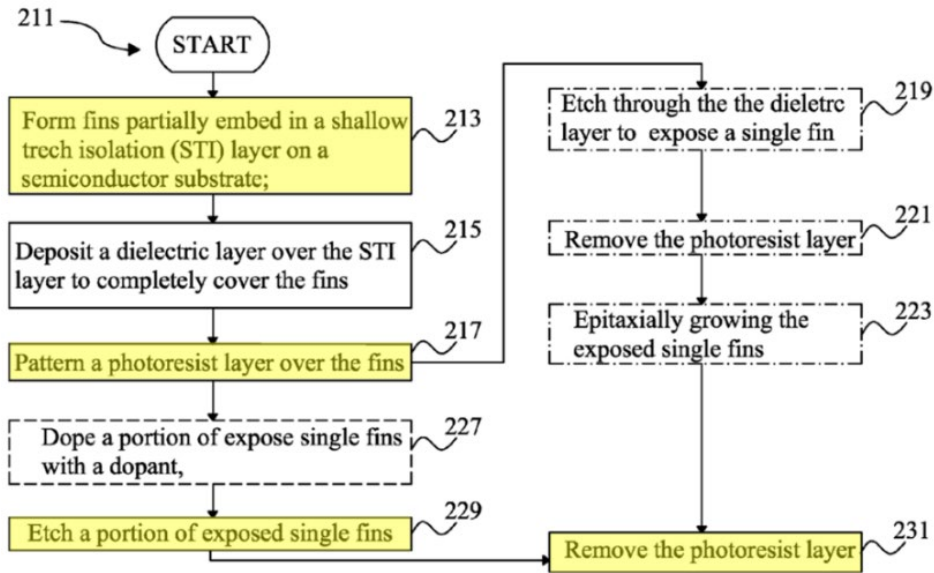
¶¶161-162. Additionally, the arrangement of the regular and shaped fins would not affect Wann’s fin-shaping process goal: to vary the channel width of a FinFET “beyond an integer multiple of a single fin dimension.” EX1007, ¶[0019]; EX1003, ¶162.



EX1003, Illustration 8.

Wann describes its fin-shaping process in the context of Figure 2 below (flowchart showing method of shaping fins; annotated) and associated Figures 3B, 5A, 5B, 6A, and 6B (Wann’s three-fin FinFET embodiment). EX1003, ¶¶171-173. The sequence of operations 213, 217, 229, and 231 (highlighted below) are directed to an embodiment of the fin-shaping process that can be used to form Wann’s five-fin FinFET embodiment shown in Illustration 8 provided by Dr. Salahuddin. EX1003, ¶¶169-186. The other operations are either optional or directed to another fin-shaping embodiment. EX1003, ¶¶172-173. Below, Dr. Salahuddin provides Charts 1-4 that map operations 213, 217, 229, and 231 of _____ properties claimed by the ’510 patent. EX1003, ¶¶169-170. This includes the most basic arrangement, where the fins are arranged exactly as described in Wann’s paragraph 24.

Figure 2 to Wann's three-fin FinFET embodiment (shown in Figures 3B, 5A, 5B, 6A, and 6B) and to Wann's five-fin FinFET embodiment (shown in Illustrations 2-5 and 8 provided by Dr. Salahuddin). EX1003, ¶¶169-186.

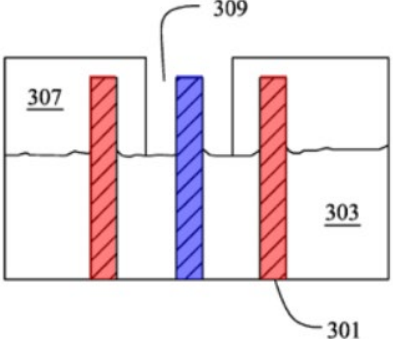
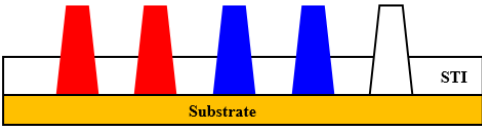


EX1007, FIG. 2 (annotated).

Referring to operation 213 in Chart 1 below and similar to Wann's three-fin FinFET embodiment, 5 regular fins (red, blue, and white) are formed by a mandrel/spacer process through etching a **semiconductor substrate** (orange), in which the 5 regular fins are partially embedded in an STI on the **semiconductor substrate** (orange), as shown in Illustration 2 provided by Dr. Salahuddin.

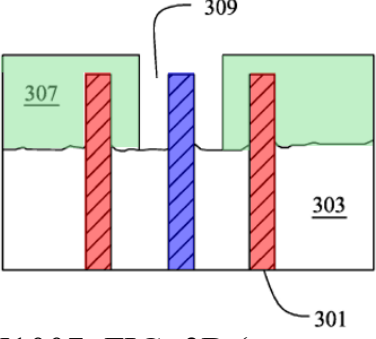
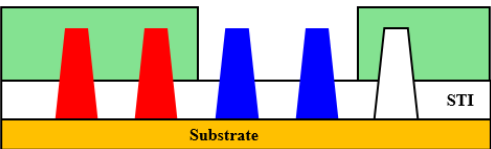
EX1003, ¶175. As discussed above in Section V.C.1.a, applying Lin's mandrel/spacer process, a POSA would have formed Wann's 5 regular fins with uniform dimensions and uniform spacing from one another to improve fin reliability and manufacturability, as shown in Illustration 2 provided by Dr.

Salahuddin. EX1003, ¶¶171-175.

Operation 213	Wann’s three-fin FinFET embodiment	Wann’s five-fin FinFET embodiment
<p>“Form fins partially embed[ded] in a shallow trench [sic] isolation (STI) layer on a semiconductor substrate” EX1007, FIG. 2.</p>	 <p>EX1007, FIG. 3B (annotated).</p>	 <p>EX1003, Illustration 2.</p>

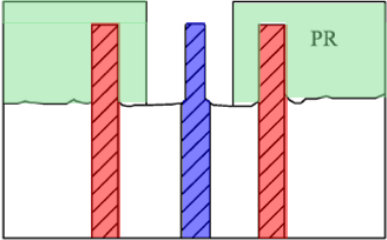
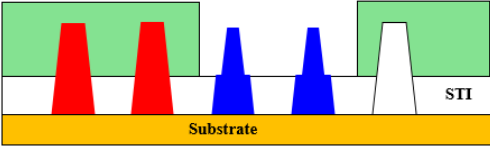
EX1003, Chart 1.

Referring to operation 217 in Chart 2 below and similar to Wann’s three-fin FinFET embodiment, a **photoresist layer** (green) is formed over the 5 regular fins (red, blue, and white) and patterned an opening to expose 2 regular fins (blue), as shown in Illustration 3 provided by Dr. Salahuddin. EX1003, ¶176.

Operation 217	Wann’s three-fin FinFET embodiment	Wann’s five-fin FinFET embodiment
<p>“Pattern a photoresist layer over the fins” EX1007, FIG. 2.</p>	 <p>EX1007, FIG. 3B (annotated).</p>	 <p>EX1003, Illustration 3.</p>

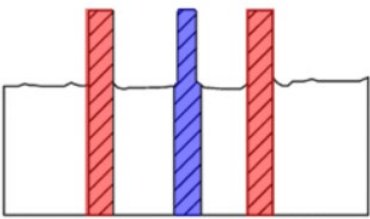
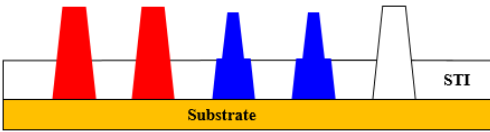
EX1003, Chart 2.

Referring to operation 229 in Chart 3 below and similar to Wann’s three-fin FinFET embodiment, portions of the exposed regular fins (blue) are etched, as shown in Illustration 4 provided by Dr. Salahuddin. EX1003, ¶¶177-178.

Operation 229	Wann’s three-fin FinFET embodiment	Wann’s five-fin FinFET embodiment
“Etch a portion of exposed single fins” EX1007, FIG. 2.	 EX1007, FIG. 5B (annotated).	 EX1003, Illustration 4.

EX1003, Chart 3.

Referring to operation 231 in Chart 4 below and similar to Wann’s three-fin FinFET embodiment, the **photoresist layer** (green) is removed, as shown in Illustration 5 provided by Dr. Salahuddin. EX1003, ¶179.

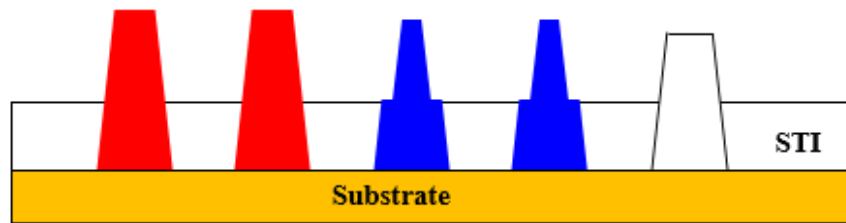
Operation 231	Wann’s three-fin FinFET embodiment	Wann’s five-fin FinFET embodiment
“Remove the photoresist layer” EX1007.	 EX1007, FIG. 6B (annotated).	 EX1003, Illustration 5.

EX1003, Chart 4.

Wann discloses that its fin-shaping process can be repeated any number of times, using the photomask and etching operations for each iteration. EX1007,

¶[0042]; EX1003, ¶180. Accordingly, the sequence of operations 217, 229, and 231 of Figure 2 can be repeated to form the 1 fin shaped in the different way in Wann’s five-fin FinFET embodiment. EX1003, ¶¶180-183.

Illustration 8 provided by Dr. Salahuddin (below) shows the resulting structure of Wann’s five-fin FinFET embodiment—as modified by Lin’s mandrel/spacer process—which can have **2 regular fins adjacent to one another** (red) and **2 fins shaped a particular way adjacent to one another** (blue) with lower parts of the fins uniformly spaced apart, just like the claimed fin-shaped structure in the ’510 patent.⁴ EX1003, ¶183.



EX1003, Illustration 8.

3. Independent Claim 1

a. [1.P]: A fin-shaped structure, comprising:

Wann and Lin disclose the preamble. EX1003, ¶¶187-190. Wann “relates generally to integrated circuit devices, and more particularly to structure and

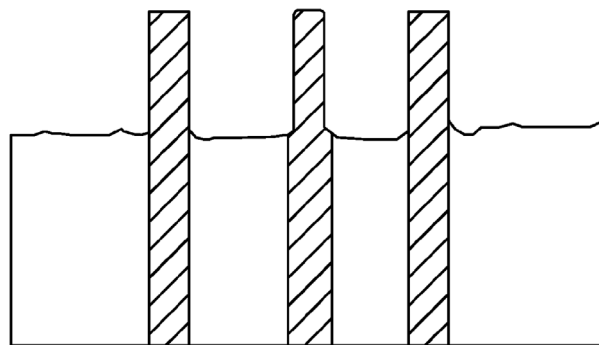
⁴ The structure shown in Illustration 8 provided by Dr. Salahuddin is also referred to herein as “the Wann-Lin five-fin FinFET structure.”

methods for forming fin field-effect transistors (FinFETs).” EX1007, ¶[0001].

Wann states that “[v]arious embodiments of the present disclosure pertain to a selective fin-shaping process to allow individual fin width and fin height control.”

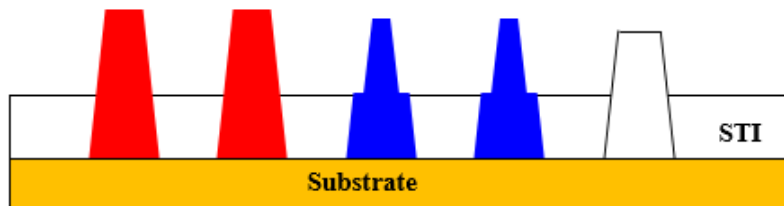
EX1007, ¶[0019]. Similarly, Lin is directed to “a method of forming a FinFET device.” EX1008, Abstract.

The ’510 patent claims can refer to a “*fin-shaped structure*” with a single FinFET or with multiple FinFETs. EX1003, ¶188. Wann teaches both. EX1003, ¶188. For example, Wann states that its disclosure is “in reference to one FinFET with 3 fins,” as shown in Figure 6B below (with a shaped fin in the middle), but “[i]n reality a FinFET may have any number of fins from 1 to several or even hundreds.” EX1007, ¶[0041]; EX1003, ¶188. Wann further states that its “disclosure is not limited [to] a FinFET having a particular number of fins.” EX1007, ¶[0041]. Wann also extends its teachings to devices with multiple FinFETs, where an “apparatus may include many FinFETs of different sizes having different number of fins.” EX1007, ¶[0042].



EX1007, FIG. 6B.

The Wann-Lin five-fin FinFET structure—shown below in Illustration 8 provided by Dr. Salahuddin (which, as discussed above, is one of the finite number of permutations of Wann’s disclosed five-fin FinFET embodiment)—is another example of a single FinFET with a fin-shaped structure. EX1003, ¶189. As discussed in Section V.C.1 above, it would have been obvious to combine Wann’s and Lin’s teachings because a POSA would have (a) been motivated to apply Lin’s mandrel/spacer process to Wann’s five-fin FinFET embodiment to improve fin reliability and manufacturability and (b) reasonably expected to succeed in doing so. EX1003, ¶189.



EX1003, Illustration 8.

- b. **[1.a]: a substrate having a plurality of first fin-shaped structures and a plurality [of] second fin-shaped structures, and the first fin-shaped structures comprising a first fin and a second fin, the second fin-shaped structures comprising a third fin and a fourth fin,**

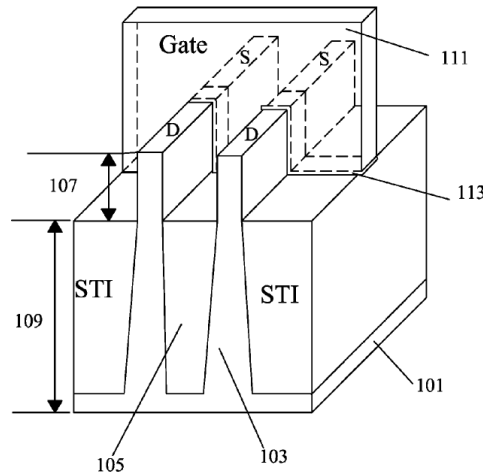
The Wann-Lin five-fin FinFET structure renders obvious this limitation.

EX1003, ¶¶191-195.

Referring to Figure 1 below, Wann discloses a FinFET with a substrate 101 having a plurality of fins 103. EX1007, ¶[0013]; EX1003, ¶192. Though a single

FinFET with two fins is shown in Figure 1, Wann discloses that “[i]n reality a FinFET may have any number of fins from 1 to several or even hundreds.”

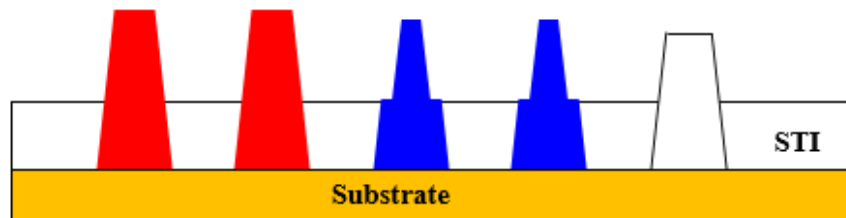
EX1007, ¶[0041].



EX1007, FIG. 1.

Referring to the Wann-Lin five-fin FinFET structure in Illustration 8 provided by Dr. Salahuddin (below), a **substrate** (orange) has **two regular fins** (red; “a plurality of first fin-shaped structures”) and **two shaped fins** (blue; “a plurality second fin-shaped structures”), as well as one fin shaped in a different way (white). The **two regular fins** (red) include two fins (“a first fin and a second fin”). The **two shaped fins** (blue) include two fins (“a third fin and a fourth fin”).

EX1003, ¶193.



EX1003, Illustration 8.

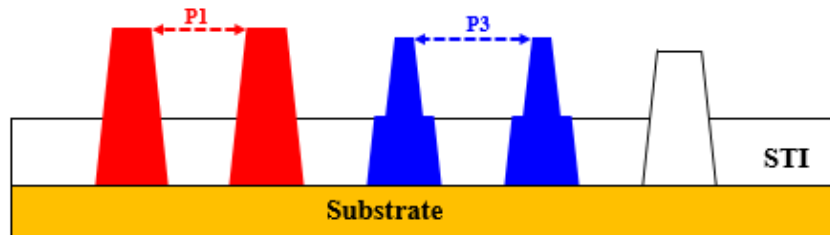
As discussed above, Wann discloses that five fins can be formed on a **substrate** (orange). As also discussed above, there are a finite number of fin arrangements satisfying Wann's disclosure of 5 fins, with two regular fins, two shaped fins, and one different fin. EX1003, ¶194. Accordingly, it would have been obvious for the two fins on the left side of the **substrate** (orange) to be the **two regular fins** (red). EX1007, ¶[0020]; EX1003, ¶194. Next, it would have been obvious, based on Wann's fin-shaping process discussed above in Section V.C.1.b, for the **two shaped fins** (blue) and the differently-shaped fin (white) to be formed such that these fins are shorter than the **two regular fins** (red). EX1007, ¶[0035]; EX1003, ¶194. Accordingly, a POSA would have understood the Wann-Lin five-fin FinFET structure to have "*a plurality of first fin-shaped structures*" and "*a plurality second fin-shaped structures.*"

- c. **[1.b]: wherein a first distance between adjacent top corners of the first fin and the second fin of the first fin-shaped structures is less than a second distance between adjacent top corners of the third fin and the fourth fin of the second fin-shaped structures**

The Wann-Lin five-fin FinFET structure renders obvious this limitation. EX1003, ¶¶196-202. Referring to the Wann-Lin five-fin FinFET structure in Illustration 10 provided by Dr. Salahuddin (below)⁵, a **first distance P1** (red; "*a*

⁵ Dr. Salahuddin provides Illustrations 9-15 to pictorially depict Wann's and

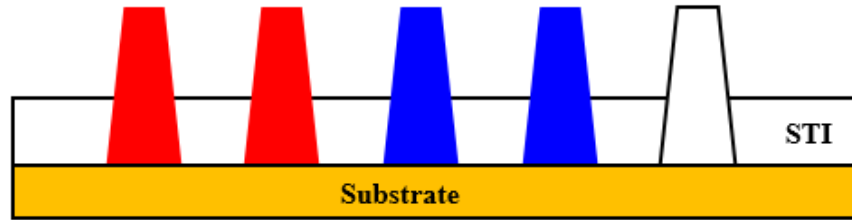
first distance”) between adjacent top corners of the **two regular fins** (red; “*the first fin and the second fin of the first fin-shaped structures*”) is less than a **second distance P3** (blue; “*a second distance*”) between adjacent top corners of the **two shaped fins** (blue; “*the third fin and the fourth fin of the second fin-shaped structures*”). EX1003, ¶196.



EX1003, Illustration 10.

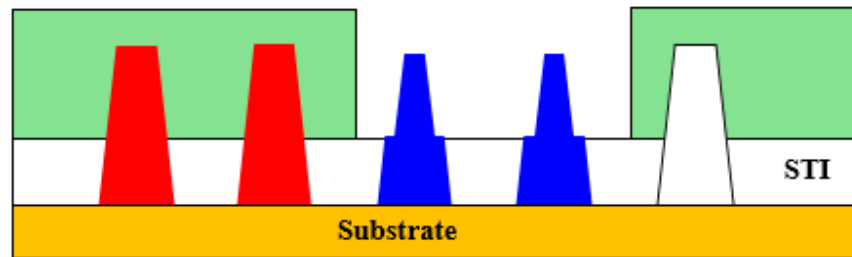
The **first distance P1** (red) is shorter than the **second distance P3** (blue) due to how the fins are formed using the Wann-Lin teachings. EX1003, ¶197. Initially, 5 regular fins (red, blue, and white) in the Wann-Lin five-fin FinFET embodiment are formed as shown in Illustration 2 provided by Dr. Salahuddin (below). EX1003, ¶197. These regular fins are the same and, as described in Section V.C.3.d below, the spacing between adjacent regular fins is also the same based on Lin’s mandrel/spacer process that forms fins with uniform dimensions and uniform spacing from one another. EX1008, ¶[0062]; EX1003, ¶197.

Lin’s textual disclosures.



EX1003, Illustration 2.

After forming the 5 regular fins, a photoresist layer is formed over the 5 regular fins and an opening is formed to expose 2 regular fins (blue), which are etched as shown in Illustration 4 provided by Dr. Salahuddin (below). EX1003, ¶¶198-199. As a result of Wann’s fin-shaping process, the exposed regular fins become the **two shaped fins** (blue). The **two shaped fins** (blue) are thinner and shorter than neighboring fins protected under a **photoresist layer** (green)—the 3 regular fins (red and white). EX1003, ¶199.



EX1003, Illustration 4.

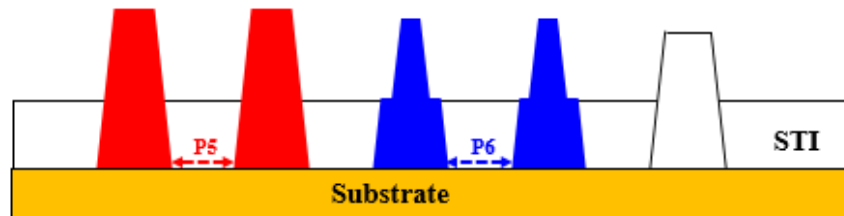
Referring to Illustration 10 provided by Dr. Salahuddin (above), because the upper parts of the **two adjacent shaped fins** (blue) are narrower than the upper parts of the **two adjacent regular fins** (red), a POSA would have understood that the Wann-Lin five-fin FinFET structure has **first distance P1** (red) between adjacent top corners of the **two adjacent regular fins** (red) that is less than **second**

distance P3 (blue) between adjacent top corners of the **two adjacent shaped fins** (blue).⁶ EX1003, ¶¶200-201.

- d. [1.c]: while a third distance between adjacent lower parts of the first fin and the second fin is the same as a fourth distance between adjacent lower parts of the third fin and the fourth fin;

The Wann-Lin five-fin FinFET structure renders obvious this limitation.

EX1003, ¶¶203-208. Referring to the Wann-Lin five-fin FinFET structure in Illustration 11 provided by Dr. Salahuddin (below), a **third distance P5** (red; “a third distance”) between adjacent lower parts of the **two regular fins** (red; “the first fin and the second fin”) is the same as a **fourth distance P6** (blue; “a fourth distance”) between adjacent lower parts of the **two shaped fins** (blue; “the third fin and the fourth fin”). EX1003, ¶203.



EX1003, Illustration 11.

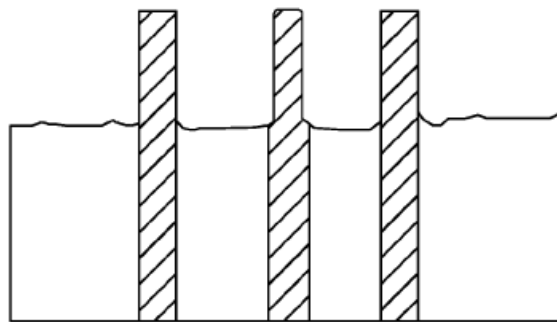
Based on Lin’s mandrel/spacer process and Wann’s fin-shaping process, a POSA would have understood that the combination of these teachings results in

⁶ As discussed in Section V.C.2, a similar fin shaping process can be used to form the 1 fin shaped in the different way (white).

third distance P5 (red) and **fourth distance P6** (blue) between each of the two fin types. EX1003, ¶204. Further, a POSA would have understood that the **third distance P5** (red) and **fourth distance P6** (blue) are the *same* as claimed.

Specifically, Lin describes a mandrel/spacer process that forms fins with uniform dimensions and uniform spacing from one another. EX1003, ¶205; EX1008, ¶[0062] (“[T]he spacing and depth between the fins 50 are better controlled and may be substantially equal between all of the fins 50.”).

Additionally, referring to Wann’s fin-shaping process for Wann’s three-fin FinFET embodiment in Figure 6B below—which applies to Wann’s five-fin FinFET embodiment—the middle fin has been shaped. EX1007, ¶[0035]. Though a top portion of the middle fin has been shaped, Wann states that “[t]he bottom portions of all three fins are substantially the same, because the bottom portions are not shaped.” EX1007, ¶[0035].



EX1007, FIG. 6B.

Based on the above teachings from Wann and Lin, the Wann-Lin five-fin FinFET structure (as shown above in Illustration 11 provided by Dr. Salahuddin)

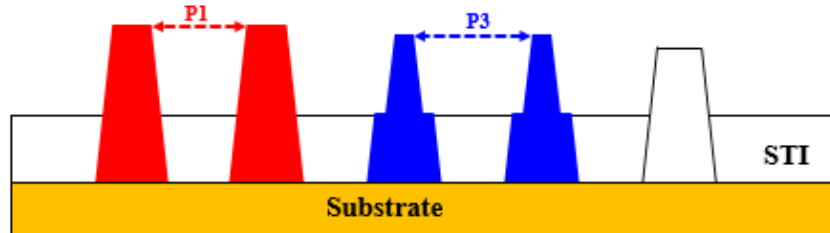
renders obvious that **third distance P5** (red) between adjacent lower parts of the **two adjacent regular fins** (red) is the same as **fourth distance P6** (blue) between adjacent lower parts of the **two adjacent shaped fins** (blue), because the bottom portions of the **two adjacent regular fins** (red) and the **two adjacent shaped fins** (blue) were made at a uniform distance apart before shaping (as described in Lin) and the bottoms of the fins are substantially unchanged throughout Wann's fin-shaping process. EX1003, ¶¶206-207.

e. [1.d]: and wherein the adjacent top corners are directly opposite each other.

The Wann-Lin five-fin FinFET structure renders obvious this limitation. EX1003, ¶¶209-211. Since there are two "*adjacent top corners*" recited in limitation [1.b], the "*adjacent top corners*" in limitation [1.d] refers to "*adjacent top corners of the first fin and the second fin*" and/or to the "*adjacent top corners of the third fin and the fourth fin*" recited in limitation [1.b]. EX1003, ¶209.

Referring to the Wann-Lin five-fin FinFET structure in Illustration 10 provided by Dr. Salahuddin (below), the top corners of the **two adjacent regular fins** are directly opposite each other and thus adjacent, and the top corners of the **two adjacent shaped fins** are directly opposite each other and thus adjacent; therefore, the Wann-Lin five-fin FinFET structure teaches limitation [1.d]. These are the same top corners referred to above when addressing the measurement of **first distance P1** (red) between adjacent top corners of the **two adjacent regular**

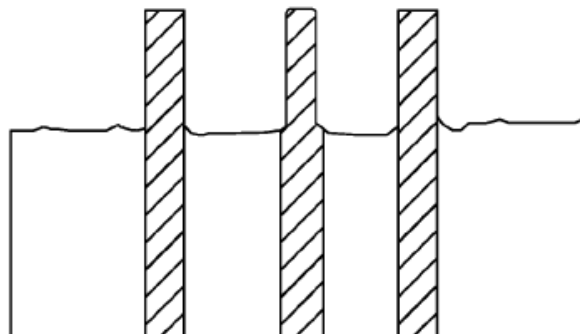
fin and **second distance P3** (blue) between adjacent top corners of the **two adjacent shaped fins**. EX1003, ¶210.



EX1003, Illustration 10.

- 4. Dependent Claim 2: wherein the width of each top part of the first fin-shaped structures is larger than the width of each top part of the second fin-shaped structures.**

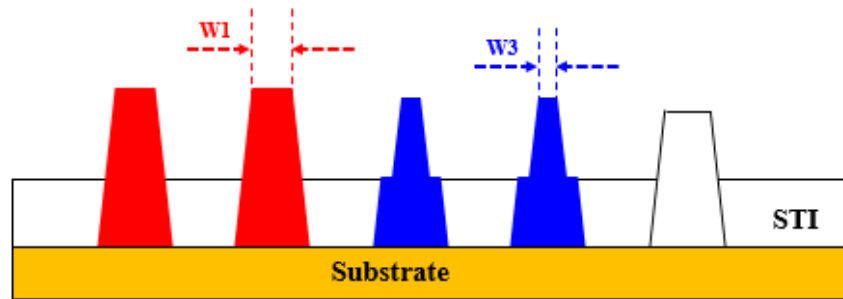
The Wann-Lin five-fin FinFET structure renders obvious claim 2. EX1003, ¶¶212-214. Referring to Figure 6B below, Wann explains that “[t]he shaped fin has a narrower top portion that may be the same, slightly shorter, or longer than the neighboring regular fins.” EX1007, ¶[0035]. A POSA would have understood that this teaching is applicable to the **two adjacent regular fins** and the **two adjacent shaped fins** in the Wann-Lin five-fin FinFET structure. EX1003, ¶212.



EX1007, FIG. 6B.

Referring to the Wann-Lin five-fin FinFET structure in Illustration 12

provided by Dr. Salahuddin (below), a **width W1** (red) of each top part of the **two regular fins** (red; “*first fin-shaped structures*”) is larger than a **width W3** (blue) of each top part of **two shaped fins** (blue; “*second fin-shaped structures*”). EX1003, ¶213.



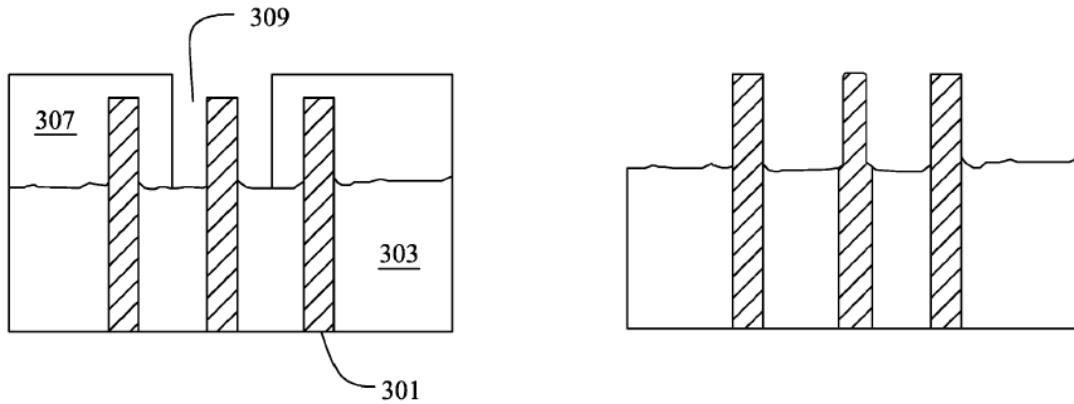
EX1003, Illustration 12.

5. Dependent Claim 3

- a. **[3.a]: an isolation structure disposed beside the first fin-shaped structures and beside the second fin-shaped structures respectively,**

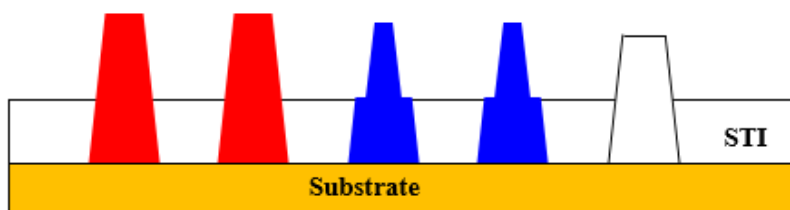
The Wann-Lin five-fin FinFET structure renders obvious this limitation. EX1003, ¶¶215-217. Referring to Figure 3B below, Wann explains that “fins partially embedded in shallow trench isolation (STI) layers are formed on a semiconductor substrate.” EX1007, ¶[0020]. Referring to Figure 6B below, while one or more top portions of the fins may be exposed to Wann’s fin-shaping process, bottom portions of the regular and shaped fins remain embedded in the STI layer and are unchanged. EX1007, ¶[0035]; EX1003, ¶216. A POSA would have understood that these teachings are applicable to the STI layer surrounding

the **two adjacent regular fins** and the **two adjacent shaped fins** in the Wann-Lin five-fin FinFET structure. EX1003, ¶216.



EX1007, FIGs. 3B (left) and 6B (right).

Referring to the Wann-Lin five-fin FinFET structure in Illustration 8 provided by Dr. Salahuddin (below), an STI layer (“*an isolation structure*”) is disposed beside the **two adjacent regular fins** (red; “*first fin-shaped structures*”) and beside the **two adjacent shaped fins** (blue; “*second fin-shaped structures*”) respectively. EX1003, ¶¶215-217.



EX1003, Illustration 8.

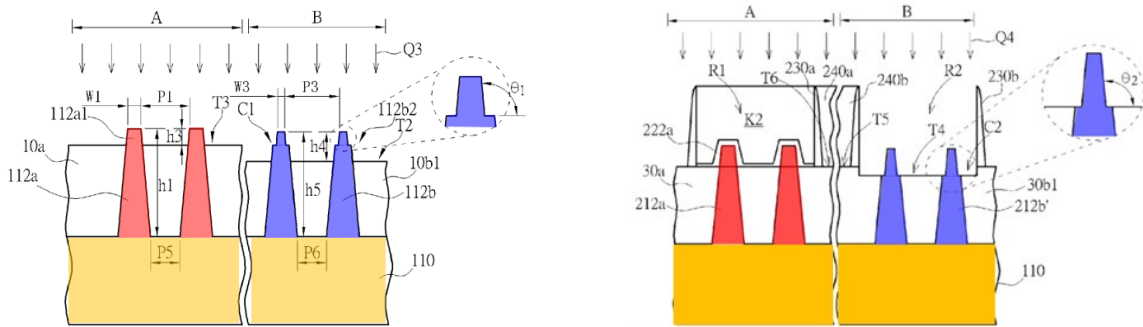
- b. [3.b]: and ladder-shaped cross-sectional profile parts of the second fin-shaped structures are higher than a top surface of the isolation structure.

The Wann-Lin five-fin FinFET structure renders obvious this limitation.

EX1003, ¶¶218-225. Figures 5 and 8 of the '510 patent (below) show examples of

ladder-shaped cross-sectional profile parts of **second fin-shaped structures**

112b/212b' (blue; shown in dashed line inset). EX1003, ¶218. The '510 patent describes these structures as having a bending angle θ_1/θ_2 preferably larger than or equal to 90° . EX1001, 5:13-18, 7:14-21. The Wann-Lin five-fin FinFET structure teaches this structure. EX1003, ¶218.

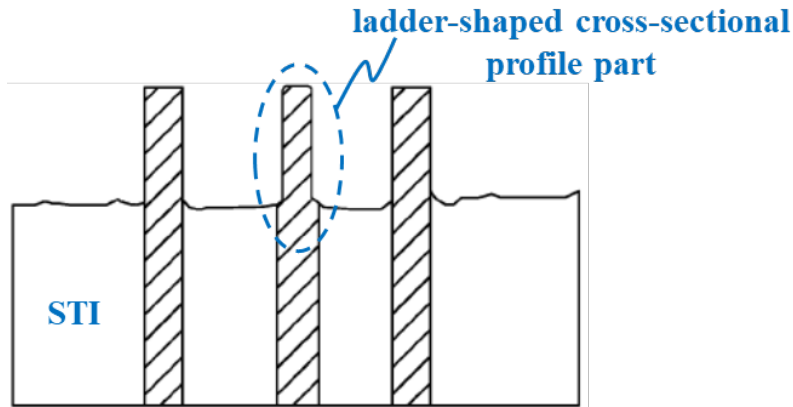


EX1001, FIG. 5 (left; annotated) and 8 (right; annotated).

In its fin-shaping process, referring to Figure 6B below, Wann states that “while the shaped fin may be shorter than the regular fins, the top portion of the shaped fin may be the same length or longer than the top portion of regular fins because the STI layer is also etched and more of the top portion of the shaped fin may be exposed.” EX1007, ¶[0035]. During Wann’s fin-shaping process, “the STI layer is also etched and more of the top portion of the shaped fin may be exposed.” EX1007, ¶[0035]. Accordingly, as would be understood by a POSA, a ladder-shaped cross-sectional profile part of the shaped fins is formed above the STI layer—similar to the ladder-shaped cross-sectional profile parts of the second fin-

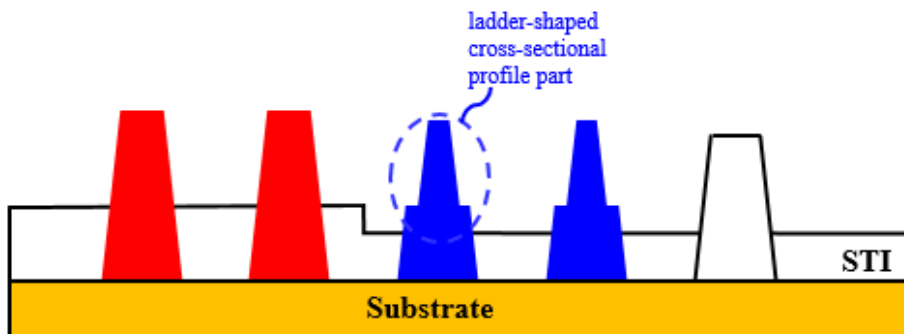
shaped structures in Figure 5 of the '510 patent (blue; see inset in dashed circle).

EX1003, ¶219.



EX1007, FIG. 6B (annotated).

Referring to the Wann-Lin five-fin FinFET structure in Illustration 13 provided by Dr. Salahuddin (below), due to Wann’s fin-shaping process, ladder-shaped cross-sectional profile parts of the **two adjacent shaped fins** (“*second fin-shaped structures*”) are higher than a top surface of the STI layer (“*isolation structure*”). EX1003, ¶220. This is because, during Wann’s fin-shaping process, “the STI layer is also etched and more of the top portion of the shaped fin may be exposed.” EX1007, ¶[0035].



EX1003, Illustration 13.

To the extent Patent Owner alleges Wann does not explicitly disclose limitation [3.b], a POSA would have understood that the height of the STI layer surrounding the shaped fin can vary for circuit design flexibility, based on a desired effective channel width. EX1007, ¶[0036]; EX1003, ¶221. Wann explains that, to achieve the desired effective channel width, “[t]he various etching methods discussed herein can shape the exposed fin a number of ways to create a profile that reduces the fin height and/or width.” EX1007, ¶[0036]. For example, referring to Figure 6B of Wann above, the STI layer around the shaped fin can be further etched—using the etching process described above—to decrease the height of the STI layer surrounding the shaped fin such that the ladder-shaped cross-sectional profile part is higher than a top surface of the STI layer. EX1003, ¶221.

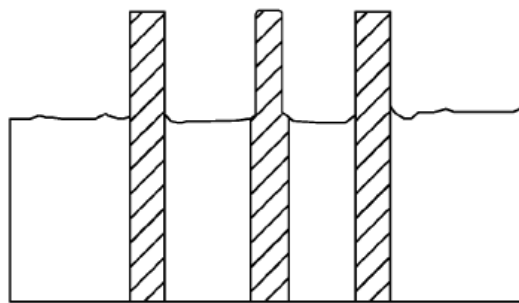
During the etching process, the ladder-shaped cross-sectional profile part maintains its shape because the etching process can be selective and remove the STI layer surrounding the shaped fin. EX1007, ¶[0035]; EX1003, ¶222. As a result, “[t]he change in profile then allows a FinFET to have an effective channel width that is not an integer multiple of a regular fin.” EX1007, ¶[0036].

Wann’s teachings above are also applicable to the Wann-Lin five-fin FinFET structure, where the heights of the STI layer surrounding the **two adjacent regular fins** (red) and the **two adjacent shaped fins** (blue) can vary based on a desired effective channel width, as shown above in Illustration 13 provided by Dr.

Salahuddin. EX1003, ¶224. Accordingly, a POSA would have understood that the ladder-shaped cross-sectional profile parts of the **two adjacent shaped fins** in the Wann-Lin five-fin FinFET structure can be higher than a top surface of the STI layer. EX1003, ¶¶218-224.

6. Dependent Claim 4: wherein a top surface of the isolation structure of a first area is higher a top surface of the isolation structure of a second area.

The Wann-Lin five-fin FinFET structure renders obvious claim 4 (which depends from claim 3). EX1003, ¶¶226-229. As discussed above with respect to dependent claim 3 (Section V.C.5) from which claim 4 depends, referring to Figure 6B below, Wann states that “while the shaped fin may be shorter than the regular fins, the top portion of the shaped fin may be the same length or longer than the top portion of regular fins because **the STI layer is also etched and more of the top portion of the shaped fin may be exposed.**”⁷ EX1007, ¶[0035].

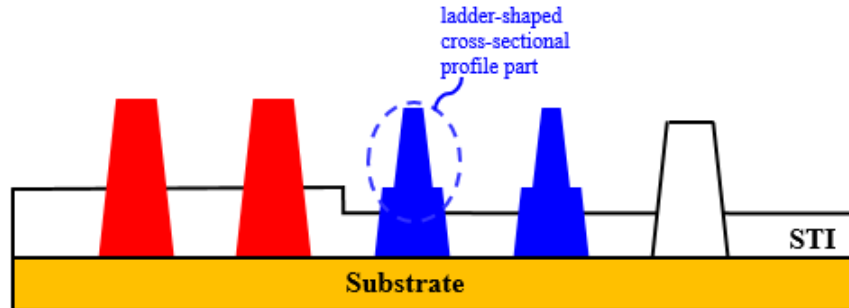


EX1007, FIG. 6B.

⁷ Emphasis added unless otherwise noted.

Referring to the Wann-Lin five-fin FinFET structure in Illustration 13

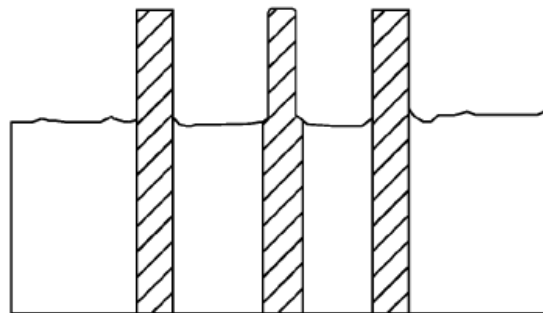
provided by Dr. Salahuddin (below), a POSA would have understood that the top surface of the STI layer surrounding the **two adjacent regular fins** (red) is higher than a top surface of the STI layer surrounding the **two adjacent shaped fins** (blue) because the STI layer surrounding the **two adjacent shaped fins** (blue) is also etched during Wann's fin-shaping process. EX1003, ¶226. Thus, a top surface of the STI layer surrounding the **two adjacent regular fins** (red; "*the isolation structure of a first area*") is higher than a top surface of the STI layer surrounding the **two adjacent shaped fins** (blue; "*the isolation structure of a second area*"). EX1003, ¶¶226-228.



EX1003, Illustration 13.

7. **Dependent Claim 5: wherein a height of the first fin-shaped structures protruding from the isolation structure is lower than a height of the second fin-shaped structures protruding from the isolation structure.**

The Wann-Lin five-fin FinFET structure renders obvious claim 5. EX1003, ¶¶230-233.⁸ As discussed above in Section V.C.5, referring to Figure 6B below, Wann states that “while the shaped fin may be shorter than the regular fins, **the top portion of the shaped fin may be the same length or longer than the top portion of regular fins** because the STI layer is also etched and more of the top portion of the shaped fin may be exposed.” EX1007, ¶[0035].

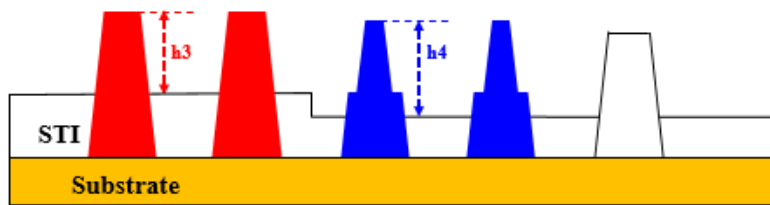


EX1007, FIG. 6B.

Referring to the Wann-Lin five-fin FinFET structure in Illustration 14 provided by Dr. Salahuddin (below), a POSA would have understood that **a height h3 of the two adjacent regular fins** (red) protruding from the STI layer is higher

⁸ For purposes of this IPR proceeding, “*the* isolation structure” recited in claim 5 is assumed to be “*an* isolation structure,” since the term “isolation structure” is not recited in independent claim 1, from which claim 5 depends.

than **a height h4 of the two adjacent shaped fins** (blue) protruding from the STI layer because the STI layer surrounding the **two adjacent shaped fins** (blue) is also etched during Wann's fin-shaping process, as discussed above. EX1003, ¶¶230-232. Put differently, **a height h3 of the two adjacent regular fins** ("the first fin-shaped structures") protruding from the STI layer ("the isolation structure") is lower than **a height h4 of the two adjacent shaped fins** ("the second fin-shaped structures") protruding from the STI layer ("the isolation structure"). EX1003, ¶232.

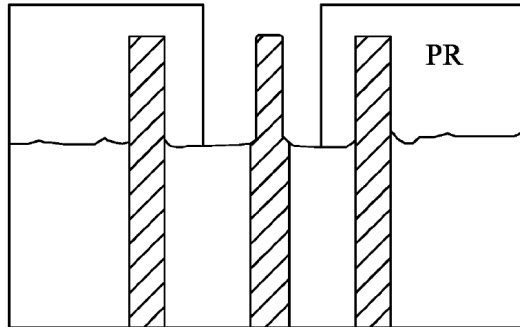


EX1007, Illustration 14.

8. **Dependent Claim 6: wherein a height of the first fin-shaped structures protruding from the substrate is higher than a height of the second fin-shaped structures protruding from the substrate.**

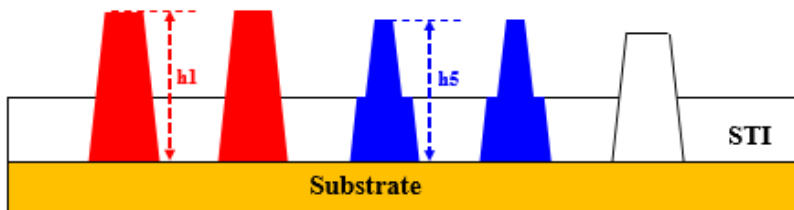
The Wann-Lin five-fin FinFET structure renders obvious claim 6. EX1003, ¶¶234-237. As discussed above in Section V.C.5, Wann states that "**while the shaped fin may be shorter than the regular fins**, the top portion of the shaped fin may be the same length or longer than the top portion of regular fins because the STI layer is also etched and more of the top portion of the shaped fin may be exposed." EX1007, ¶[0035]. Further, with regard to Figure 5B below, Wann states

“the exposed single fin is thinner and somewhat shorter than neighboring fins that are protected under the photoresist.” EX1007, ¶[0029].



EX1007, FIG. 5B.

Referring to the Wann-Lin five-fin FinFET structure in Illustration 15 provided by Dr. Salahuddin (below), a POSA would have understood that **a height h1 of the two adjacent regular fins** (red; “*first fin-shaped structures*”) protruding from the substrate is higher than **a height h5 of the two adjacent shaped fins** (blue; “*second fin-shaped structures*”) protruding from the substrate. EX1003, ¶¶234-237.



EX1003, Illustration 15.

VI. MANDATORY NOTICES (37 C.F.R. § 42.8(A)(1))

REAL PARTY-IN-INTEREST: The real party-in-interest is Taiwan Semiconductor Manufacturing Company Ltd.

RELATED MATTERS: U.S. Patent Nos. 10,930,517 and 10,418,251 claim the benefit of the '510 patent.

LEAD AND BACK-UP COUNSEL: Under 37 C.F.R. §§ 42.8(b)(3) and 42.10(a), Petitioner appoints **Christian A. Camarce** (Reg. No. 65,021) as lead counsel; and **Donald R. Banowit** (Reg. No. 42,289), **Richard Bemben** (Reg. No. 68,658), and **Zhichun Zhang** (Reg. No. 77,776) as back-up counsel, all at the address: STERNE, KESSLER, GOLDSTEIN & FOX PLLC, 1101 K Street, NW, 10th Floor, Washington, DC, 20005, phone (202) 371-2600, and facsimile (202) 371-2540.

SERVICE INFORMATION: Petitioner consents to electronic service by email at: **ccamarce-PTAB@sternekessler.com**, **dbanowit-PTAB@sternekessler.com**, **rbemben-PTAB@sternekessler.com**, **zzhang-PTAB@sternekessler.com**, and **PTAB@sternekessler.com**.

VII. GROUNDS FOR STANDING (37 C.F.R. § 42.104(A))

The undersigned and Petitioner certify that the '510 patent is available for *inter partes* review. Petitioner is not barred or estopped from requesting *inter partes* review on the grounds herein.

VIII. CONCLUSION

For the reasons above, *inter partes* review and cancellation of claims 1-6 of the '510 patent are requested.

Respectfully submitted,

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IX. CLAIMS APPENDIX

1. [1.P] A fin-shaped structure, comprising:

[1.a] a substrate having a plurality of first fin-shaped structures and a plurality [of] second fin-shaped structures, and the first fin-shaped structures comprising a first fin and a second fin, the second fin-shaped structures comprising a third fin and a fourth fin,

[1.b] wherein a first distance between adjacent top corners of the first fin and the second fin of the first fin-shaped structures is less than a second distance between adjacent top corners of the third fin and the fourth fin of the second fin-shaped structures

[1.c] while a third distance between adjacent lower parts of the first fin and the second fin is the same as a fourth distance between adjacent lower parts of the third fin and the fourth fin;

[1.d] and wherein the adjacent top corners are directly opposite each other.

2. The fin-shaped structure according to claim 1, wherein the width of each top part of the first fin-shaped structures is larger than the width of each top part of the second fin-shaped structures.

3. The fin-shaped structure according to claim 1, further comprising:
 - [3.a]** an isolation structure disposed beside the first fin-shaped structures and beside the second fin-shaped structures respectively,
 - [3.b]** and ladder-shaped cross-sectional profile parts of the second fin-shaped structures are higher than a top surface of the isolation structure.

4. The fin-shaped structure according to claim 3, wherein a top surface of the isolation structure of a first area is higher a top surface of the isolation structure of a second area.

5. The fin-shaped structure according to claim 1, wherein a height of the first fin-shaped structures protruding from the isolation structure is lower than a height of the second fin-shaped structures protruding from the isolation structure.

6. The fin-shaped structure according to claim 1, wherein a height of the first fin-shaped structures protruding from the substrate is higher than a height of the second fin-shaped structures protruding from the substrate.

CERTIFICATE OF WORD COUNT (37 C.F.R. § 42.24(d))

1. This Petition complies with the type-volume limitation of 14,000 words, comprising 13,064 words, excluding the parts exempted by 37 C.F.R. § 42.24(a).

2. This Petition complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft® Word 2016 in 14-point Times New Roman.

Respectfully submitted,

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CERTIFICATE OF SERVICE (37 C.F.R. §§ 42.6(e), 42.105(a))

The undersigned hereby certifies that on August 29, 2025, true and correct copies of the foregoing **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,786,510** and all associated exhibits were served in their entireties on the following parties via FedEx Express®:

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