

4. The integrated circuit of claim 1, further comprising power supply lines in at least a second layer of the IC.

5. The integrated circuit of claim 1, wherein the power supply lines are coupled to the shielding mesh through vias between the first layer and the at least one layer.

6. The integrated circuit of claim 1, wherein at least one of the power supply lines is coupled to at least two of the first plurality of lines.

7. The integrated circuit of claim 1, wherein shielding mesh is configured to even out a distribution of temperatures on the IC, the shielding mesh including a first line on the at least one layer of the IC to carry the first reference voltage and a second line on the at least one layer of the IC to carry the second reference voltage.

8. The integrated circuit of claim 7, wherein the first line and the second line are substantially parallel.

9. The integrated circuit of claim 7, wherein the temperatures are determined at a plurality of different locations on the IC.

10. The integrated circuit of claim 7, wherein the temperatures represent a temperature profile of the IC and wherein the shielding mesh is configured to reduce a variation of the temperatures in the temperature profile.

11. The integrated circuit of claim 7, wherein the temperatures are determined through at least one of a processing device and a measuring device.

12. The integrated circuit of claim 7 wherein the temperatures are estimated temperatures determined while designing the IC with a computer aided design (CAD) process.

13. The integrated circuit of claim 7, wherein the shielding mesh is represented by at least one of data representing the shielding mesh in a CAD software and at least one mask layer used to manufacture the IC.

14. A method to manufacture an integrated circuit (IC) comprising:

generating using a processor a representation of a shielding mesh in at least one layer of a representation of a design of the IC, the shielding mesh having a first plurality of lines which are designed to provide a first reference voltage and having a second plurality of lines which are

designed to provide a second reference voltage and wherein the shielding mesh comprises a window in which signal lines are routed with less shielding than signal lines which are routed in the shielding mesh; and generating using a processor a representation of power supply lines in at least a first layer of the representation of the IC, the first layer containing the representation of the power supply lines being different than the at least one layer which contains the shielding mesh, the power supply lines being coupled to the shielding mesh and being larger in width than the first plurality of lines and the second plurality of lines, wherein shielding mesh is configured to even out a distribution of temperatures on the IC, the shielding mesh including a first line on the at least one layer of the IC to carry the first reference voltage and a second line on the at least one layer of the IC to carry the second reference voltage.

15. The method of claim 14, wherein the shielding mesh is inserted into at least one layer of the IC if the distribution of temperatures is substantially uneven.

16. The method of claim 14, wherein the first line and the second line are substantially parallel.

17. The method of claim 14, wherein the temperatures are determined at a plurality of different locations on the IC.

18. The method of claim 14, wherein the temperatures represent a temperature profile of the IC and wherein the shielding mesh is configured to reduce a variation of the temperatures in the temperature profile.

19. The method of claim 14, wherein the temperatures are determined through at least one of a processing device and a measuring device.

20. The method of claim 14, wherein the temperatures are estimated temperatures determined while designing the IC with a computer aided design (CAD) process.

21. The method of claim 14, wherein the shielding mesh is represented by at least one of data representing the shielding mesh in a CAD software and at least one mask layer used to manufacture the IC.

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