A 5-V-Only One-Transistor 256K EEPROM with Page-Mode Erase

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***Abstract*—A 5-V-only one-transistor 256K EEPROM with page-mode erase is described. Erasing and programming are achieved through electron tunneling. In order to inhibit the programming to the unselected cells, the unselected bit lines and word lines are applied with the program-inhibiting voltages. The number of parity bits for ECC is five per two bytes, which are controlled by the lower byte (LB) signal. Using a conventional 1.5-μm design rule n-well CMOS process with a single metal layer and two polysilicon layers, the memory cell size is 7×8 μm² and the chip size is 5.55×7.05 mm². The chip size is reduced to 70 percent of a full-featured EEPROM with on-chip ECC.**

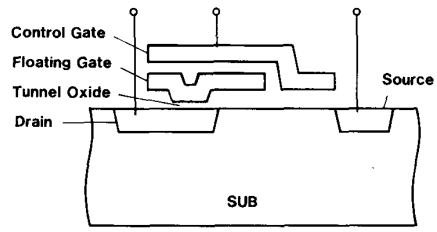

Fig. 1. Cross section of one-transistor memory cell.

I. Introduction

RECENTLY, several types of the flash EEPROM have been proposed [1]–[3]. These flash EEPROM's have an EPROM-like one-transistor memory cell and all memory cells are erased electrically. They can be housed in an inexpensive plastic package and still be fully tested in contrast to a one-time PROM. However, they require an external high voltage supply for programming. Furthermore, their ERASE/WRITE cycling is limited to less than 1000 cycles, because programming is accomplished by hot-electron injection into the floating gate. On the other hand, full-featured EEPROM's [4], [5] which are byte erasable are guaranteed 10^4–10^6 ERASE/WRITE (E/W) cycles, because these are erased and programmed by the Fowler–Nordheim tunneling current. The ECC technique is also used to enhance the endurance. The memory cell, however, consists of a bit select transistor per bit, a memory transistor per bit, and a byte select transistor per byte. Because of the large cell size and four parity bits per byte required for ECC, the chip size is two to three times larger than those of EPROM's and flash EEPROM's.

This paper presents a 5-V-only one-transistor page erase type 256K EEPROM in order to realize a highly reliable and small chip size EEPROM. The 256K EEPROM is erased and programmed by the electron tunneling and is program inhibited by program-inhibiting voltages applied to the drains and the control gates of unselected memory cells. The number of parity bits for ECC is five per two bytes controlled by the lower byte (LB) signal. LB is the lowest address input. The chip size has been reduced to 70 percent of conventional EEPROM's by the small size memory cell and reduction of the parity bits. The device has fast 2-byte serial access mode.

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II. One-Transistor Cell Technology

A. Cell Structure and Programming Scheme

The cell cross section is shown in Fig. 1. The cell is based on the FLOTOX-type EEPROM cell, and integrates the select transistor. The cell size is reduced to 80 percent of a full-featured EEPROM. The first-level polysilicon is a floating gate and the second-level polysilicon is a control gate and a select gate. The tunnel oxide layer is located between the floating gate and the drain. The thickness of the tunnel oxide and the oxide between the polysilicon gates is 100 and 300 Å, respectively. Because the select gate is merged into the control gate, the program-inhibiting voltage must be applied to the unselected cells.

The programming scheme of the cell is shown in Fig. 2. The erase operation is similar to that of a conventional EEPROM. The selected word line, WL_k, is applied with a programming high voltage V_{PP}, and all bit lines are grounded. Only the selected cells that correspond to $M1$ and $M2$ are erased. $M1$ and $M2$ are written ONE. In a program operation, bit lines connected to the memory cells to be written ZERO are applied with V_{PP}. In order to inhibit the programming of the unselected cells, the unselected bit lines and word lines are applied with program-inhibiting voltages V_{BPI} and V_{WPI}, respectively. Table I shows the

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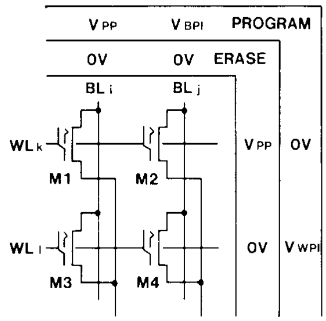

Fig. 2. Programming scheme of cell.

TABLE I
POTENTIAL DIFFERENCE IN PROGRAM CYCLE

Cell	VD - VG
M1	V_{PP}
M2	V_{BPI}
M3	$V_{PP} - V_{WPI}$
M4	$V_{BPI} - V_{WPI}$

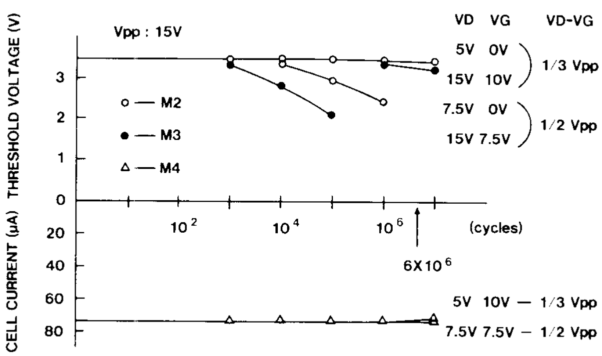

Fig. 3. Program-inhibiting characteristics. Cell current: $V_D = 1$ V, $V_G = 2$ V.

potential difference between the control gate and the drain of the cells in the program operation. The potential difference of $M2$, $M3$, and $M4$ is small enough to be compared with that of $M1$. As the tunneling current strongly depends on the electric field across the oxide, it is possible to prevent programming of the unselected cells. Consequently, the only selected cell that corresponds to $M1$ is programmed (ZERO is written), $M2$ retains the data ONE, and the other cells maintain the previous condition. Each cell has its own source line, and all source lines are held floating in the program operation. There is no leakage current flown through the unselected cells ($M3$, $M4$).

B. Cell Characteristics

The program-inhibiting characteristics of a single-bit test device are shown in Fig. 3. The cell is erased and programmed by a 4-ms 15-V V_{PP} pulse. The open circles, black circles, and triangles correspond to the unselected

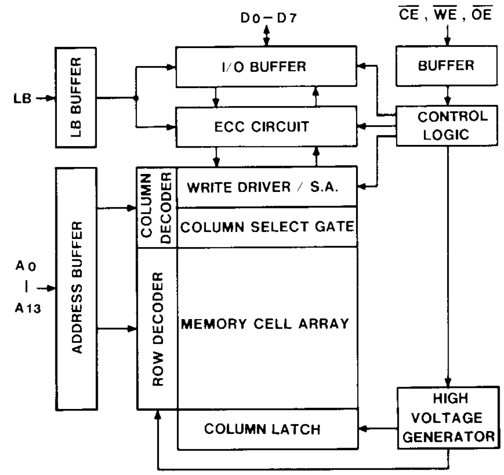

Fig. 4. Block diagram of 256K EEPROM.

memory cells $M2$, $M3$, and $M4$, respectively. It is shown that if V_{BPI} is set to 2/3 V_{PP} (10 V) and V_{WPI} is set to 1/3 V_{PP} (5 V), the program-inhibitable cycling is over 10^7 cycles. In a page-mode-only 256K EEPROM that consists of 512 pages of 64 bytes, the program-inhibitable cycling required is 511 (the number of word lines minus one) times 10^4 (E/W cycles). So the 10^7 cycles is enough to realize a page erase type 256K EEPROM with this architecture. Although the potential difference between the drain and the control gate is maintained to be the same, the program-inhibiting characteristics between the two conditions, that is $V_D = V_{BPI}$, $V_G = 0$ V (designated by open circles) and $V_D = V_{PP}$, $V_G = V_{WPI}$ (black circles), are different. It is estimated that the difference is caused by the coupling between the floating gate and the substrate (channel region). When $V_D = V_{PP}$ and $V_G = V_{WPI}$, the average potential of the channel relative to the drain is lower than that of the other condition, so that the potential difference between the floating gate and the drain is larger.

III. CIRCUIT TECHNOLOGY OF 256K EEPROM

As described above, in order to realize the 5-V-only one-transistor EEPROM, program-inhibiting voltages must be generated on the same chip and distributed to the bit lines and the word lines. A high-voltage generator which supplies V_{PP} and program-inhibiting voltages (V_{WPI}, V_{BPI}) and a column latch circuit which includes a data latch for page-mode programming and a high-voltage switching circuit were developed. As the erase mode is restricted to page mode, parity bit reduction is possible. In the normal full-featured EEPROM [4], four parity bits are generated from eight bits. In this device, five parity bits are generated from the serially inputted two bytes. These two bytes are controlled by the LB signal that is the lowest address input. A block diagram of the 256K EEPROM is shown in Fig. 4. The memory cell array consists of 16K words of 16 bits. The higher order address bits $A_5 - A_{13}$ select row address, and $A_0 - A_4$ and LB select column address.

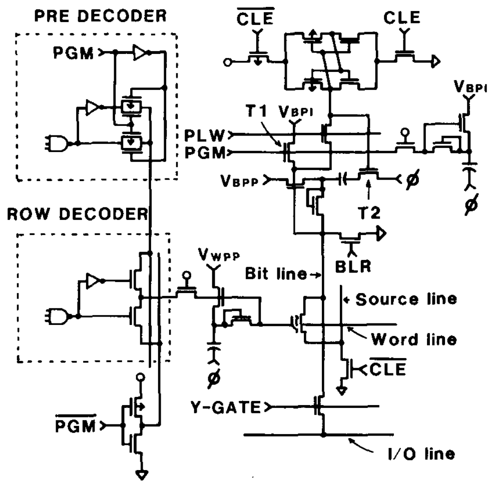

Fig. 5. Circuit diagram of column latch and row decoder.

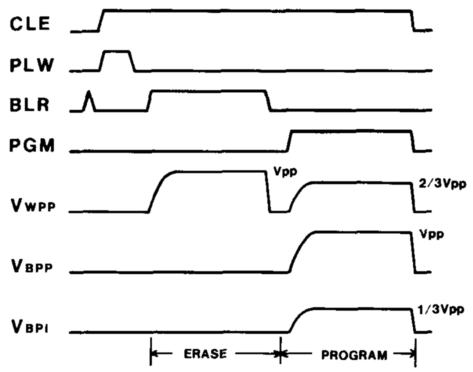

Fig. 6. Clock timing diagram.

A. Column Latch and Row Decoder

A circuit diagram of the column latch and row decoder is shown in Fig. 5. The clock timing diagram is shown in Fig. 6. A V_{PP} switch is a high-voltage pumping circuit. In an erase operation, *PGM* is set to "L," and the selected word line is pumped up to V_{PP} by the V_{PP} switch and unselected word lines are grounded. As *BLR* is set to "H," all bit lines are grounded. The electric field across the tunnel oxide in the selected cell causes electrons to tunnel from the drain to the floating gate. The threshold voltage of the selected cell shifts high.

In a program operation, as *PGM* is set to "H," all bit lines are precharged to V_{BPI} through a transistor $T1$. If the latched data are high, transistor $T2$ turns on. Then, the only bit lines that are latched "H" are pumped up to V_{PP} by the V_{PP} switch circuit. The other bit lines are maintained at V_{BPI} level. The selected word line is grounded and the unselected word lines are applied with the program-inhibiting voltage V_{WPI} by the inverting circuit of the row decoder output. The threshold voltage of the selected cell shifts low. The inverting circuit of the row decoder output consists of a predecoder, a row decoder, and an inverter. In a READ and ERASE cycle, this circuit acts as a normal row decoder.

This device also has a flash erase mode that is accomplished by applying V_{PP} to all word lines and grounding all bit lines.

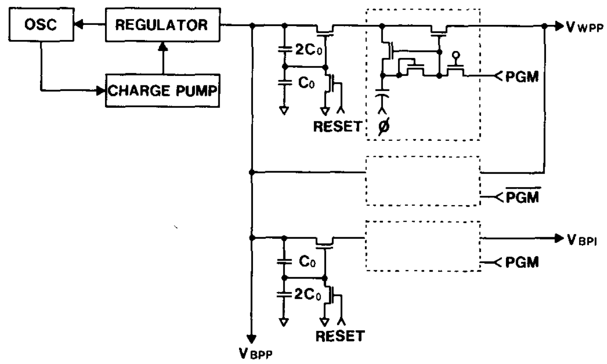

Fig. 7. Block diagram of high-voltage generator.

B. High-Voltage Generator

A block diagram of the high-voltage generator is shown in Fig. 7. All high voltages, V_{BPP}, V_{WPP}, and V_{BPI}, are generated internally. V_{BPP} (programming high voltage, V_{PP}) and V_{BPI} (program-inhibiting voltage, $1/3\ V_{PP}$) are applied to bit lines and V_{WPP} is applied to word lines. V_{WPP} has two different voltage levels that correspond to V_{PP} (erasing high voltage) and V_{WPI} (program-inhibiting voltage, $2/3\ V_{PP}$). As the program-inhibiting characteristics of the cell are sensitive to the potential difference between the control gate and the drain, the ratio of program-inhibiting voltage to V_{PP} must be accurate. Therefore, the program-inhibiting voltage is generated from the divided output of only one charge pump circuit. As there is no dc pass to the ground, the current drivability of the charge pump is enough to feed the capacitance of all bit lines and word lines. Each voltage level difference between V_{BPP} and V_{WPI}, V_{WPI} and V_{BPI} is always maintained to be $1/3\ V_{PP}$ level in the program operation. Accordingly, the program disturbance is minimized. The frequency of the oscillator is 7 MHz. The V_{BPP} level is controlled to be 15 V by the V_{PP} regulator. V_{WPI} and V_{BPI} are regulated to be 10 and 5 V, respectively.

C. ECC Circuit

The floating-gate-type EEPROM's with tunnel oxide have a failure mode of the tunnel oxide breakdown. The intrinsic cell endurance has been demonstrated to be more than 10^6 E/W cycles. However, there is a possibility of a few weak bits in the memory array wearing out in less than 10^4 cycles. As the probability is negligible that any two bits in the neighboring two bytes will be worn out in 10^4 cycles, the device has been designed to correct any single bit error in each two bytes. An ECC block diagram is shown in Fig. 8. In a WRITE cycle, two bytes of data, that

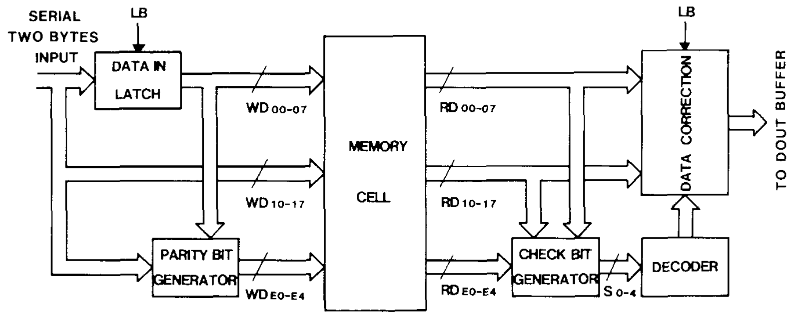

Fig. 8. Block diagram of ECC.

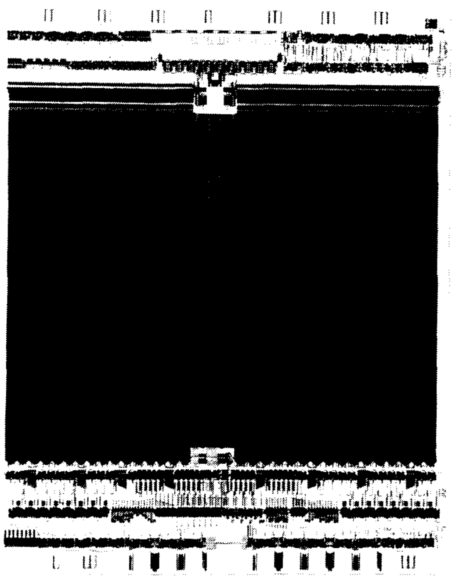

Fig. 9. Photomicrograph of 256K EEPROM.

TABLE II
FEATURES AND MEASURED AC CHARACTERISTICS OF DEVICE

Process	1.5μm design rule
	N-well CMOS
	single metal, double polysilicon
Organization	32K $\times$ 8b
Cell Size	7 $\times$ 8 μm^2
Chip Size	5.55 $\times$ 7.05 mm^2
Address Access Time	80 nsec
LB Access Time	20 nsec
Programming Time	10 msec/page
Active Current	40 mA
Standby Current	100 μA
Supply Voltage	single 5V
Pin Out	28 pin

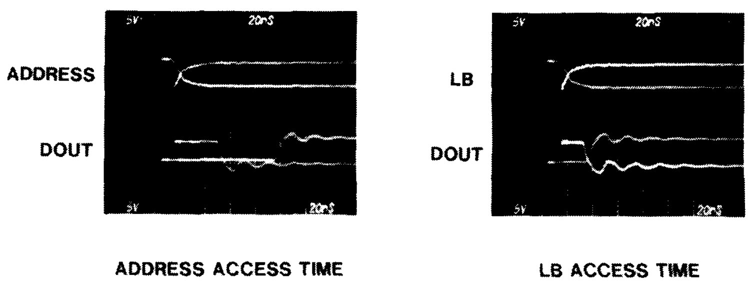

Fig. 10. Photograph of address and *LB* access time.

is the first byte (WD_{00-07}) in LB = "H" and the second byte (WD_{10-17}) in LB = "L" at the same address input, must be inputted serially. The first inputted byte is latched in the data-in latch. Then, five parity bits (WD_{E0-E4}) are generated using a modified Hamming code from first and second inputted bytes. In a READ cycle, five check bits (S_{0-4}) are generated from the 21 bits (RD_{00-07}, RD_{10-17}, and RD_{E0-E4}), and decoded to correct the READ data. One of these corrected 2-byte data switched by LB is transferred to the data output buffer.

IV. Device Characteristics

A photomicrograph of the chip [6] is shown in Fig. 9. The memory cell array is divided into two blocks. The row decoder is placed in the center of the array. The ECC circuit occupies approximately 10 percent of the chip area. The process technology is a conventional 1.5-μm design rule n-well CMOS process with a single metal layer and two polysilicon layers. The chip size is 5.55 $\times$ 7.05 mm^2 and the cell size is 7 $\times$ 8 μm^2.

Photographs of the address access time and LB access time are shown in Fig. 10. The address access time of 80 ns and *LB* access time of 20 ns were achieved at a typical condition. The access time delay by the ECC circuit is estimated to be 10 ns.

The features and measured ac characteristics of the device are summarized in Table II. The programming time is 10 ms/page. The active and standby currents in the worst case are below 40 mA and 100 μA, respectively. The device is housed in a 28-pin package.

V. Conclusion

A 5-V-only one-transistor 256K EEPROM with page-mode erase has been proposed. The program-inhibiting scheme has been developed in order to realize a one-transistor memory cell. As the cell is erased and programmed by the F–N tunneling mechanism, 5-V-only operation and 10^4 E/W cycles have been achieved. The chip size of the device is reduced to 70 percent of the full-featured EEPROM, because of the small cell size and reduction of the number of parity bits. The 256K EEPROM is pin compatible with a full-featured 256K EEPROM.

The device will be suitable for the memory card application that is expected to replace the magnetic memory devices.

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