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(71) Applicant 000003078
Toshiba Corporation
1-1-1 Shibaura, Minato-ku, Tokyo

(74) Agent 110000408
Takahashi, Hayashi and Partner Patent Attorneys, Inc.

(72) Inventor Takahiro Nakauchi
c/o Toshiba Corporation
1-1-1 Shibaura, Minato-ku, Tokyo

(72) Inventor Minoru Aoki
c/o Toshiba Corporation
1-1-1 Shibaura, Minato-ku, Tokyo

(72) Inventor Toshiyuki Kondo
c/o Toshiba Corporation
1-1-1 Shibaura, Minato-ku, Tokyo

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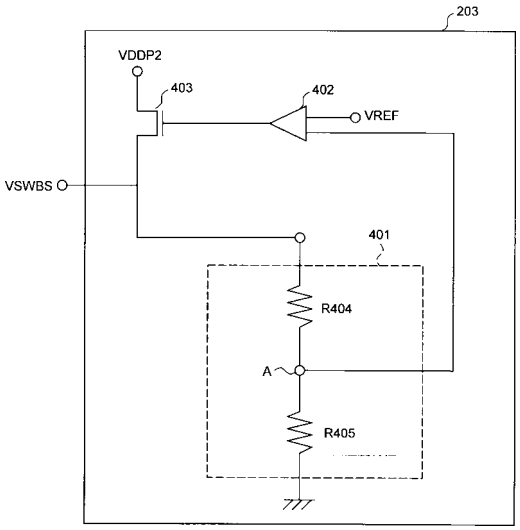
(54) [Title of the Invention] Non-volatile semiconductor storage device

(57) [Abstract]

[Problem] Provide a non-volatile semiconductor storage device that can reduce the amount of deterioration of the tunnel oxide film and reduce the data erasure time.

[Means for Solving] The non-volatile semiconductor storage device 100 comprises a non-volatile memory cell 201 having a charge storage part on the tunnel insulating film, and a voltage adjustment circuit 203 that adjusts the program voltage based on the combined resistance value of the synthetic resistance element 401 serially connecting a first resistance element R404 of a negative temperature characteristic whose resistance value decreases with increasing temperature and a second resistance element R405 of a positive temperature characteristic whose resistance value increases with increasing temperature to supply drain electrodes of the non-volatile memory cell.

[Representative Drawing/Figure] Figure 4



[Scope of Patent Claims]

[Claim 1]

A non-volatile semiconductor storage device characterized in that it comprises a non-volatile memory cell having a charge storage part on a tunnel insulating film, and a voltage adjustment circuit that adjusts the program voltage based on a combined resistance value of a synthetic resistance element serially connecting a first resistance element of a negative temperature characteristic whose resistance value decreases with increasing temperature and a second resistance element of a positive temperature characteristic whose resistance value increases with increasing temperature to supply drain electrodes of the non-volatile memory cell.

[Claim 2]

A non-volatile semiconductor storage device according to Claim 1, characterized in that the voltage adjustment circuit has a regulator circuit and a voltage supply transistor, the regulator circuit supplying an adjusted voltage to a gate electrodes of the voltage supply transistor, the voltage being adjusted based on a combined resistance value of a synthetic resistance element serially connecting the first resistance element and the second resistance element, the voltage supply transistor adjusting the program voltage supplied to drain electrodes based on the adjusted voltage from a regulator circuit supplied to the control gate electrodes to supply drain electrodes of the non-volatile memory cell.

[Claim 3]

The non-volatile semiconductor storage device of Claim 2, characterized in that the regulator circuit comprises an operational amplifier in which a reference voltage is input to one of the input terminals and a voltage from the nodes of the first and second resistance elements in the synthetic resistance element is input to the other of the input terminals, and a transistor in which a voltage is supplied to a gate electrodes of the voltage supply transistor based on a voltage input to the drain electrodes and an output voltage of the operational amplifier input to the control gate electrodes.

[Claim 4]

A non-volatile semiconductor storage device characterized in that it comprises a non-volatile memory cell having a charge storage part on a tunnel insulating film, and a voltage adjustment circuit that adjusts the gate voltage based on a combined resistance value of a synthetic resistance element serially connecting a first resistance element of a negative temperature characteristic whose resistance value decreases with increasing temperature and a second resistance element of a positive temperature characteristic whose resistance value increases with increasing temperature to supply gate electrodes of the non-volatile memory cell.

[Claim 5]

The non-volatile semiconductor storage device of Claim 4, characterized in that the voltage adjustment circuit has a regulator circuit that adjusts the gate voltage of the gate electrodes of the non-volatile memory cell based on a synthetic resistance value of the synthetic resistance element serially connecting the first and second resistance elements, the regulator circuit comprising an operational amplifier in which a reference voltage is input to one of the input terminals and a voltage from a node of the first and second resistance elements in the synthetic resistance element is input to another input terminal, and a transistor supplying a voltage to the gate electrodes of the non-volatile memory cell based on a voltage input to the drain electrodes and an output voltage of the operational amplifier input to the control gate electrodes.

[Detailed description of the invention]

[Technical Field]

[0001]

The present invention relates to non-volatile semiconductor storage devices, and in particular to non-volatile semiconductor storage devices that program data using the Hot Carrier Injection (HCI) method.

[Background art]

[0002]

In non-volatile semiconductor storage devices using the HCI method, there are some that supply a program voltage to the memory cell such that it is a constant voltage for temperature changes adjusted by the regulator circuit.

[0003]

In such non-volatile semiconductor storage devices, as the memory cell becomes finer and the gate length is shrunk, if the drain voltage does not change with generation, the electric field of the drain diffusion layer increases and the amount of HCI injected into the floating gate electrodes (charge storage layer) of the memory cell increases. In this case, the program characteristics improve, but the amount of HCI increases, so the amount of degradation of the tunnel oxide film increases. As a result, if the data erasure operation is performed using the erase method that provides high voltage to the circuit board and control gate electrodes (control electrodes), the data erasure time is increased. In other words, the deterioration of the oxide film is correlated with the HCI amount, so if the programming characteristics are good, the trap amount of electrons increases, leading to an increase in the erasure time. In particular, this increase in erasure time manifests prominently as the number of programs and erasures increases.

[0004]

On the other hand, a method of reducing the HCI amount is one in which the programming decreases the drain voltage as much as possible. However, even with this method, it is difficult to achieve a temperature range at the time of programming, that is, an HCI amount that would satisfy all from high temperature to low temperature. Specifically, for example, the HCI amount at a high temperature of (HT) of 85°C is an amount of HCI that does not cause oxide film degradation, while the HCI amount at low temperatures (LT) of -40°C is increased compared to high temperatures.

[0005]

In addition, non-volatile semiconductor storage devices equipped with temperature detection circuits are described, for example, in the following patent literature 1 through 3.

[Patent literature 1] Japanese Unexamined Patent Application Publication Number 2002-184192

[Patent literature 2] Japanese Unexamined Patent Application Publication Number 2002-215258

[Patent literature 3] Japanese Unexamined Patent Application Publication Number 2006-65945

[Disclosure of the Invention]

[Problem to be Solved by the Invention]

[0006]

The present invention provides non-volatile semiconductor storage devices that can reduce the amount of degradation of the tunnel oxide film and reduce the data erasure time.

[Means for Solving the Problem]

[0007]

A first aspect of the present invention comprises, in a non-volatile semiconductor storage device, a non-volatile memory cell having a charge storage part on tunnel insulating film, and a voltage adjustment circuit that adjusts program voltage based on a synthetic resistance value of a synthetic resistance element serially connecting a first resistance element of negative temperature characteristics in which the resistance value decreases with increasing temperature and a second resistance element of positive temperature characteristics in which the resistance value increases with increasing temperature to supply drain electrodes of the non-volatile memory cell.

[0008]

A second aspect of the present invention comprises, in a non-volatile semiconductor storage device, a non-volatile memory cell having a charge storage part on tunnel insulating film, and a voltage adjustment circuit that adjusts gate voltage based on a synthetic resistance value of a synthetic resistance element serially connecting a first resistance element of negative temperature characteristics in which the resistance value decreases with increasing temperature and a second resistance element of positive temperature characteristics in which the resistance value increases with increasing temperature to supply control gate electrodes of the non-volatile memory cell.

[Effect of the Invention]

[0009]

According to one embodiment of the present invention, the amount of degradation of the tunnel oxide film can be reduced and the data erasure time can be reduced by adjusting the program voltage based on the combined resistance value of the synthetic resistance element serially connecting a first resistance element of negative temperature characteristics where the resistance value decreases with increasing temperature and the second resistance element of positive temperature characteristics where the resistance value increases with increasing temperature.

[Best Embodiments of the Invention]

[0010]

The embodiment of the present invention will be described in detail below referencing the drawings. The present embodiment illustrates an example of the invention applied to a NOR-type flash memory device (NOR EEPROM). The present invention is not limited to these embodiments.

[0011]

(Embodiment 1)

Figure 1 is a block diagram illustrating the configuration of a NOR-type flash memory device (non-volatile semiconductor storage device) 100 according to Embodiment 1 of the present invention. As shown in Figure 1, NOR-type flash memory device 100 includes a memory cell array 101, power supply circuit 102, primary control circuit 103, row decoder 104, column decoder 105, program readout part 106, voltage adjustment circuit 107, interface circuit 108, and data register 109.

[0012]

Memory cell array 101 includes a plurality of (non-volatile) electrically reprogrammable memory cells disposed at the intersection of the bit line and the word line. These memory cells are arranged in a matrix.

[0013]

The power supply circuit 102 is connected to and supplies power to the primary control circuit 103, the row decoder 104, the column decoder 105, the program readout part 106, the voltage adjustment circuit 107, the interface circuit 108, and the data register 109.

[0014]

The primary control circuit 103 controls the power supply circuit 102, the row decoder 104, the column decoder 105, the program readout part 106, and the data register 109 based on the control signals from the interface circuit 108.

[0015]

The primary control circuit 103 provides row decoder 104 and column decoder 105 with access information to the memory cells of memory cell array 101. Row decoder 104 and column decoder 105 control the program readout part 106 based on this access information and data to read, program, or erase data for memory cells.

[0016]

The voltage adjustment circuit 107 adjusts the program voltage so that the HCI amount is almost constant in response to temperature changes and supplies it to the memory cells of the memory cell array 101.

[0017]

The interface circuit 108 sends and receives data and control signals (such as access information to the memory cells) to and from external devices. The interface circuit 108 receives data and control signals from external devices and performs predetermined processing to provide them to the primary control circuit 103 and the data register 109.

[0018]

Figure 2 is a circuit diagram illustrating a part of a NOR-type flash memory device 100 according to Embodiment 1. Memory cell array 101 includes a plurality of memory cells 201 and a plurality of column gate transistors 202. Memory cell array 101 is connected to voltage adjustment circuit 107 via resistance R2 (the parasitic resistance of a wire resistor or control transistor (column gate transistor 202 and voltage supply transistor 204)). In Figure 2, only one memory cell 201 and column gate transistor 202 are shown. The voltage adjustment circuit 107 includes a regulator circuit 203 and a plurality of voltage supply transistors 204. The output terminals (VSWBS) of the regulator circuit 203 are each connected to the gate electrodes of the plurality of voltage supply transistors 204. The voltage adjustment circuit 107 adjusts the program voltage from the bit line supplied to the voltage supply transistor 204 based on the combined resistance value of the synthetic resistance element of the regulator circuit 203 to supply the drain electrodes of the memory cell 201 via the column gate transistor 202.

[0019]

The drain electrodes of memory cell 201 are connected to the source electrodes of column gate transistor 202 via resistance R1 (wire resistance or parasitic resistance of control transistors (column gate transistor 202)). A word line (WL) is electrically connected to the gate electrodes of the memory cell 201, and the source electrodes of memory cell 201 are grounded.

[0020]

Specifically, as shown in Figure 3, the memory cell 201 is practically configured with a conductive field effect transistor having floating gate electrodes (charge storage part) 301 and control electrodes 302. The floating gate electrode part 301 is composed of polycrystalline silicon (polysilicon) and is arranged interposing a tunnel insulating film 303 on a substrate (sub). The control gate electrode 302 comprise a polycrystalline silicon (polysilicon) and a silicide layer (e.g., WSi_2) disposed interposing an insulating film 304 on the floating gate electrodes 301. A bit line is connected to the drain area (D) of the memory cell 201 via the voltage adjustment circuit 107. In the source area (S) of the memory cell 201, a source line (reference power supply Vss) is connected. The drain region and source region of the memory cell 201 comprise a diffusion layer.

[0021]

The control gate electrodes of the column gate transistor 202 is electrically connected with a selection gate line, and the source electrodes of the column gate transistor 202 is connected to the drain electrodes of the memory cell 201 via resistance R1 (wire resistance or parasitic resistance of the control transistor). The drain electrodes of the column gate transistor 202 are connected to the source electrodes of the voltage supply transistor via resistance R2 (wire resistance or channel parasitic resistance of the control transistor). The column gate transistor 202 supplies programming, read, and erase voltage to the drain electrodes of the memory cell 201 based on the applied voltage to the control gate electrodes.

[0022]

The two input terminals of regulator circuit 203 are each connected to power supply circuit 102. One of the input terminals of regulator circuit 203 receives voltage (VDDP2) and the other input terminal of regulator circuit 203 receives reference voltage (VREF). The output terminal (VSWBS) of the regulator circuit 203 is also connected to the control gate electrodes of the voltage supply transistor 204. Also, one end of regulator circuit 203 is grounded.

[0023]

The drain electrodes of the voltage supply transistor 204 are connected to a bit line (BL), and the gate electrodes of the voltage supply transistor 204 are connected to an output terminal (VSWBS) of the regulator circuit 203. The source electrodes of the voltage supply transistor 204 are connected to the drain electrodes of the column gate transistor 202 via resistance R2 (wire resistance or channel parasitic resistance of the control transistor).

[0024]

Next, the regulator circuit 203 is described using Figure 4. Figure 4 is a circuit diagram illustrating regulator circuit 203. Regulator circuit 203 includes a synthetic resistance element 401, an operational amplifier 402, and a transistor 403. The regulator circuit 203 adjusts the program voltage such that the amount of HCI to the floating gate electrodes (charge storage part) of the memory cell 201 is substantially constant in response to temperature changes.

[0025]

The synthetic resistance element 401 includes a first resistance element R404 and a second resistance element R405. The first resistance element R404 and the second resistance element R405 are connected in series to form a synthetic resistance element 401. One end of the synthetic resistance element 401 is connected to the voltage supply transistor 204 via an output terminal (VSWBS) of the regulator circuit 203, and the other end of the synthetic resistance element 401 is grounded.

[0026]

Specifically, one end of the first resistance element R404 is connected to the voltage supply transistor 204 via an output terminal (VSWBS) of the regulator circuit 203 and is connected to the source electrodes of the transistor 403. The first resistance element R404 and the second resistance element R405 are connected in series. The other end of the second resistance element R405 is grounded. Node A of the first resistance element R404 and the second resistance element R405 is connected to one of the input terminals of the operational amplifier 402.

[0027]

In the synthetic resistance element 401, the first resistance element R404 has a negative temperature characteristic in which the resistance value decreases with increasing temperature. The first resistance element R404 is composed of, for example, a polysilicon resistance element (e.g., an N-type polysilicon resistance element). On the other hand, the second resistance element R405 has a positive temperature characteristic that increases the resistance value as the temperature increases. For example, it is composed of a diffusion layer resistance element (e.g., an N-type diffusion layer resistance element or a P-type diffusion layer resistance element).

[0028]

One of the input terminals of the operational amplifier 402 is connected to node A of the first resistance element R404 and the second resistance element R405 in the synthetic resistance element 401. Other input terminals of the operational amplifier 402 are connected to the power supply circuit 102. One of the input terminals of the operational amplifier 402 receives an output voltage from node A of the first resistance element R404 and the second resistance element R405, and the other of the input terminals of the operational amplifier 402 receives a reference voltage (VREF) from the power supply circuit 102. This operational amplifier 402 supplies a constant voltage to the gate electrodes of the transistor 403 based on the output voltage from node A of the first resistance element R404 and the second resistance element R405 and the reference voltage from the power supply circuit 102.

[0029]

The drain electrodes of the transistor 403 are connected to the power supply circuit 102 and receive a voltage (VDDP2). The gate electrodes of the transistor 403 are connected to the output terminal of the operational amplifier 402, and the source electrodes of the transistor 403 are connected to the output terminal (VSWBS) of the regulator circuit 203. This transistor 403 is in the ON state due to the voltage input to the drain electrodes (VDDP2) and the output voltage of the operational amplifier 402 input to the gate electrodes, supplying voltage to the gate electrodes of the voltage supply transistor 204 and to the synthetic resistance element 401.

[0030]

Next, the current-voltage characteristics of the synthetic resistance element 401 are described using Figure 5. Figure 5 is a diagram illustrating current-voltage characteristics of the first resistance element R404 and the second resistance element R405 at node A of the synthetic resistance element 401. In this case, the first resistance element R404 is configured with a polysilicon resistance element and the second resistance element R405 is configured with a diffusion layer resistance element.

[0031]

The solid line 501 shown in Figure 5 shows the current-voltage characteristics at low temperatures (LT) of the polysilicon resistance element R404 and the solid line 502 shows the current-voltage characteristics at low temperatures of the diffusion layer resistance element R405. Also, the dotted line 503 shows the current-voltage characteristics at high temperatures (HT) of the polysilicon resistance element R404, and the dotted line 504 shows the current-voltage characteristics at high temperatures of the diffusion layer resistance element R405.

[0032]

In the case of low temperatures, as shown in solid line 501, the polysilicon resistance element R404 has a negative temperature characteristic that reduces the resistance value as the temperature increases, so the current decreases as the applied voltage increases. On the other hand, as shown in solid line 502, the diffusion layer resistance element R405 has a positive temperature characteristic that increases the resistance value as the temperature increases, so the current increases as the applied voltage increases. In addition, the polysilicon resistance element R404 and the diffusion layer resistance element R405 are connected in series to form the synthetic resistance element 401, so that the synthetic resistance values of the synthetic resistance element 401 are intermediate values of the resistance value of the resistance elements of each other. Specifically, the current-voltage characteristics at low temperatures in node A of the polysilicon resistance element R404 and the diffusion layer resistance

element R405 are indicated by the operating points (intersection points) 505 of solid lines 501 and 502.

[0033]

In addition, at high temperatures, as shown in the dotted line 503, the polysilicon resistance element R404 has a negative temperature characteristic in which the resistance value decreases as the temperature increases, so the current decreases as the applied voltage increases. As shown in the dotted line 504, the diffusion layer resistance element R405 has a positive temperature characteristic that increases the resistance value as the temperature increases, so the current increases as the voltage applied increases. Then, because the polysilicon resistance element R404 and the diffusion layer resistance element R405 are connected in series to form a synthetic resistance element 401, the synthetic resistance values of this synthetic resistance element 401 are an intermediate value of the resistance value of each other's resistance element. Specifically, the current-voltage characteristics at low temperatures in node A of the polysilicon resistance element R404 and the diffusion layer resistance element R405 are indicated by the operating points (intersection points) 506 of the dotted lines 503 and 504.

[0034]

The regulator circuit 203 then supplies an adjusted voltage to the output terminal (VSWBS) based on the combined resistance value of the synthetic resistance element 401 connecting the polysilicon resistance element R404 and the diffusion layer resistance element R405 in series. For example, at low temperatures the voltage indicated by arrows from intersection point 505 shown in Figure 5 (VSWBS_LT) is the adjusted voltage, and at high temperatures the voltage indicated by arrows from intersection point 506 shown in Figure 5 (VSWBS_HT) is the adjusted voltage. This adjusted voltage has a temperature characteristic, unlike a constant voltage supplied from a regulator circuit, which is a prior art according to the present embodiment.

[0035]

The voltage (drain voltage) supplied to the drain electrodes of the memory cell 201 selected by the column gate transistor 202 will have the opposite temperature-voltage characteristics as compared to the prior art according to the present embodiment, as shown in Figure 6. Specifically, as shown in Figure 6 (A), when using the prior art regulator circuit according to the present invention, the drain voltage at low temperature (Vd2_cell_LT) of the memory cell is greater than the drain voltage at high temperature (Vd_cell_HT). On the other hand, as shown in Figure 6 (B), when using regulator circuit 107 according to Embodiment 1 of the present embodiment, the drain voltage (Vd2_cell_LT) at a low temperature of memory cell 201 is less than the drain voltage (Vd_cell_HT) at a high temperature.

[0036]

As a result, as shown in the current-voltage (Id-Vd) characteristic diagram of Figure 7, the drain voltage to the memory cell 201 at low temperature can be approximately the same voltage as at high temperature or less, so the program current at low temperature (Iprog_LT) can be reduced. That is, even if there is a temperature change, it is almost constant with the amount of HCI at high temperature, so the amount of degradation of the tunnel oxide film can be reduced.

[0037]

Next, a program operation of a NOR-type flash memory device 100 having the configuration described above will be described.

[0038]

The program voltage (VDDP) from the bit line applied to the drain electrodes of the voltage supply transistor 204 is adjusted by applying an adjusted voltage to the control gate electrodes of the voltage supply transistor 204; the voltage is adjusted based on the combined resistance value of the synthetic resistance element 401 serially connecting the first resistance element R404 of negative temperature characteristics and the second resistance element R405 of positive temperature characteristics. This regulated program voltage is a program voltage having temperature characteristics and is lower at low temperatures than at high temperatures.

[0039]

The adjusted program voltage output from the voltage supply transistor 204 is input to the drain electrodes of the column gate transistor 202 via resistance R2 (wire resistance and channel resistance of the control transistor). The column gate transistor 202 is in the ON state due to the voltage supplied to the gate electrodes, and it provides an adjusted program voltage to the drain electrodes of the memory cell 201 via the resistance element R1.

[0040]

The adjusted program voltage supplied to the drain electrodes of the memory cell 201 and the gate voltage (Vg) supplied to the word line cause a high voltage between the channel region and the word line, injecting electrons as data from the channel region through the tunnel insulating film into the floating gate electrodes (charge storage part), thereby programming the data.

[0041]

As such, the non-volatile semiconductor storage device 100 according to Embodiment 1 of the present embodiment comprises a non-volatile memory cell 201 having a charge storage part on the tunnel insulating film, and a voltage adjustment circuit 107 that adjusts the program voltage from the bit line based on the combined resistance value of the synthetic resistance element 401 serially connecting a first resistance element R404 of a negative temperature characteristic whose resistance value decreases with increasing temperature and a second resistance element R405 of a positive temperature characteristic whose resistance value increases with increasing temperature to supply drain electrodes of non-volatile memory cell 201.

[0042]

As a result, according to Embodiment 1 of the present embodiment, the program voltage is adjusted so that the amount of HCI injected into the charge storage part of the memory cell is almost constant even in the event of a temperature change, and is supplied to the drain electrodes of the memory cell, so that the amount of degradation of the tunnel oxide film can be reduced and the data erasure time can be reduced.

[0043]

In addition, according to Embodiment 1 of the present embodiment, the first resistance element can be configured by the diffusion layer comprising the source region and the drain region of the memory cell, so that it can be manufactured in the same manufacturing process. Furthermore, according to Embodiment 1 of the present embodiment, the second resistance element can be configured by means of a polysilicon comprising floating gate electrodes (charge storage part) and control gate electrodes of a memory cell, so that it can be manufactured in the same manufacturing process.

[0044]

(Embodiment 2)

In Embodiment 1 described above, the temperature adjustment circuits adjusted the program voltage supplied to the drain electrodes of the non-volatile memory cell in response to the temperature change. In Embodiment 2 of the present invention, the temperature adjustment circuits adjust the gate voltage supplied to the control gate electrodes of the non-volatile memory cell in response to a temperature change.

[0045]

Figure 8 is a block diagram illustrating the configuration of a NOR-type flash memory device (non-volatile semiconductor storage device) 1000 according to Embodiment 2 of the present invention. The NOR-type flash memory device 1000 shown in Figure 8 includes a memory cell array 101, a power supply circuit 102, a primary control circuit 103, a row decoder 104, a column decoder 105, a program readout part 106, an interface circuit 108, a data register 109, a voltage supply circuit 1001, and a voltage adjustment circuit 1002. In the NOR-type flash memory device 1000 shown in Figure 8, the same configuration as the NOR-type flash memory device 100 of Figure 1 is marked with the same reference symbol, so its description is omitted.

[0046]

The row decoder 104 controls the program control unit 106 based on access information from the primary control circuit 103 to read or erase data from the memory cell. The row decoder 104 also supplies a gate voltage to the control gate electrodes of the memory cell to the voltage adjustment circuit 1001 based on access information from the primary control circuit 103.

[0047]

The voltage supply circuit 1001 receives voltage from the power supply circuit 102, generates a program voltage that is constant voltage for temperature changes, and supplies it to a memory cell of the memory cell array 101.

[0048]

The voltage adjustment circuit 1002 receives the gate voltage from the row decoder 104, adjusts the gate voltage so that the amount of HCI is almost constant in response to temperature changes, and supplies it to the memory cells of the memory cell array 101.

[0049]

Figure 9 is a circuit diagram illustrating a part of a NOR-type flash memory device 1000 according to Embodiment 2 of the present embodiment. In the NOR-type flash memory device 1000 shown in Figure 9, the same configuration as the NOR-type flash memory device 100 of Figure 2 is marked with the same reference symbol, so its description is omitted.

[0050]

Memory cell array 101 includes a plurality of memory cells 201 and a plurality of column gate transistors 202. One end of the memory cell array 101 is connected to the voltage supply circuit 1001 via the resistance element R2, and the other end of the memory cell array 101 is connected to the voltage adjustment circuit 1002. In Figure 9, only one memory cell 201 and a column gate transistor 202 are shown. The voltage supply circuit 1001 includes a regulator circuit 1100 and a plurality of voltage supply transistors 204. The output terminals (VSWBS2) of the regulator circuit 1100 are each connected to the control gate electrodes of a plurality of voltage supply transistors 204. In Figure 9, only one voltage supply transistor 204 is shown. The voltage adjustment circuit 1002 consists of, for example, the regulator circuit 1101. Based on the combined resistance value of the synthetic resistance element of this regulator circuit 1101, the gate voltage supplied from the row decoder 104 is adjusted to supply the control gate electrodes of the memory cell 201.

[0051]

The drain electrodes of memory cell 201 are connected to the source electrodes of column gate transistor 202 via resistance R1 (wire resistance and channel parasitic resistance of control transistor (column gate transistor 202)). The control gate electrodes of the memory cell 201 are connected to the output terminal (VSWBS3) of the regulator circuit 1101, and the source electrodes of the memory cell 201 are grounded.

[0052]

The input terminal of the regulator circuit 1100 is connected to the power supply circuit 102 and receives voltage (VDDP2). The output terminal (VSWBS2) of the regulator circuit 1100 is connected to the control gate electrodes of the voltage supply transistor 204. Also, one end of regulator circuit 1100 is grounded.

[0053]

The drain electrodes of the voltage supply transistor 204 are connected to a bit line (BL), and the control gate electrodes of the voltage supply transistor 204 are connected to an output terminal (VSWBS2) of the regulator circuit 1100. The source electrodes of the voltage supply transistor 204 are connected to the drain electrodes of the column gate transistor 202 via a resistance R2 (wire resistance and channel parasitic resistance of the control transistor (voltage supply transistor 204 and column gate transistor 202)).

[0054]

One of the two input terminals of the regulator circuit 1101 is connected to the row decoder 104 via a word line, and the other of the input terminals of the regulator circuit 1101 is connected to the power supply circuit 102. The output terminal (VSWBS3) of the regulator circuit 1101 is connected to the control gate electrodes of the memory cell 201. Also, one end of regulator circuit 1101 is grounded. The gate voltage (Vg) from the row decoder 104 to the control gate electrodes of memory cell 201 is input to one of the input terminals of regulator circuit 1101. The reference voltage (VREF) from the power supply circuit 102 is input to the other input terminals of the regulator circuit 1101.

[0055]

The regulator circuit 1101 is then described using Figure 10. Figure 10 is a circuit diagram illustrating a regulator circuit 1101. Regulator circuit 1101 includes a synthetic resistance element 401, an operational amplifier 402, and a transistor 403. The regulator circuit 1101 adjusts the gate voltage such that the amount of HCI to the floating gate electrodes (charge storage part) of the memory cell 201 is almost constant in response to temperature changes. In the regulator circuit 1101 shown in Figure 10, the same configuration as the regulator circuit 203 shown in Figure 4 is marked with the same reference symbol, so its description is omitted.

[0056]

The synthetic resistance element 401 includes a first resistance element R404 and a second resistance element R405. The first resistance element R404 and the second resistance element R405 are connected in series to form a synthetic resistance element 401. One end of the synthetic resistance element 401 is connected to the control gate electrodes of the memory cell 201 via an output terminal (VSWBS3) of the regulator circuit 1101, and the other end of the synthetic resistance element 401 is grounded.

[0057]

Specifically, one end of the first resistance element R404 is connected to control gate electrodes of the memory cell 201 via an output terminal (VSWBS3) of the regulator circuit 1101 and is connected to source electrodes of the transistor 403. The first resistance element R404 and the second resistance element R405 are connected in series. The other end of the second resistance element R405 is grounded. Node A of the first resistance element R404 and the second resistance element R405 is connected to one of the input terminals of the operational amplifier 402.

[0058]

One of the input terminals of the operational amplifier 402 is connected to node A of the first resistance element R404 and the second resistance element R405 in the synthetic resistance element 401. Other input terminals of the operational amplifier 402 are connected to the power supply circuit 102. One of the input terminals of the operational amplifier 402 receives an output voltage from node A of the first resistance element R404 and the second resistance element R405, and the other of the input terminals of the operational amplifier 402 receives a reference voltage (VREF) from the power supply circuit 102. This operational amplifier 402 supplies a constant voltage to the control gate electrodes of the transistor 403 based on the output voltage from node A of the first resistance element R404 and the second resistance element R405 and the reference voltage from the power supply circuit 102.

[0059]

The drain electrodes of transistor 403 are connected to row decoder 104 and receive a gate voltage (Vg). The control gate electrodes of the transistor 403 are connected to the output terminal of the operational amplifier 402, and the source electrodes of the transistor 1200 are connected to the output terminal (VSWBS3) of the regulator circuit 1101. This transistor 403 is in the ON state due to the gate voltage input to the drain electrodes and the output voltage of the operational amplifier 402 input to the control gate electrodes, supplying voltage to the synthetic resistance element 401.

[0060]

The regulator circuit 1101 then supplies an adjusted voltage to the output terminal (VSWBS3) based on the combined resistance value of the synthetic resistance element 401 connecting the first resistance element R404 and the second resistance element R405 in series. For example, at low temperatures, the voltage indicated by arrows from intersection point 505 shown in Figure 5 (VSWBS_HT) is the adjusted voltage, and at low temperatures, the voltage indicated by arrows from intersection point 506 shown in Figure 5 (VSWBS_LT) is the adjusted voltage. This adjusted voltage has a temperature characteristic, unlike the constant voltage supplied from the prior art regulator circuit according to the present embodiment.

[0061]

As a result, the adjusted gate voltage supplied to the control gate electrodes of the memory cell 201 have the opposite temperature-voltage characteristics as compared to the prior art according to the present embodiment, as shown in Figure 11. Specifically, as shown in Fig. 11(A), when using the prior art regulator circuit according to the present embodiment, the low temperature gate voltage (Vg2_cell_LT) of the memory cell is greater than the high temperature gate voltage (Vg_cell_HT). On the other hand, as shown in Figure 11(B), when using regulator circuit 1101 according to Embodiment 2 of the present embodiment, the low temperature gate voltage (Vg2_cell_LT) of memory cell 201 is less than the high temperature gate voltage (Vg_cell_HT).

[0062]

As a result, as shown in the current-voltage (Ig-Vg) characteristic diagram of Figure 12, the gate voltage to the memory cell 201 at low temperatures can be approximately the same voltage as at high temperatures, or less, so that the program current (Iprog_LT) at low temperatures can be reduced compared to conventional cases. That is, even if there is a temperature change, it is almost constant with the amount of HCI at high temperature, so the amount of degradation of the tunnel oxide film can be reduced.

[0063]

Next, program operation of NOR-type flash memory device 1000 having the configuration described above will be described.

[0064]

Due to the constant voltage output from regulator circuit 1100, voltage supply transistor 204 is in the ON state, and program voltage (VDDP) from the bit line applied to the drain electrodes is output to the drain electrodes of column gate transistor 202 via resistance element R1. The column gate transistor 202 is in the ON state due to the voltage supplied to the control gate electrodes and supplies the program voltage to the drain electrodes of the memory cell 201 via the resistance element R1.

[0065]

The gate voltage adjusted based on the synthetic resistance value of synthetic resistance element 401, which connects the first resistance element R404 with negative temperature characteristics and the second resistance element R405 with positive temperature characteristics in series, is input to the control gate electrodes of memory cell 201 from regulator circuit 1101. The adjusted gate voltage is a gate voltage with temperature characteristics, and it is lower at low temperatures than at high temperatures.

[0066]

The program voltage input to the drain electrodes of the memory cell 201 is then adjusted by the adjusted gate voltage input to the control gate electrodes, high voltage is generated between the channel region and the word line, and electrons as data are injected from the channel region through the tunnel insulating film into the floating gate electrodes (charge storage part), and data is thereby programmed.

[0067]

In this way, the non-volatile semiconductor storage device comprises a non-volatile memory cell having a charge storage part on tunnel insulating film, and a voltage adjustment circuit that adjusts gate voltage based on a synthetic resistance value of a synthetic resistance element serially connecting a first resistance element of negative temperature characteristics in which the resistance value decreases with increasing temperature and a second resistance element of positive temperature characteristics in which the resistance value increases with increasing temperature to supply control gate electrodes of the non-volatile memory cell.

[0068]

As a result, according to Embodiment 2 of the present embodiment, the gate voltage is adjusted so that the amount of HCI injected into the charge storage part of the memory cell is almost constant even in the event of a temperature change, and is supplied to the control gate electrodes of the memory cell, so that the amount of degradation of the tunnel oxide film can be reduced and the data erasure time can be reduced.

[0069]

In addition, according to Embodiment 2 of the present embodiment, the second resistance element can be configured by the diffusion layer comprising the source region and the drain region of the memory cell, so that it can be manufactured in the same manufacturing process. Furthermore, according to Embodiment 2 of the present embodiment, the first resistance element can be configured by means of a polysilicon comprising floating gate electrodes (charge storage part) and control gate electrodes of a memory cell, so that it can be manufactured in the same manufacturing process.

[0070]

It should be noted that Embodiments 1 and 2 of the present invention may be combined. That is, a program voltage and a gate voltage having temperature characteristics may be supplied to the drain electrodes and control gate electrodes of the memory cell. This allows for approximately the same program characteristics at high and low temperatures in addition to the effects described in the above Embodiments 1 and 2 of the present embodiment.

[0071]

Also, in Embodiments 1 and 2 of the present invention, the so-called floating gate EEPROM in which the memory cell has floating gate electrodes (charge storage electrodes) and control gate electrodes is described by way of example, but not limited to the example. That is, the present invention is applicable to those having a charge storage part on a tunnel insulating film, for example, it is also applicable to a Metal Nitride Oxide Semiconductor (MNOS) type EEPROM.

[Brief Description of the Drawings]

[0072]

[Figure 1] A block diagram showing the configuration of a non-volatile semiconductor storage device according to Embodiment 1 of the present invention.

[Figure 2] A circuit diagram showing a part of the non-volatile semiconductor storage device according to Embodiment 1 of the present embodiment.

[Figure 3] A diagram for describing the non-volatile memory cell according to Embodiment 1 of the present embodiment.

[Figure 4] A circuit diagram showing the regulator circuit according to Embodiment 1 of the present embodiment.

[Figure 5] A diagram showing the current-voltage characteristics of the first resistance element and the second resistance element in node A of the composite resistance element of the regulator circuit according to Embodiment 1 of the present embodiment.

[Figure 6] A diagram showing the voltage-temperature characteristics of the non-volatile semiconductor storage device according to Embodiment 1 of the present embodiment.

[Figure 7] A diagram showing current-voltage characteristics at low temperatures of the non-volatile semiconductor storage device according to Embodiment 1 of the present embodiment.

[Figure 8] A block diagram showing the configuration of the non-volatile semiconductor storage device according to Embodiment 2 of the present invention.

[Figure 9] A circuit diagram showing a part of the non-volatile semiconductor storage device according to Embodiment 2 of the present embodiment.

[Figure 10] A circuit diagram showing the regulator circuit according to Embodiment 2 of the present embodiment.

[Figure 11] A diagram showing the voltage-temperature characteristics of the non-volatile semiconductor storage device according to Embodiment 2 of the present embodiment.

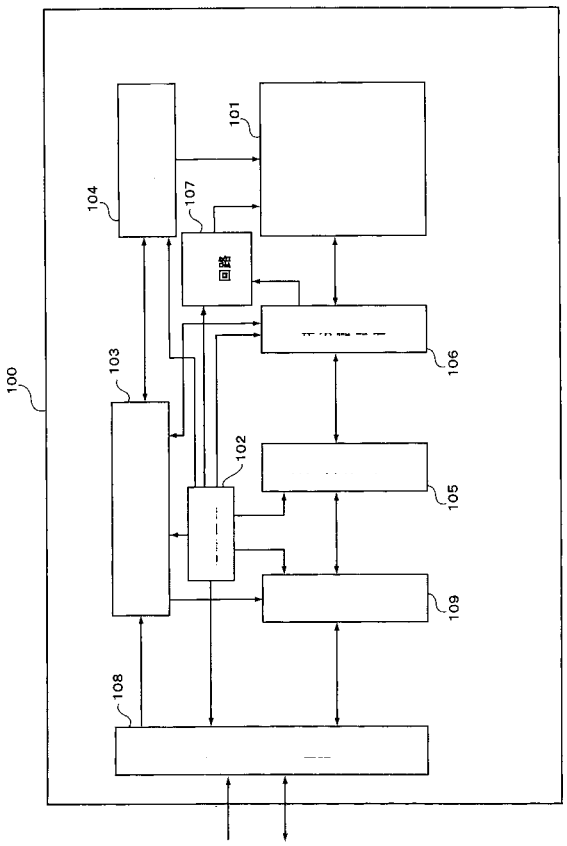
[Figure 12] A diagram showing current-voltage characteristics at low temperatures of the non-volatile semiconductor storage device according to Embodiment 2 of the present embodiment.

[Explanation of References]

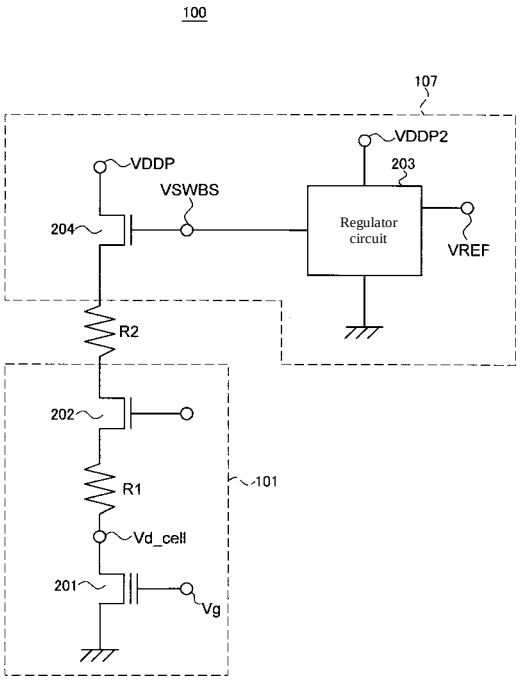
[0073]

100, 800, 1000 and 1500 NOR-type flash memory devices (non-volatile semiconductor storage devices)
101 memory cell array
102 power supply circuit
103 primary control circuit
104 row decoder
105 column decoder
106 program readout part
107, 1002 voltage adjustment circuit
201 non-volatile memory cell
202 column gate transistor
203, 801, 1101, and 1501 regulator circuits
204 voltage supply transistor
301 floating gate electrodes (charge storage part)
302 control gate electrodes
303 tunnel insulating film
401, 802 synthetic resistance elements
402 operational amplifier
403 transistor
R404 first resistance element
R405 second resistance element
T803 transistor

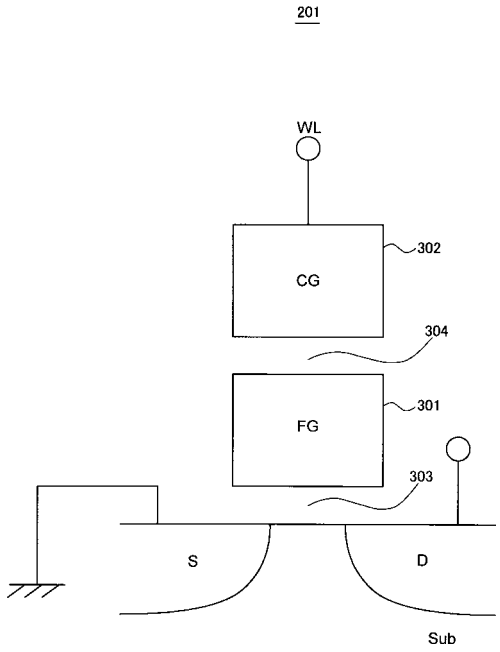
[Figure 1]



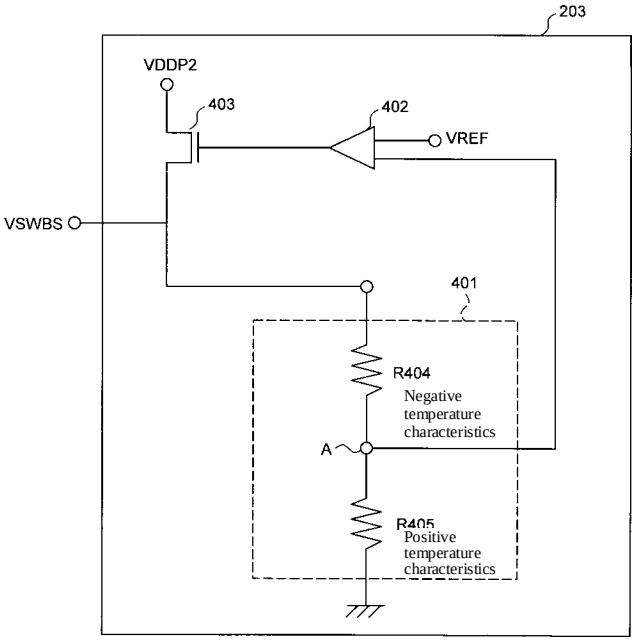
[Figure 2]



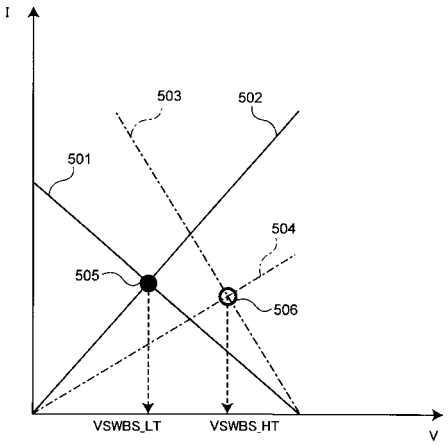
[Figure 3]



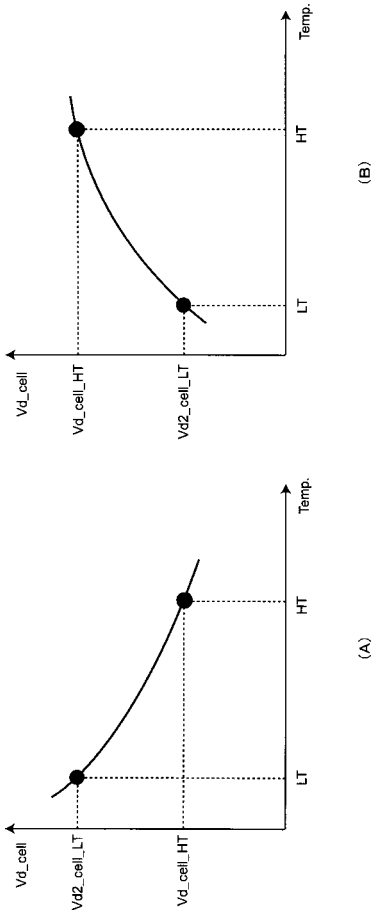
[Figure 4]



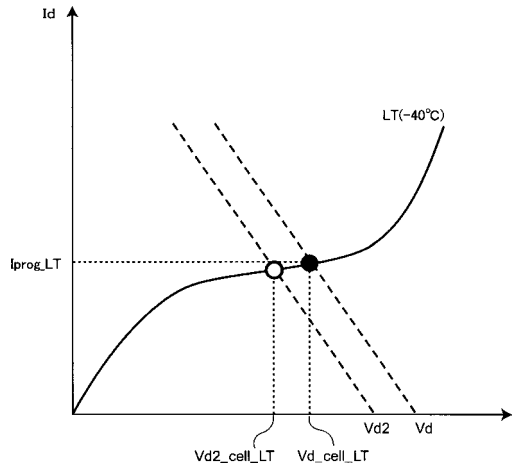
[Figure 5]



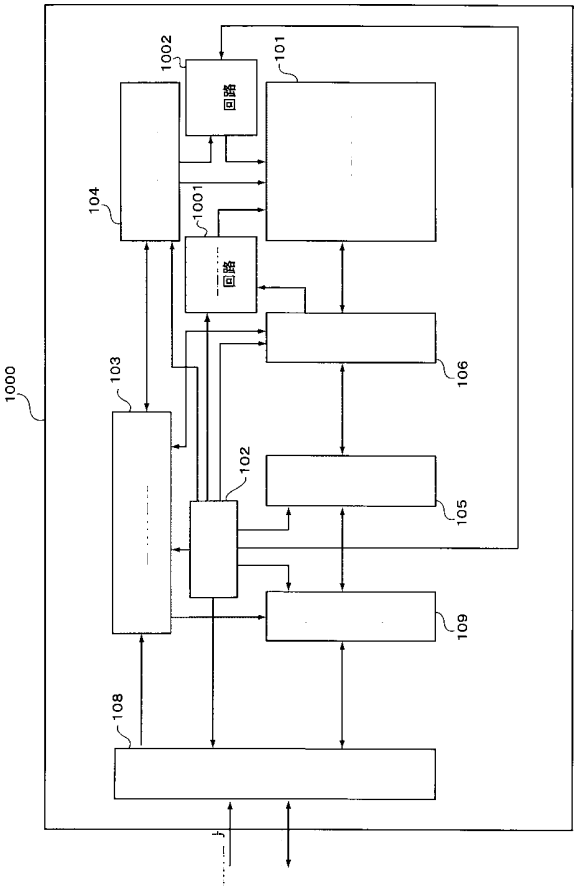
[Figure 6]



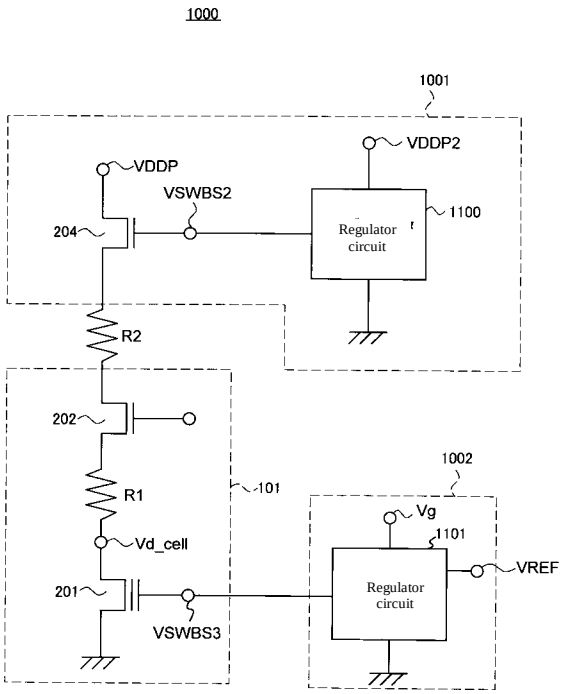
[Figure 7]



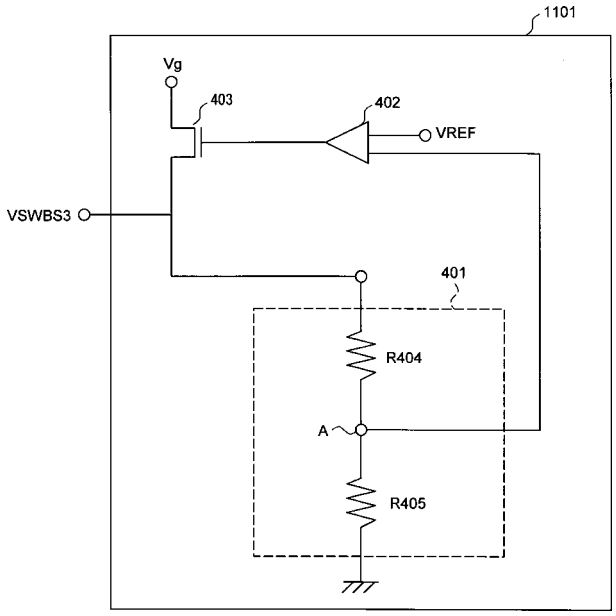
[Figure 8]



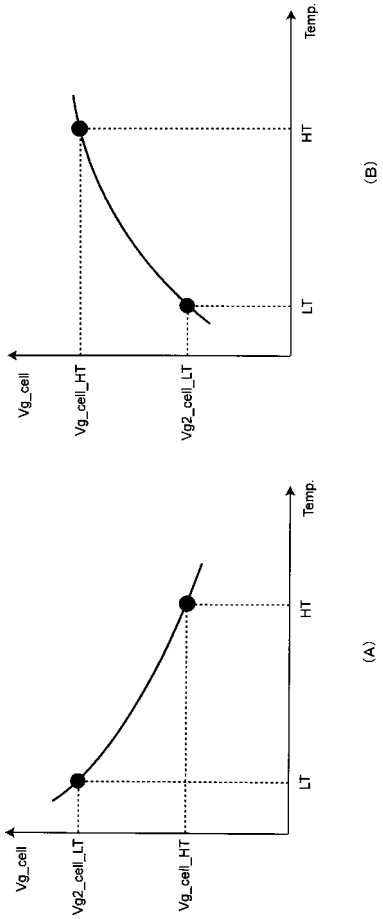
[Figure 9]



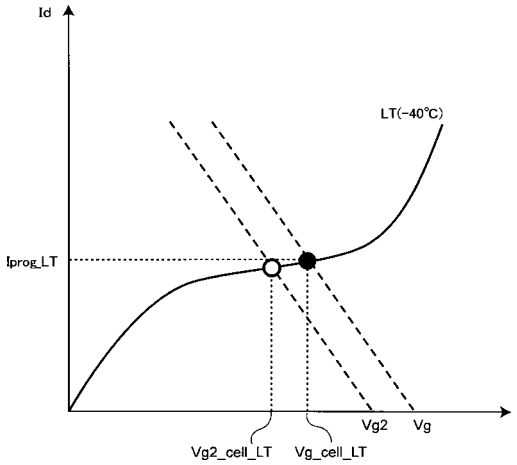
[Figure 10]



[Figure 11]



[Figure 12]



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(72) Inventor Norimasa Hara
c/o Toshiba Corporation 1-1-1 Shibaura, Minato-ku, Tokyo
(72) Inventor Kiyomi Naruke
c/o Toshiba Corporation 1-1-1 Shibaura, Minato-ku, Tokyo

F term [reference] 5B125 BA02 CA13 CA27 EA01 EB02 EB04 EG02 EG08 EH08
EJ03 FA05

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I hereby further declare that all statements made herein of my own knowledge are true and that all statements made on the information and belief are believed to be true; I declare under penalty of perjury that the foregoing is true and correct, and understand that willful false statements and the like are punishable by fine or imprisonment, or both pursuant to 18 U.S.C. 1001.

JP2008217914A (Nakauchi)

Dan McDonald

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Linguist Name

May 26, 2025

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Date