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Self-sealed circular channels for micro-fluidics

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Abstract

The paper elaborates a technique to realize fully circular self-sealed channels with diameter varying from few micrometers to less than 100 nm using standard silicon processes like trench formation, doped silicon oxide filling and thermal cycle for its re-flow. The integration of the channels with the fluidic reservoirs, their packaging with input and output ports for fluids and external electrodes is also presented. Such a chip is used as lateral patch clamp to record the electrical activity of the cells.

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Keywords: Circular; Self-sealed; Micro-channels; Lateral patch clamp

1. Introduction

The evolutions in micro- and nano-fabrication technologies have allured many biologists and biophysicists for numerous applications pertaining to detection and manipulation of single molecules or cells [1–3]. These miniaturized chips have advantages like smaller sample volume, parallel analysis in separate devices in array format and possibility to integrate various process and analysis requirements like extraction, chemical treatments, identifications, etc. on a single chip. For sample transport and detection in these chips a network of fluidic channels, valves, pumps and optical/electrical sensors are essential. The channel's dimensional specifications vary from <100 nm to couple of micrometers for diameter and few to hundreds of micrometers for length. A wide range of techniques are being employed for the fabrication of micro or nano-channels using materials like silicon, quartz, polymers, metals and plastics [4–11] but they are either limited by the channel dimensions that they can realize or the complexity of the process.

Silicon and quartz are most common substrates, which are patterned and etched to form micro grooves. The etching process could be either isotropic or anisotropic using wet or dry chemistries. Cavities thus formed are capped by bonding a sec-

ond wafer or by depositing a film. Kaplan et al. [4] have used quartz substrate and wet isotropic etching process to create channels, 10–100 μm width, which are capped by oxidation of masking poly-silicon layer followed by LPCVD based silicon oxide deposition. Tjerkstra et al. [5] used combination of wet and dry anisotropic and isotropic etching processes to create channels in silicon substrates followed by LPCVD silicon nitride and silicon oxide sealing or glass wafer bonding.

Surface machined metallic micro-channels on silicon and glass are also reported [6] where nickel is used as the structural material and gold as the coating of inside walls. Individual micro-channels ranged from 30 μm to 1.5 mm in width, 500 μm to several mm in length and 13–40 μm in thickness. Man et al. [7] fabricated isolated plastic capillaries (0.5–100 μm in height) on silicon, glass, and polycarbonate wafers. Micro channel with a cross section of 50 $\mu\text{m} \times 50 \mu\text{m}$ are also realized using SU-8 photoresist as structure material [8]. Above processes are mainly suitable for the channels having cross-sections in few micro-meters to tens of micro-meters.

For the fabrication of sub-micrometer or nanometer dimensional channels many new techniques have emerged. Electron beam lithography is one of the most used among these processes. Matsumoto et al. [9] have employed electron beam (EB) lithography and fast atom beam (FAB) to form nano-channels (50 nm wide and 360 nm deep; pitched at 100 nm) on Quartz chip. Nano-channels are also formed by stress induced fracturing along with laser based micro-channel fabrication [10]. Width of these nano-

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channels was about 450 nm. Another simple technique reported is based on etching of a sacrificial nanowire, which is formed on the side wall of a step [11]. Height and width of these nano-channels are about 90 and 40 nm, respectively. They have also elaborated another technique to realize nano-channels which is based on the adhesion of the capping layer to the substrate after removal of a sacrificial strip separating the two. The height and width of the channels thus formed are about 50 and 400 nm respectively. None of these methods are capable of fabricating fully rounded channels.

This paper elaborates the key design and process optimization features of the fully round lateral channels and their integration with the fluidic chambers, in silicon chip. The packaging aspects of the chambers using poly dimethyl siloxane (PDMS) block containing input/output fluid ports and the electrical tests performed on the chip for cell trapping at the circular channel are also presented.

2. Fabrication details

Realization of micro-fluidic chip in silicon wafers commences with the fabrication of lateral circular channels varying in diameter from a few microns to sub-micron. The process involves trench etching in silicon wafers (Fig. 1a); their partial filling (Fig. 1b) by doped silicon oxide like phospho-silicate glass (PSG) or boro-phospho-silicate glass (BPSG); heat treatment to squeeze the void (Fig. 1c) and finally channel with circular cross-section is achieved (Fig. 1d).

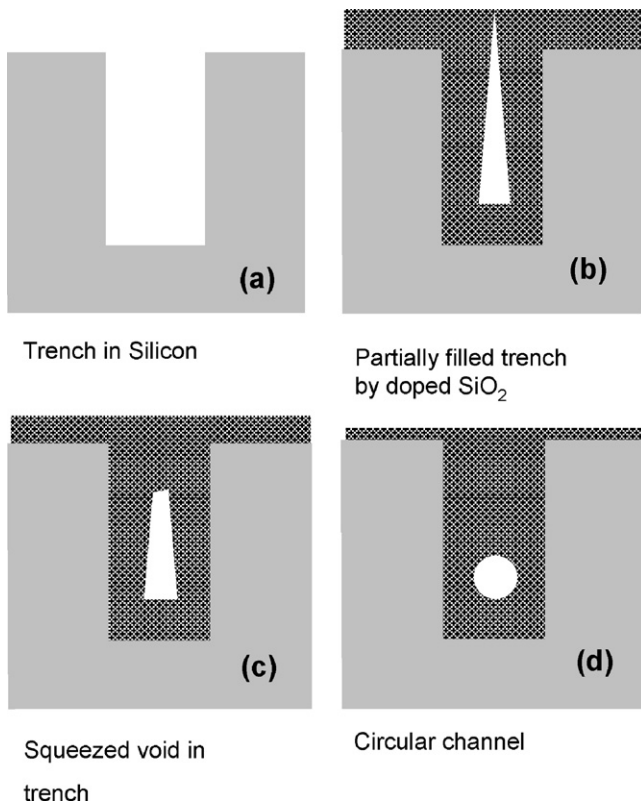


Fig. 1. Schematics depicting circular channel formation: (a) trench in silicon, (b) partially filled trench by PSG, (c) reduced void after heat treatment and (d) further reduction in void to form circular channel.

The self-sealed channel's diameter depends on the trench dimensions (mainly width and depth) and the thermal cycle. We investigated trenches 0.2–5 μm wide and 0.5–7 μm deep. However, trenches with smaller or larger dimensions may be required for different target dimensions of the channels. Doped silicon dioxide, i.e. phospho-silicate glass (PSG) was filled in the trenches at 2.5 T and 350 $^{\circ}\text{C}$ wafer-chuck temperature, using a PECVD process. These filling conditions were so chosen to keep a desired void in the trench. The void volume can be tailored by deposition conditions. For example, the PSG deposition rate reduces with the decrease in chamber pressure. This may lead to larger void volume or trench may not close after the same deposition time, due to conformal deposition. If deposition time is significantly increased, it may finally result in fully filled trench. The wafers were subjected to thermal cycles above PSG's softening temperature (950 $^{\circ}\text{C}$), i.e. at 1100–1200 $^{\circ}\text{C}$ for different timings depending on the final cross-section of channel required. To integrate the channels with other device structures like chamber or reservoir, chemical mechanical polishing (CMP) is used to planarize the wafer surface; followed by masking and etching of silicon oxide and silicon. Fluidic input and output port were formed in PDMS block, which capped the open reservoirs.

3. Modelling of micro-channel

The final cross sectional diameter of the self-sealed channels depends on the deposition and re-flow conditions. Their minimum dimension can be estimated as discussed subsequently. Let the non-conformal doped silicon oxide is filled in the trenches at temperature T_i and pressure P_i . This leads to a void in the trench with cross sectional area A_i . Since the void created in the trench is at sub-atmospheric pressure, the void has tendency to reduce if the silicon oxide is softened. Depending on the softening conditions, the final dimension (A_f) of the void can be predicted. If the softening is done at temperature T_f and pressure P_f , from gas law:

$$\frac{(P_i \times V_i)}{T_i} = \frac{(P_f \times V_f)}{T_f} \quad (1)$$

where V_i and V_f are initial and final volume of the void. Since, the length of the void (channel) can be assumed to remain unchanged, as its length is significantly larger than the cross-sectional dimensions; A_i and A_f can replace V_i and V_f , respectively in Eq. (1). So we get:

$$\frac{(P_i \times A_i)}{T_i} = \frac{(P_f \times A_f)}{T_f} \quad (2)$$

$$A_f = \left(\frac{P_i}{P_f} \right) \times \left(\frac{T_f}{T_i} \right) \times A_i \quad (3)$$

Say, in a typical case, doped silicon oxide (BPSG) is deposited at 400 $^{\circ}\text{C}$ and 50 Torr pressure. It is observed that it creates a void of $\sim 6 \mu\text{m}^2$ cross sectional area, in the 2 μm wide and $\sim 7.7 \mu\text{m}$ deep trench. This void can be reduced to the minimum circular cross sections as mentioned in Table 1, if doped oxide is allowed to re-flow for sufficient long time. However, the circular channel dimensions, greater than the least diameter are also achieved

Table 1
Expected final cross-sectional minimum dimensions of the channel at different reflow temperatures

	Sample no.		
	1	2	3
Initial cross-sectional area (A_i) (μm^2)	6.0	6.0	6.0
Re-flow temperature ($^\circ\text{C}$)	900	950	1000
Final cross-sectional area (A_f) (μm^2)	0.688	0.717	0.746
Radius of channel calculated (μm)	0.467	0.477	0.487
Actual radius of channel (μm)	0.406	0.443	0.505

by proper controlling the temperature and time of the thermal cycles. The softening temperature of PSG being higher than that of BPSG, it requires more time and temperature to re-flow by same amount.

As per model suggested, the final radius of the channel is expected to be more if oxide-reflow is done at higher temperature. At reflow temperature of 900, 950 and 1000 $^\circ\text{C}$, radius of the channels is expected as 0.467, 0.477 and 0.487 μm , respectively. But actual measured cross sectional radius of three samples is 0.406, 0.443 and 0.505 μm , respectively. These values follow the trend predicted but do not match exactly the calculated values. The reasons for the deviations could be errors in estimating the initial cross-sectional area, as it is not a regular structure (Fig. 2) and the reduction in channel length during re-flow process.

4. Results and discussions

4.1. Optimization of channel cross-section

The final diameter of the self-sealed channel depends on various parameters; prominent of them are trench width and depth,

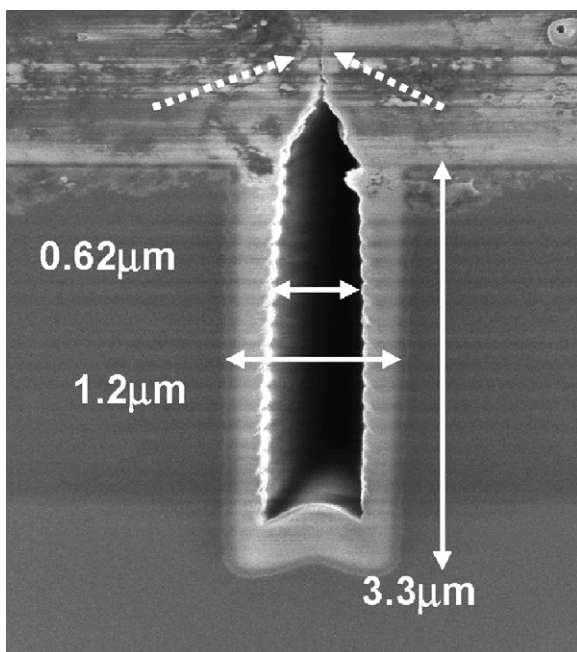


Fig. 2. SEM cross-section of trench (width 1.2 μm and depths of 3.3 μm) partially filled with doped silicon oxide.

doped oxide deposition and re-flow (temperature and time) conditions. The trench dimensions and the oxide filling state decides the initial volume of the void while the temperature and duration of the thermal cycle ensures the final shape and size of the channel. A typical SEM cross-section of silicon trench (width and depths of 1.2 and 3.3 μm , respectively); partially filled with doped silicon oxide to yield 0.61 μm wide void with inverted V-top is illustrated in Fig. 2. Due to non-conformal deposition processes for doped silicon oxides, the top edge of the trenches get more material and seals the trench before being completely filled. Dotted arrows in Fig. 2 indicate the pinch-off point of oxides from two sides. By increasing the trench width, the channel sealing time is prolonged and leads to higher void volume.

The effect of trench width (4.4–1.2 μm) on channel cross-sections, after PSG deposition and thermal treatment (1100 $^\circ\text{C}/30$ min) is depicted in Fig. 3, where 4.4 μm wide trench remain open while 1.2, 2.3 and 3.3 μm wide trenches form sealed void tunnels with varied cross-sectional dimensions. These conditions could not yield circular cross-sections, in any of these trenches, due to insufficient re-flow. However, the images clearly suggest that the re-flow of PSG strongly depends on aspect ratio of trench; wider the trench, it is easier to squeeze in; hence, the void shape is more circular in case of wider trench (3.3 μm) than the narrower trenches (2.3 and 1.2 μm). The filling in 1.2 μm wide trench is minimal. This proposes that 2.3–3.3 μm wide trenches are suitable for ~ 1 μm diameter circular channels.

Since 4.4 μm wide trench remains open after 4 μm PSG deposition and re-flow, it is not considered for re-flow optimization cycles. By increasing thermal treatment at 1100 $^\circ\text{C}$ for 45 min, the channel cross-sections reduce additionally (Fig. 4). On other hand, re-flow at 1200 $^\circ\text{C}/20$ min completely vanishes the channels in 2.3 and 3.3 μm wide silicon trenches (Fig. 5). As per model discussed earlier, the expected channel diameter in these cases is ~ 5 nm (where deposition pressure and temperature are 3 mTorr and 350 $^\circ\text{C}$, respectively, and re-flow is accomplished at 1200 $^\circ\text{C}$ in atmospheric furnace). Such small channels are extremely difficult to achieve because as the sample cools, the channel continues to squeeze due to soft PSG and the gases in the channel can diffuse into the surrounding silicon oxide. The optimal conditions for 2 μm wide trenches to yield fully circular channel (with diameter ~ 1 μm) are achieved at 1150 $^\circ\text{C}$ for 30 min (Fig. 6). The channel cross-section after various thermal cycles, in 2.3 μm wide trenches is shown in Fig. 7. Here, the self-sealed channels treated at 1100 $^\circ\text{C}/30$ min is elongated (Fig. 7a) while channels after 1150 $^\circ\text{C}/30$ min and 1200 $^\circ\text{C}/5$ min (Fig. 7b and c) yield circular cross-section with diameters 1.4 and 0.7 μm , respectively. Nano-channels with 73–195 nm diameters are also realized using 200–220 nm wide and 500 nm deep trenches (Fig. 8) after 1150 $^\circ\text{C}$ treatments for 30 min.

4.2. Device packaging

A micro-fluidic chip integrated with channels and fluidic reservoirs is realized (Fig. 9) and tested for patch clamp applications. After the formation of circular channels, chemical mechanical polishing planarizes the surface; reservoirs defined

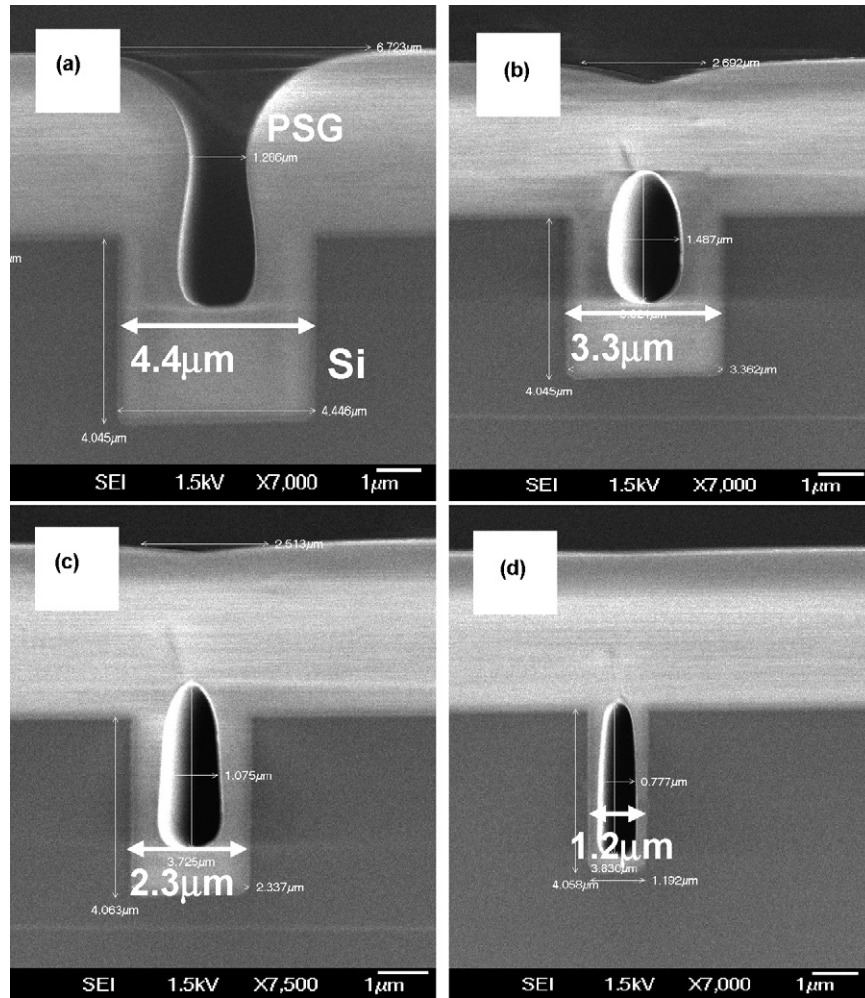


Fig. 3. SEM cross-sections of 4 μm deep, 200 μm long trenches filled with 4 μm thick PGS and thermally treated at 1100 $^{\circ}\text{C}$ for 30 min: (a) 4 μm wide trench with open void, (b–d) 3–1 μm wide trenches, respectively, with self-sealed elongated channels.

by lithography followed by reactive ion etching of silicon oxide and silicon. The channel's edge is smoothed by heat treatment in nitrogen/ oxygen ambient at 1050 $^{\circ}\text{C}$ for 30 min (inset of Fig. 9). Since the depth of the reservoirs in the silicon chip is about 5 μm , remaining chamber height is obtained through a PDMS cap. Chips with higher chamber depths (15–20 μm) are also realized. Such devices do not require recess in the cap. PDMS cap containing input/output fluidic ports along with reser-

voirs was separately realized, manually aligned and bonded to the chip [12,13].

4.3. Electrical testing

Patch clamp experiments were performed in a Faraday cage and the signals were recorded using a commercial amplifier, EPC10 (HEKA Inc.). Before each patch clamp testing,

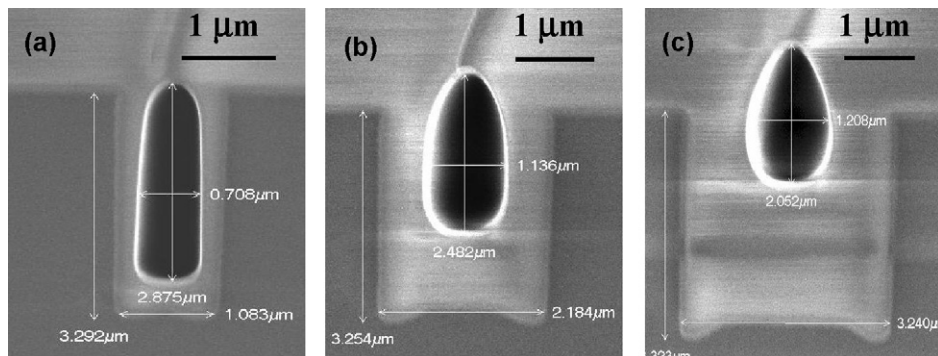


Fig. 4. SEM x-section of keyholes after PSG re-flow at 1100 $^{\circ}\text{C}$ for 45 min show less Elliptical channel in all: (a) 1.2 μm wide, (b) 2.3 μm wide and (c) 3.3 μm wide Si trenches.

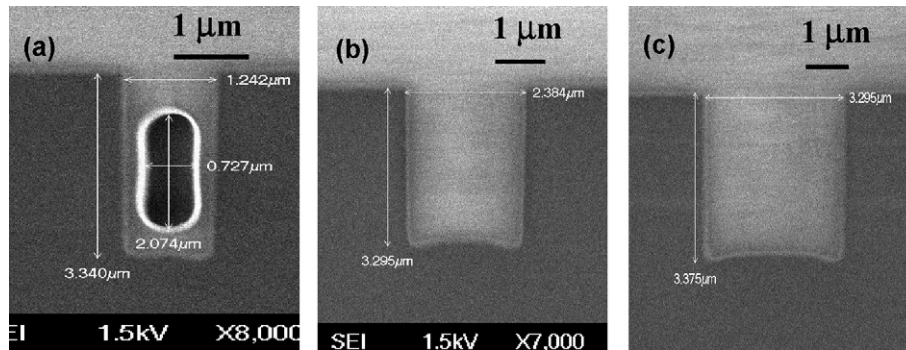


Fig. 5. SEM x-section of keyhole after PSG re-flow at 1200 °C for 20 min: (a) elliptical channel in 1.2 μm wide Si trench, (b) 2.3 μm wide and (c) 3.3 μm wide Si trenches are fully filled with PSG.

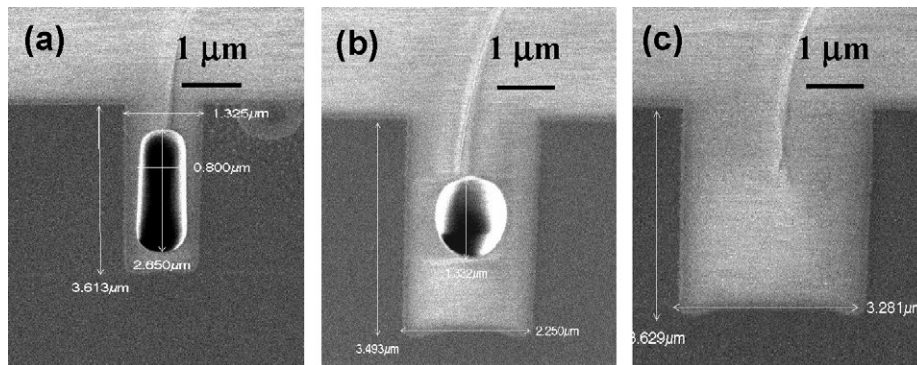


Fig. 6. SEM x-sections of keyhole after PSG reflow at 1150 °C for 30 min show: (a) elliptical channel in 1 μm Si trench, (b) circular channel in 2 μm Si trench and (c) 3 μm wide Si trench is fully filled.

devices surface preparation is done by priming the chambers with an ionic solution of composition (in mM): 150 NaCl, 2.8 KCl, 10 CaCl₂, 1 MgCl₂, 10 4-(2-hydroxyethyl)-1-piperazineethanesulfonic acid (HEPES), and 2 mg/ml glucose; pH 7.2 (310 m Osm). Rat pheochromocytoma cells (PC12) were used for evaluating the seal formability of the round channels. The cells were incubated with a fluorescent dye of 5 μg/ml Calcein-AM (Invitrogen) for 15 min at 37 °C. They were then trypsinized, spun down (1000 rpm, 4 °C and 5 min) and re-suspended in the above solution.

Electrical resistances (R) across different lengths of electrolyte-filled tunnels are presented in Fig. 10. These data agree with the classical $R = \rho L/A$ formula; where resistance is a function of resistivity (ρ), length (L) and cross-sectional area (A).

A thin layer of thermal oxide is originally grown on the surfaces of the silicon chips for electrical insulation. But the channel resistance, after the introduction of the electrolyte shows a large capacitance effect due to the silicon substrate (Fig. 11). The magnitude of this coupling is dependent on several factors, mainly

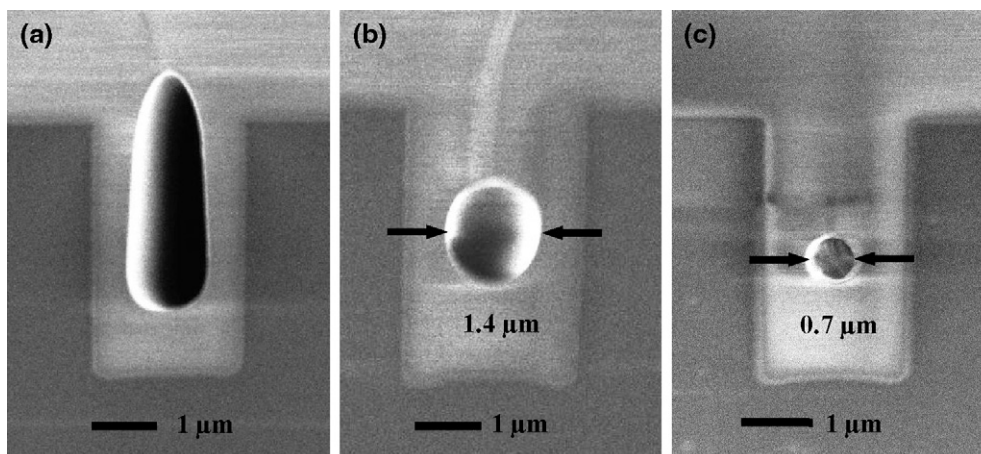


Fig. 7. SEM cross-section of 4 μm deep, 2 μm wide and 200 μm long trenches filled with 4 μm thick PGS and thermally treated at (a) 1100 °C/30 min (b) 1150 °C/30 min and (c) 1200 °C for 5 min.

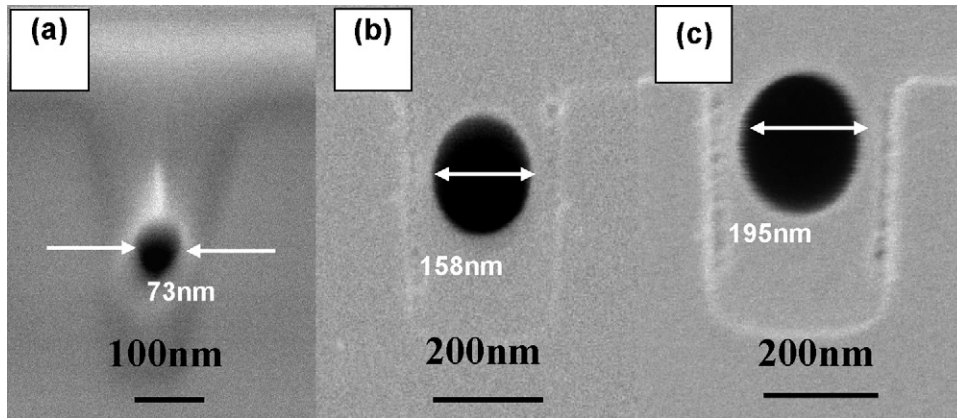


Fig. 8. SEM cross-section of trenches ~ 500 nm deep; $2 \mu\text{m}$ thick PGS filled and re-flow at $1150^\circ\text{C}/30$ min: (a) tapering trench with 120–240 nm width, (b) 200 nm wide trench and (c) 220 nm wide trench.

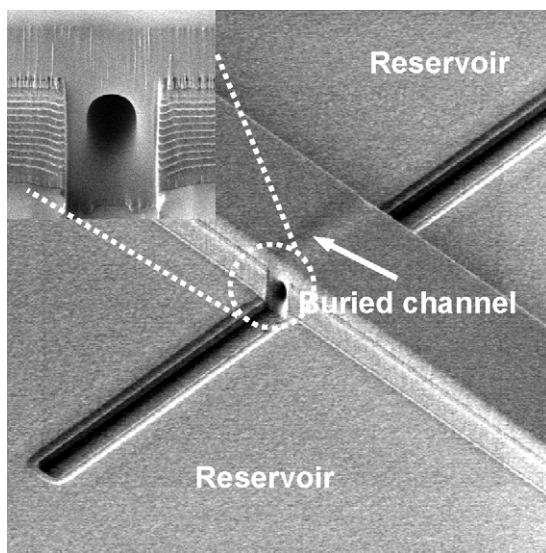


Fig. 9. Ten-micrometer long channel integrated with reservoirs on two sides. Inset: close-up of smoothed channel edge.

contact area of electrolyte with the chip and thickness of dielectric layer on silicon. This spike is undesirable, as it cannot be effectively compensated away using commercial patch clamp amplifiers. In order to reduce such spikes, various dielectric layers in different thicknesses are deposited on the chips. With a consistent voltage pulse applied by EPC10, the responses of

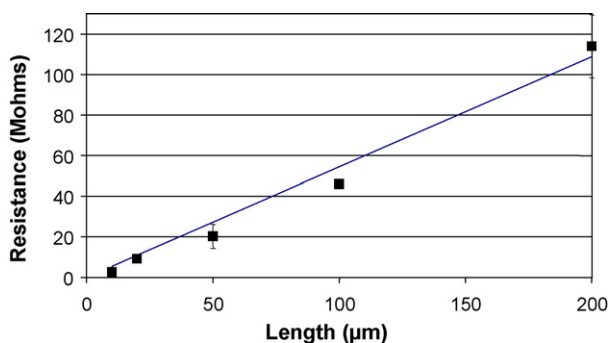


Fig. 10. Electrical resistances across different lengths of electrolyte-filled tunnels.

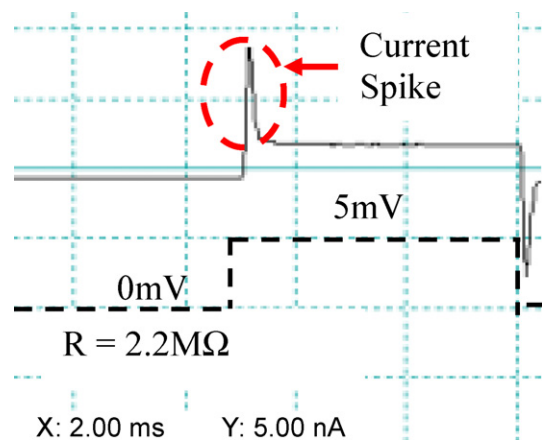


Fig. 11. Typical current recording through an electrolyte-filled channel.

the different layers were obtained as shown in (Table 2). It is observed that at least $2 \mu\text{m}$ thick silicon oxide is preferred to reduce the spike to ~ 0.3 nA corresponding to capacitance of below 50 pF.

The cells are introduced into the reservoir and a cell within $50 \mu\text{m}$ reach of the patch aperture could be attracted to the opening of the channels (Fig. 12a) by applying ~ 25 kPa suction to the recording chamber through a manual syringe pump. The fluorescence view of a trapped cell under UV excitation is shown in Fig. 12b. A typical current through a $50 \mu\text{m}$ long channel with cell trapped is depicted in Fig. 13. From this current trace, the seal resistance achieved is $400 \text{ M}\Omega$. With the current sealing level, whole-cell recording is possible.

Table 2

Average capacitive spike recorded during electrolyte-filled channel resistance measurement with different dielectric layers in the chambers

Surface layer	Average spike magnitude
Original surface	~ 20 nA
$0.1 \mu\text{m}$ silicon nitride	~ 10 nA
$0.5 \mu\text{m}$ oxide	~ 2 nA
$1.0 \mu\text{m}$ oxide	~ 1.4 nA
$1.5 \mu\text{m}$ oxide	~ 0.75 nA
$2 \mu\text{m}$ oxide	~ 0.3 nA

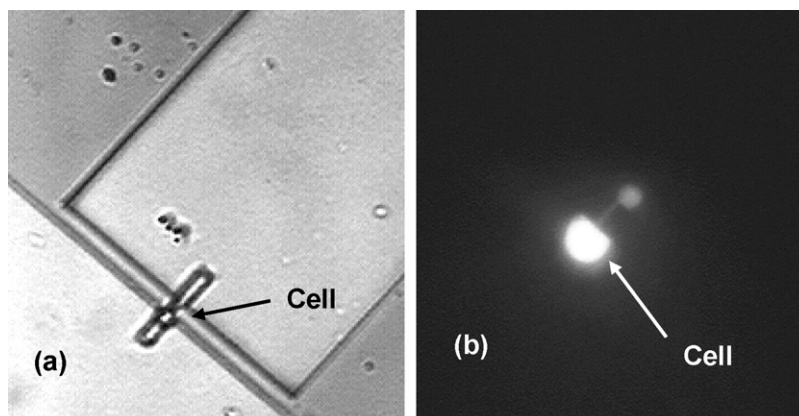


Fig. 12. (a) Optical image depicting cell trapped with 10 μm long and 1.2 μm diameter channel packaged by PDMS and (b) fluorescence image of the trapped cell.

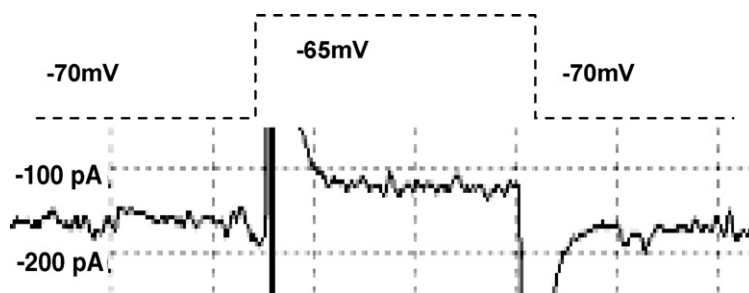


Fig. 13. Current recording through 50 μm channel with trapped cell in response to voltage pulses.

5. Conclusions

Fully rounded and self-sealed channels with diameter varying from microns to less than 100 nm, and length in few tens to hundreds of microns range have been realized. Apart from fluidic interconnects and valves, they find numerous applications in micro-fluidic devices pertaining to detection and manipulation of single molecules, cells or biological species. The chip with fully round lateral channel with smoothed aperture and fluid chambers was used to trap the cell. A chamber coating with dielectrics to reduce the spike during electrical measurements is optimized; 2 μm silicon oxide has significantly reduced the spike to ~ 0.3 nA corresponding to capacitance of below 50 pF. The rounded edge of the aperture also aid in achieving the high resistance seal (>0.4 G Ω) during cell clamping. The process can also be used to fabricate multiple self-aligned channels in array configuration for multiplexed analysis.

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Biographies

Ajay Agarwal received PhD from Birla Institute Technology and Science, Pilani, India in high temperature superconducting materials and devices. Currently, he is working in Bio-Electronics Program of Institute of Microelectronics, Singapore and leading the development of silicon nanowires for biological and chemical sensors, in array format and integrated with fluidics. He is also actively

involved in the development of biochips like lateral patch-clamp arrays with circular channels; micro-fluidics on transparent substrates; silicon-based substrates for surface-enhanced Raman scattering (SERS) and others. The devices are based on silicon nanotechnologies pertaining to nanowires, nanochannels, nanostructures, etc.

Nagarajan Ranganathan received his BE degree in 1982 in electronics and telecommunications engineering from Osmania University, Hyderabad and MTech degree in 1984 in integrated electronics and circuits from Indian Institute of Technology, New Delhi (India). He is presently working in Institute of Microelectronics, Singapore as member of technical staff. His present research interests are bulk and surface micromachining technologies for MEMS, NEMS and Bio-MEMS applications, 3-D wafer level packaging technologies and polymer electronics.

Wee-Liat Ong is currently a research staff in the Institute of Microelectronics, A*STAR, Singapore. He received his BEng (1st class honours, 2002) and MEng (2004) degrees in mechanical engineering from the National University of Singapore. His masters degree dissertation was in the implementation of an automated robotics-based patch clamping setup. His current research inter-

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Tang Kum Cheong received his MSc degree in MEMS in 2005 from Nanyang Technological University, Singapore and has been working at the Institute of Microelectronics since then. His research interests are in the development of micro-fluidic devices for lab-on-a-chip applications and micro devices fabrication using cleanroom processes.

Levent Yobas is currently leading the BioMicrofluidics Group at the Institute of Microelectronics (IME) Singapore. Prior to IME, he was with Standard MEMS Inc., Massachusetts, where he worked on the development of MEMS-based products for drug screening technologies. His earlier work on silicon microvalves led to a low-cost tactile display system which is currently commercialized by iActiv Corporation, Ohio. His research interest covers a wide range of topics with a main emphasis on applications of micro-fluidics and microfabrication technologies to life sciences and medicine. Dr. Yobas received his BSc degree in electrical engineering from Hacettepe University, Ankara, and MSc and PhD degrees both in biomedical engineering from Case Western Reserve University, Cleveland, Ohio.