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Trench Sidewall Doping for Lateral Power Devices

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Abstract:

Sidewall doping of trenches with a high aspect ratio and a high grade of anisotropy (90° ± 0.5°) by ion implantation has been investigated. Two-dimensional (2D) process simulation and delineation experiments have shown a good agreement between simulation and experimental results. The doping of the trenches has been evaluated in order to manufacture functional wells for lateral power devices. 2D device simulation has been performed to compare optimized sidewall profiles of lateral power devices with the profiles reached by ion implantation. From these data, the process parameters for the ion implantation process referring to optimal device performance have been determined.

1. Introduction

Lateral power devices such as Lateral Insulated Gate Bipolar Transistor (LIGBT), Lateral Double Diffused Metal Oxide Silicon Transistor (LDMOS) and lateral pin diodes for smart-power net appliances need novel device concepts like the Reduced Surface Field (RESURF) principle [1],[2] and adapted technology concepts in order to support the device conception.

One important technology is the dielectric isolation of the power devices to protect the low voltage parts of smart-power circuits for net applications against parasitic currents and voltages [3]. The key process for manufacturing dielectric insulating islands is the trench etching process on Silicon On Insulator (SOI) substrate material. The sidewall doping of these trenches is crucial for device performances as mentioned above. The lateral distribution of the concentration of the dopants as well as the vertical homogeneity of the doping profile of the sidewall are critical parameters. The benefit of ion implantation is the good controllability of the doping process, via implantation energy the projected depth and via implanted dose, the concentration of dopants are adjustable. Another benefit using ion implantation instead of doping, e.g. via Chemical Vapour Deposition (CVD) of a doped glass, is that there is no need depositing homogeneous glass layers in deep trenches with high aspect ratios and removing these glasses after the diffusion process.

In order to find an optimum set of parameters for the ion implantation process such as implantation angle and projected horizontal depth of p-n junction with respect to the thickness of the screen oxide layer, 2D equations have to be solved. The most important difficulty in controlling the distribution and homogeneity of the dopant concentration is the scattering effect of ions at the trench sidewalls due to the impact of the ions with sidewall atoms. For this reason, simulation of the device manufacturing process and in parallel of the electrical parameters has to be performed to find the optimal process parameters in accordance with the device performance needs. All simulation work has been performed using TCAD tools of ISE [4,5].

2. Process simulation

For process simulation, a deep trench topology with high aspect ratio (15:1), as proposed for a high voltage smart-power process, was configured. The trench geometry was determined by the application of the power devices as net switches and the technological limitations, i.e. the withstand voltage of 600 V on the one hand and the void free refill process on the other hand. The trench depth was varied in the range of 40 to 50 microns and the width was defined via the aspect ratio. The trench walls were covered with a screen oxide of 10 to 20 nm. Because of the small implantation angle and the calculated projected horizontal depth, it was necessary to implant at an implantation energy in the range of 100 to 200 keV. To prevent doping of the surface of the silicon substrate a thick oxide mask was required.

For simulation of the ion implantation process, a simulation tool based on Monte Carlo (crystal trim) simulation was used [6], especially regarding the scattering effect of ions from the sidewalls of the trench. In several iterations of 2D process and 2D device

simulation, the optimum trench geometry and implantation process parameters have been evaluated.
The substrate material was phosphorous doped with a specific resistivity in the range of 10 to 20 ohm·cm, because lateral n-channel power devices are considered. Therefor, the sidewalls have to be p-type doped with boron. The implantation doses have been varied from $5 \cdot 10^{14}$ cm^{-2} to $5 \cdot 10^{15}$ cm^{-2}. In figure 1, a simulation result of an optimized doped trench structure on SOI substrate material is shown. A maximum doping concentration of $1 \cdot 10^{18}$ cm^{-3} (boron) and a p-n junction depth of 5.7 microns has been considered as optimum for device performance in blocking mode.

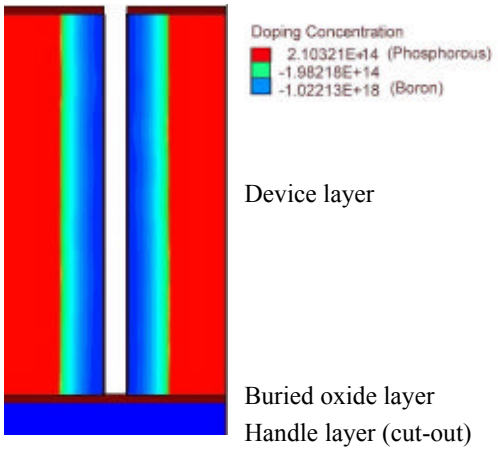

Figure 1. Optimized sidewall doped trench structure

Figure 2 shows the simulated lateral doping profile in the middle and at the bottom of the trench wall.

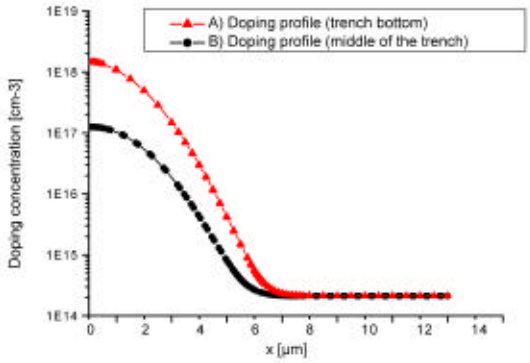

Figure 2. Horizontal doping profiles
(A) trench bottom, B) middle of the trench)

Boron profile (B) was taken from the middle of the trench wall. At the bottom of the trench wall (A) the absolute doping concentration is a factor of ten higher than in case A (middle position of sidewall) and in lateral direction, the well (p-n junction) is 0.35 µm deeper than in the middle (figure 5). This is due to the scattering effect of ion implantation. But this rise in concentration and well extension at the lower part of the trench (especially last three microns) is nearly negligible for device functionality, as will be shown below.

3. Device simulation

The above process parameters have been optimized for lateral power devices in high voltage smart-power ICs. The device concept is based upon the RESURF principle [2] and the use of SOI substrate material. SOI material with a 40 to 50 µm thick device layer was chosen. To protect the low voltage parts of smart-power ICs from parasitic currents and voltages, it is necessary to isolate the power device parts from the rest of the IC. The device areas are defined by deep trenches (as described in 2.) and the buried oxide layer (BOX) of the SOI material. The trenches are refilled with dielectric insulating material. A cross-section of the simulated device structure, a LIGBT with the idealized doping profiles, i.e. homogenous doping along the whole trench wall, is shown in figure 3.

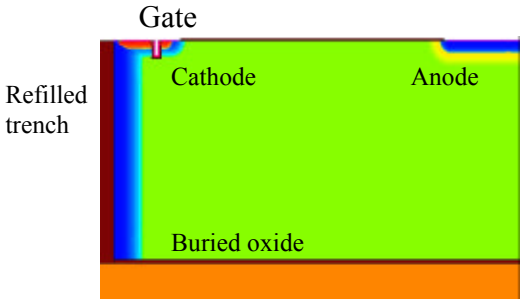

Figure 3. LIGBT half cross-section with idealized doping profiles

These structures require broad sidewall wells in lateral direction, because of the influence of the sidewall p-n junction depth on the potential and field distribution in blocking mode. Figure 4 displays the ideal distribution of the potential lines in the blocking mode, at 600 V, over the cross-section of the device. The simulation was performed using the idealized doping profile of figure 3.

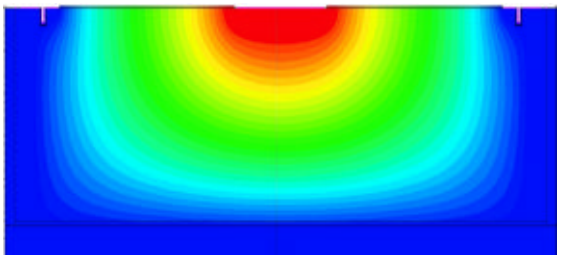

Figure 4. Cross-section of the potential distribution of a LIGBT in blocking mode at 600 V

To take into account the disturbance of the distribution of potential lines due to the accumulation of dopants at the bottom of the trench walls the modified structure of figure 5 has to be analyzed. To figure out the influence of the variations of the sidewall doping profile, a device structure with an inhomogenous doping profile and with a homogenous profile at the bottom of the trench have been compared.

A detail of this modelled device structure with an inhomogenous profile is shown in the figure 5.

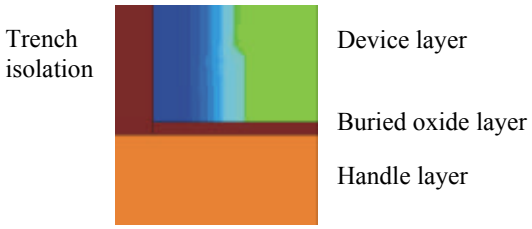

Figure 5. Detailed cross-section of modelled device structure

As the most important parameter, the influence of the described doping inhomogeneity has been considered on blocking characteristics of the LIGBT. Therefor, the blocking characteristics of device structures with homogenous and real doping profile has been simulated. The differences in blocking characteristics of the two cases can be seen in figure 6.

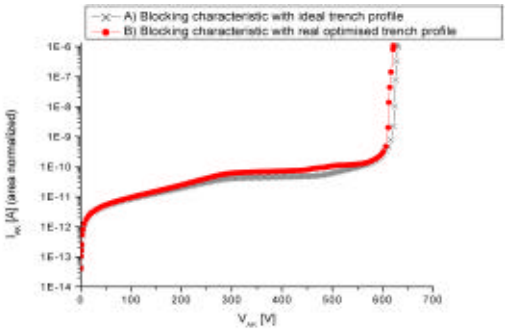

Figure 6. Blocking characteristics of a LIGBT with
A) "ideal" (homogenous) trench doping profile
B) modelled "real" trench profile

The two simulated blocking characteristics show nearly the same performance, except for a 5 V higher breakdown voltage of the "ideal" device structure. This means less than one percent of breakdown voltage loss by using ion implantation for sidewall doping of deep trenches.

4. Experiments

Deep trenches in silicon have been manufactured by anisotropic dry etching. These processes were based on the Advanced Silicon Etch (ASE) process [7]. The aspect ratio has been 15:1. The angle between the trench sidewall and the trench bottom has been 90°±0.5°.
The results of 2D process simulation have been the basis for the ion implantation experiments. The variation of implantation energy, angle and dose has been combined in an experimental matrix (as described in 2.). Regarding the variation of the parameters in an optimized process window, a trade-off between process and device needs, e.g. thickness of screen oxide (10nm), doping concentration profile (analog figure 1) and thickness of the device layer (50µm), has been found. After the implantation, the annealing for implant damage and diffusion has been performed. The temperatures and times have been adjusted to the thermal budget needed for manufacturing a LIGBT. For delineation of the sidewall doping, the cross sectioned samples have been exposed to a special silicon etchant [8]. The preparation process is based upon the selectivity of the etchant, i.e. p-doped silicon is etched faster than n-doped silicon. Etching contours will become visible under scanning electron microscopy which represent equi-concentration lines. Calibration of these contour lines has been performed using samples with a doping profile in vertical direction and analyzing the doping profiles of these samples by Secondary Ion Mass Spectroscopy (SIMS). All samples have been etched with the etchant described in table 1 and the samples have been illuminated with a halogen lamp during etching.

Table 1. Process parameters for sample preparation [9]

Acids	Volumes [ml]	Time [sec]
Hydrofluoric acid	7	20
Nitric acid	20	
Acetic acid	53	

Using Scanning Electron Microscopy (SEM), the samples have been inspected. Because of the selectivity of this etching process, the low p-type doped silicon near the metalurgical p-n junction shows less material removal than the regions with higher boron concentration. Figure 7 shows an expample of a ion implanted doped trench, etched to reveal the p-n junction and doping concentration lines.

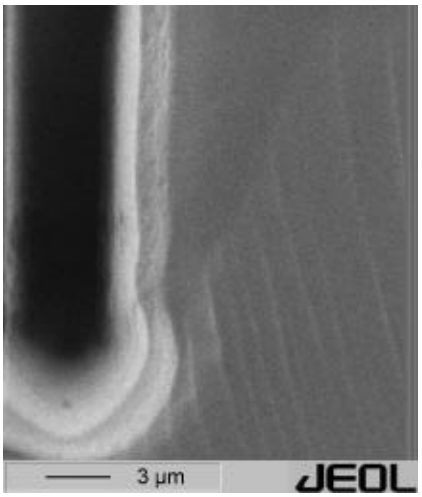

Figure 7. Etched sample inspected with SEM

5. Results and discussion

When designing the complete process, i.e. trench and smart-power device formation in a well defined manner, the annealing and diffusion processes of the smart-power devices can act for the drive-in steps of the trench well implantation. This means a reduction in the number of manufacturing steps in comparison to glass doping. Furthermore, there is no need in removing glass in deep trenches, which is a difficulty in deep trenches with high

aspect ratio. For the 2D process simulation as well as for the experiments, the same process parameters have been used. Comparison of figure 8 a and b shows, that the 2D process simulation of the p-n junction depth of 5.7 microns is in excellent agreement with the experimental determined junction depth. Further on, the simulated doping concentration lines are in good agreement with the experimental results, as can be seen in figure 8 a and b, too. The peak concentrations of the vertical profile, in the middle of the trench, have been in the range of 1 to $3 \cdot 10^{18}$ cm^{-3} (boron) for simulation and measured vertical SIMS profile.

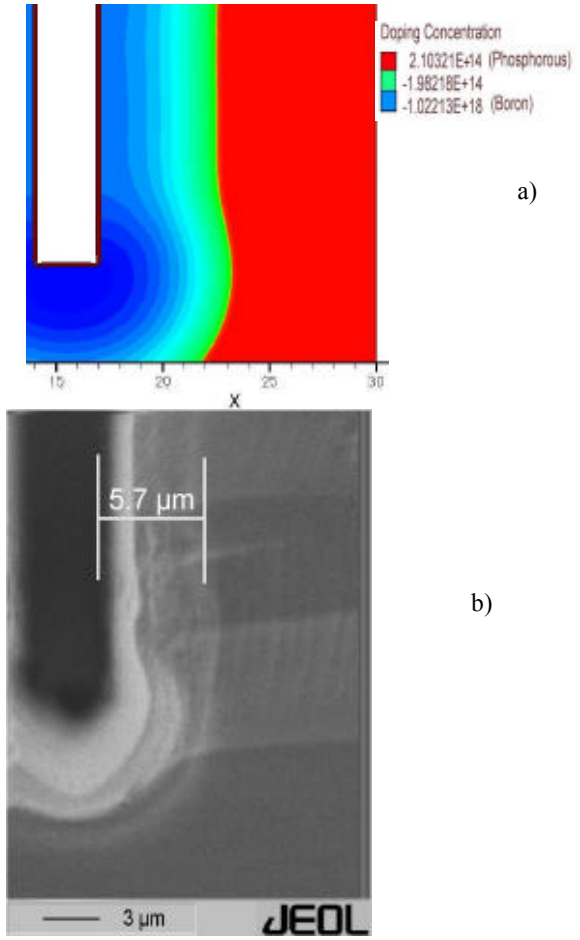

Figure 8. a) Simulated, b) experimental doping profile

The influence of inhomogeneity in trench sidewall doping profile at the bottom of the trench on device functionality has been investigated and minimized. Therefor, by the use of 2D device and process simulation, the trench sidewall doping process has been optimized, in a way that parasitic effects due to inhomogeneities of doping concentration distribution are nearly negligible.
The well defined ion implantation process opens new fields of application, e.g. 3D RESURF structures like CoolMOS or integrable passive 3D devices.

6. Acknowledgements

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7. References

[1] J. A. Appels, H.M.J. Vaes, "High Voltage Thin Layer Devices" (RESURF Devices), ESSDERC 79, Munich, Germany.

[2] A.W. Ludikhuize, "A Review of RESURF Technology", ISPSD 2000, May 22-25, Toulouse, France.

[3] M. Stoisiek, "Technologien für Hochvolt-ICs", Electrical Engineering 1996, pp. 379 - 392, Springer Verlag.

[4] DIOS-ISE, ISE TCAD Release 7.5 User`s Manual, Zurich, 2001.

[5] DESSIS-ISE, ISE TCAD Release 7.5 User`s Manual, Zurich, 2001.

[6] J.P. Biersack, S. Berg, and C. Nender, "T-DYN Monte Carlo simulations applied to ion assisted thin film processes," Nucl. Instr. and Meth. in Phys. Res. B59/60, pp. 21-27, 1991.

[7] J. Bhardwaj , H. Ashraf, A. McQuarrie, "Dry Silicon Etching for MEMS", The Symposium on Microfabricated Systems at the Annual Meeting of the Electrochemical Society, Montreal, Quebec, Canada, May 4-9, 1997.

[8] S.K. Ghandhi, "VLSI Fabrication Principles", Wiley, 1983.

[9] L. Gong, A. Barthel, J. Lorenz, H. Ryssel, "Lateral Spread of Implanted Ions into Silicon", Experiments, Proc. ESSDERC 89, pp.198, Berlin 1989.