A 4-Mbit DRAM with Trench-Transistor Cell

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Abstract—**An experimental 5-V-only 1M word×4-bit dynamic RAM with the page and SCD modes has been built in a relatively conservative 1-μm CMOS technology with double-level metal and deep trenches. It uses an innovative cross-point one-transistor (1-T) trench-transistor cell (TTC) that measures only 9 μm^2. A novel double-ended adaptive folded (DEAF) bit-line architecture used on this DRAM provides the breakthrough needed to take full density advantage of this cross-point cell. The 30-fF storage capacitance of this cell is expected to provided high alpha immunity since the charge is stored in polysilicon and is oxide isolated from the substrate. A 150-ns RAS access time and 40-ns CAS access time have been observed.**

I. Introduction

The DRAM development efforts at 4-Mbit level and beyond will have to rely on innovative cell structures which provide improved cell isolation and noise immunity while maintaining sufficiently large storage capacitance for high-speed signal sensing yet occupying no more than 10 μm^2.

The corrugated capacitor cell (CCC) [1] uses a three-dimensional capacitor formed inside a silicon substrate in order to provide an increased cell capacitance for a given silicon surface area. Although this cell is adequate for 1-Mbit DRAM's, it suffers from cell-to-cell leakage current on further scaling [2], [3]. Merging the trench capacitor with the isolation [4], [5] eliminates this leakage problem caused by the punchthrough between adjacent cells. However, it inherits a leakage problem due to a parasitic transistor formed on the trench sidewall. Furthermore, the advantage of these cells in terms of alpha-particle immunity is not clear. Another version of isolation-merged cell [6] stores the signal charge in the polysilicon node isolated by oxide for improved alpha-particle immunity, but has the drawbacks of larger cell size and trench sidewall leakage. The novel one-transistor (1-T) trench-transistor cell (TTC) used on this 4-Mbit DRAM [13] integrates both the pass transistor and the storage capacitor on the sidewalls of an 8-μm-deep trench [8]. The transistor and the capacitor are connected by a novel subsurface lateral contact scheme which enables an oxide-isolated charge storage for high noise immunity. Moveover, since the pass transistor wraps around itself, it is self-isolating and thus eliminates any parasitic leakage currents unlike other pass transistors. The lateral contact junctions have been characterized and simulated [3] for leakage currents and they are well within the requirements of a dynamic 1-T memory cell.

This paper describes an experimental 4-Mbit DRAM using this cell. A truly cross-point cell array has been realized using a novel double-ended adaptive folded (DEAF) bit-line architecture. Circuit and layout techniques are also described. The peripheral circuits have been placed and interconnected semiautomatically to achieve a short design cycle time. The performance of the experimental device and the trench transistor cell are also described in this paper.

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II. The Trench Transistor Cell

A. Fabrication Process and Cell Structure

The 4-Mbit DRAM is fabricated in a twin-well 1-μm CMOS technology that is basically the same as that for the 1-Mbit DRAM [7]. A shallow 4.5-μm p^- epitaxial layer is grown on a 1×10^{19} cm^{-3} p^+ substrate. A heavily doped substrate is needed for the capacitor storage plate while the shallow epitaxial layer provides latch-up immunity. The shallow epi also allows this process to be scaled even further. The p-channel and n-channel devices are formed inside the n-tank and p-tank, respectively. The effective channel length of these LDD devices is 1.0 μm. The self-aligned silicide process (SALICIDE) provides source–drain junctions as well as gate electrodes with less than 1-Ω/□ sheet resistance. This process uses two levels of interconnect to improve the layout density. Fig. 1 shows

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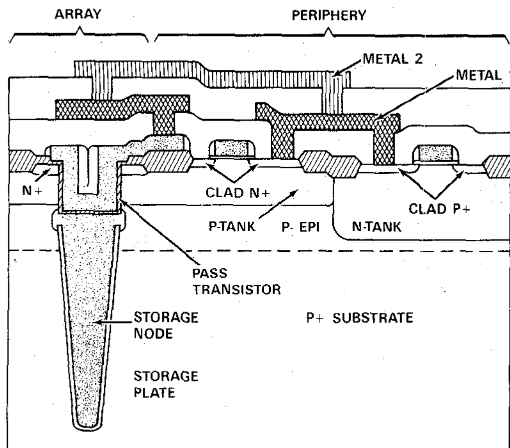


Fig. 1. Typical cross section of process topography.

a typical cross section of the process topography. The array and the periphery are shown together for the sake of completeness.

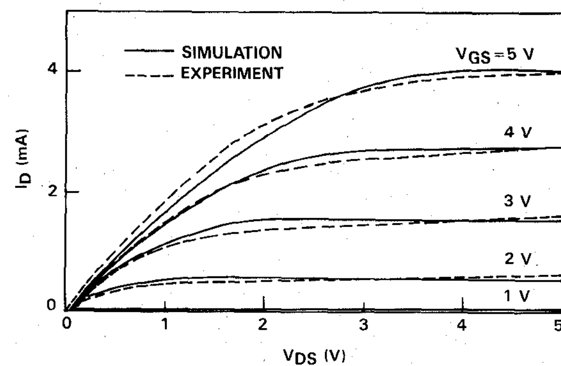
An 8-μm-deep rectangular trench is etched in the p-tank on the p^+ substrate (Fig. 1). A vertical pass transistor is made in the top 2 μm of the trench. The storage capacitor is also in the trench, below the pass transistor. The inner plate of the capacitor is an n^+ polysilicon plug, and the outer plate is the p^+ substrate. The source of the transistor is connected to the n^+ polysilicon plug of the capacitor by a subsurface lateral contact which is made by oxide undercut etch and refilling with polysilicon [8]. The drain, gate, and source of the trench pass transistor are made of diffused buried-n^+ bit line, n^+ polysilicon word line, and a lateral contact, respectively.

B. Device Simulation

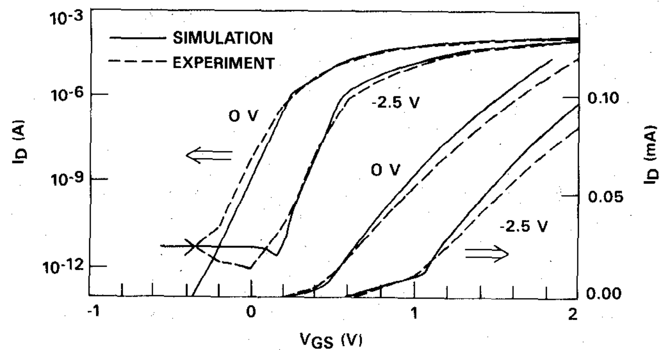
The trench transistor has been studied using a two-dimensional device simulator (PISCES) [9]. The gate oxide thickness and channel length are 25 nm and 1.5 μm respectively, while the transistor width is determined by the perimeter ($1.3 \mu m \times 1.5 \mu m$) of the trench. The threshold of the transistor is adjusted by a deep boron implant which results in a nonuniform Gaussian profile along the channel, with a peak (3.4E16 cm^{-3}) near the drain, leading to DMOS-type transistor behavior. The threshold voltage V_t and subtheshold slope S are determined by the highly doped part of the channel although the gain K is determined by the entire channel length. The measured device characteristics are within 10 percent of the results of the PISCES simulations in the linear and saturation regions, as shown in Fig. 2. The linear region and subthreshold transfer characteristics indicate that a low V_t suitable for 5-V operation and low S adequate for the sharp turn-off required for long refresh time, have been achieved.

C. Device Uniformity

The uniformity of device characteristics is crucial for their applicability as pass transistors in a 4-Mbit DRAM



(a)



(b)

Fig. 2. TTC pass-transistor $I-V$ characteristics: $W = 42$ μm; $L = 1.5$ μm; and $t_{ox} = 25$ nm. (a) Trench-transistor output characteristics. (b) Trench-transistor linear and subthreshold characteristics.

and beyond. Statistical data, shown in Fig. 3(a), from 960 trench transistors on a die indicate that the V_t is 1.1 ± 0.02 V. Die-to-die variations on the same slice are larger, with the threshold voltage varying by ± 0.08 V. The drive currents within a die, shown in Fig. 3(b), are reproducible to within ± 5 percent. However, the variation across a slice is ± 10 percent. All the devices were found to have very low (0.1 pA) leakage current at $V_{gs} = 0$ V. There are several possible reasons for the variations. The cell lateral contact is made by outdiffusing phosphorus through an undoped poly plug. The series source resistance is expected to be high and vary considerably, leading to variations in device characteristics. Second, the gate oxide thickness depends on the crystallographic orientation of the trench sidewall. Since, after lithography and etching, the trenches have an oval cross section, the gate oxide, and hence the transistor parameters such as V_t, K, and S vary along the trench perimeter [12]. This contributes to variability of the transistor parameters and leads to soft turn-on characteristics for these transistors.

III. The 4-Mbit DRAM

A. The Architecture

The early DRAM's used the open bit-line architecture for the array almost exclusively and were generally organized 1 bit wide. The open bit-line architecture pro-

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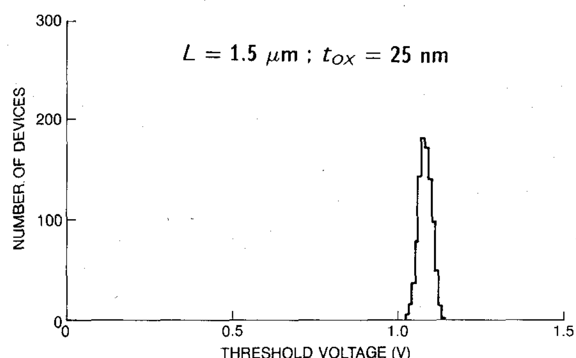
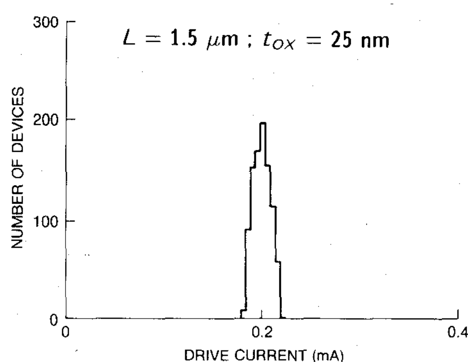


(a)



(b)

Fig. 3. TTC pass-transistor uniformity. (a) Threshold voltage uniformity. (b) Drive current uniformity.

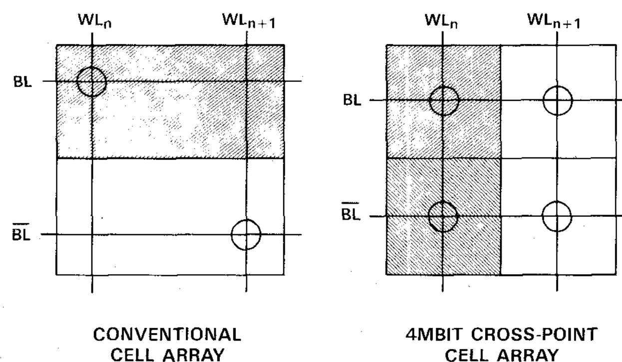


Fig. 4. Limitations of conventional folded bit-line architecture.

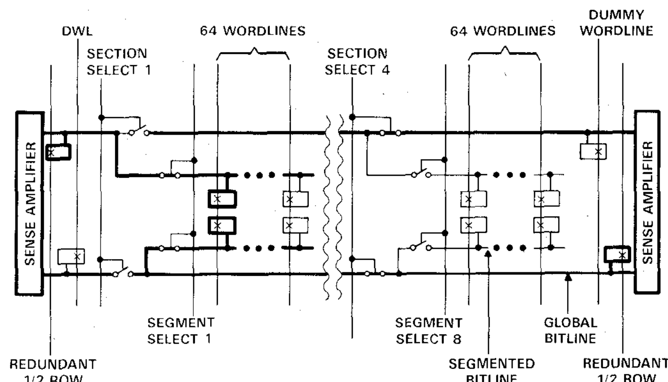


Fig. 5. Basic DEAF bit-line architecture.

vides a very dense memory cell array and is relatively simple to implement for the memory cells that are large enough to allow reasonable layout pitches for the decoders and sense amplifiers. However, the S/N ratio of the open bit-line architecture deteriorates as the cell area, and consequently the storage capacitance, decreases with higher level of integration. Also, the implementation of this architecture becomes more difficult due to smaller layout pitches for the decoders and sense amplifiers. The folded bit-line architecture [10] was adopted at the 64-kbit DRAM level to improve the noise immunity of the device and at the same time provide larger layout pitches for the sense amplifier and decoders. This conventional folded bit-line architecture has been able to match the array density of the open bit-line architecture since even the scaled-down memory cells have been large enough to accommodate two word lines and a bit line or vice versa. However, the folded bit-line architecture fails to match the array density of an open bit-line architecture for a cross-point memory cell such as TTC since a cross-point cell, by definition, is only as large as one word-line pitch and one bit-line pitch as shown in Fig. 4.

The DEAF bit-line architecture used on this 4-Mbit DRAM has all the advantages of the conventional folded bit-line scheme, such as noise immunity and larger layout pitches, and at the same time realizes a very dense, truly cross-point memory cell array. This architecture is explained in Fig. 5. It uses a segmented or divided bit-line approach [7], [11]. Eight diffused segments, with 64 cells each, are connected to a Metal-2 global bit-line through segment select transistors. Each of the global bit lines is divided into four sections by section select transistors. A pair of these global bit lines is connected to a pair of sense amplifiers, one at each end. The segment select transistors are normally OFF and the section select transistors are normally ON. A memory cell is placed at every intersection of word lines and the diffused segments. Metal-1 straps contact word lines at every 128 columns. Since the pass-transistor width is determined by the trench perimeter, it is larger than those used in conventional 1-T cells. The word-line capacitance is approximately 10 pF and has relatively short time constant due to metal straps.

When a word line is selected, corresponding segment select transistors are turned ON and the corresponding section select transistors are turned OFF. The section select transistors that are turned OFF divide the global bit-line pairs into two shorter pairs of bit lines. Each of these shorter pairs of bit lines forms the folded bit lines for the corresponding sense amplifier. A reference cell is provided at each sense amplifier. The two adjacent selected cells of the cross-point array are connected to these pairs of folded bit lines such that each one is sensed and amplified by the corresponding sense amplifier as shown in this figure. However, each of these shorter pairs of folded bit lines has an inherent capacitive imbalance. The bit line connected to the storage cell, as opposed to the reference cell, has an additional capacitance of the associated diffused segment. A simple technique to achieve perfectly balanced bit lines

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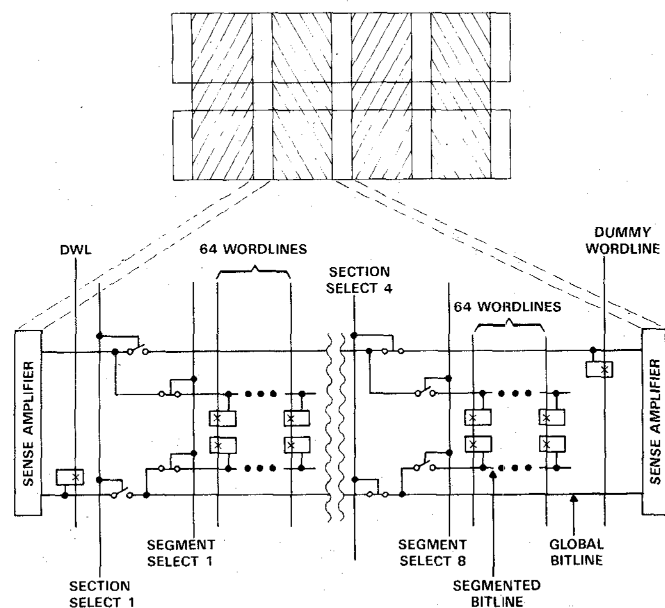

Fig. 6. Extension of DEAF bit-line architecture to form a block.

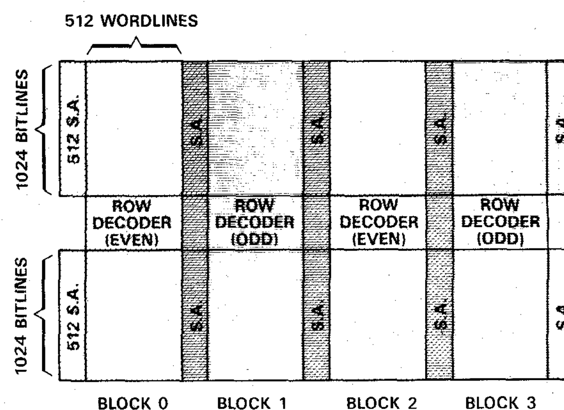

Fig. 7. A 4-Mbit DRAM array architecture.

is described later in this section. In this scheme, in the worst case, three section select transistors in series are encountered during the charge transfer between a cell and a sense amplifier. The charge-transfer mechanism has been simulated in great detail to quantify its time-delay components. The charge transfer between a cell and corresponding segment typically lasts for 4 ns. The charge transfer from the farthest segment to the sense amplifier takes another 4 ns. These delays are commensurate with the state-of-the-art DRAM.

A 1-Mbit block of 512 rows × 2048 bit lines is formed by extending this basic structure in the word-line direction as explained in Fig. 6. There are four such blocks as shown in Fig. 7. Each block is bracketed by an array of sense amplifiers as described above. The row decoders run across through the middle. The global bit lines run across all the four blocks with four section select transistors in each block. Only the alternate blocks are selected at a time in order to multiplex the three inner arrays of sense amplifiers between the adjacent memory blocks. The outer sense amplifiers are dedicated to outer blocks. Two word lines are activated simultaneously in two selected blocks. Four sets of corresponding sense amplifiers are activated and 4096 bits are accessed simultaneously. The fifth array of sense amplifiers remains inactive. For example, if the even numbered blocks are selected, a word line in blocks 0 and 2 will be activated along with the three inner arrays of sense amplifiers and the outer arrays of sense amplifiers associated with block 0. The other outer array of sense amplifiers associated with the unselected outer block, in this example block 3, remains inactive.

Fig. 8 shows the technique for perfectly balancing the folded bit lines. The first and the last (fourth) section select transistors are turned OFF and the first and the last (eighth) segment select transistors are turned ON in the unselected blocks to provide the minimum load required for perfectly balancing the shorter folded bit-line pairs associated with the inner multiplexed sense amplifiers. In the above example this corresponds to the section and segment select transistors in blocks 1 and 3 that are the closest to the sense amplifiers. Dummy segments, with 64 cells each, are provided on the outer nonmultiplexed sense amplifiers to balance corresponding shorter folded bit-line pairs in the outer blocks.

Fig. 5 also shows the row redundancy implementation in this architecture. The redundant cells are placed near the sense amplifiers such that they do not need any segment or section decoding. As a result, two rows of cells with cells on alternate bit lines are needed to replace one normal row of the cross-point array. A pair of redundant rows can replace any normal row within the same block. The redundancy scheme is designed to replace up to four normal rows. The column redundancy is implemented by providing two redundant columns. A column is formed by a pair of bit lines and all the associated circuits.

B. Design and Layout

The overall emphasis has been on a conservative design and layout to demonstrate the viability of the unconventional TTC and the DEAF bit-line scheme. A $V_{cc}/2$ sensing scheme with conservative timing is used to sense a very small signal. A conventional CMOS sense amplifier is used. The word line, segment select, and section select timing waveforms are shown in Fig. 9. This timing sequence was carefully designed to minimize the differential noise on the bit lines. The section select transistors are turned OFF after the segment select transistors are turned ON so that the noise generated by the segment select lines is in common mode for the sense amplifiers. The noise from the section select lines is always in common mode for both the sense amplifiers. Moreover, the balancing segment also provides countercoupling to minimize differential noise components. Thus this timing sequence almost eliminates all the differential noise prior to sensing. A full size reference cell is provided at the sense amplifiers. An on-chip reference voltage generator provides 2.2 V for the reference cell to provide equal margins for sensing a ZERO and a ONE.

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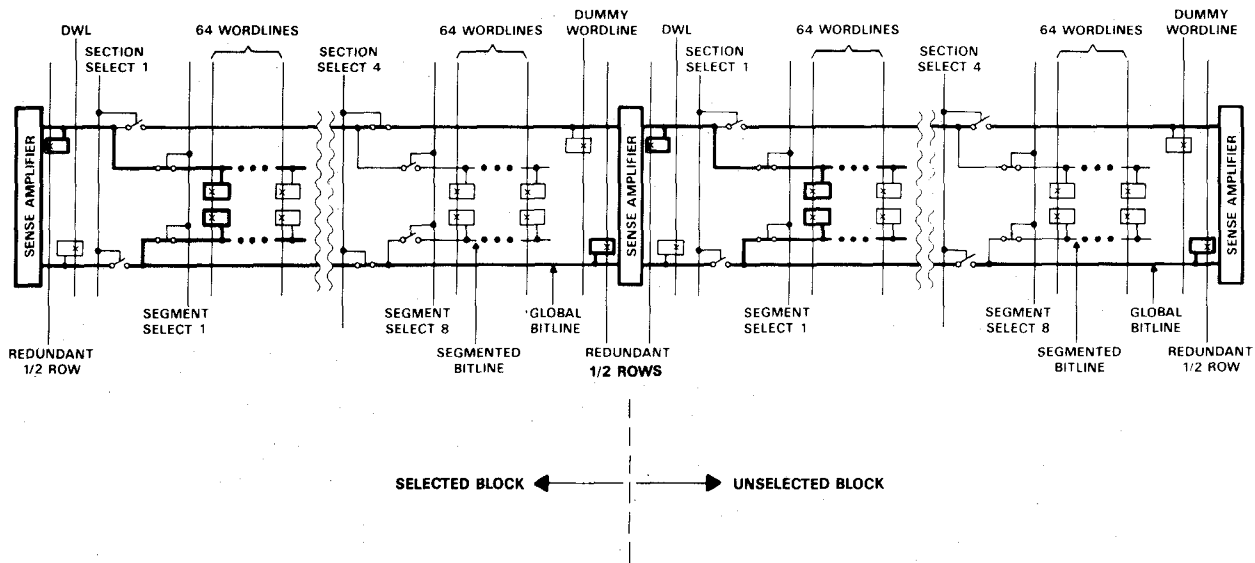

Fig. 8. Technique to perfectly balance the folded bit lines in DEAF architecture.

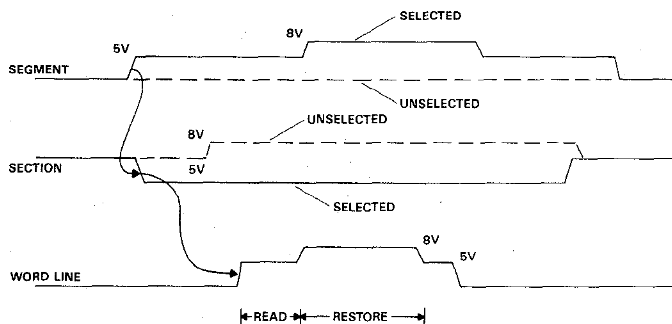

Fig. 9. Word-line, segment-select, and section-select timing details.

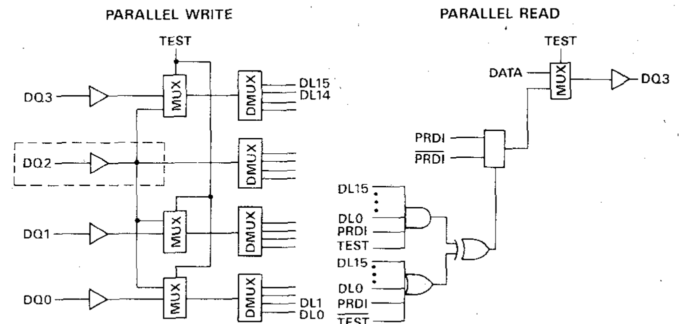

Fig. 10. Test time reduction: 16-bit parallel test.

The device is organized as 1M words × 4 bits. The column decoding circuitry and the data-line drivers are part of the sense-amplifier array. The global bit lines run across the sense amplifiers, however, since they are formed in Metal-2, the increase in bit-line capacitance is not significant. In order to reduce the power dissipation and peak currents, all of the four bits are accessed from the same array of active sense amplifiers instead of one from each of the four arrays of amplifiers. Moreover, the restore operation is staggered among the four active sense-amplifier arrays to further reduce the current transients and the power dissipation.

Various testability modes have also been implemented on this device to allow easier engineering characterization and to reduce the test time requirements. A goal not to exceed the test time required by a 256-kbit DRAM has been achieved by providing a 16-bit parallel test mode. Since four arrays of sense amplifiers are activated simultaneously, and since each of these arrays is designed to address four bits at a time, internally 16 bits are accessible concurrently for parallel test. Fig. 10 shows the functional diagram that achieves parallel READ and WRITE. The data from the input *DQ*2 are fanned out to all the 16 internal data lines during the parallel WRITE. The process is reversed in parallel READ test mode. These data lines are matched with the expected data during parallel READ mode. If all the data lines match the expected data, the expected data appears on output *DQ*3. However, if any one of the data lines does not match the expected data, the complement of the expected data appears on the output *DQ*3.

Fig. 11 shows the chip photomicrograph. Since a 10X stepper was used in the fabrication of this device, its form factor, which is nearly unity, was primarily determined by the field size limitations of the stepper. The chip measures 9.8×10.2 mm^2. Table I summarizes key device and process features.

A symbolic layout system was used to lay out all the peripheral circuits except the sense amplifiers and decoders. Individual circuit layouts were created directly on the graphics system using this symbolic layout system. To further reduce the chip layout time, automatic cell placement and semiautomatic interconnect software systems were used. The use of the graphics system was minimized as a result. The modifications in cell placement and interconnections were simply accomplished by editing corresponding data files on a VAX computer systems.

No attempts were made to optimize the peripheral circuit layouts. Also, the area utilization by decoder and sense-amplifier circuits is not efficient due to very tight layout pitches. As a result, memory array area utilization is

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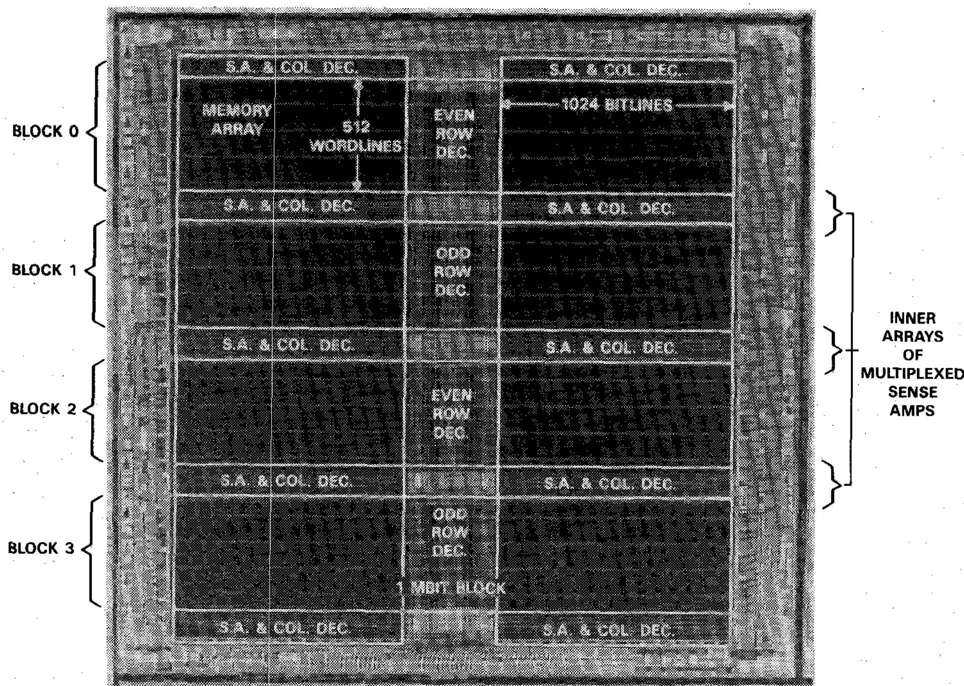

Fig. 11. A 4-Mbit chip photomicrograph.

TABLE I
SUMMARY OF PROCESS AND DEVICE FEATURES

ORGANIZATION	1,048,576 WORDS × 4 BITS DOUBLE-ENDED ADAPTIVE FOLDED BITLINE ARCHITECTURE FULL TTL COMPATIBILITY		
TECHNOLOGY	1 μm CMOS TWIN-WELL TECHNOLOGY WITH DEEP TRENCHES,LDD, AND DOUBLE LEVEL METALLIZATION		
DESIGN RULES	POLY AND DIFFUSION PITCH FIRST METAL PITCH SECOND METAL PITCH EFFECTIVE GATE LENGTH	2.0 μm 2.5 μm 3.5 μm 1.0 μm	
CELL SIZE	2.6 μm × 3.4 μm (8.9 μm²)		
DIE SIZE	9.8 mm × 10.2 mm		
ACCESS TIMES	RAS ACCESS TIME SCD MODE ACCESS TIME PAGE MODE ACCESS TIME	= 150 ns = 40 ns = 40 ns	5V, 25°C
SUPPLY CURRENT (V_{CC} = +5V)	ACTIVE STANDBY	75 mA 2 mA	25°C
REDUNDANCY	LASER REDUNDANCY WITH 4 ROWS AND 2 COLUMNS		

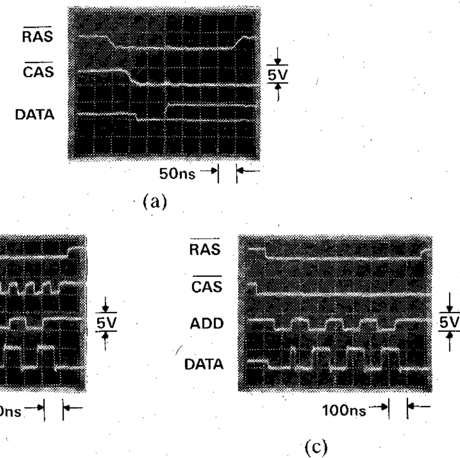

Fig. 12. Device performance. (a) Address access time. (b) Page-mode access time. (c) SCD mode access time.

less than 40 percent, however, the memory array and the chip are the smallest reported to date in the 1.0-μm technology.

C. Device Performance

Fig. 12 shows the access time of the device in various modes of operation. The oscilloscope waveforms of Fig. 12(a) show a RAS access time of 150 ns. In this experiment, we opted to include both the page and the SCD modes on the same device so that no mask changes are required. This was accomplished by the CAS before RAS detection circuit. When CAS follows RAS, a normal RAS cycle is initiated. This allows the page-mode operation. The access time in page mode is shown in Fig. 12(b). When CAS precedes RAS, the SCD mode is activated. Fig. 12(c) shows the waveforms and access time in the SCD mode. A 40-ns access time has been achieved in both the page and the SCD modes.

The circuit and timing technique for reduction in power dissipation and peak currents have resulted in 375 mW of average power dissipation with 175 mA of maximum peak current at 350-ns cycle time. As mentioned before, the chip floor plan for memory array and peripheral circuits was primarily determined by the field size constraints of a 10X stepper. Further optimizations in circuit design/layout, chip floor plan, and process technology will result in an even higher performance 4-Mbit DRAM.

IV. CONCLUSIONS

A truly three-dimensional VLSI 4-Mbit DRAM with capacitor, pass transistor, and a contact all integrated inside a trench has been successfully demonstrated. We

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believe that this cell, the array architecture, and the process technology will result in 16-Mbit and denser DRAM's with further scaling.

Acknowledgment

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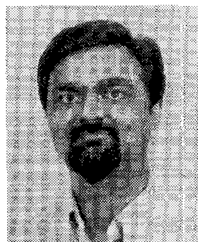

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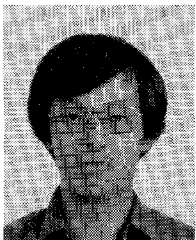
Chu-Ping Wang (M'85), photograph and biography not available at time of publication.

Richard H. Womack (M'80) was born in Waco, TX, on August 6, 1956. He received the B.S. degree in physics and the B.S. degree in electrical engineering from Texas A&M University, College Station, in 1978. He received the M.S. degree in electrical engineering from Southern Methodist University, Dallas, TX, in 1983.

He joined Texas Instruments Incorporated, Dallas, TX, in 1978 as a Design Engineer engaged in the design of 12L and STL logic circuits. From 1979 to 1983 he designed several advanced Schottky TTL devices. In 1983 he moved to advanced memory design and was a co-designer of 4-Mbit DRAM. He is now with Krysalis Corporation in Albuquerque, NM.

James D. Gallia (S'71–M'74) was born in Dallas, TX, in March 1950. He received the B.S. and M.S. degrees in electrical engineering from Southern Methodist University, Dallas, TX, in 1973 and 1974, respectively. His thesis work focused on the design and characterization of an optical communication link using semiconductor lasers.

In 1975 he joined an integrated circuit design group at Texas Instruments Incorporated, Dallas, TX, where he designed memory and logic chips in Schottky TTL, I^2L, ECL, and CMOS. Since 1981 he has been a member of the VLSI Design Laboratory at Texas Instruments, where he has contributed to the circuit design simulation and characterization of the VHSIC 8K×9 SRAM and the 4MEG DRAM. In 1986, he was elected a Senior Member of the Technical Staff at Texas Instruments.



Hisashi Shichijo (S'78–M'80) was born in Kagawa, Japan, on October 24, 1952. He received the B.E. degree from the University of Tokyo, Tokyo, Japan, in 1976, and the M.S. and Ph.D. degrees in electrical engineering from the University of Illinois, Urbana, in 1978 and 1980, respectively. From 1976 to 1979 he worked on the fabrication and analysis of III–V quantum well lasers and InGaAsP lasers in the visible spectrum. His Ph.D. work involved theoretical studies of high-field transport in III–V semiconductor heterojunctions including the development of new Monte Carlo method and the analysis of real space transfer in heterostructures.

In 1980, he joined Texas Instruments Incorporated as a Member of Technical Staff at the Central Research Labs, Dallas, TX. He was involved in the processing of submicrometer MOS devices, the studies of device scaling and device physics, and the process development for VHSIC 1.25-μm MOS SRAM technology including the silicide and LDD technologies. From 1982 to 1985, as a member of the design team to design the first 4-Mbit DRAM at Texas Instruments, he was responsible for the device and cell design. Presently, he is a Senior Member of the Technical Staff, and is working on new GaAs device concepts and process development using GaAs-on-silicon materials and HEMT structures.

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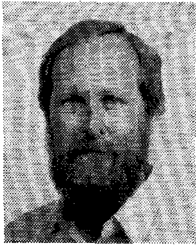
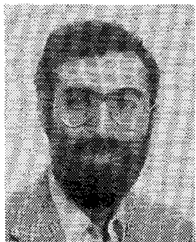


Harvey E. Davis was born in the Texas Panhandle in 1948 in the small town of Lockney. He graduated from high school and attended Frank Phillips College in Borger, TX, graduating with the Associate in Arts degree.

He joined the United States Army Security Agency in 1970, attaining the rank of SP5. Leaving the Army in 1973, he joined Texas Instruments' Circuit Design and Development group working in the Bipolar Memory Design branch as part of a team seeing many bipolar designs to completion. He is now a Member of the Technical Staff in the VLSI Design Laboratory, Dallas, TX, assigned to the Memory Design Branch since its inception. Currently, he is working on the 4-Mbit DRAM project.



Mostafa Elahy (S'84–M'84) was born in Islamabad, Iran, in 1955. He received the B.S. degree in physics from the University of California at Los Angeles in 1978 and the Ph.D. degree in solid state physics from the Massachusetts Institute of Technology, Cambridge, in 1983. His doctoral research studied and modeled the two-dimensional phase transition in magnetic graphite intercalation compounds.

He joined Texas Instruments Incorporated, Dallas, TX, in 1983. As a Member of the Memory Concept Branch of the VLSI Design Lab in Corporate Research Development and Engineering, he has been investigating the limitations of the three-dimensional integration with trench and silicon on insulator structures. He is the author of more than 20 articles in scientific and technical journals and conferences.

Dr. Elahy is a member of the American Physical Society.

Sanjay K. Banerjee (S'80–M'83) received the B.Tech. degree from the Indian Institute of Technology, Bombay, and the M.S. and Ph.D. degrees from the University of Illinois, Urbana, in 1979, 1981, and 1983, respectively, all in electrical engineering.

He is a Member of Technical Staff at Texas Instruments Incorporated, Dallas, TX, and works in the 4-Mbit program. His research interests are ion implantation and annealing, silicon-on-insulator and polysilicon devices, and three-dimensional IC technology.

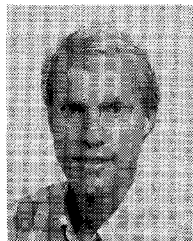
Gordon P. Pollack was born in Chicago, IL, on April 2, 1942. He received the B.S. degree in chemistry from Kalamazoo College, Kalamazoo, MI, in 1964 and the M.S. and Ph.D. degrees in physical chemistry from Wayne State University, Detroit, MI, in 1966 and 1970, respectively.

Since joining Texas Instruments in 1969, he has been involved in a wide range of research activities relating to semiconductor device technology. These include work on doped oxide diffusion sources, solid state sensors, e-beam device fabrication, polysilicon MOSFET's, and process development for NMOS and CMOS memory products. Before assuming his present responsibilities, he was Project Manager for the 4-Mbit DRAM process development activity. He is presently Manager of the Advanced Device Technologies branch of the Semiconductor Process Laboratory, Dallas, TX.

William F. Richardson (M'80) was born in Lincoln, NE, in 1940. He received the B.S. degree in chemistry from New Mexico State University, Las Cruces, in 1965, the M.A. degree in chemistry and the M.S. degree in electrical engineering from the University of Missouri, Columbia, in 1975, and the Ph.D. degree in electrical engineering from the University of Missouri in 1981.

In 1978 he joined the Texas Instruments Technical Staff in Dallas, TX, to work on device and circuit development for nonvolatile semiconductor memories. He is currently doing device and process development of advanced dynamic RAM applications.

Dr. Richardson is a member of the American Chemical Society.



D. Mark Bordelon (S'82–M'83) received the B.S. degree in material science from the University of Florida, Gainesville, in 1981 and the M.S. degree in material science from the University of Texas, Austin, in 1983. His masters research involved the study of the interaction of picosecond IR radiation with crystalline silicon.

He joined Texas Instruments, Dallas, TX, in 1983 and is currently a Member of the Technical Staff in the Semiconductor Process Laboratory. His present work involves process development and characterization of devices for advanced DRAM applications.

Satwinder D. S. Malhi (S'78–M'78) was born in Jullundur, Punjab, India, on March 26, 1955. He received the B.E. degree in electronics and electrical communications from Punjab University in 1976, and the M.A.Sc. and Ph.D. degrees, both in electrical engineering, from the University of Toronto, Toronto, Ont., Canada, in 1979 and 1981, respectively.

He was a Teaching and Research Assistant at the University of Toronto from 1979 to 1981. During his graduate study he worked in cooperation with Linear Technology Incorporated, Burlington, Ont., Canada. He developed a novel cost-effective bipolar-compatible low-voltage JFET structure, which formed the basis of a micropower JFET/bipolar technology. He also designed the micropower Operational Amplifier LC700, suitable for a single 1.3-V battery operation, which featured several novel building blocks made possible with the low-voltage JFET's. On the basis of a part of that work, he was the winner of the IEEE International Electron Devices Meeting Best Student Paper Award in 1980. He joined Texas Instruments Incorporated, Dallas, TX, in September 1981. From 1981 to 1982 he was involved in exploratory research in SOI device modeling and process development. Since then his primary interest has been device technology development for three-dimensional integration, using SOI and trench technologies. In 1983 he was a member of the team that demonstrated the first three-dimensional VLSIC-a 64K stacked CMOS static RAM.

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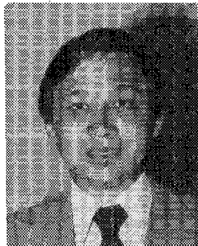
Charles J. Pilch, Jr. received the B.S. degree in electrical engineering from Clarkson College in 1982, where he also finished his requirements for the B.S. degree in physics from the New York State University at Oneonta.

He joined Texas Instruments, Houston, TX, in 1983 and is working as a Design Engineer in the Advanced Development Group at the present time.



Bao Tran graduated with the B.S. degree from Cal Poly University in Pomona, CA, in 1980.

He started at Texas Instruments, Houston, Texas, as a Design Engineer for the DRAM MOS Memory Group. Since then he has been involved in 64K NMOS DRAM and 4Meg CMOS DRAM.

Pallab K. Chatterjee (S'74–M'76–SM'84–F'86) received the B.Tech. degree in electronics and communication engineering from the Indian Institute of Technology, Kharagpur, India, in 1972, and the M.S.E.E. and Ph.D. degrees from the University of Illinois, Urbana/Champaign, in 1974 and 1976, respectively. He was awarded the President of India Gold Medal for curricular excellence and B.C. Roy Memorial Gold Medal for extracurricular excellence at the Indian Institute of Technology in 1972.

He joined Texas Instruments, Dallas, TX, in 1976, where he worked on CCD memories and storage cells for DRAM's, modeling and fabrication of submicrometer MOS devices and device scaling. He has been responsible for development of VLSI static and dynamic memory and for development of device structures now used in VLSI CMOS. He was elected a Texas Instruments Senior Fellow in 1985 and is currently Director of the Semiconductor Process and Design Center of Texas Instruments. His responsibilities include developing VLSI process and design technology for Texas Instruments. He has published more than 100 articles in international scientific and technical journals and conferences, and has been awarded over ten U.S. patents.

Dr. Chatterjee is a member of the American Physical Society. He won the IEEE "Keys to the Future" award in 1984.

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