

A 0.25 μm SiGe BiCMOS Technology including Integrated RF Passive Components optimised for Low Power Applications

S. Van Huynenbroeck, S. Jenei, G. Carchon, A. Piontek, F. Vleugels and S. Decoutere
IMEC vzw, Kapeldreef 75, B-3001 Leuven, Belgium
Stefaan.VanHuynenbroeck@imec.be

Abstract

A high performance SiGe HBT has been integrated in a 0.25 μm BiCMOS technology optimised for low power applications. A deep trench module is implemented offering a reduction of the perimeter collector-substrate capacitance with a factor of 5 while at the same time maintaining the wafer surface topography. The in-situ boron doped SiGe profile has been optimised towards a reduction of the base-emitter capacitance. High-quality, low-cost passive components like varactors, high-Q post-processed inductors and highly linear nondispersive MIM capacitors are offered, broadening the low power capabilities of this technology.

1. Introduction

For applications in the 2-5 GHz range, state of the art HBT devices usually have sufficient high peak F_t and F_{max} . However, the transistors in the RF circuits are biased at lower current densities, such that for the given frequency range, higher gain and hence higher F_t needs to be realized at lower current densities, without degradation of the peak F_t . High Q passives are needed to reach the stringent phase noise specs for the VCO and for an improved LNA performance.

2. Deep Trench Module

The IMEC 0.25 μm CMOS process uses poly encapsulated LOCOS (PELOX) as lateral isolation. The deep trench module is introduced between active area formation and pregate oxidation. First, a bi-layer of nitride and oxide is deposited for the two following reasons: it acts as a hard mask during the deep trench etch and serves as a local oxidation mask during the trench filling. Then the trench reticle is printed, the pattern is transferred into the hard mask and the field oxide by a dry etch step, and the deep trench is etched into the silicon substrate after stripping the photo resist. The trench is lined with a thin screen oxide and implanted at the bottom by a blanket 0-degree tilt implantation. Then it is refilled with a liner oxidation followed by a thick poly silicon deposition. The wafer surface is etched back to clear the excess poly silicon and

remove the top oxide of the hard mask. The poly silicon filler is over etched down into the trench with a recessed level about at half the thickness of the field oxide. Finally, the filler is oxidized to cap it and the masking nitride layer is removed restoring an almost planar surface in the trench region (Figure 1). Low stress generation is achieved by realizing a good bottom rounding and by a proper choice of the growth conditions and temperature for the liner oxide and capping oxide.

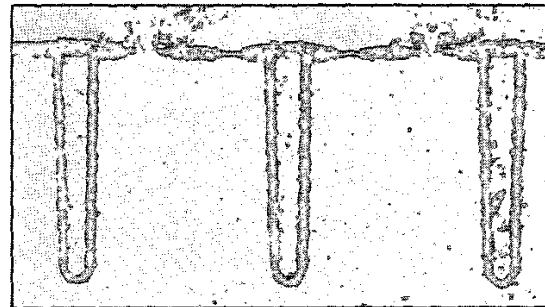


Figure 1. SEM cross section of the deep trench after complete BiCMOS processing.

The isolation properties of the deep trench module have been checked on arrays of 10,000 devices with 1.0 μm wide shared trenches. The collector-to-collector leakage current does not exceed a current density of 5 $\text{pA}/\mu\text{m}^2$. The voltage breakdown is reached at 15V. The breakdown current is given by the turn-on of the parasitic nMOS transistor at a threshold voltage that is controlled by the trench channel stop implantation.

The area and perimeter components of the collector substrate capacitance have been extracted by measuring the capacitance values on HBT devices having different lengths. The area component follows the normal depletion capacitance behaviour as a function of the reverse bias voltage. The perimeter capacitance stays constant as a function of the applied reverse bias, this due to the presence of the deep trenches around the HBT device (Figure 2). The perimeter component has been reduced from 1.0 $\text{fF}/\mu\text{m}$ without deep trench to 0.17 $\text{fF}/\mu\text{m}$ with the deep trench (table 1).

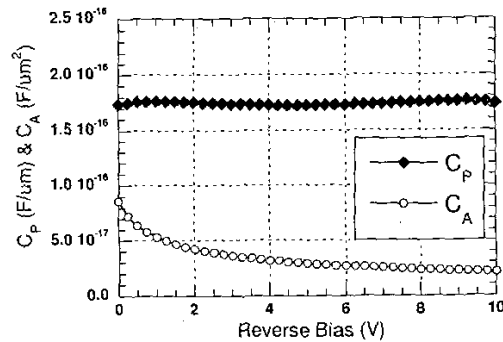


Figure 2. C_p and C_a collector-substrate capacitance as a function of the bias for NPN devices surrounded by a deep trench.

3. NPN devices

The SiGe HBT devices described in this paper are implemented in a 0.25 μm core CMOS process having the same junction RTA temperature as the reference 0.35 μm BiCMOS technology [1]. A double poly self-aligned architecture using an L-shaped inside spacer module is realised. The base epitaxial layer is grown selectively. An optimised Ge profile is introduced in the 0.25 μm BiCMOS process, having a graded profile between a low Ge plateau at the emitter side and a high Ge plateau at the collector side (Figure 3). This results in an additional degree of freedom to tune the current gain, by tuning the Ge % in the low Ge plateau, while still having a graded profile with the associated boost in early voltage and reduction of base transit time. The flat high Ge plateau at the collector side accommodates the extension of the base/collector depletion region, resulting in a more pronounced grading in the neutral base itself. The boron profile is adapted, with a higher boron concentration in the neutral base (boron spike) while the concentration in the Si cap layer is lowered. The intention is to keep the same pinched base sheet resistance, but to obtain a reduced perimeter C_{je} component.

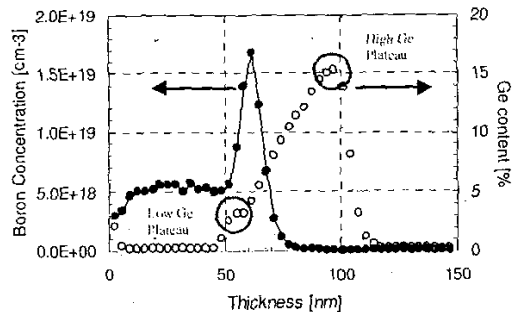


Figure 3. Boron and Ge as-grown SIMS profiles for the 0.25 μm BiCMOS process.

The reduction of the various capacitance values is summarized in table 1. Besides the already discussed reduction of C_{je} and C_{jc} , also the base-collector capacitance C_{jb} is lower due to the more aggressive layout rules used in the 0.25 μm BiCMOS technology.

	0.35 μm	0.25 μm
C_{je}	2.8	2.2
C_{jb}	1.65	1.2
$C_{jc} - \text{perim}$	1.0	0.17

Table 1. NPN capacitance values of the 0.35 μm and 0.25 μm BiCMOS technology, measured at 0V [fF/ μm]

The current gain of the standard NPN device is around 150, the early voltage exceeds 50V and the BV_{ce0} is 3.55V. Additionally, a NPN device without selectively implanted collector doping is available. This device reaches a BV_{ce0} value of 5.5V. The bipolar yield has been assessed by the measurement of arrays of 10,000 parallel-connected transistors (Figure 4).

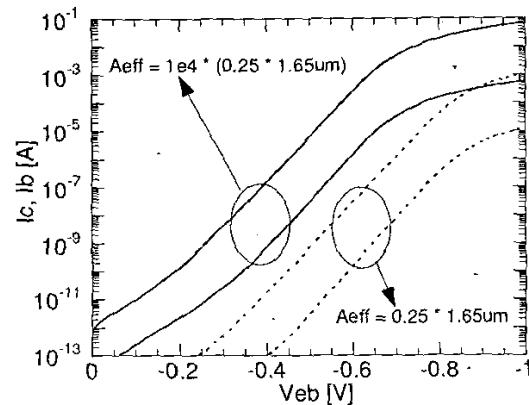


Figure 4. Gummel plot, single device and yield array.

The bipolar devices reach an $F_T \cdot BV_{ce0}$ product of 200, a state of the art value for this generation of HBT devices. The main improvement with respect to the low performance capabilities of this optimized 0.25 μm BiCMOS technology is illustrated in the F_T and F_{max} versus I_c curves (Figure 5). Results are benchmarked against the data of the previous generation. Due to the reduced capacitance values, the collector current needed to obtain for instance a 40 GHz F_T value is reduced with 40 %, this for similar BV_{ce0} range. The F_{max} value at this current is significantly increased because of the reduction of the collector-substrate perimeter capacitance by the introduction of the deep trench module.

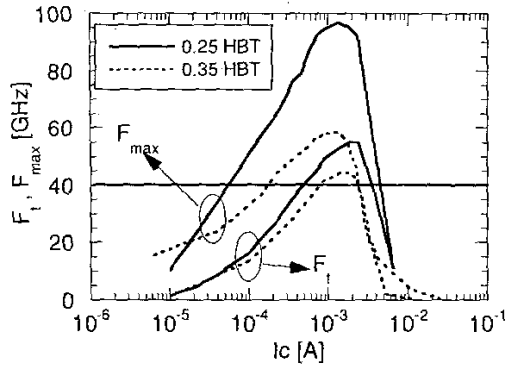


Figure 5. F_t & F_{max} as a function of the collector current for the $0.35\mu\text{m}$ and $0.25\mu\text{m}$ BiCMOS technology.

4. Varactors

By the use of the deep trench module and a proper selection of the doping profile of the n-type region, an improvement of both the tuning range and the Q factor of the MOS accumulation-depletion varactors is obtained. Standard stripe geometry MOS varactor structures are making use of the variable n-well to poly capacitance. The optimized structure presented here however, employs the bipolar collector n-type epitaxial region. This epitaxial layer has a lower doping level compared to an n-well region, allowing a reduction of the depletion capacitance and consequently an increase of the tuning range. In addition, the application of the deep trench module provides better isolation from the p-substrate, hereby reducing the parasitic capacitance with 10 to 20 % and allowing an improvement in the Q factor of around 10% (see Figure 6). While the reference varactor, having a 1 pF capacitance value, has a minimum Q factor of 22.5, the optimized varactor obtains a minimum Q factor equal to 25. The tuning range reaches a value of 2.5.

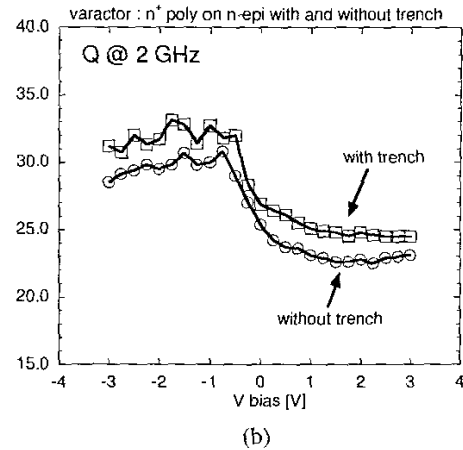
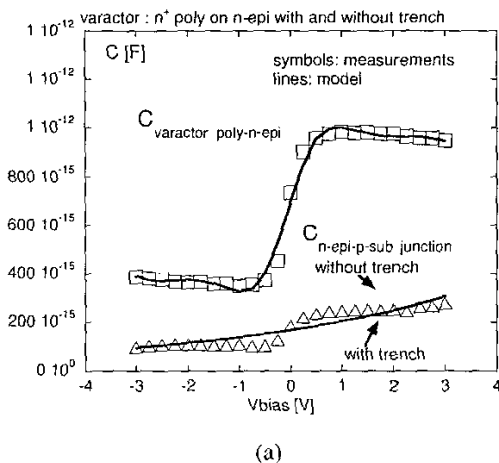


Figure 6. (a) Extracted and simulated $C(V)$ curves of the reference varactor on n-epi without a deep trench and the optimized varactor with the deep trench (b) extracted Q factors at 2 GHz on the same devices.

5. Inductors

For the moderate and high GHz frequency operating ranges (2-10 GHz), a target for the present RF applications, requested inductance values are in the range of 1 to 5 nH. These values can be realized on-chip consuming a realistic amount of the chip area. However, the inductors should also reach satisfactory Q factors at these operating frequencies. This is difficult to obtain in conventional Si technologies since both the available conductors and the substrate is lossy.

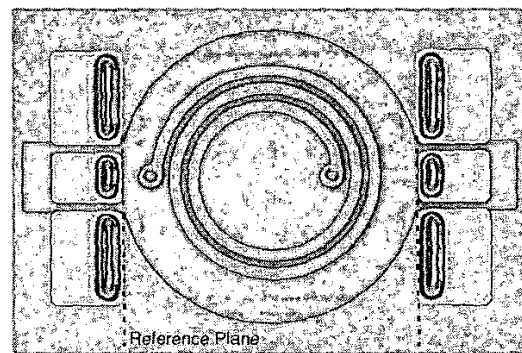


Figure 7. Top view of a post-processed inductor: the inductor is realized using $10\mu\text{m}$ thick Cu, the underpass is realized on the 5th BEOL metal. A patterned poly silicon ground shield is present underneath the inductor.

An attractive solution is to make the inductors above passivation using thin-film wafer-level packaging techniques. Inductors can then be realized using thick Cu (5 to $10\mu\text{m}$) and thick ($5\mu\text{m}$ to $16\mu\text{m}$) low-k dielectrics (BCB), hereby resulting in high-Q cost-effective solutions for on-chip inductors [2]. They allow us to obtain the difficult specifications on low power and low

noise for the RF circuit building blocks [3]. A picture of a post-processed inductor, on top of a 5 level of metal BEOL is given in Figure 7.

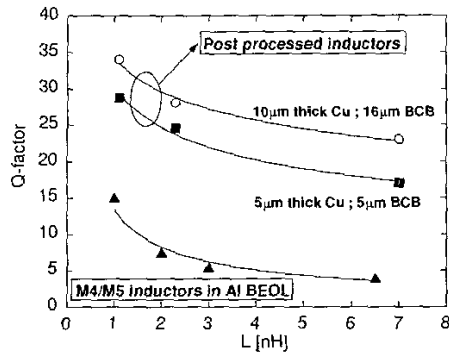


Figure 8. Q factors for the different types of inductors.

Post-processed inductors exhibit higher Q factors than inductors embedded in the conventional BEOL. In Figure 8 we have compared Q factors of the BEOL inductors and the post-processed ones for the same inductance value. Post-processed inductors perform better as the spiral metal traces are formed in a thick Cu layer having a considerably lower sheet resistance and thus resulting in lower series losses. In addition, capacitive coupling to the lossy Si is reduced since the inductor is spaced further away from it.

6. MIM capacitor

A low complexity planar MIM capacitor module in the Al BEOL is developed that can be introduced between different levels of metal, depending on the routing strategy of the particular RF circuit. This MIM module makes use of commonly available multilevel metalization and requests only one additional lithography mask. The MIM module meets strict analog specifications on voltage linearity and matching (slope of the Pelgrom plot of only 0.3 % μm), while maintaining its RF capability.

Different combinations of PECVD oxide and nitride have been tested for the MIM capacitor dielectric, ranging from pure nitride, over NO, ON and ONO combinations to pure oxide. In all cases, the layer thicknesses have been chosen in order to obtain an equivalent oxide thickness of 30nm, which allows us to perform the study under equal conditions of capacitance per unit area. In Figure 9, the voltage linearity curves are shown for the different dielectrics. The ONO balances between the pure oxide and nitride voltage linearity, and cancels out largely the quadratic component of the voltage linearity, which had opposite signs for pure oxide and pure nitride. It can also be seen that combinations of ON and NO obtain for respectively negative and positive bias similar voltage linearity as the ONO combination, but deviate for the opposite sign of the bias.

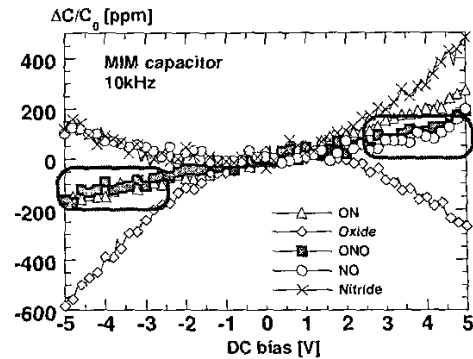


Figure 9. MIM capacitor voltage linearity for different PECVD dielectrics (ONO case: $V_{cl} = 25$ ppm/V, $V_{co} = -1$ ppm/V²).

Besides the excellent voltage linearity, the use of an ONO dielectric stack also suppresses significantly the tunnel current at moderate dc bias, caused by the large amount of traps present in a PECVD nitride layer. A MIM capacitor with ONO dielectric can hereby compete with a capacitor device having a pure oxide dielectric layer. Furthermore, it is proven that this MIM capacitor module with ONO dielectric does not suffer from frequency dependent voltage linearity [4].

7. Conclusions

A 0.25 μm SiGe BiCMOS technology optimised for low power applications has been presented. The reduction of the capacitances, by a proper design of the base profile and by the implementation of a deep trench module, moves the operation current for the same speed performance to almost half of the original value. The capabilities of this technology with respect to low power applications is further enhanced by the availability of high Q varactors and post-processed inductors and by the presence of a highly linear nondispersive MIM capacitor. The authors acknowledge the IWT and AMIS for partially supporting this work in the frame of the MEDEA program ASGBT.

References

- [1] S. Decoutere, F. Vleugels, R. Kuhn, R. Loo, M. Caymax, S. Jenei, J. Croon, S. Van Huylenbroeck, M. Da Rold, E. Rosseel, P. Chevalier and P. Coppens, "A 0.35 μm SiGe BiCMOS Process Featuring a 80 GHz Fmax HBT and integrated High-Q RF Passive Components", BCTM 2000, pp 106-109, 2000
- [2] G. Carchon, S. Jenei, L. Carbonell, M. Van Hove, S. Decoutere, W. De Raedt, K. Maex, E. Beyne, "High-Q RF inductors on standard silicon realized using wafer-level packaging techniques", accepted for the MTTT 2003
- [3] D. Linten, S. Jenei, G. Carchon, P. Wambacq, C. Soens, S. Decoutere, S. Donnay, and W. De Raedt, "Influence of Back-end architectures on the performance of RF CMOS VCOs", SSMSD 2003, pp 150-155, 2003
- [4] S. Van Huylenbroeck, S. Decoutere, R. Venegas, S. Jenei and G. Winderickx, "Investigation of PECVD Dielectrics for Nondispersive Metal-Insulator-Metal Capacitors", IEEE Electron Device Letters, Vol. 23, No 4, pp 191-193, 2002