Trench Transistor DRAM Cell

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Abstract—**A new one-transistor DRAM cell with both the transistor and the capacitor fabricated on the trench sidewalls is described. With the signal stored on the polysilicon node surrounded by oxide, the cell is expected to have a high alpha particle immunity. The cell occupies only 9 μm^2 using 1-μm design rules. This cell size is sufficiently small to enable a 4-Mbit DRAM of reasonable chip size with these design rules, and possesses further scalability for 16-Mbit DRAM's.**

I. Introduction

THE development of future DRAM's beyond 4-Mbit capacity must rely on an innovative DRAM cell which circumvents the problems of cell isolation and alpha-particle-induced soft errors while maintaining sufficient cell capacitance for adequate signal sensing. The Corrugated Capacitor Cell (CCC) [1] uses an etched-moat capacitor formed into a silicon substrate in order to provide an increased cell capacitance for a given silicon surface area. Although it is adequate for 1-Mbit DRAM's, the cell suffers from cell to cell leakage current upon further scaling [2], [3]. The idea of merging the trench capacitor with isolation [4], [5] avoids this problem of punchthrough between adjacent cells. However, this type of cell suffers from the leakage due to a parasitic transistor formed on the trench sidewall. Furthermore, the advantage of these cells in terms of alpha particle immunity is not clear. Another version of isolation-merged cell [6] stores the signal charge in the polysilicon node isolated by oxide for improved alpha particle immunity, but has drawbacks of larger cell size and trench sidewall leakage.

In this letter, a new one-transistor DRAM cell with both the transistor and the capacitor fabricated on the sidewalls of an 8-μm-deep trench is described. The transistor and the capacitor are connected by a novel lateral-buried contact scheme, which enables the signal charge to be stored on the polysilicon node surrounded by oxide. The experimental demonstration of the cell functionality and some electrical characteristics are discussed.

II. Cell Structure

The schematic cross section and the SEM micrograph of the new Trench Transistor Cell (TTC) are shown in Fig. 1. The trench dimensions are 1.3 × 1.5-μm, and 8-μm deep. The diffused n^+ region forms the bit line, which serves as the drain of the vertical n-channel pass transistor around the top lip of the trench. The width of the transistor is determined by the perimeter of the trench. The nominal gate length is 1.5 μm along the sidewalls of the trench. The source of the transistor is connected to the n^+ polysilicon capacitor storage node by a novel lateral-buried contact. This contact is fabricated by an oxide undercut etch and refill with polysilicon [7]. The other electrode of the capacitor is formed by the heavily doped p^+ substrate in order to avoid the depletion which would otherwise reduce the effective storage capacitance. This structure utilizes a thin epitaxial layer on a heavily boron doped substrate which is compatible with a latchup-free CMOS process [8]. Except for the small source junction area, the storage node is oxide isolated from the bulk. Therefore a high immunity to alpha-particle induced soft errors is expected.

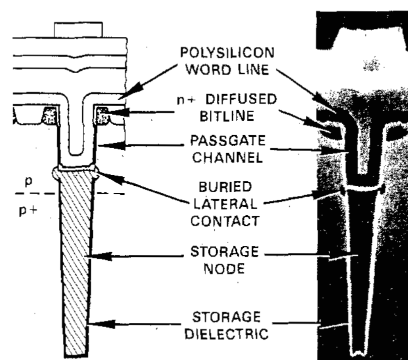

Fig. 1. TTC schematic diagram and SEM cross section.

III. Electrical Results

The electrical performance of the TTC is primarily determined by the behavior of the vertical pass transistor and the storage capacity of the trench capacitor.

Although a 1.5 × 1.3-μm rectangle is patterned to form the trench, some rounding occurs during photolithography and etching, resulting in an oval opening with the trench sidewalls having miscellaneous crystallographic directions. This causes gate oxide thickness variations along the trench sidewalls and a higher interface state density than in the (100) surface. The fast interface state density is also likely to be higher than for planar transistors, because the trenches are formed by reactive ion etching, which results in a damaged crystal surface. Furthermore, the threshold voltage is adjusted by a deep boron

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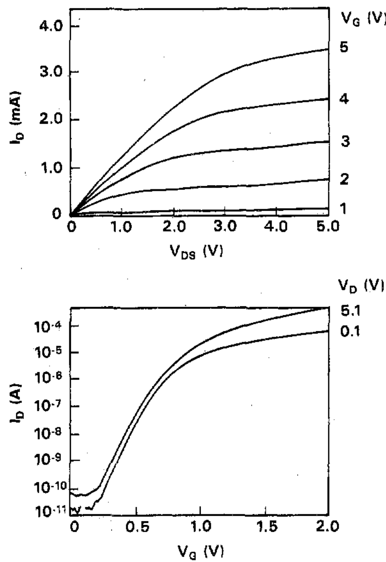

Fig. 2. TTC transistor I–V characteristics; $W = 42$ μm, $L = 1.5$ μm, and tox = 25 nm.

implant which results in a Gaussian profile along the channel, with a peak (1E17 cm^{-3}) near the drain. All these features make the trench transistor different from a conventional planar transistor.

The typical current-voltage characteristics of the trench transistor is shown in Fig. 2. At -2.5 V back-bias, a 42/1.5-μm device has a threshold voltage of 0.74 V and a subthreshold slope of 81 mV/decade. These values agree closely with the results of device simulations using PISCES [9]. The theoretical threshold voltage and subthreshold slope are 0.76 V and 74 mV/decade, respectively, for this transistor. These pass transistors also have adequate drive current to enable fast read/write from the cell and low leakage characteristics for long storage times.

A capacitor in a DRAM cell typically requires at least 20 fF for adequate signal sensing. The measured cell capacitance versus trench depth for a 1.5×1.3-μm trench with the transistor in the upper 2 μm of the trench and a 30-nm capacitor oxide is shown in Fig. 3. The test structure consists of a large number of cells in parallel. Since the capacitor in TTC is formed between the n^+ poly inside the trench and the substrate, any depletion of the trench sidewall would degrade the effective cell capacitance. In order to avoid the excessive depletion of the substrate around the trench, the starting material uses a thin (4–6 μm) epitaxial layer on p^+ substrate, enabling the boron to updiffuse and increase the trench sidewall doping. For the process flow used in the TTC fabrication, the calculated cell capacitance taking into account the depletion effects and the full oxide capacitance are also shown in Fig. 3 for comparison. The cell capacitance can be increased by introducing trench sidewall boron doping in the capacitor region, and by using a nitride or nitride/oxide stack as the storage dielectric.

A test circuit to verify the cell functionality, with a source follower on the bitline, along with the signal waveforms is shown in Fig. 4. By comparing the signals from the TTC and the conventional planar cell connected on the same bit line, the

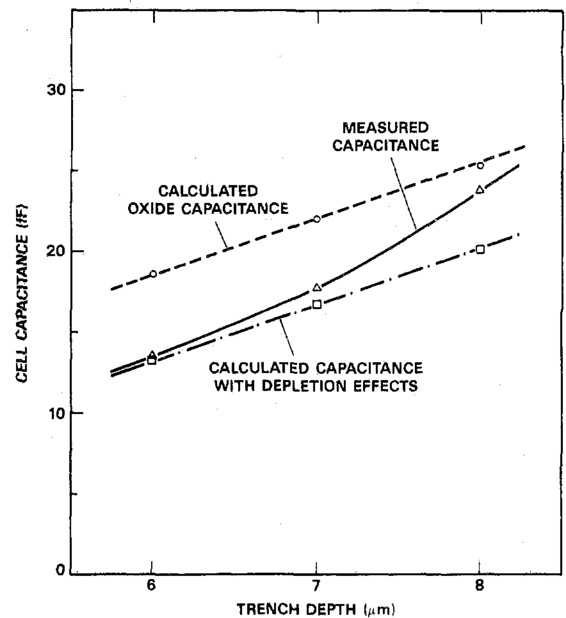

Fig. 3. TTC capacitance versus depth for a storage gate oxide thickness of 30 nm: oxide capacitance; capacitance corrected for depletion effects; and measured capacitance.

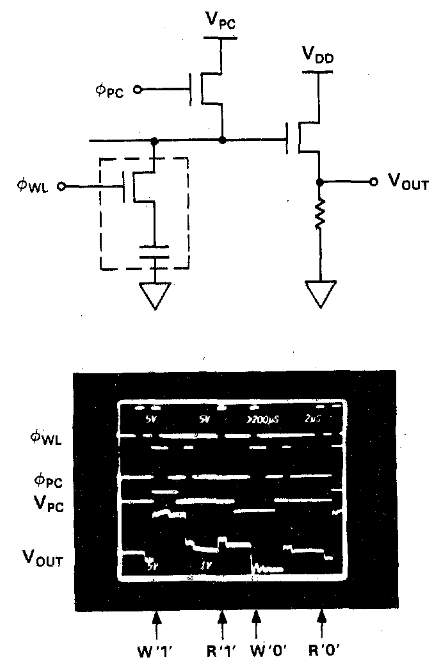

Fig. 4. TTC test circuit and signal waveforms.

cell capacitance of a single TTC with an 8-μm trench and 20-nm capacitor oxide is determined to be 28 fF. Using the same structure, the refresh time of around 0.6 s at room temperature, and 20 ms at 100 C have been measured.

IV. Conclusions

A novel cross-point DRAM cell with both the pass transistor and the storage capacitor in a trench has been demonstrated. It has been shown that the trench transistor is well behaved and sufficient capacitance can be achieved in a trench capacitor.

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This cell is suitable for a 4-Mbit DRAM and has the potential of being scaled down for a 16-Mbit DRAM.

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