A VARIABLE-SIZE SHALLOW TRENCH ISOLATION (STI) TECHNOLOGY WITH DIFFUSED SIDEWALL DOPING FOR SUBMICRON CMOS

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ABSTRACT

This paper presents a Shallow Trench Isolation (STI) technology using RIE, CVD oxide fill, and planarization to realize lithography-limited, submicron device and isolation dimensions. A novel boron diffusion technique is used for nMOSFET field doping, so that the parasitic sidewall inversion (leakage) problem is eliminated. It is shown that both the channel width bias (ΔW) and the narrow channel effect are greatly reduced in the STI technology.The diffused field also allows the boron doping to be self-aligned to the n-well with a single masking step in CMOS. STI is used in conjunction with MINT cell (1) in 16Mb DRAM technology.

INTRODUCTION

It is widely recognized that LOCOS isolations cannot be extended to deep submicron dimensions for density-driven memory applications because of the inherent "bird's beak" and field boron encroachment problems caused by the long thermal oxidation. Another scaling barrier of the LOCOS isolations is the field oxide thinning at submicron isolation widths due to 2-dimensional oxidation effects (2).

Trench isolations have been proposed as possible solutions to CMOS isolation scaling down to submicron dimensions (3,4,5). However, there is a parasitic leakage path in a trench-isolated nMOSFET device due to the inversion of the trench sidewalls which cannot be doped in a standard field implant process (3). Angled field implant has been used to passivate the trench sidewalls (5).

In this work an oxide filled shallow trench isolation technology is presented. The field dopant for the nMOSFET is provided by boron diffusion from p^+ poly or BSG, which readily passivates the trench sidewalls. It is shown that shallow field doping profile can be obtained with a final surface concentration of about mid-$10^{17}cm^{-3}$. No additional field dopant is necessary for pMOSFET due to the higher concentration of n-well and phosphorous pile-up during the brief thermal oxidation. STI is used in conjunction with thin epi for improved latch-up immunity since the p^-/p^+ epi transition is much sharper without the extended thermal oxidation cycle in a LOCOS isolation process

STI PROCESS

The STI process is shown schematically in Fig.1. First, the isolation pattern is defined over nitride/pad oxide, and silicon RIE'ed to a depth of 0.3-0.5 μm. A boron diffusion source, consisting of either in-situ doped p^+ poly or borosilicate glass (BSG), is then deposited (Fig.1b). A lithography step is applied to etch the p^+ poly or BSG film outside the n-channel area (Fig.1c). The same resist can be used to mask the n-well implant so that the boron source is self-aligned to the n-well and a mask is saved. After resist strip, a thermal cycle is carried out between 800°C and 900°C to drive the boron into the bottom and the sidewall of the trench. There is no boron diffusion into the active device area since the nitride film is a diffusion barrier (Fig.1d). The diffusion source is then stripped, followed by a brief thermal oxidation (25-50 nm) to passivate the trench sidewalls. During this oxidation, boron segregates into the oxide and its concentration in silicon is reduced. The trenches are then filled with CVD oxide (Fig.1e). A block resist is then patterned over large isolation area followed by a planarizing resist coat. The CVD oxide and the resist are then etched back and the surface is planarized (Fig.1f).

Fig.2 shows the SEM cross section of STI intersecting with the deep trench in the 16Mb DRAM cell. In this structure, the deep trench (DT) for storage node is formed first, followed by the shallow trench isolation. Fig.3a,b show that the bird's beaks are virtually eliminated with STI, whereas they consume more than half of the 1 μm wide device region in the LOCOS case. Fig.3c,d show that there is about 20% oxide thickness reduction in the middle of a submicron isolation region for LOCOS (with reference to large field area) due to 2-dimensional oxidation effects, while the oxide thickness of STI shows no feature-size dependence.

In the boron diffusion process, although the initial source doping level for either p^+ poly or BSG is in the $1x10^{20}cm^{-3}$ range, a final field doping of mid-$10^{17}cm^{-3}$ can easily be achieved by adjusting the drive-in cycle with the help of the boron segregation effect. Fig.4 shows the simulated boron profiles in the silicon after the drive-in and a brief thermal oxidation (50nm). Two different boron concentrations of the diffusion source ($1x10^{20}cm^{-3}$ and $2x10^{20}cm^{-3}$) are used. After an 850°C, 30 min drive-in, the boron surface concentration is in the $6x10^{18}cm^{-3}$ range. After a 50nm thermal oxide is grown, the boron peak concentration is in the $2x10^{17}cm^{-3}$ range (Fig.4), suitable for a high field threshold voltage without too much diffusion capacitance. It is important to note that by changing the source concentration from $1x10^{20}cm^{-3}$ to $2x10^{20}cm^{-3}$ (2X), the final peak boron concentration changes from $1.7x10^{17}cm^{-3}$ to $4.2x10^{17}cm^{-3}$ (2.5X). Therefore the reduction of the boron concentration by about 3 orders of magnitude (from the diffusion source to the final profile) is not a subtractive process, leading to a reproducible field doping profile. The experimental boron SIMS profiles before and after the p^+ poly strip (by a concentration sensitive etch) are shown in Fig.5. A pulsed C-V profile

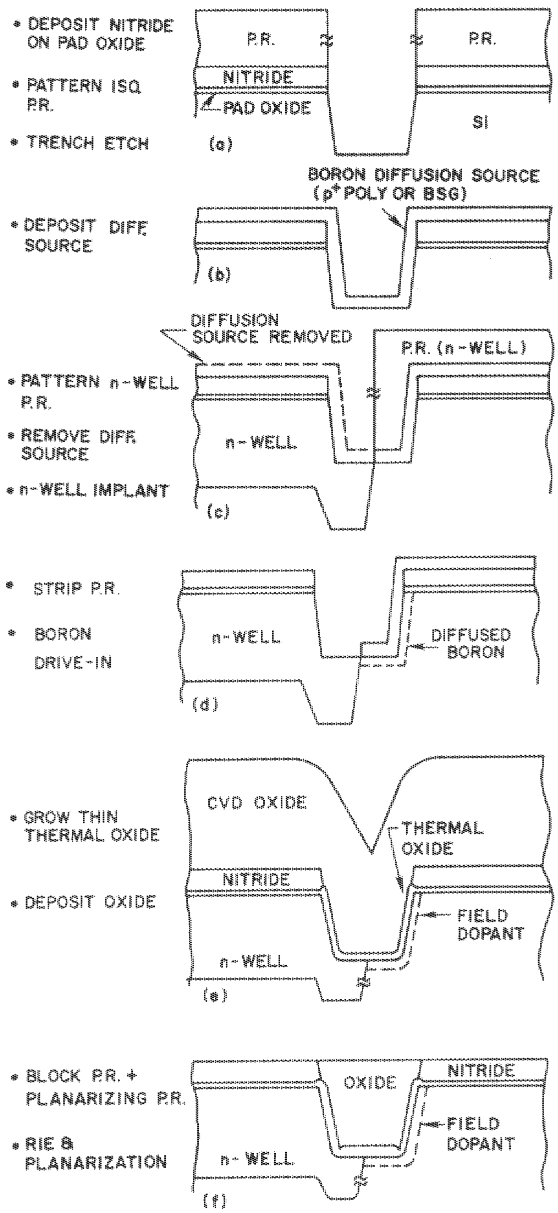

FIG.1 Shallow Trench Isolation process flow

of the final boron doping in the field region is shown in Fig.6. The boron profile is very shallow ($\approx 0.1\ \mu m$) since there is minimal oxidation-enhanced diffusion in the STI process. This is important for the reduction of boron encroachment as well as field-diffusion capacitance.

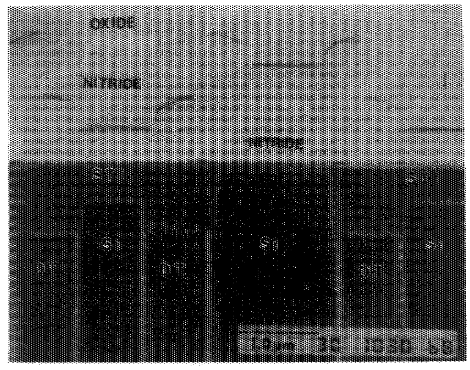

FIG.2 Shallow Trench Isolation (STI) and the poly filled Deep Trench (DT) storage node integration in the MINT (ref.1) DRAM cell

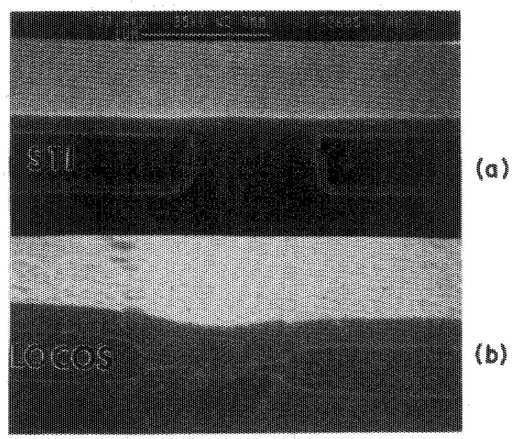

FIG.3 a,b STI versus LOCOS in the narrow active region

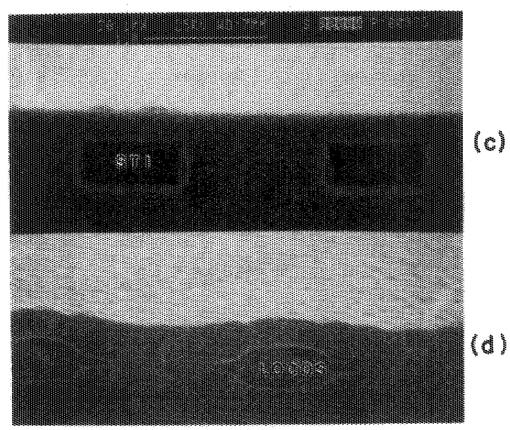

FIG.3 c,d STI versus LOCOS in the narrow isolation region (No oxide thickness reduction for STI)

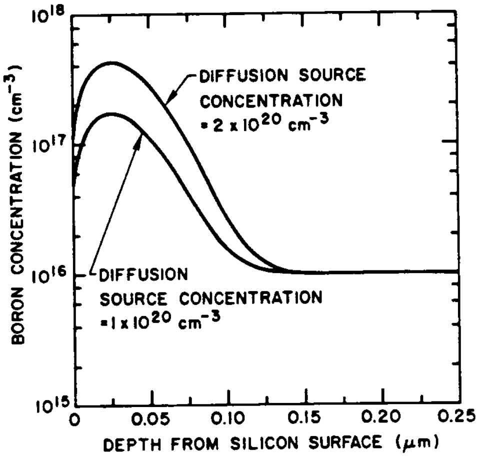

Fig.4 Simulated Boron concentration profiles after drive-in (850°C, 30 min) and 50 nm thermal oxide

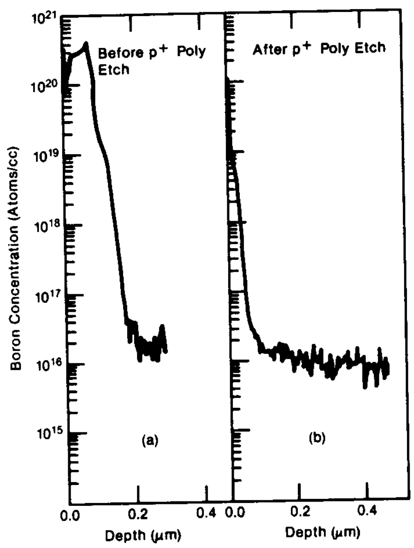

FIG.5 Boron concentration profiles (SIMS) after drive-in (850°C, 30 min), before and after p^+ poly etch

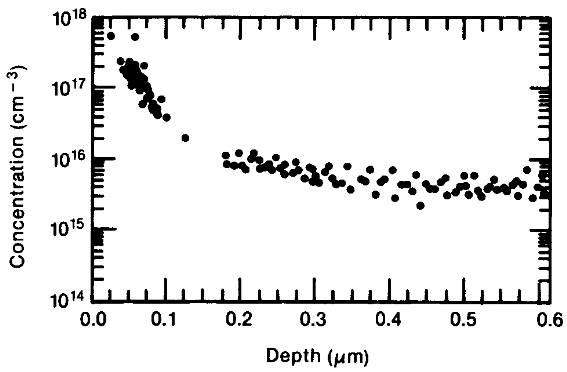

FIG.6 Pulse C-V profile of the final doping concentration of the diffused field

ELECTRICAL CHARACTERISTICS

0.5 μm ground rule CMOS circuits have been fabricated using the shallow trench isolation process. The gate oxide thickness is 12.5 -15.0 nm. Self-aligned $TiSi_2$ is formed over source/drain and salicide or polycide gates are used. Subthreshold characteristics of nMOSFET's with and without sidewall doping are shown in Fig.7. It is clear that doping of the STI sidewall by boron diffusion is necessary to suppress the parasitic sidewall leakage which shows up as a hump in the subthreshold curve. Both the nMOSFET channel width bias (ΔW) and threshold voltage shift (narrow channel effect) are greatly reduced with STI compared with LOCOS (Fig.8) due to the elimination of bird's beak and the shallow field boron profile. For pMOSFET, almost zero narrow channel effect ($\Delta W<0.1\mu$m) is obtained. The STI punch-through characteristics are measured by applying a constant current (80 nA/μm) through two n^+ diffusions across an STI region, and monitoring

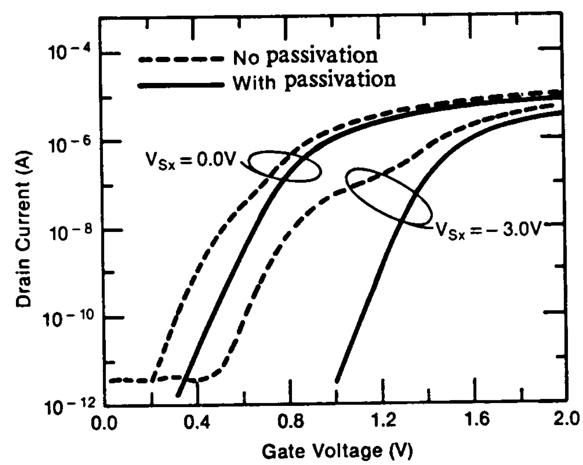

FIG.7 Sub-threshold characteristics of the nMOSFET devices isolated by STI, with and without sidewall passivation

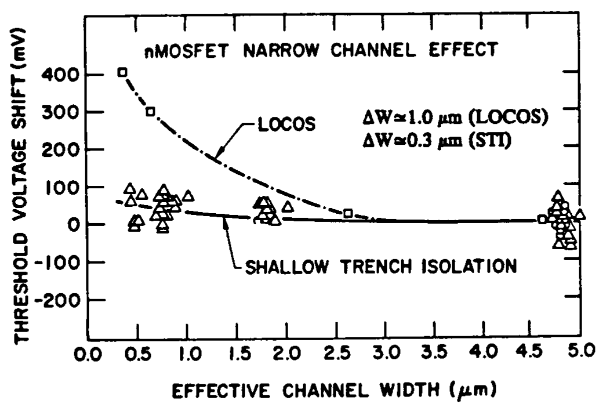

FIG.8 nMOSFET narrow channel effect of Shallow Trench Isolation and LOCOS the voltage. For STI isolation widths down to 0.5 μm (mask), the punch-through voltage is higher than 10 volts. Fig.9 shows the typical n^+ and p^+ source/drain junction (silicided) leakage characteristics. Very low junction leakages (comparable to or better than the LOCOS isolation) are achieved, partly due to the STI vertical sidewalls which are less sensitive to the isolation pull-back during the process. The field threshold voltage is high ($>$15V) using either BSG or p^+ poly diffusion sources. Excellent gate oxide breakdown characteristics are achieved (99% yield for breakdown field$>$ 8MV/cm, Fig.10). Fig.11 shows a plot of the retention time fails for 0.5 μm ground rule (4.06 μm^2) 16 Mb DRAM cells using STI. The very low fail percentage demonstrates successful integration of the STI process.

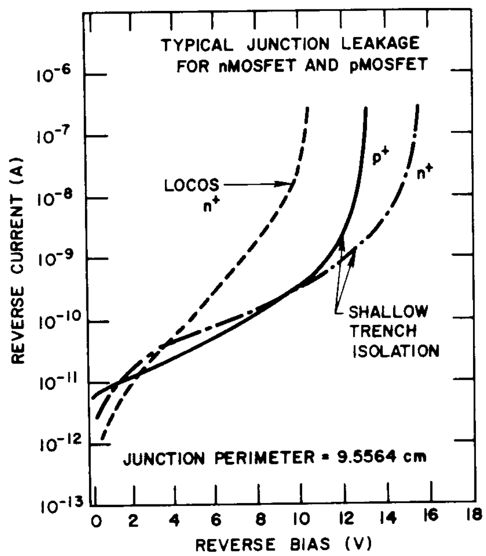

FIG.9 Source/Drain junction leakage (silicided) for STI and LOCOS

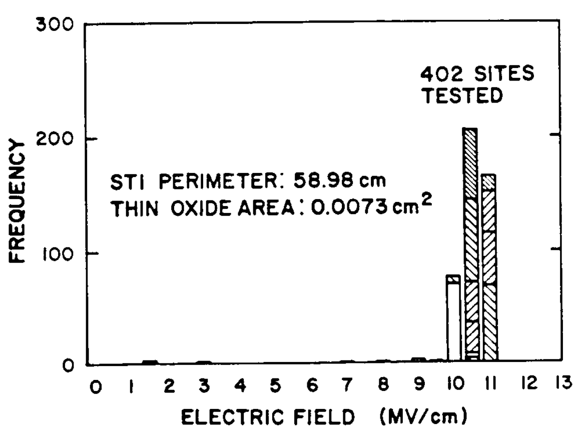

Fig.10 Gate oxide breakdown field with STI

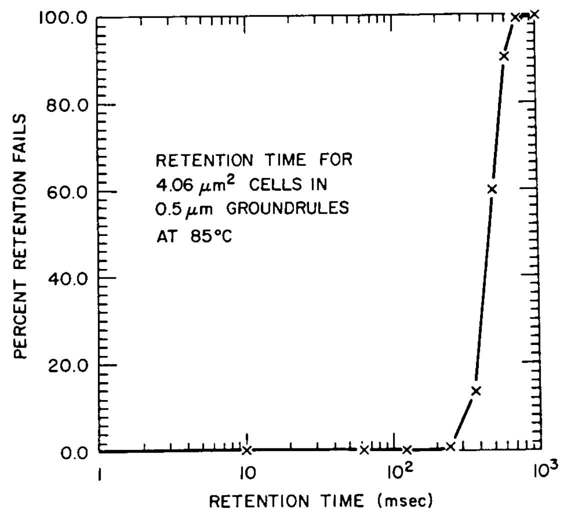

FIG.11 Retention time fail percent for 16 Mb DRAM cells, using STI

CONCLUSION

A variable-size shallow trench isolation technology, with a novel diffused field dopant technique is presented. Excellent electrical characteristics are demonstrated, including the successful fabrication of 16 Mb DRAM cells which shows the feasibility of STI for lithography limited, density-driven, submicron CMOS technologies.

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