Interconnecting drivers to flexible displays

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Abstract — Several options to interconnect driver chips to a flexible display are discussed and investigated. In the first option, bare test dies are flip-chip (FC) assembled onto polyethylene terephthalate (PET) display substrates. The second option involves test flexible polyimide (PI) substrates, imitating tape-carrier-packaged drivers (TCP), bonded onto the same PET substrates, whereas the third option uses actual TCPs on stainless-steel display substrates. Each option makes use of bonding technology with anisotropically conductive adhesive, supplied as film (ACF). The reason for using ACF is that drivers typically have high output counts, and therefore very fine pad features, 200-μm pitch and below. The technology has been adapted for each option, considering the requirements of the substrate. Every option includes an explanation of the bond test setup, the bonding process itself, and a discussion of the test results. The conclusion summarizes the achievements made in the research reported in this article.

Keywords — *Driver bonding, flexible display interconnection.*

1 Introduction

Many great efforts are currently investigating flexible electronics for various purposes. Compared to rigid PCBs, they are flexible, thin, lightweight, robust, conformable, portable, and require less material. These advantages are applicable to displays and are therefore gaining interest from the major players in the display-manufacturing industry.

Although alternatives exist, for example, embedding the chips in the display substrate is a promising option currently under development, this paper looks more closely at the possibilities of assembling the drivers either packaged or naked chips to separately fabricated flexible displays. This has the advantage that driver development and display fabrication can be carried out independently, merely considering the interface in the design steps. Bonding TCP-packaged drivers to displays is already standard in display system assemblies, but switching to flexible display substrates introduces some specific issues in the bonding process. These issues are addressed and solved for the different options below.

2 Background

The principle of assembly technology using ACF is shown in Fig. 1: the ACF is applied to the substrate, then the component is aligned and positioned and, finally, the assembly is cured under thermocompression. As the ACF, Hitachi AC8408Y was used.[1] The conductive particles are gold-coated plastic spheres, approximately 5 μm in diameter. These are coated with a very thin insulation layer that has to be cracked open during the thermocompression step. The purpose of this insulator is to prevent lateral conduction due to clustering particles.

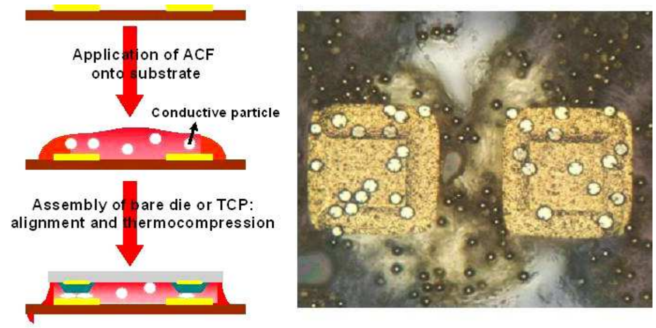

FIGURE 1 — Principle of assembly technology using ACF.

Important measurements to keep in mind when developing assembly technologies are threefold: optical, mechanical, and electrical. Optical measurements involve alignment accuracies, mechanical measurements involve adhesion tests, and electrical measurements range from daisy chains and four-point contact resistance to capacitance and shorts testing. Several tests are incorporated and explained in what follows.

For the actual bonding, which is a thermocompression step, a semi-automatic (modified) Farco bonder is used. This tool allows us to use different sizes of thermode heads, align the thermode to the bonding area, vary the bonding pressure, and program a temperature profile for the thermode.

Another issue to bear in mind here is thermal expansion. All substrates expand (or contract) with temperature, as characterized by the coefficient of linear thermal expansion (CTE), expressed in ppm/K (parts per million per Kelvin). The CTE can thus be used to calculate (linearly) the expansion of a material, when it is heated up (or cooled down). During thermocompression bonding, the whole setup is heated, and the substrates will expand according to

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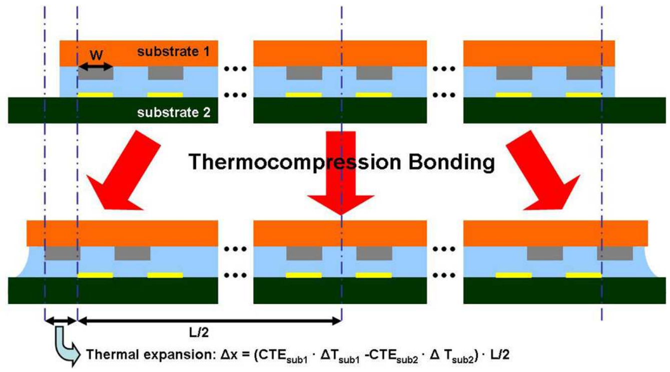

FIGURE 2 — Principle of linear mismatch due to a difference in the thermal expansion of the two substrates: L is the total bond length, W is the width of the bond pads, and ΔT is the difference between the thermocompression and room temperature.

their CTE. Usually, the two substrates will not expand equally, due to a CTE mismatch, and a difference in temperature is experienced by the substrates. This means that the pads on both substrates, while matching at room temperature, may not match when curing sets in. The principle is illustrated in Fig. 2.

This means that thermal expansion becomes more critical with smaller contacts, increasing bond length and temperature. More accurately, with the notations in Fig. 2, there is no problem as long as $W \geq \Delta x$. Then, all the bonded pads will overlap at least half the bond pad area, if the middle area is accurately aligned. Although this will result in a doubling of contact resistance at the sides compared to the middle area, it usually does not pose a problem in display applications because the contact resistance plays only a very minor role in comparison to the high resistivity of row and column conductors.

Thermal expansion is usually pre-compensated in the design, based on either theoretical expansion models or practical bonding trials. Actual trials are recommendable because many of the factors in the complete setup influence the thermal behavior during bonding: not only the substrates, but also the conductive patterns and the surrounding setup (such as carrier substrates) can play a significant role. In the experiments discussed here, thermal expansion was always determined beforehand through bonding trials.

3 Option 1: Flip-chip on PET

3.1 Test setup and design

In this option, the technology of directly assembling the driver chips on the display substrate is investigated. To this end, tests were designed, where test chips are placed and bonded on the substrate by means of the flip-chip technique. Test chips and corresponding substrates have been designed for different sizes and pitches. The specifics are given in Table 1. The test chips are slim, simulating actual driver chips.

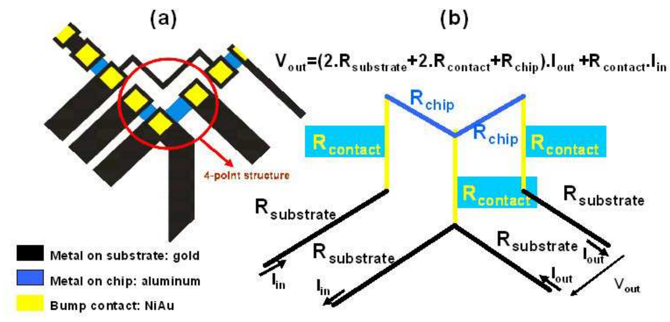

FIGURE 3 — Principle of four-point measurement: (a) top view and (b) 3-D view explaining the principle.

The patterns include daisy chains to measure contact yield and four-point structures to measure the contact resistance. The principle of four-point measurement is illustrated in Fig. 3: a "large" current I_{in}, on the order of 1 mA, is driven through two contacts, and the voltage V_{out} is measured in between the two neighboring contacts. V_{out} is measured by a measuring current I_{out}, much smaller than I_{in}, typically below 1 µA. If I_{out} is small enough compared to I_{in}, the first term in the formula for V_{out} can be neglected and we find $R_{\mathrm{contact}} = V_{\mathrm{out}}/I_{\mathrm{in}}$.

The substrates, mounted on a glass carrier, were provided and patterned by Plastic Logic Ltd. (PLL).[2] They were 100 × 100 mm in size and approximately 150 µm thick. The gold metal pattern on the substrate is 60–100 nm thick. Figure 4 shows some photographs of those substrates. The test chips themselves were fabricated in-house, with the layer buildup shown in Table 2.

Two batches of wafers were processed. They yielded some good test chips for the coarser pitches of 200 and 100 µm. However, overplating and underplating, respectively in the first and second batch, in the bumping stage rendered the 50-µm pitch test chips unusable from an electrical point-of-view, as is illustrated in Figs. 5 and 6.

TABLE 1 — Different sizes and pitches designed for FC tests.

size (mm x mm)	pitch (μm)	# contacts	# 4-point structures
2.5 x 7.5	200	90	6
2.5 x 7.5	100	194	6
2.5 x 7.5	50	380	6
2.5 x 15	200	166	6
2.5 x 15	100	338	6
2.5 x 15	500	680	6

TABLE 2 — Layer buildup of the test chips.

layer	deposition step #	thickness (μm)
Electroless Au plating	5	0.1
Electroless Ni bumping	4	10-15
PECVD Si_3N_4	3	0.4
Sputtered TiW + Al	2	0.02 + 0.5
PECVD SiO_2	1	0.4
Si wafer	0	700

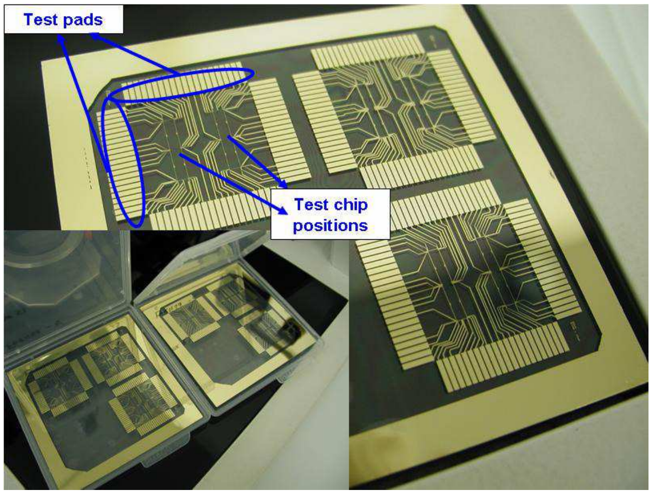

FIGURE 4 — Photographs of Au-patterned PET substrates for flip-chip tests layer.

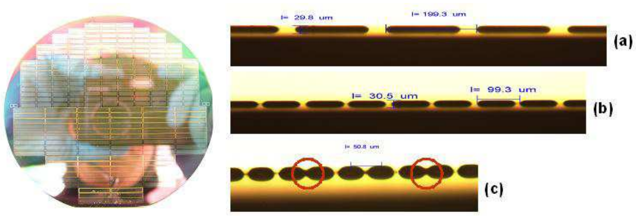

FIGURE 5 — Resulting chips from the first batch: pitches (a) 200 μm, (b) 100 μm, and (c) 50 μm (overplated and shorted).

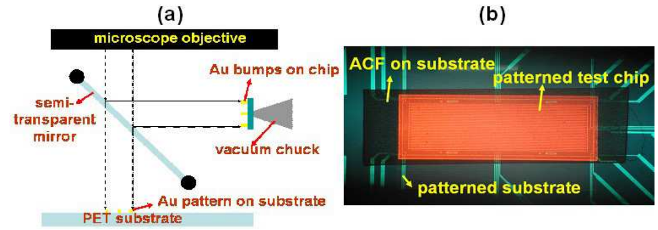

FIGURE 7 — Alignment of the chip to the substrate: (a) side view of the principle and (b) top view through a microscope.

3.2 Bonding process

The actual bonding process consists of several steps. The sequence is shown in Table 3. Precleaning of the substrate is important because otherwise prebonding fails. The alignment of the chip to the substrate and the placement is performed by using a semiautomatic flip-chip aligner (Karl Suss). The chip is picked up by a vacuum chuck, and a beamsplitter mirror is used so that the pattern on the chip and on the substrate can be viewed at the same time and can thus be aligned and positioned. This is shown in Fig. 7. It is clear that the calibration of the beamsplitter mirror is crucial for the accuracy of the alignment.

For the actual heat-bonding step, the placed chip (on the substrate) is aligned with the thermode. A 0.2-mm interposer tape from ShinEtsu Chemicals is placed on top of the chip to redistribute slight pressure differences. Then the thermode is lowered onto the chip with a set pressure of

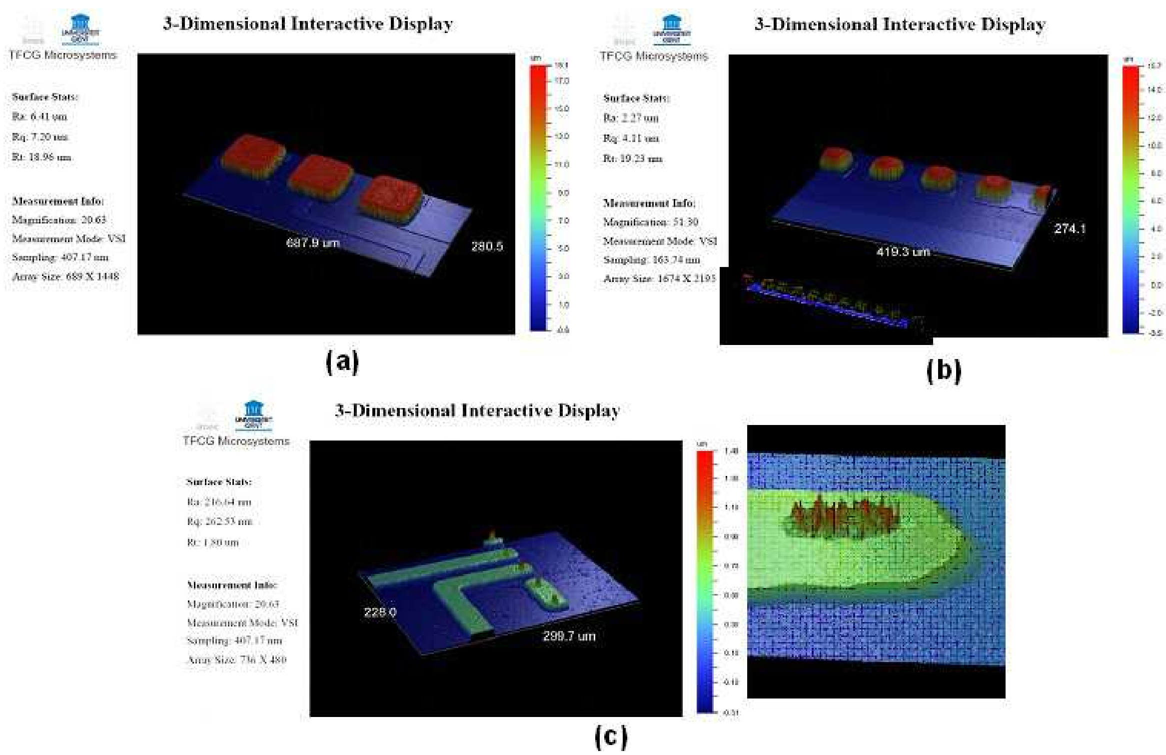

FIGURE 6 — Optical inspection of the wafer surface (second batch) shows the results of the test-chip bumping process: pitches (a) 200 μm, (b) 100 μm, (c) 50 μm (underplated).

TABLE 3 — The bonding process.

step #	process step	remarks
1	Clean substrate and chip	With isopropanol
2	Cut and apply ACF on substrate	Slightly larger than bond area for homogeneous bonding
3	Pre-bond ACF	4s @ 90°C, 1mm silicone interposer
4	Remove ACF release film	Should be easily removed
5	Align chip to substrate	Calibration beforehand concerning mirror tilt
6	Place chip	
7	Align chip to thermode	
8	Bond chip	30s @ 170°C, 0.2-mm silicone interposer

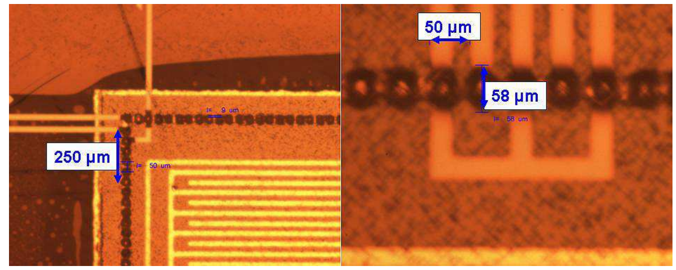

FIGURE 9 — Photographs of a flip-chip assembled test chip, proving the feasibility of aligning 50-µm pitch chips to a patterned substrate; note the overplated contacts.

1–2.5 bar (depending on chip and bump size) and gradually heated to the final bonding temperature of 200°C. At this temperature, the ACF has a much lower viscosity, the applied pressure ensures electrical contact, and the excess adhesive flows out from under the chip. Gradual heating is needed to achieve optimal adhesion: if the thermode is heated too fast, the ACF is cured too suddenly and inhomogeneously, resulting in bubble formation (which means lower adhesion). After 30 sec, the thermode heating is switched off so that the thermode cools down, while it still presses on the chip. This is to minimize residual stresses in the adhesive material of the ACF, which will help in providing optimal adhesion. When the thermode temperature has reached a temperature of 100°C, low enough so that the ACF has solidified sufficiently, the thermode is lifted up again. Thermocouple measurements result in the temperature profile shown in Fig. 8.

The bonding conditions had to be optimized for bonding on PET because the temperatures and pressures cannot be as high as when glass is used as the substrate. When conditions used for bonding on glass (namely, 30 sec @ 300°C, without interposer) are used on PET, it "melts," and the chip is pressed into the partially liquified PET substrate. Because no interposer is placed in between the chip and thermode, the molten PET sticks to the thermode. Subsequently, when cooling down, the PET solidifies again and when the thermode retracts, it pulls plastic strings right out of the substrate.

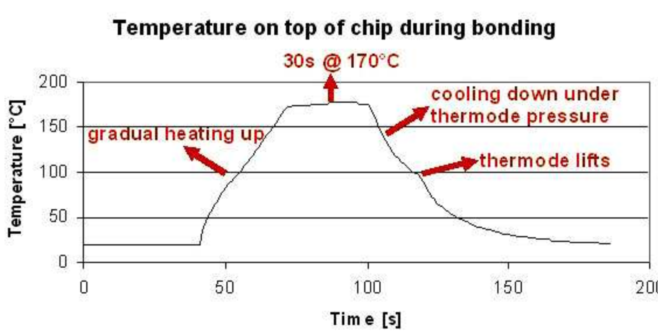

FIGURE 8 — Temperature on top of chip throughout the actual bonding process.

3.3 Test results

First, the feasibility to align bumped 50-µm pitch chips to a gold patterned PET substrate has been proven. This is illustrated in Fig. 9. Second, no significant thermal-expansion difference between substrate and chip was observed in any of the tests. This means no compensation has to be calculated in the substrate design beforehand (at least when the chips used remain smaller than 2.5 × 15 mm).

Third, it is important to level the thermode head accurately with the substrate. Uneven bonding results in a large variation in contact resistance, and even loss of contact along the length of the chip in the worst case.

Furthermore, the bumps are always slightly pressed into the substrate (causing some plastic deformation) to ensure electrical contact between the bump and substrate path. Figure 10 shows this effect under high magnification.

Electrical four-point measurements on the 200- and 100-µm-pitch chips bonded show contact resistances well below 1 Ω. This resistance value can be neglected because the used thin-film gold interconnection lines on the substrate show resistances in the range of 0.51 Ω/□.

The relatively high values in the standard deviation in Table 4 can be attributed to (minor) misalignment: the contact resistance can vary significantly with the overlapping area of bump and contact on the substrate.[3] The daisy-chain measurements show that a contact yield of 100% could be achieved for 184 contacts at a pitch of 200 µm and 356 contacts at a pitch of 100 µm.

As for the mechanical adhesion, tests show that when a chip is pushed off the substrate (die shear), some adhesive still sticks to the substrate, while some holds on to the chip.

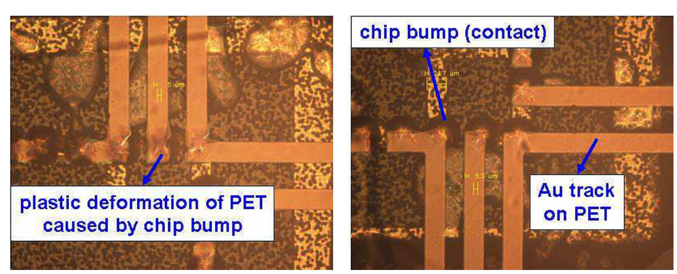

FIGURE 10 — Pictures of a flip chip assembled 50-µm-pitch test chip: the contacts are pressed slightly into the substrate.

TABLE 4 — Electrical four-point measurements: Results.

pitch (μm)	contact resistance (Ω)	# measurements
200	0.27 ± 0.23	82
100	0.27 ± 0.13	39

On the one hand, some bumps are torn off the chip; on the other hand, some of the gold pattern is torn off the substrate. This should indicate sufficient adhesion.

The die shear strength for a standard bonded test chip, 2.5×7.5 mm, 200-μm pitch, was measured over 500 N using a Dage bondtester fitted with a DS100Kg cartridge. This corresponds to over 50 kgf, while a widely used standard for die shear strength, the U.S. military MILSTD883 2019,[4] only stipulates a die shear strength of over 5 kgf, if the die is larger than 64×104 IN2, equalling approximately 2×2 mm (most demanding requirement).

4 Option 2: TCP on PET

4.1 Setup

Another option to interconnect drivers to the display is to bond TCPs to the display. This is currently standard in manufacture of flat-panel displays (LCD, plasma, and e-paper) on glass substrates. Again, this type of technology has to be modified for flexible substrates. The relative thermal expansion was determined beforehand as 57 μm for a length of 40 mm, and compensated in the designs for the tests.

The tests were designed for PET display substrates, delivered by DuPont and patterned by Plastic Logic, and the tape material was provided by Shindo, a Japanese TCP manufacturer for ST Microelectronics.[5] The tape material consists of a 75-μm base PI layer, with a 25 μm copper top layer, both held together by a 12-μm adhesive layer.

Two types of tests were designed: one test for daisy-chain measurements, another for testing for shorts, combined with capacitance measurements. The contacts in both cases are spaced at 100-μm pitch, patterning lower pitches was tried at 80- and 60-μm pitch, but proved too difficult to achieve with standard spray-etching techniques with an acceptable yield. To finish it off, a 20-μm solder-mask is applied and the contacts are electroless NiAu-plated. The daisy-chain pattern comprises 400 contacts. Figure 11 illustrates the setup designs and the patterned substrates, both tape and display PET.

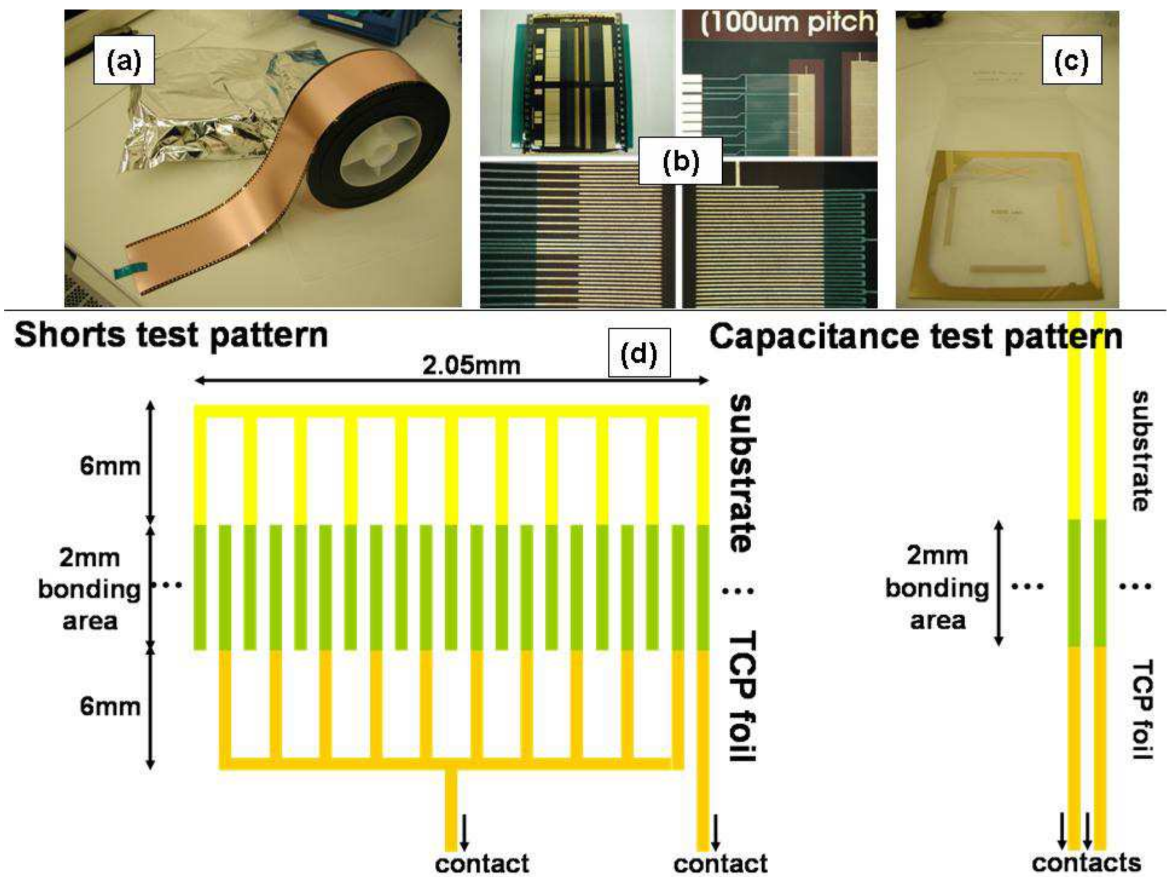

FIGURE 11 — Tape material as delivered (a), after processing (b), patterned PET substrate (c) and design setup for shorts and capacitance testing (d).

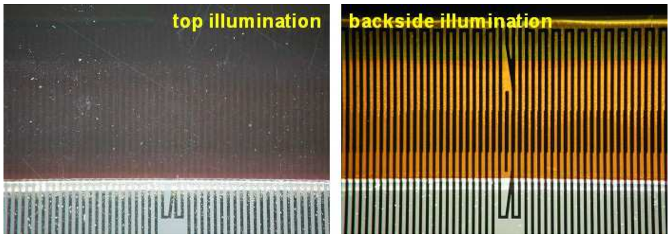

FIGURE 12 — Aligning is much easier with backside illumination, mainly due to the thick PI.

4.2 Bonding process

The bonding process itself is quite similar to the bonding of chips: bonding was carried out with the same temperature profile and with a pressure of 2 bar, using the same semi-automatic bonder, but with a slim thermode head of 2 × 70 mm. However, the aligning and placing were manually performed, under a microscope, for the TCPs, and both ends are attached temporarily to the substrate with a soldering tool before final bonding. As the PET substrates are attached to transparent glass carriers, backside illumination offers better viewing, as is illustrated in Fig. 12.

4.3 Test results

Optically, tape expansion, relative to the display substrate, was correctly compensated in the design, 57 µm for a length of 40 mm. Also, it is possible and rather convenient to optically check whether electrical interconnection is established: this is the case when the particles are slightly squeezed into the display substrate's contacts. Both of these are illustrated in Fig. 13.

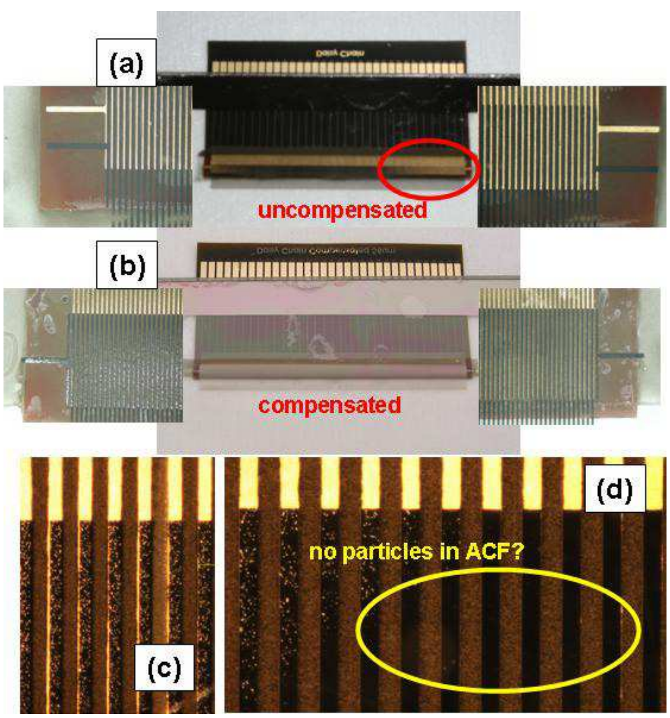

FIGURE 13 — (a) Expansion leads to mismatch at the edges after bonding. (b) Compensation of expansion minimizes mismatch. (c) ACF particles are pressed into the contacts, as seen through the substrate. (d) No electrical interconnection due to a lack of particles in the ACF (visible because no indentations are noticed).

TABLE 5 — Electrical results for TCP on PET trials.

Daisy chain measurements			
# contacts	# squares	line length (mm)	resistance (Ω)
12	880	48	571 ± 33
14	960	56	665 ± 38
16	1040	64	753 ± 39
Check for shorts			
0			
Capacitance measurements			
line length (mm)	C_{meas} (pF)	C_{offset} (pF)	C_{net} (pF)
8	12 ± 1	6	6 ± 1

Electrically, three types of measurements were carried out: daisy chains, shorts between neighboring contacts, and capacitances, all listed in Table 5. The daisy chains show that the total resistance is primarily due to the resistance of the thin-film gold on the substrates, so that contact resistance can be neglected. No shorts were found that were not already present before assembly (defects from prior processing steps). Capacitance between two neighboring lines that are 8 mm long was 12 ± 1 pF. It should be mentioned that this is near the lower limit of the multimeter tool used, and 6 pF is the value measured when the probes are simply placed next to each other, 10 mm apart on the table.

Industrial requirements for data line resistance and capacitance for electrophoretic active-matrix displays are typically below 12 kΩ and 180 pF for 200 mm long, 100 µm wide lines spaced at a pitch of 200 µm. With some recalculation, it is possible to extrapolate the measurements so that a comparison can be made. The results are shown in Table 6, where it is clear that the requirements are adequately met. Photographs can be found in Fig. 14.

One more remark concerns accuracy requirements: even major misalignment does not affect electrical interconnection significantly. A misalignment of 40 µm for example, shown in Fig. 15, gives comparable measurements as a perfectly aligned assembly. Of course contact resistances can be expected to vary significantly, but this is not reflected in the

TABLE 6 — Extrapolation needed to compare measurements with requirements.

Extrapolation of measurements			Requirements
line length (mm)	line width (µm)	resistance (Ω)	
48 → 200	50 → 100	571 → 1190	≤ 12 kΩ
56 → 200	50 → 100	665 → 1188	
64 → 200	50 → 100	753 → 1177	
line length (mm)	line width (µm)	capacitance (pF)	
8 → 200	50 → 100	6 → 150	≤ 180 pF

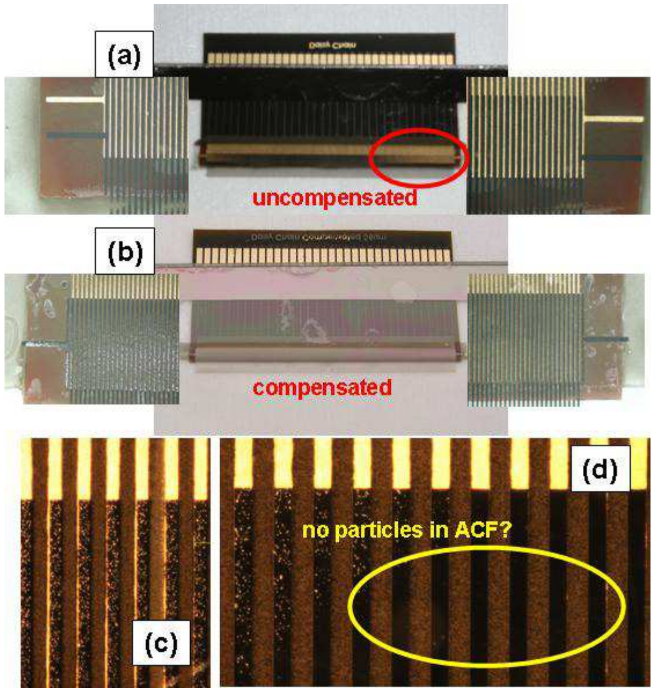

FIGURE 14 — Assembled test TCPs (not on scale, widened): daisy chain (a) and shorts and capacitance (b) designs.

measurements due to the much higher thin-film resistance on the substrate.

Adhesion can be determined by testing for peel strength. The results indicate good adhesion. Measurements can be performed perpendicular to the bond length or along the bond length, setups are as shown in Fig. 16. The PET substrate is still attached to its rigid carrier when it is clamped in a holder that can be moved at a given speed while pulling.

Perpendicular test results linger around 2000 g/40 mm, and both substrate and TCP metallization are damaged in this type of peel test. Along the length of the bond, however, this is 1030 g/2.5 mm. The results are slightly lower as compared to values reported in a glass display interconnection[6] of around 0.3 kN/m, but the top layer of the PET sub-

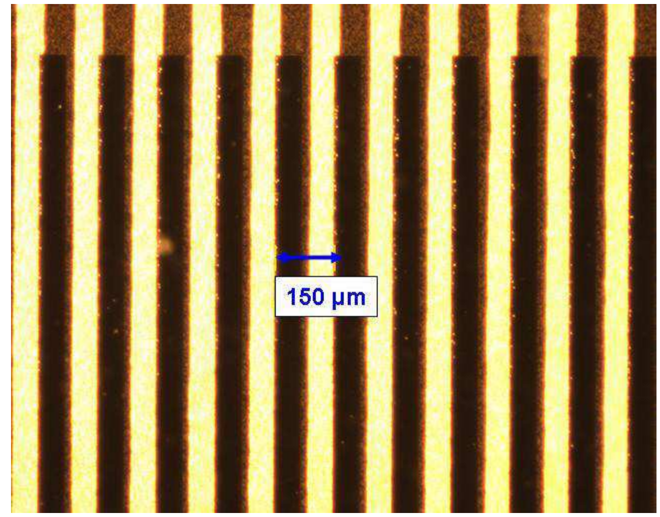

FIGURE 15 — Despite misalignment electrical interconnection is still ensured through the ACF particles (indents still visible in the tiny overlap areas).

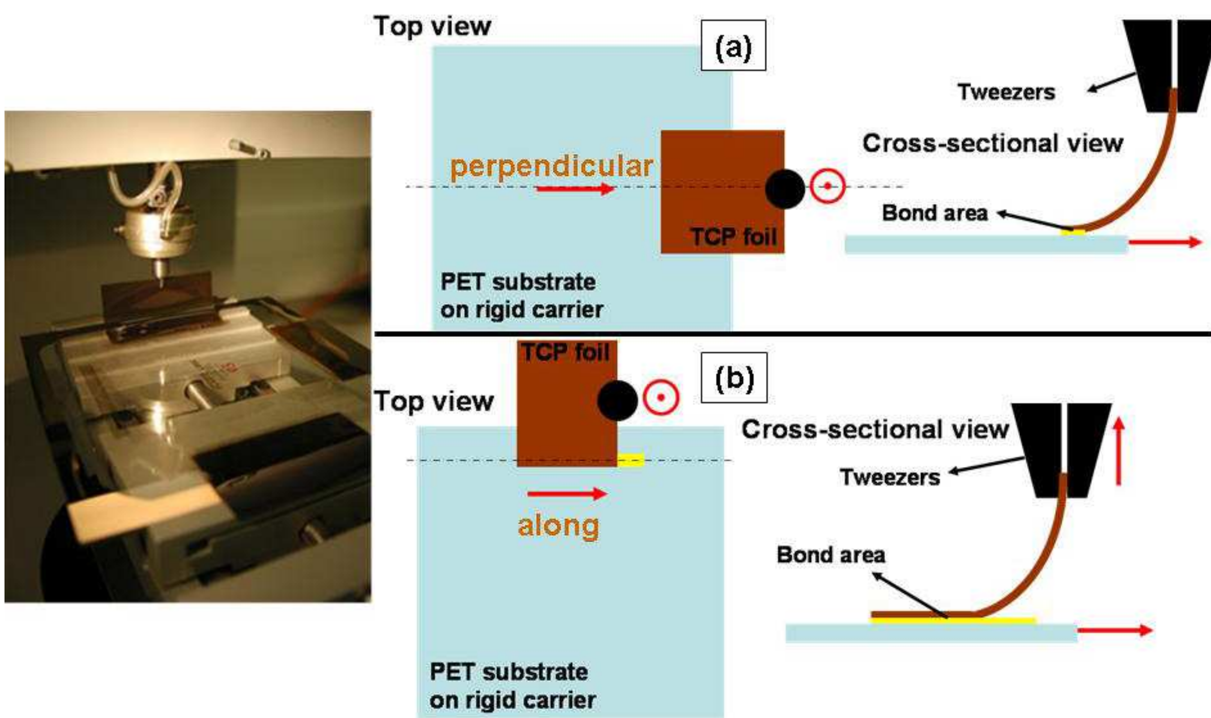

FIGURE 16 — Setup for peel strength tests (a) perpendicular to and (b) along the bond length; the movement of substrate and tweezer (pulling) is indicated by the red arrows.

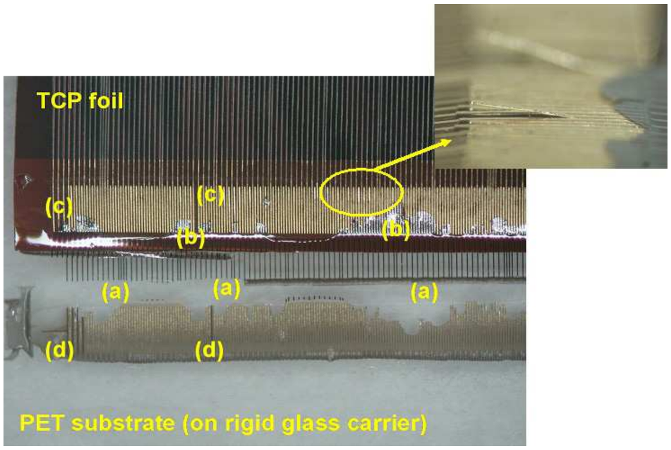

FIGURE 17 — Resulting surfaces after peel strength testing perpendicular to the bond length. In some areas, a layer (with gold metallization) is torn from the PET substrate (a), and still clings to the TCP foil (b), in other areas, copper traces are torn from the TCP foil (c) and still cling to the substrate (d); the zoomed view shows a copper trace that is partially torn off the TCP foil, while at the same time a layer of the PET substrate is still sticking to the TCP foil.

strate tends to peel off (the failure is not due to the ACF) and this interface thus becomes the limiting factor. This is shown in Figs. 17 and 18 and the assembly, with this type of substrate and TCP can be considered successful.

5 Option 3: TCP on stainless steel

5.1 Setup

In the first two options, chips and TCPs are bonded to PET substrates. These substrates are suitable for flexible display substrates, with e-paper applications in mind. The third

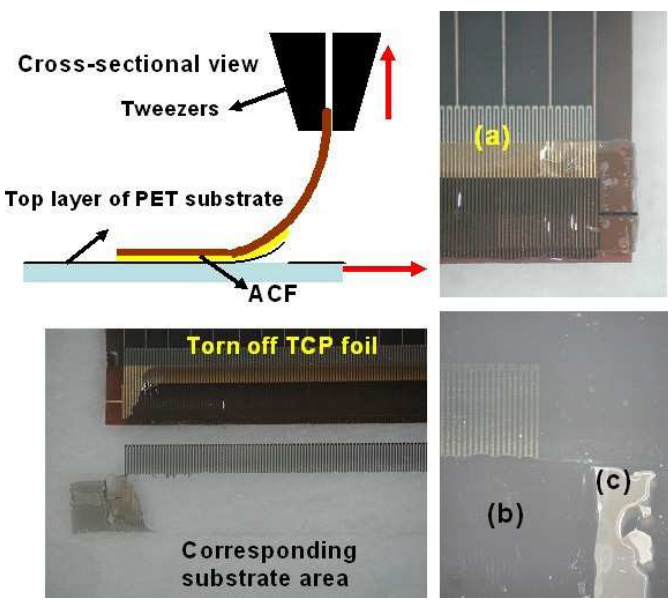

FIGURE 18 — (a) Results for peel strength tests along the bond length: the top layer of the PET substrate is torn loose and remains attached to the TCP foil, (b) avoid area is left behind on the PET substrate, (c) with the exception of some adhesive leftovers at the sides.

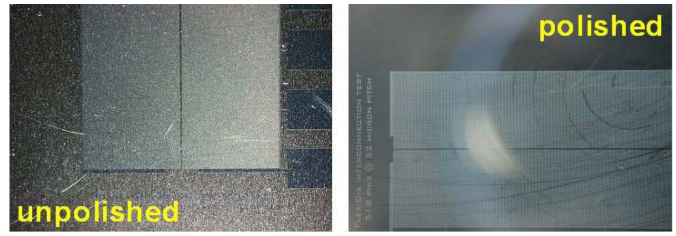

FIGURE 19 — Comparison of polished and unpolished steel substrates.

TABLE 7 — Specifications of driver TCPS used.

	Pitch (μm)	# contacts	PI (μm)	Adhesive (μm)	Cu (μm)
NEC	90	267	38	none	8 (Sn-plated)
Hitachi	52	519	75	12	15 (Sn-plated)

option involves stainless-steel substrates, more suitable for organic light-emitting diode (OLED) displays because OLED deposition processes require higher temperatures than what PET can withstand. In this option, functional TCP-packaged drivers from NEC (uPD160702ANL) and Hitachi (HD66358T03E) are bonded to stainless-steel substrates that were supplied and patterned by CEALETI.[7] These are 152 µm thick and need to be polished before they are covered with a 1.5-µm-thick SiO_2 insulator layer and a 350-nm-thick TiMo metal pattern, matched to the TCP contacts. The polishing reduces the average roughness of the stainless steel from 95 to 0.6 nm, which is needed to avoid shorts from the metallization to the backpanel. It also improves the visibility of the metallization, as is illustrated in Fig. 19. The specifications of the driver TCPs are given in Table 7, and it is also worth mentioning that the Hitachi TCP's contacts are shrunk by 40 µm to compensate for thermal expansion during bonding. This is not the case for the NEC TCP.

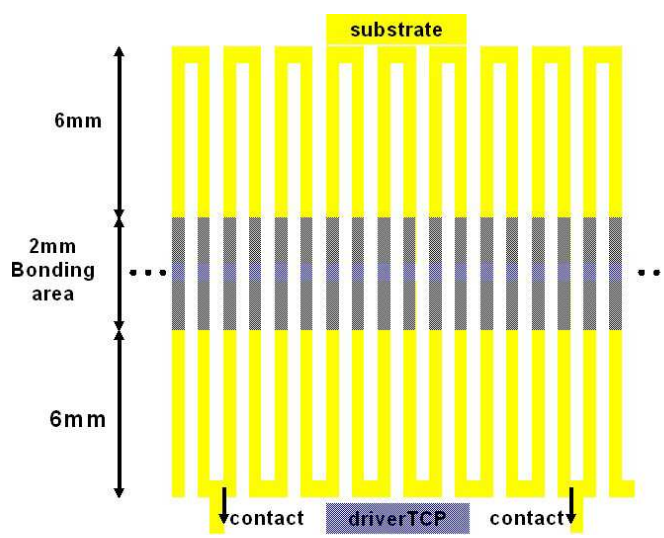

FIGURE 20 — Setup for electrical interconnection testing of bonds with existing TCPs.

As the tests are carried out with actual TCPs, design options for electrical testing are limited: the substrates are patterned with incomplete daisy chains that can only be completed by a correctly bonded TCP. The setup is shown schematically in Fig. 20.

5.2 Bonding process

The bonding process is again quite similar to the previous option, although there are a few important differences.

First of all, steel is not transparent and this means backside illumination is not an option. Next, the contacts that need to be interconnected have a finer pitch, down to 52 μm for the Hitachi driver. These differences mean that placing and aligning are far more difficult, although not impossible. Then there is also the fact that the contacts have lower bumps, so the bonding pressure is raised from 2 to 2.7 bar to squeeze out more adhesive. Finally, it should be mentioned that heat dissipation is rather different, as steel conducts heat far better than PET on a glass carrier. However, the temperature of the bonding head (thermode) does not need to be raised if an insulating glass plate is placed between the substrate and the (metallic) substrate table.

5.3 Test results

Optical and electrical results are summarized in Table 8. The thermal expansion is sufficiently within range using the current bonding parameters, so that all TCP outputs can be electrically interconnected to the substrate. The measured resistances are, as earlier on with the other options on PET, mostly due to the thin-film resistance of the metallization on the substrates, and are supposed to be low enough for current active-matrix OLED displays.

Note that not all daisy-chain patterns of the bonded samples have been included in the measurements. This is because of errors made in the bonding process and the steps preceding this, such as (slight) misalignment, the thermode that is not sufficiently aligned to the substrate (resulting in uneven pressure during bonding), insufficient cleaning, as well as problems due to the steel backpanel (bypassing several daisy-chain patterns and thus disrupting electrical measurements), and shorts between neighboring contacts due to defects introduced during patterning (mask faults, dust contamination, *etc.*).

TABLE 8 — Results and measurements on assembled daisy chains.

	NEC TCP	Hitachi TCP
# samples bonded	7	11
misalignment before bonding [μm]	-0.5 ± 2.0	-0.7 ± 2.6
misalignment after bonding [μm]	16.6 ± 4.6	3.1 ± 4.5
expansion measured [μm]	34 ± 12	46 ± 9
# daisy chains measured	45 (out of 49)	53 (out of 77)
# contacts / daisy chain	76 (38 x 2)	148 (74 x 2)
# squares on substrate	7600	25615
line length [mm]	532	1036
resistance [Ω]	3020 ± 135	12049 ± 1942

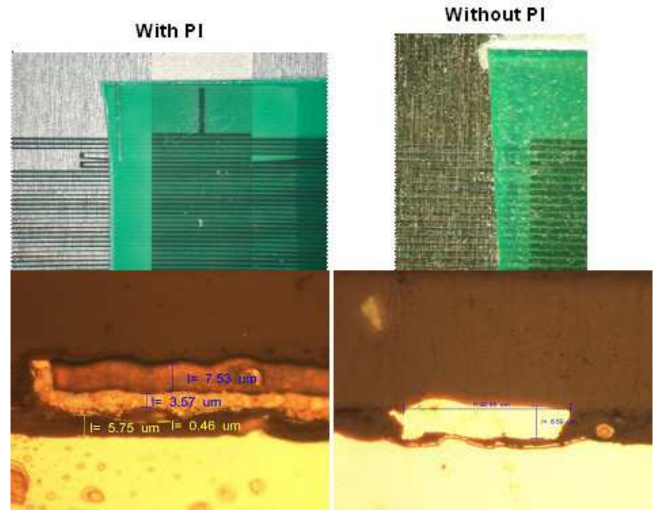

FIGURE 21 — A PI insulating layer *vs.* an SiO_2 insulating layer for steel substrates.

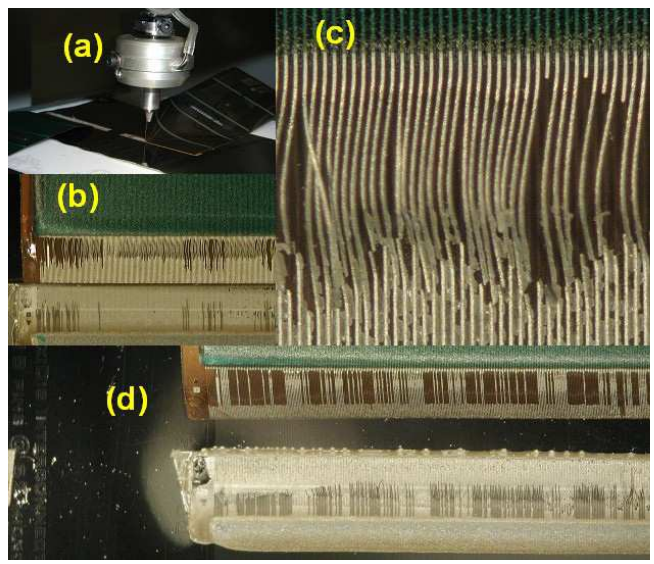

FIGURE 22 — Peel strength tests on a bonded Hitachi TCP: (a) peel setup, (b) result of peeling along the bond length, (c) under high magnification, and (d) result of peeling perpendicular to the bond length.

One issue requiring special attention involves the mentioned problems with the steel back panel. The 1.5 μm SiO_2 insulating layer suffers from pinholes due to the surface roughness of the steel substrates, even after polishing. One solution would be to use a thicker (*e.g.*, 5 μm) organic PI layer as a spunon planarizing layer. This would also significantly enhance viewing the metallization. This is illustrated in Fig. 21.

Adhesion was tested with the same setups as described in Fig. 20, resulting in the damage shown in Fig. 22 for the Hitachi TCP and Fig. 23 for the NEC TCP. For the Hitachi TCP, the peel strength was measured as 1400 g/40 mm perpendicular to the bond length and 150 g/2.5 mm along the bond length. It is clear that some tracks on the TCP have

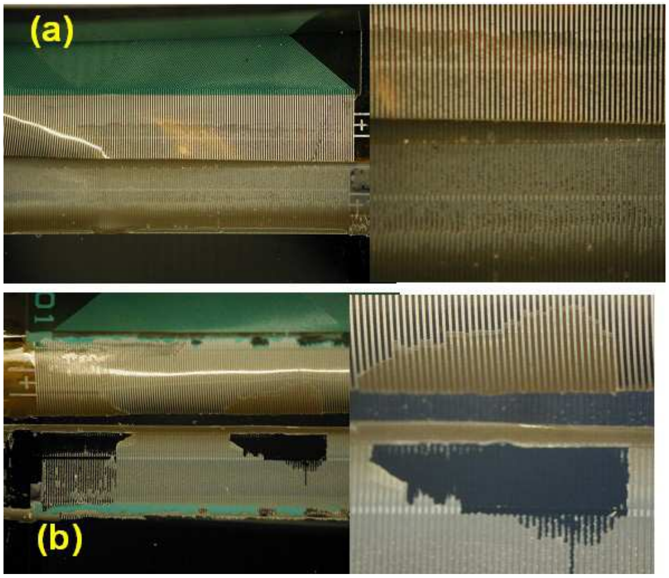

FIGURE 23 — Peel strength tests on a bonded NEC TCP: (a) result of peeling along the bond length, (b) result of peeling perpendicular to the bond length.

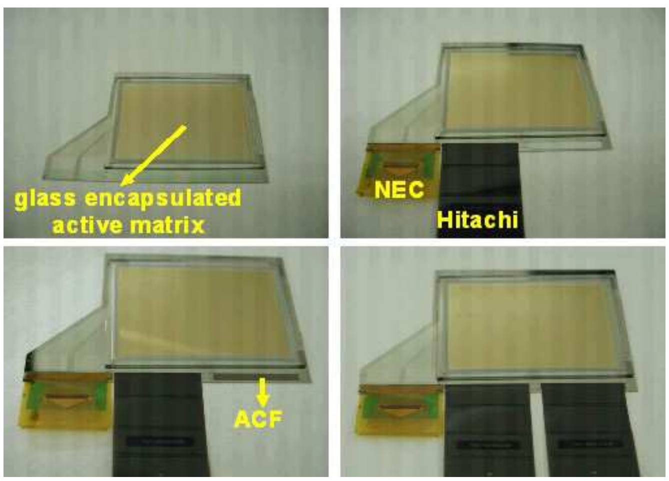

FIGURE 24 — Assembly of a flexible display on a stainless steel substrate with row (NEC) and column (Hitachi) drivers packaged as TCP.

been torn off the TCP substrate, illustrating that adhesion between the metal tracks (Ti/Mo on substrate and Cu/Sn on TCP) is comparable to the adhesion between the copper and PI layer in the TCP buildup. As for the NEC TCP, the peel strength was measured as over 2500 g/40 mm (out of the set range of the bond tester) perpendicular to the bond length, and 150 g/2.5 mm along the bond length. Here, the pictures show a different result: it is the ACF that is peeled off.

6 Conclusion

In this article, research on interconnection technologies for flexible displays is reported. This work describes how the existing industrial technologies in glass-based display manufacturing are adapted to fit the requirements introduced by switching to flexible PET and stainless-steel substrates. All the steps that are needed to assemble the drivers using ACF are elaborated, and encountered issues are reported. Each technology is optically, electrically, and mechanically evaluated. The report is therefore a description of technologies that can be used to successfully bond drivers, either packaged on tape or as bare die, to flexible display substrates.

These technologies are relevant and are currently under investigation by industrial display manufacturers, nearing the stage of application, as for example, Plastic Logic (U.K.), intending to industrially manufacture flexible e-paper devices on PET substrates. As for stainless-steel substrates with flexible OLED displays, these are being prototyped and considered for, among others, integration in the sleeves of a jacket. The technology described above is currently being used to assemble demonstrator prototypes for displays, illustrated in Fig. 24.

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