UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MUNDRA SOLAR PV LIMITED
Petitioner

v.

FIRST SOLAR, INC.
Patent Owner

U.S. Patent No. 9,666,732
IPR2025-01411

DECLARATION OF DR. SANJAY BANERJEE, PH.D.

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Ex. 1004	Curriculum Vitae of Dr. Sanjay Banerjee, Ph.D.
Ex. 1005	Yablonovitch, E., Gmitter, T., Swanson, R. M., & Kwark, Y. H. (1985). *A 720 mV open-circuit voltage SiO_x:c-Si:SiO_x double heterostructure solar cell*. Applied Physics Letters, 47(11), 1211-1213 ("**Yablonovitch**").
Ex. 1006	Thomas, J. H., & Feigl, F. J. (1972). *Electron trapping levels in silicon dioxide thermally grown on silicon*. Journal of Physics and Chemistry of Solids, 33(12), 2197–2216 ("**Thomas**").
Ex. 1007	Kragler, G., Bender, H., Willeke, G., Bucher, E., & Vanhellemont, J. (1994). *Characterization of SIPOS films by spectroscopic ellipsometry and transmission electron microscopy*. Applied Physics A, 58(1) ("**Kragler**").
Ex. 1008	Crabbé, E. F., Hoyt, J. L., Pease, R. F. W., & Gibbons, J. F. (1988). *Electrical characterization of polysilicon-to-silicon interfaces*. Materials Research Society Symposium Proceedings, 106, pp. 247-52. © Materials Research Society.
Ex. 1009	Ghoshtagore, R. N. (1975). *Silicon dioxide masking of phosphorus diffusion in silicon*. Solid-State Electronics, 18(5), 399–406. https://doi.org/10.1016/0038-1101(75)90041-6 ("**Ghoshtagore**").
Ex. 1010	Shimakura, K., Suzuki, T., & Yadoiwa, Y. (1975). *Boron and phosphorus diffusion through an SiO_2 layer from a doped polycrystalline Si source under various drive-in ambients*. Solid-State Electronics, 18(11), 991–997. https://doi.org/10.1016/0038-1101(75)90117-3 ("**Shimakura**").
Ex. 1011	RESERVED

Exhibit	Description
Ex. 1012	RESERVED
Ex. 1013	May, Gary S., and Simon M. Sze. *Fundamentals of Semiconductor Fabrication*. John Wiley & Sons, 2004 ("**May**")
Ex. 1014	Hamasaki M., Adachi T., Wakayama S., & Kikuchi M. (1978). *Crystallographic study of semi-insulating polycrystalline silicon (SIPOS) doped with oxygen atoms.* Journal of Applied Physics, 49(7), 3987–3992 ("**Hamasaki**").
Ex. 1015	Yablonovitch, E., Swanson, R. M., Eades, W. D., & Weinberger, B. R. (1986). Electron-hole recombination at the Si-SiO_2 interface. *Applied Physics Letters, 48*(3), 245–247. https://doi.org/10.1063/1.96570 ("Yablonovitch III").
Ex. 1016	Gan, J. Y., & Swanson, R. M. (1990, May). *Polysilicon emitters for silicon concentrator solar cells.* In *Conference Record of the Twenty-First IEEE Photovoltaic Specialists Conference* (pp. 245–250). Kissimmee, FL, USA: IEEE. https://doi.org/10.1109/PVSC.1990.111625 ("**Gan**").
Ex. 1017	Kwark, Y. H. (1984). *SIPOS heterojunction contacts to silicon* (Doctoral dissertation). Stanford University, Stanford, CA ("**Kwark**").
Ex. 1018	Kwark, Y. H., Sinton, R. A., & Swanson, R. M. (1984, December). *SIPOS heterojunction contacts to silicon*. In *Proceedings of the 1984 International Electron Devices Meeting* (IEDM) (pp. 742–745). IEEE. https://doi.org/10.1109/IEDM.1984.190832 ("**Kwark II**").
Ex. 1019	Kwark, Y. H., & Swanson, R. M. (1987). *N-type SIPOS and poly-silicon emitters*. *Solid-State Electronics, 30*(11), 1121–1125. https://doi.org/10.1016/0038-1101(87)90076-1 ("**Kwark III**").
Ex. 1020	Swanson, R. M. (2005, January). *Approaching the 29% limit efficiency of silicon solar cells*. In *Conference Record of the 31st IEEE Photovoltaic Specialists Conference* (pp. 889–894). IEEE ("**Swanson**").
Ex. 1021	Neamen, D. A. (2012). *Semiconductor physics and devices: Basic principles* (4th ed.). McGraw-Hill ("**Neamen**").

Exhibit	**Description**
Ex. 1023	Cook, G., Billman, L., & Adcock, R. (1991). *Photovoltaic fundamentals* (SERI/TP-220-3957). Solar Energy Research Institute.
Ex. 1024	Neudeck, G. W.; Pak, J. H.; and Bagri, R., "*Poly silicon Contacted Emitter Bipolar Transistors: Fabrication Development*" (1988). Department of Electrical and Computer Engineering Technical Reports. Paper 597.
Ex. 1025	Wolstenholme, G. R., Jorgensen, N., Ashburn, P., & Booker, G. R. (1987). *An investigation of the thermal stability of the interfacial oxide in polycrystalline silicon emitter bipolar transistors by comparing device results with high-resolution electron microscopy observations*. *Journal of Applied Physics*, *61*(1), 225-233. https://doi.org/10.1063/1.338861
Ex. 1027	Jorgensen, N., Barry, J. C., Booker, G. R., Ashburn, P., Wolstenholme, G. R., Wilson, M. C., & Hunt, P. C. (1985). *TEM investigation of the effect of anneal temperature and arsenic concentration on the polysilicon/thin oxide/single-crystal-silicon emitter of a new high-performance bipolar transistor*. In A. G. Cullis & D. B. Holt (Eds.), *Microscopy of Semiconducting Materials, 1985* (*Institute of Physics Conference Series*, Vol. 76, pp. 471). Adam Hilger Ltd.
Ex. 1029	Sah, C. T., Sello, H., & Tremere, D. A. (1959). Diffusion of phosphorus in silicon oxide film. *Journal of Physics and Chemistry of Solids*, *11*(3-4), 288-298. https://doi.org/10.1016/0022-3697(59)90159-8
Ex. 1030	Tsubo, Y., Komatsu, Y., Saito, K., Matsumoto, S., Sato, Y., Yamamoto, I., & Yamashita, Y. (2000). Phosphorus diffusion from doped polysilicon through ultra-thin SiO_2 films into Si substrates. *Japanese Journal of Applied Physics*, *39*(10A), L955-L957.
Ex. 1031	Ni, J., & Arnold, E. (1981). Electrical conductivity of semi-insulating polycrystalline silicon and its dependence upon oxygen content. *Applied Physics Letters*, *39*(7), 554-556.
Ex. 1032	Thurston, M.O., et. al., "*Diffusion of impurities into Silicon through an Oxide Layer*", Ohio State University Research Foundation, AD 261201, Contract No. DA-36-039-SC-83874, Final Report, Columbus, Ohio, March 1961.

Exhibit	**Description**
Ex. 1033	Wesoff, E. (2011, June 29). *SunPower's Dick Swanson Still Very Much Alive*. Greentech Media. https://www.greentechmedia.com/articles/read/sunpowers-dick-swanson-still-very-much-alive
Ex. 1034	Batra, S., Picone, K., Park, K.H., Bhattacharya, S., Banerjee, S., Lee, J., Manning, M., and Dennison, C. (1992) "Study of Lateral Non-Uniformity as a Function of Junction Depth in Ultra-Shallow Junctions and its Effect on Leakage Behavior in As-Deposited Polycrystalline Si and Amorphous Si Diodes." ("Batra")

CHALLENGED CLAIMS

Claim 1	
[1Pre]	A method of fabricating a solar cell, comprising:
[1a]	providing a substrate,
[1b]	providing an interface passivation layer over the substrate,
[1c]	providing a passivating film over the interface passivation layer, the passivating film comprising a passivating material and a conductive dopant,
[1d]	wherein providing the interface passivation layer and providing the passivating film comprise:
[1d.1]	providing an amorphous silicon-containing compound over an upper surface of the substrate, the compound comprising oxygen dopant and the conductive dopant,
[1d.2]	thermally treating the amorphous silicon-containing compound to diffuse the oxygen dopant, at least in part, into the upper surface of the substrate to form an oxide layer over the substrate, the oxide layer defining the interface passivation layer; and
[1d.3]	wherein remaining amorphous silicon-containing compound above the oxide layer defines the passivating film; and
[1d.4]	wherein the thermally treating also diffuses at least a portion of the conductive dopant throughout the interface passivation layer to facilitate electrical connection to the substrate; and
[1e]	providing at least one electrode over the passivating film, wherein the conductive dopant within the passivating film and throughout the interface passivation layer provides direct electrical connection between the at least one electrode and the substrate
Claim 2	

2	The method of claim 1, wherein the thermally treating crystallizes, at least in part, the passivating film to establish a crystallized passivating film.
Claim 3	
3	The method of claim 2, wherein the crystallized passivating film is a transparent film.
Claim 4	
4	The method of claim 2, wherein the crystallization of the passivating film improves a passivation of the passivating film.
Claim 5	
5	The method of claim 2, wherein the interface passivation layer protects the substrate from crystallization or re-crystallization during the thermally treating and crystallization of the passivating film.
Claim 6	
6	The method of claim 1, wherein the interface passivation layer has a thickness selected to permit tunneling of electrical carriers through the interface passivation layer into the substrate
Claim 7	
7	The method of claim 1, wherein the thermally treating diffuses a portion of the conductive dopant through the interface passivation layer into the substrate.
Claim 8	
8	The method of claim 1, further comprising providing an anti-reflective film over the conductive upper surface of the passivating film.
Claim 9	
9	The method of claim 1, wherein the at least one electrode only electrically connects to the substrate through the passivating film via the conductive dopant

I. INTRODUCTION

1. My name is Sanjay Banerjee. I have been retained by Petitioner Mundra Solar PV Limited (collectively, "Mundra" or "Petitioner") to provide expert opinions with respect to U.S. Patent No. 9,666,732 (the "'732 Patent"), which I understand is assigned to Patent Owner First Solar, Inc. ("First Solar" or "Patent Owner").

2. I am being compensated at my standard consulting rate for my time, plus reasonable out-of-pocket expenses. I have received no additional compensation for my work in this matter, and my compensation does not depend upon the content of my opinions, any testimony that I may provide, or the ultimate outcome of the matter. All opinions set forth in this declaration are my own.

II. BACKGROUND AND QUALIFICATIONS

3. Full descriptions of my educational background, professional work, qualifications, and publications are set forth more fully in my curriculum vitae, which is attached to this declaration as Exhibit 1004. Here, I provide a summary of my background and qualifications.

4. I currently serve as the Cockrell Family Regents Chair Professor of Electrical and Computer Engineering. I was also the Director of the Microelectronics Research Center at the University of Texas at Austin ("UT") from September 1999 to January 2025. Prior to this position, I was first an Assistant

Professor (September 1987 - August 1990) and later an Associate Professor (September 1990 - August 1993) at UT, before being named a Professor in September 1993. Prior to starting my academic work at UT, I was a member of the technical staff at Texas Instruments (Corporate R&D) from the time I completed my doctoral studies in 1983 until August 1987.

5. I received my Ph.D. in Electrical Engineering from the University of Illinois in 1983. I also received an M.S. in Electrical Engineering from the University of Illinois in 1981. I received a B. Tech. in Electronics from the Indian Institute of Technology at Kharagpur in 1979.

6. I have more than 40 years of experience in the field of electrical engineering, including extensive experience in semiconductor development and fabrication including that of solar cells, passivation, and dielectric materials, including more than 15 years of experience in the field of silicon solar cells. For example, I am a named author on 24 publications and conference proceedings relating to solar cells, as can be seen from my curriculum vitae, which include:

(1) "Neural Network Modeling of Degradation of Solar Cells," Gupta H., Ghosh B., Banerjee S.K., Conference Information: International Conference on Enabling Science and Nanotechnology, DEC 01-03, 2010 Kuala Lumpur City Ctr, Kuala Lumpur, MALAYSIA ENABLING

SCIENCE AND NANOTECHNOLOGY Book Series: AIP Conference Proceedings Volume: 1341 Pages: 249-253 Published: 2011;

(2) “Monocrystalline Si solar cell technology,” R. Rao, L. Mathew, S. Saha, E. Oneyagam, D. Jawarani, J. Fossum and S. Banerjee, 37th IEEE Photovoltaic Specialists Conf. Washington DC. July 2011;

(3) “Novel low cost 25 micron thin exfoliated monocrystalline Si solar cell technology,” R. Rao, L. Mathew, S. Saha,. D. Jawarani, E. Oneyagam, S. Banerjee and J. Fossum, European PVSC, Hamburg, Germany, Sept. 2011;

(4) Exfoliated Thin, Flexible Monocrystalline Germanium Heterojunction Solar Cells., E. U. Onyegam, D. Sarkar, M. Hilali, S. Saha, R.A. Rao, L. Mathew, D. Jawarani, S. Smith, S.K. Banerjee, 38th IEEE PVSC 2012, Austin, TX;

(5) Remote Plasma Chemical Vapor Deposition for High Efficiency Ultra Thin ~25 Microns Crystalline Si Solar Cells, D. Sarkar, E. U. Onyegam, S. Saha, A. Rao, L. Mathew, R.S. Smith, D. Xu, D. Jawarani, R. Garcia, S.K. Banerjee, Presented at 38th IEEE PVSC 2012, Austin, TX;

(6) “A Low-Cost Kerfless Thin Exfoliated Si Solar Cell Technology,” R. Rao, L. Mathew, D. Sarkar, S. Smith, S. Saha, R. Garcia, R. Stout, A.

Gurmu, M. Ainom, E. Onyegam, D. Xu, D. Jawarani, U. Das, S. Banerjee, J. Fossum, Presented at 38th IEEE PVSC 2012, Austin, TX;

(7) "A Novel Low-Cost ~25μm-Thin Monocrystalline Silicon Bifacial Solar Cell Technology with Flexible and Rigid Form-Factor and Electroplated Contacts," L. Mathew, R. Rao, D. Sarkar, S. Banerjee, D. Jawarani, J. Fossum, R. Garcia, S. Smith, D. Xu, M. Ainom, E. Onyegam, R. Stout, S. Saha, A. Gurmu, Presented at 38th IEEE PVSC 2012, Austin, TX;

(8) "Integration and Reliability of Ultrathin Silicon Solar Cells and Modules Fabricated using SOM Technology," D. Jawarani, D. Xu, R. S. Smith, R. S. A. Rao, L. Mathew, S. Saha, D. Sarkar, C. Vass, S. K. Banerjee, P. S. Ho, 38th IEEE PVSC, June, 2012;

(9) "Integration and Reliability of Thin Silicon Solar Cells and Modules Fabricated using SOM® Technology," D. Jawarani, D. Xu, R. S. Smith, S. Saha, R. S. A. Rao, L. Mathew, D. Sarkar, E. U. Onyegam, M. Ainom, R. S. Garcia, A. Gurmu, R. S. Stout, C. Vass, S. K. Banerjee, P. S. Ho, J. G. Fossum, 27th EU PVSEC, September 2012;

(10) L. Mathew, R.-A. Rao, S. Saha, S. Smith, R. Garcia, R. Stout, A. Gurmu, M. Ainom, D. Xu, D. Jawarani, D. Sarkar, J. Fossum, E. Onyegam, S. Banerjee, "A Novel Low Cost ~25μm Thin Monocrystalline Silicon Bi-

Facial Solar Cell Technology with Flexible and Rigid Form-Factors and Electroplated Contacts," EU PVSC, 2012, Germany;

(11) Mohamed M Hilali, Shuqiang Yang, Mike Miller, Frank Xu, Sanjay Banerjee and S. V. Sreenivasan, "Enhanced photocurrent in thin-film amorphous silicon solar cells via shape controlled three-dimensional nanostructures," Nanotechnology 23 405203, September 2012;

(12) "Exfoliated, thin, flexible germanium heterojunction solar cell with record FF=58.1%," Onyegam, EU; Sarkar, D; Hilali, M; Saha, S; Rao, RA; Mathew, L; Jawarani, D; Mantey, J; Ainom, M; Garcia, R; James, W;Banerjee, S. K., Solar Energy Materials and Solar Cells, Volume: 111 Pages: 206-211, April 2013;

(13) "Single heterojunction solar cells on exfoliated flexible similar to 25 μm thick mono-crystalline silicon substrates," Saha, S; Hilali, MM; Onyegam, EU; Sarkar, D; Jawarani, D; Rao, RA; Mathew, L; Smith, RS; Xu, DW; Das, UK; Sopori, B; Banerjee, Sanjay K, APL, Volume: 102, Issue: 16, 2013;

(14) "A Novel Low-Cost Method for Fabricating Bifacial Solar Cells," S. Saha, R. A. Rao, L. Mathew, M. Ainom and S. K. Banerjee, PVSC, 2013;

(15) "Improved Cleaning Process for Textured similar to 25 μm Flexible Mono-Crystalline Silicon Heterojunction Solar Cells with Metal Backing,"

Saha, Sayan; Hilali, Mohamed M.; Onyegam, Emmanuel U.; S.K.Banerjee, ECS Journal Of Solid State Science And Technology, Volume: 3 Issue: 7 Pages: Q142-Q145 Published: 2014;

(16) “Realization of dual-heterojunction solar cells on ultra-thin similar to 25 μm, flexible silicon substrates,” Onyegam, Emmanuel U.; Sarkar, Debraj; Hilali, Mohamed M.; Banerjee, S.K.; Applied Physics Letters, Volume 104, Issue 15 Article Number: 153902 April 14 2014;

(17) “Light trapping in ultrathin 25 μm exfoliated Si solar cells,” Hilali, Mohamed M.; Saha, Sayan; Onyegam, Emmanuel; Rao, Rajesh; Mathew, Leo; Banerjee, S.K., Applied Optics, Volume: 53 Issue: 27 Pages: 6140-6147 September 20, 2014;

(18) “2D Materials Synthesis and Graphene Thinned Silicon Solar Cell,” Harry Chou, Jae Hyun Ahn, Rudresh Ghosh, Ariel Ismach, Xiaohan Wang, Yufeng Hao, Luigi Colombo, Rodney Ruoff, and Sanjay K. Banerjee, SRC Techcon 2016;

(19) “Graphene-Al2O3-silicon heterojunction solar cells on flexible silicon substrates”, J. Ahn, H Chou, S.K. Banerjee, Journal of Applied Physics 121 (16), 163105, 2017;

(20) "Progress in Materials Development for the Rapid Efficiency Advancement of Perovskite Solar Cells," W. Chi and S.K. Banerjee, Small, May 2020.

(21) "Stability Improvement of Perovskite Solar Cells by Compositional and Interfacial Engineering," W. Chi, S.K. Banerjee, Chemistry of Materials, v.33 (2021).

(22) "Development of perovskite solar cells by incorporating quantum dots," W. Chi, S. K. Banerjee, Chemical Engineering Journal, 131588, 2021.

(23) "Achieving Resistance against Moisture and Oxygen for Perovskite Solar Cells with High Efficiency and Stability," W. Chi, S.K. Banerjee, Chemistry of Materials, 2021.

7. I am a Fellow of the Institute of Electrical and Electronics Engineers ("IEEE"), the American Physical Society ("APS"), and the American Association for the Advancement of Science ("AAAS"). I have served on numerous professional and government committees in the electrical engineering field, including chairing multiple IEEE committees, meetings, and programs, serving on Morgan & Claypool's editorial board, and serving as a member on the International Technology Roadmap for Semiconductors ("ITRS").

8. I have taught courses in Semiconductor Physics, Solid State Electronic Devices, and Microelectronic Device Fabrication at UT. In particular, I have taught an undergraduate course every year for 30 years on Semiconductor Devices out of a textbook, "Solid State Electronic Devices," by Ben Streetman and Sanjay Banerjee (ISBN 0-13-335603). Several of my lectures out of the textbook relate to solar cells. In addition, I have delivered many courses to industry professionals on Semiconductor Devices and Memory and Semiconductor Processing. As a principal investigator, I have been the advisor to over 80 Doctoral and Masters students.

9. I am the co-author of several books and invited book chapters covering the area of electronic and semiconductor devices, including: Dopant Diffusion, Solid State Electronic Devices (three editions). I have authored or coauthored more than 1,000 papers and presentations in the areas of semiconductor devices and electronics development over the course of my career.

10. I have been the recipient of fifty grants to fund my research from a variety of funding agencies, including the National Science Foundation ("NSF"), DARPA, the Department of Energy, Semiconductor Research Corporation, the Department of Defense-Multidisciplinary University Research Initiative, and the Office of Naval Research. A number of the sponsored research grants on which I have been a principal or coinvestigator have related to solar cells and various deposition techniques for optoelectronic devices, including for example,

"Optoelectronic Devices by Photo-enhanced Chemical Vapor Deposition," (National Science Foundation, August 1988-July 1993), and "Bay Area PV Consortium led by Stanford/Berkeley," (Department of Energy, September 2015-August 2017).

11. I have received numerous other awards recognizing my extensive work in the electrical engineering field. For example, I was on the Advisory Board, and the Silicon Solar Cell Thrust Lead for the Bay Area Photovoltaics Consortium funded by the U.S. Department of Energy. This and other awards are described in more detail in my curriculum vitae. I have served on the Technical Advisory Board of two solar cell startups, AstroWatt and Applied Novel Devices.

12. As a result, I am thoroughly familiar with the theory, practice, and history of the technology described and claimed in the '732 patent.

III. LEGAL UNDERSTANDING

13. I am not a lawyer and am not providing any legal opinions. In providing my opinions in this declaration, I am relying upon certain basic legal principles that have been explained to me by counsel and which I am summarizing below.

14. First, I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious from what was known before the invention was made.

15. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as "prior art" and generally includes patents and printed publications (e.g., books, journal publications, articles on websites, product manuals, etc.).

16. I understand that in this proceeding the Petitioner has the burden of proving that the claims are anticipated by or obvious from the prior art by a preponderance of the evidence. I understand that "a preponderance of the evidence" is evidence sufficient to show that a fact is more likely true than it is not.

17. I understand that in this proceeding, the claims should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. The claims after being construed in this manner are then to be compared to the information in the prior art.

18. I understand that in this proceeding, the information that may be evaluated is limited to patents and printed publications. My analysis below compares the claims to patents and printed publications that are prior art to the claims.

19. I understand that there are various ways in which prior art may render a patent claim unpatentable based on prior art patents and printed publications. First, the prior art can be shown to "anticipate" the claim. Second, the prior art can be

shown to have made the claim "obvious" to a person of ordinary skill in the art. My understanding of the legal standards is set forth below.

A. Anticipation

20. I understand that the following standards govern the determination of whether a patent claim is "anticipated" by the prior art.

21. I have applied these standards in my evaluation of whether the claims would have been anticipated by the prior art.

22. I understand that the "prior art" includes patents and printed publications that existed before the earliest filing date (the "effective filing date") of the claim in the patent. I also understand that a patent will be prior art if it was filed before the effective filing date of the claimed invention, while a printed publication will be prior art if it was publicly available before that date.

23. I understand that, for a patent claim to be "anticipated" by the prior art, each and every requirement of the claim must be found, expressly or inherently, in a single prior art reference as recited in the claim. I understand that claim limitations that are not expressly described in a prior art reference may still be there if they are "inherent" to the thing or process being described in the prior art. I understand that a limitation can be "inherent" if that limitation is necessarily present in or the natural result of the elements explicitly disclosed by the prior art.

24. I understand that if a reference incorporates other documents by reference, the incorporating reference and the incorporated reference(s) should be treated as a single prior art reference for purposes of analyzing anticipation.

25. I understand that it is acceptable to consider evidence other than the information in a particular prior art document to determine if a feature is necessarily present in or inherently described by that reference.

B. Obviousness

26. I understand that a claimed invention is not patentable if it would have been obvious to a person of ordinary skill in the field of the invention at the time the invention was made.

27. I understand that the obviousness standard is defined in the patent statute (35 U.S.C. § 103(a)[1]) as follows:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art

[1] I understand from counsel that the versions of 35 U.S.C. §§ 102 & 103 enacted prior to the America Invents Act ("AIA") apply to these proceedings (i.e., "pre-AIA" 102 and 103).

> to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

28. I understand that the following standards govern the determination of whether a claim in a patent is obvious. I have applied these standards in my evaluation of whether the claims would have been considered obvious as of the priority date of the patent.

29. I understand that to find a claim in a patent obvious, one must make certain findings regarding the claimed invention and the prior art. Specifically, I understand that the obviousness question requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;
- The differences between the prior art and the claims at issue;
- The knowledge of a person of ordinary skill in the pertinent art; and
- Whatever objective factors indicating obviousness or non-obviousness may be present in any particular case.

30. In addition, I understand that the obviousness inquiry should not be done in hindsight, but must be done using the perspective of a person of ordinary skill in the relevant art as of the effective filing date of the patent claim.

31. I understand the objective factors indicating obviousness or non-obviousness may include: commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the

invention; copying of the invention by others in the field; unexpected results achieved by the invention; praise of the invention by those in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the patentee proceeded contrary to the accepted wisdom of the prior art. I also understand that any of this evidence must be specifically connected to the invention rather than being associated with the prior art or with marketing or other efforts to promote an invention. I am not presently aware of any evidence of "objective factors" suggesting the claimed methods are not obvious, and reserve my right to address any such evidence if it is identified in the future.

32. I understand the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I understand that when the prior art does not expressly disclose a claim limitation, inherency may also supply a missing claim limitation in an obviousness analysis. I understand that inherency is established in the context of obviousness when the limitation at issue necessarily must be present, or the natural result of the combination of elements explicitly disclosed by the prior art. I also understand that an example of a solution in one field of endeavor may make that solution obvious in another related field. I also understand that market demands or design considerations may prompt variations of a prior art system or process, either in the

same field or a different one, and that these variations will ordinarily be considered obvious variations of what has been described in the prior art.

33. I also understand that if a person of ordinary skill can implement a predictable variation, that variation would have been considered obvious. I understand that for similar reasons, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using that technique to improve the other device would have been obvious unless its actual application yields unexpected results or challenges in implementation.

34. I understand that the obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, but instead can take account of the "ordinary innovation" and experimentation that does no more than yield predictable results, which are inferences and creative steps that a person of ordinary skill in the art would employ.

35. I understand that sometimes it will be necessary to look to interrelated teachings of multiple patents/publications; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art. I understand that all these issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

36. I understand that the obviousness analysis cannot be confined by a formalistic conception of the words "teaching, suggestion, and motivation." I understand that in 2007, the Supreme Court issued its decision in *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, where the Court rejected the previous requirement of a "teaching, suggestion, or motivation to combine" known elements of prior art for purposes of an obviousness analysis as a precondition for finding obviousness. It is my understanding that KSR confirms that any motivation that would have been known to a person of skill in the art, including common sense, or derived from the nature of the problem to be solved, is sufficient to explain why references would have been combined.

37. I understand that a person of ordinary skill attempting to solve a problem will not be led only to those elements of prior art designed to solve the same problem. I understand that under the KSR standard, steps suggested by common sense are important and should be considered. Common sense teaches that familiar items may have obvious uses beyond the particular application being described in a reference, that if something can be done once it is obvious to do it multiple times, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents/publications together like pieces of a puzzle. As such, the prior art considered can be directed to any need or problem known in the field of endeavor and can provide a reason for combining the elements of the prior art in the manner

claimed. In other words, the prior art does not need to be directed towards solving the same problem that is addressed in the patent. Further, the individual prior art references themselves need not all be directed towards solving the same problem.

38. I understand that obviousness does not require that the features of a secondary reference be bodily incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of those references would have suggested to a Skilled Artisan. The disclosures of the prior art references need not be physically combinable. Combining the teachings of references should be the focus of the analysis.

39. I understand that an invention that might be considered an obvious variation or modification of the prior art may be considered non-obvious if one or more prior art references discourages or leads away from the line of inquiry disclosed in the reference(s). A reference does not "teach away" from an invention simply because the reference suggests that another embodiment of the invention is better or preferred. My understanding of the doctrine of teaching away requires a clear indication that the combination should not be attempted (e.g., because it would not work or explicit statements saying the combination should not be made).

40. I understand that a person of ordinary skill is also a person of ordinary creativity.

41. I further understand that in many fields, it may be that there is little discussion of obvious techniques or combination, and it often may be the case that market demand, rather than scientific literature or knowledge, will drive design trends. When there is such a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within their technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious. The fact that a particular combination of prior art elements was "obvious to try" may indicate that the combination was obvious even if no one attempted the combination. If the combination was obvious to try (regardless of whether it was actually tried) or leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than innovation.

IV. SUMMARY OF INVALIDITY GROUNDS

42. I understand that Petitioner requests *inter partes* review of Claims 1-9 of the '732 Patent based on the following grounds:

Ground	**Claims**	**Statute**	**Prior Art**
1	1-4 and 6-9	35 U.S.C. § 103	Yablonovitch, Kwark
2	5		Yablonovitch, Kwark, Batra

V. TECHNICAL BACKGROUND

A. Solar Cells, PN Junctions, and Doping

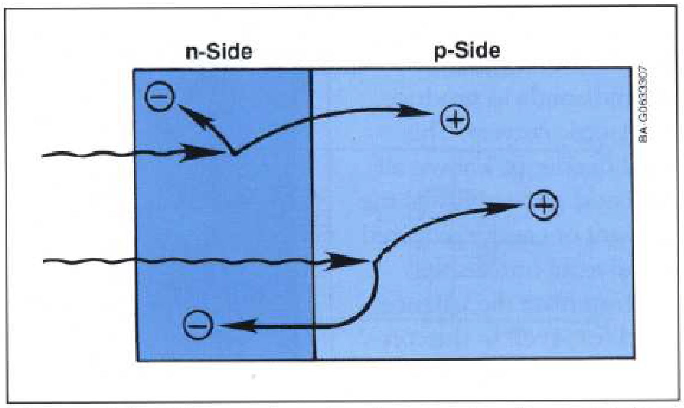
43. Solar cells fundamentally operate based on the photovoltaic effect, which describes how when photons of light strike a photovoltaic cell, the energy of a given photon is transferred to an electron in an atom of a semiconductor, which allows the atom to escape from its normal position within the atom and become part of electrical current. In order to collect this electric current as electricity, PV cells use a built-in electric field to provide the voltage needed to drive the current through an external load. This is done using a p-n junction formed by a p-type semiconductor region and an n-type semiconductor region. *See* G. Cook, *et al.*, "Photovoltaic Fundamentals" (1991) ("Cook")(Ex. 1023).

44. The electric field is created by doping the silicon. Doping involves intentionally introducing impurity atoms into the semiconductor crystal lattice to alter its electrical properties. For instance, adding Group V elements like phosphorus to silicon creates an excess of free electrons, resulting in an n-type semiconductor. Conversely, introducing Group III elements like boron leads to an excess of "holes" (vacant electron states), forming a p-type semiconductor. The interface formed when p-type and n-type semiconductor regions are joined is known as a p-n junction. *See* Cook, pp. 12-13. As a result, "[t]he electric field drives

positive and negative charges in opposite directions. The movement of charge carriers (through an external circuit) is what defines electricity." *Id*.

45. Specifically, a p-n junction formed by a p-type semiconductor region and an n-type semiconductor region builds an intrinsic electric field because the electrons in the n-region diffuse to the p-region, while holes from the p-region diffuse to the n-region. The electrons and holes recombine, thereby exposing immobile positively charged donors on the n-side and negatively charged acceptors on the p-side in a depletion region. This causes a build-up of opposite charges at the interface of the p-n junction (see forming of "+" and "-" at the junction in images below). Cook, pp. 14-15. As a result, "[a]t equilibrium, when all the charge carriers have settled down again, a net charge concentration exists on each side of the junction. This overpopulation of opposite charges creates an electric field across the interface." *Id*.

46. As a result of the electric field, as shown below, "[w]hen sunlight striking a cell creates charge carriers, the electric field pushes new electrons to one side of the junction and new holes to the other. This sorting-out process is what drives the charge carriers in an electric circuit." Cook, p. 15.



Cook, p. 15

47. Thus, the PV cell's foundational operation generate electrons and holes from photons, and collect the electrons at the n-type semiconductor region and the holes at the p-type semiconductor region, which generates electricity.

B. Recombination

48. As has been recognized as textbook level knowledge for many decades (for example in Cook 1991), if a generated electron and hole "recombine" before they are collected as current, they "contribute nothing to an electrical current." Cook 1991, p. 15. As a result, the solar cell is less efficient.

49. A known way to increase solar cell efficiency is to increase the number of electrons and holes exiting through the electrodes by preventing them from "recombining" before exiting. "Recombination" happens when an electron freed by a photon collides with (and fills) a hole before reaching an electrode, preventing both the electron and hole from contributing to the output current and reducing efficiency.

One well known mechanism of recombination is "surface recombination," whereby electrons or holes recombine at surfaces or interfaces between different materials, though other recombination mechanisms exist. In surface recombination, broken bonds at the surface of the silicon substrate or its interface with many other materials (e.g., metals) introduce defect states for recombination.

C. Passivation by Polysilicon and Thin Oxides

50. Passivation refers to the treatment of a material's surface to make it chemically stable and to reduce unwanted reactions or defects. By sweeping electrons and holes away from the device surfaces, the field increases the likelihood that carriers contribute rather than being lost. Polycrystalline silicon (polysilicon) is a semiconductor material composed of numerous small crystalline grains. Its electrical properties are highly dependent on its grain structure, size, and dopant concentration. A specific variant, Semi-Insulating Polycrystalline Silicon (SIPOS), is essentially polysilicon, but additionally incorporates oxygen. SIPOS and polysilicon were widely utilized as passivation films in silicon solar cells due to their unique microstructure and semi-insulating properties. (See, for example, Cook 26 ("[e]ven very small crystals of silicon make successful solar cells").

51. A high-temperature treatment or "anneal" is essential for activating dopants by incorporating them into substitutional lattice sites, and for crystallizing SIPOS and polysilicon films. During annealing, amorphous or fine-grained silicon

within the deposited SIPOS/polysilicon layer undergoes crystallization and grain growth, leading to the precipitation and enlargement of silicon microcrystalline grains Also during annealing, a thin interfacial oxide layer can be formed by diffusion of oxygen from the SIPOS film to the SIPOS-Si interface, where they react with Si atoms at the surface leading to the formation of interfacial SiO_2. There is also often a native oxide or adventitious oxygen on the surface of the Si wafer on which SIPOS, polysilicon or amorphous Si is deposited. These oxygen atoms at the interface can also lead to formation of an interfacial oxide upon heat treatment of the sample.

52. Interfacial oxides were well-known for their advantageous passivation qualities, including their ability to significantly reduce surface recombination at the surface of silicon. The impact of this interfacial oxide on both majority and minority carrier transport was well documented before the relevant time.

VI. THE ’732 PATENT

A. Effective Filing Date of the ’732 patent

53. I have been asked to assume that the earliest possible priority date for the ’732 patent is April 21, 2009, which I understand is the filing date of the provisional application No. 61/171,194 listed on the face of the ’732 patent. I have therefore analyzed the prior art as of that date.

B. Overview of the ’732 patent

54. The ’732 patent is entitled “High-efficiency Solar Cell Structures and Methods of Manufacture.” The ’732 patent includes nine claims: independent claim 1 (which is a method claim) and eight dependent claims (claims 2–9). The ’732 patent is generally directed to processes for manufacturing a solar cell composed of a substrate, conductive layer(s), antireflection layer(s), passivation layer(s), and electrode(s). ’732 patent, Abstract, 1:46-2:31.

55. The ’732 patent purports that these layers “provide combined functions of passivation, transparency, sufficient conductivity for vertical carrier flow, the junction, and/or varying degrees of anti-reflectivity.” ’732 patent, Abstract, 1:46-57. The ’732 patent also describes an objective of “improved manufacturing methods including single-side CVD deposition processes and thermal treatment for layer formation and/or conversion.” ’732 patent, 1:54-57. The ultimate object of the ’732 patent is to create “solar cells which attain high operational efficiency, and which can be manufactured in a cost effective manner.” ’732 patent, 1:39-41.

56. The ’732 patent states that “[t]he present invention includes methods of fabricating” several examples of various structures that generally include: “providing a wafer as a central substrate; deposition or growth of interface passivation layers xx4 and xx6 over the substrate; deposition of conductive layers xx3 and xx7 over the passivation layers: providing thermal treatment; optional

deposition of antireflective layers xx2 and xx8 (including possibly a low reflective index layer for a good internal mirror on the back); and providing metallization as electrodes." '732 patent, 18:46-54.

57. For example, Figure 6 shows a solar cell structure which contains a "n- or p-type wafer 65", "Electrically passivating interface layer" 64 and 66, "Electrically passivating and conductive film" layers 63 and 67, "transparent and conductive film" layers 62 and 68, "front metal electrode" 61 and "back metal electrode" 69. '732 patent, 5:14-6:25, FIG. 6.

58. The '732 patent also describes that "a heat treatment" may cause a film to "separate[] into a surface passivating interface layer and a highly doped polycrystalline passivation layer with high transparency." '732 patent, 1:66-2:3, 16:53-17:11 ("a layer deposited in a single process can split into two (or more) layers" when "incorporated oxygen in the amorphous deposited layer migrates toward the silicon interface and a thin oxide can be grown").

59. The '732 patent does not explicitly define an "electrically passivating interface layer" but describes several options for such a layer, including "silicon oxide, silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon, aluminum oxide, aluminum nitride, phosphorus nitride, titanium nitride." '732 patent, 5:61-66, 6:5-11.

60. Similarly, the ’732 patent does not explicitly define an “electrically passivating and conductive film” but provides a broad range of options, including “n-type amorphous or polycrystalline silicon carbides,” “n-type amorphous or polycrystalline silicon,” and “n-type amorphous or poly-crystalline diamond-like-carbon.” ’732 patent, 5:47-58, 6:12-24.

C. The Prosecution History

61. On April 13, 2016, the Examiner issued a Non-Final Rejection of the pending independent claim under pre-AIA 35 U.S.C. § 103(a) based on U.S. Patent No. 6,821,875 (“Wenham”) in view of WO2007/125903A1 (“Fukushima”), which were both included in Applicant’s IDS filed August 19, 2015. Prosecution History, 239. The Examiner relied on Fukushima as teaching “providing at least one electrode over the passivating film.” *Id.,* 240.

62. On July 13, 2016, the Applicant responded to the Non-Final Rejection by amending the pending independent claim to include the following limitations:

> wherein providing the interface passivation layer and providing the passivating film comprise:
>
> > providing an amorphous silicon-containing compound over an upper surface of the substrate, the compound comprising oxygen dopant and the conductive dopant;
> >
> > diffusing the oxygen dopant, at least in part, into the upper surface of the substrate to form an oxide layer over the substrate, the oxide layer defining the interface passivation layer; and

> wherein remaining amorphous silicon-containing compound above the oxide layer defines the passivating film.

Prosecution History, 264.

63. On August 26, 2016, the Examiner issued a second Non-Final Rejection under pre-AIA 35 U.S.C. § 112. Prosecution History, 306.

64. The Examiner noted that the pending independent method claim required a "thermally treating" step involving diffusion of the "conductive dopant" "throughout the interface passivation layer." Further, the Examiner noted the oxygen diffusion step formed the "the oxide layer defining the interface passivation layer," but was a separate step to the "thermally treating" step. The Examiner found that the specification teaching of the oxygen diffusion step (which I referred to above as '732 patent at 16:53-17:11) taught that the oxygen diffusion and conductive dopant diffusion were part of the same thermal treating step. Thus, according to the Examiner, the temporal relationship between the interface passivation layer and the thermal treating step was unclear in light of the specification. Prosecution History, 308.

65. On November 28, 2016, the Applicant responded to the Non-Final Rejection by amending the pending independent claim primarily to recite that it is the "thermally treating" that diffuses the oxygen dopant. Prosecution History, 323

66. On January 30, 2017, a Notice of Allowance was issued by the Examiner. Prosecution History, 337. The patent issued on May 30, 2017. Prosecution History, 355.

VII. LEVEL OF ORDINARY SKILL IN THE ART

67. I am familiar with the level of ordinary skill in the art regarding the ’732 patent as of around April 21, 2009. Considering the ’732 patent, the technology, the educational level and experience of workers in the field relating to the patent, and problems and solutions in that field, and drawing on my own experience, I believe the person of ordinary skill in the art in the ’732 patent’s field of solar cell design or manufacture by 2009 (“POSITA”) would have been someone with a bachelor’s degree involving the disciplines of electrical engineering, applied physics, chemistry, or materials science, and at least two years of experience designing, developing, or researching in the field. Alternatively, a person with less formal education but additional relevant practical experience, or vice versa, would also qualify as a person of ordinary skill in the art. By that definition, I was a POSITA before April 21, 2009, the earliest purported effective filing date of the ’732 patent.

68. My opinions in this Declaration regarding the ’732 patent and the prior art (including the state of the art) are from the perspective of one of ordinary skill in

the art as I defined above, during the relevant timeframe (the time of the alleged invention), which I discussed above as being around April 21, 2009.

VIII. CLAIM CONSTRUCTION

69. I understand that when considering the meaning of patent claims, one must consider the language of the claims, the specification, and the prosecution history of the patent. I also understand that claim terms are typically given their ordinary and customary meanings as would have been understood by a person of ordinary skill in the art at the time of the invention for the patent. For the '732 patent, as I explained above in Section VI, the relevant time that I have been asked to consider is around April 21, 2009. For purposes of my opinions in this declaration, I have been asked to consider the challenged claims under their plain and ordinary meanings as understood by a person of ordinary skill in the art at the time of the alleged invention in context of the '732 patent as I discussed above, and I have applied such understandings in my analysis of the '732 patent and the prior art.

IX. OVERVIEW OF THE PRIOR ART

A. Yablonovitch (Ex. 1005)

70. Yablonovitch, entitled "A 720 mV open circuit voltage SiO_x:*c*-Si:SiO_x double heterostructure solar cell", is a scientific article published in *Applied Physics Letters,* a peer-reviewed scientific journal, that was available as of December 1, 1985. *See* Yablonovitch at 1. I understand that Yablonovitch thus qualifies as prior art under at least 35 U.S.C. § 102(a) and (b).

71. Yablonovitch is in the field of solar cell design. As shown below in Table II, Yablonovitch discloses the processing sequence (i.e., method of fabrication) for the double heterostructure solar cell. Yablonovitch, Table II.

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2.
5. Ramp up to 650 °C while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2.
7. Deposit SIPOS from 1000 ppm SiH_4, 50 ppm PH_3, and 10 ppm O_2.
8. Ramp furnace to 900 °C.
9. Anneal for 15 min.
10. Ramp furnace down to 450 °C.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

Yablonovitch, Table II

72. Yablonovitch teaches that for maximal performance, solar cells are like semiconductor lasers: in the form of a double heterostructure. Yablonovitch, 1211. Though wide band-gap heterocontact layers may be single crystal and lattice matched to assure high performance, Yablonovitch notes that such layers are needed only to "be of sufficient electronic quality to support the quasi-Fermi level separation in the high quality narrow-gap active layer." *Id.,* 1211. Further, due to the larger band gap, there may be quality and disorder issues in the active layer. *Id.,* 1211. Additionally, the interface states at the heterocontacts must be passivated. *Id.,* 1211.

73. Figure 3 below shows the wafer as the base for other layers during fabrication of the solar cell. Yablonovitch, Fig. 3.

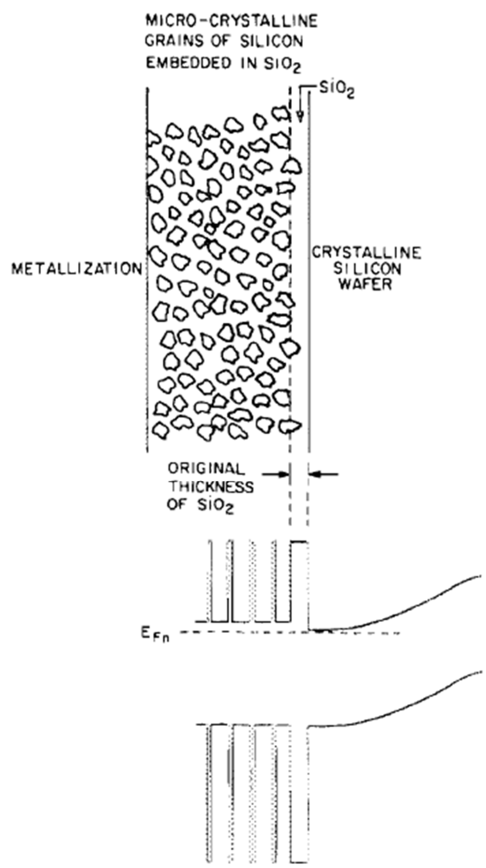


FIG. 3. Model for the metallurgical configuration of the SIPOS-Si heterojunction. Electron conduction is thought to proceed via the microcrystalline grains which protrude into the thin oxide layer.

Yablonovitch, FIG. 3

74. Further, Figure 2 shows the test configuration of the semiconductor structure for the solar cell.

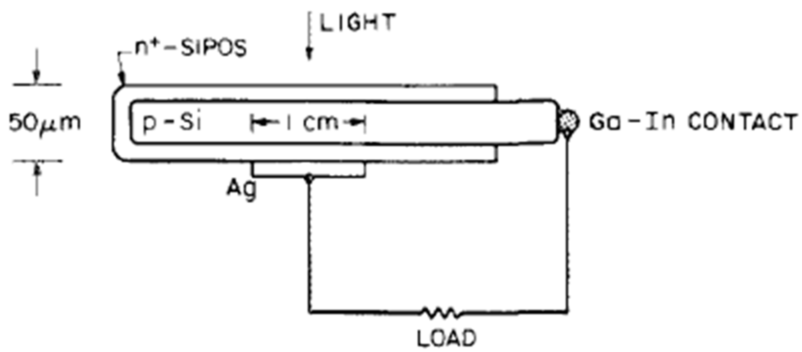


FIG. 2. Test configuration for the SIPOS : *c*-Si : SIPOS double heterostructure solar cells. In this design the fill factor was limited by the bulk resistance of the *p*-Si wafer itself.

Yablonovitch, FIG. 2

75. Furthermore, Yablonovitch teaches that since crystalline silicon has no useful lattice-matched heterocontacts, that SIPOS (semi-insulating polycrystalline silicon) is considered as a disordered semiconductor heterojunction material. Yablonovitch, 1211. SIPOS provides "superior" passivation, preventing electrons and holes from recombining, while allowing current to flow where needed. *Id.* As such, Yablonovitch teaches a design with better light trapping with 24-25% efficiency. Yablonovitch, 1213.

76. In addition, the use of thin interfacial SiO_2 layers further passivates the interface, minimizing the recombination and improving overall device performance. Yablonovitch, 1213. Thus, Yabolonovitch recognizes that thin interfacial SiO_2

passivate the interface of SIPOS and crystalline silicon. These teachings provide a foundation for interface passivation and dopant diffusion techniques.

B. Kwark (Ex. 1017)

77. Kwark, entitled "SIPOS heterojunction contacts to silicon", is a doctoral dissertation published in 1984. I understand that Kwark qualifies as prior art under at least 35 U.S.C. § 102(a) and (b). *See* Kwark, Cover.

78. Kwark is in the field of solar cell design. *See* Kwark, Abstract.

79. Kwark explains the presence or absence of an interfacial chemical oxide, as well as the thermal treatment, impacts the reverse saturation current, J_{oe}, which impacts cell efficiency. *Id.*, 95. Further, Kwark explains that the physical properties and phenomenon that result in carrier transport properties in relation to oxide thickness described by Yablonovitch in greater detail. *Id.,* 171. Kwark teaches how SIPOS with an interfacial oxide can yield solar cells with high open circuit voltage and efficiency alongside insight for implementing complex interface design considerations to optimize the thin oxide used in solar cells. *Id.,* 178.

80. More specifically, Kwark discloses the use of lower oxygen content Semi-Insulating Polycrystalline Silicon (SIPOS) films whose lower bulk resistivities would allow utilization of these films in structures such as scaled VLSI bipolar devices and high concentration point contact solar cells where series resistance is detrimental to device performance. *Id.,* 62. Kwark discloses "an interfacial layer

between the SIPOS and underlying silicon may play an important, if not dominant, role with the implication that the high oxygen concentrations previously used may not be essential for J_{0e} reduction." *Id.,* 121. Kwark Figure 7.19 further discloses that the SIPOS crystallizes during subsequent annealing instead of being crystallized as-deposited. Kwark, FIG. 7.19.

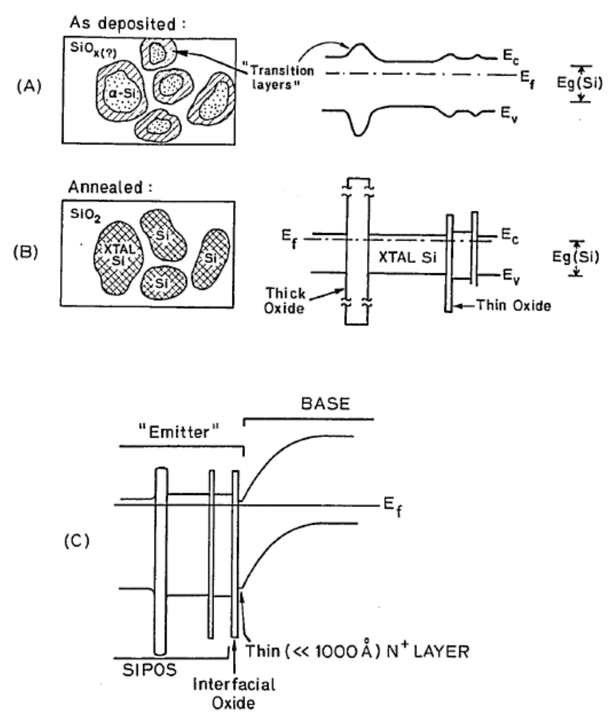


Figure 7.19: influence of annealing on SIPOS microstructure

Kwark, Figure 7.19

81. Many of the teachings of Kwark regarding SIPOS and interfacial oxides were published in peer-reviewed journals, including Kwark II – *SIPOS*

heterojunction contacts to silicon (Ex. 1018) – in 1984, and Kwark III – N-type SIPOS and poly-silicon emitters (Ex. 1019) – in 1987.

C. Batra (Ex. 1034)

82. Batra, entitled "Study of lateral non-uniformity and function of junction depth in ultra-shallow junctions and its effect on leakage behavior in as-deposited polycrystalline Si and Amorphous Si Diodes" is a scientific article published in July 1993 in *Solid-State Electronics,* a peer-reviewed scientific journal. *See* Batra, 955. I understand that Batra qualifies as prior art under at least 35 U.S.C. § 102(a) and (b). *See* Batra.

83. Batra is in the field of polycrystalline Si films, which are present in solar cells. Batra, 955.

84. Batra teaches that "heavily implanted polycrystalline Si films are finding increasing applications as solid diffusion sources." *Id.,* 955. As such, Batra explains the importance of determining the effect of the interface passivation layer ("SiO_2") on the substrate ("crystalline silicon wafer") during anneal. *Id.,* 955.

85. Batra's findings about nonuniformity in junctions apply to interface passivation layers given that Batra teaches how annealing changes the crystal structure and dopant distribution such that higher-temperature or longer anneals lead to a more uniform junction, which resolves the underlying problem of crystallization

or re-crystallization of the passivating film since the even dopant distribution reduces pn junction lateral non-uniformity. *Id.,* 955.

86. Batra's Figures 3 and 5 reproduced below illustrate that the crystallization of the Poly Si does not to create damage in the substrate and vice versa which a POSITA would understand is due to an interfacial oxide. *Id.,* Figs. 3, 5.

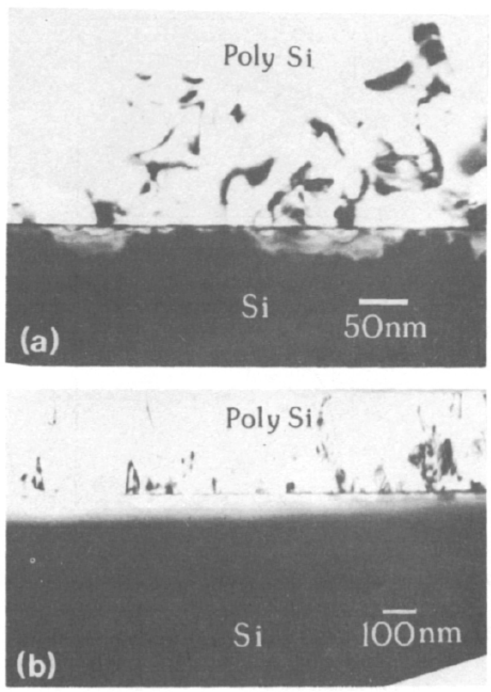


Fig. 3. XTEM micrographs of arsenic-implanted, (a) as-deposited amorphous Si; and (b) as-deposited polycrystalline Si films after at 60 s, 950°C RTA. A concentration-dependent etch was used to delineate the diffusion fronts.

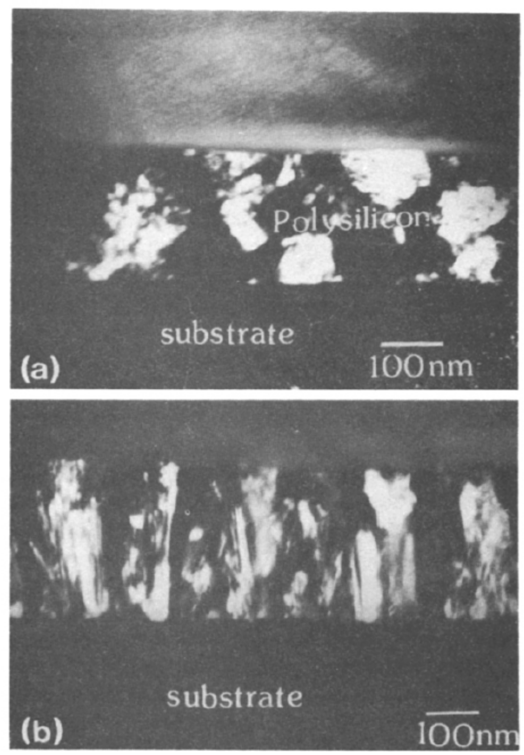


Fig. 5. XTEM micrographs of BF_2-implanted, (a) as-deposited amorphous Si, and (b) as-deposited polycrystalline Si films after a 60 s, 950°C RTA.

Batra, Figs. 3, 5

X. THE PRIOR ART DISCLOSES AND/OR SUGGESTS ALL RECITED FEATURES OF CLAIMS 1-9 OF THE ’732 PATENT

87. In my opinion, the prior art discussed below discloses and/or suggests the limitations of claims 1-9.[2]

A. Yablonovitch in View of Kwark Renders Obvious Claims 1-4 and 6-9

1. Combined Teachings of Yablonovitch in View of Kwark

a) Motivation to Combine Yablonovitch and Kwark

88. It is my opinion that a POSITA would have found it obvious to apply the teachings of Kwark to Yablonovitch. Yablonovitch and Kwark are analogous art because each is in the same field of endeavor as the ’732 patent—solar cell design. Ex. 1005 (Yablonovitch), Abstract, p. 1211; Ex. 1017 (Kwark), Introduction (pp. 1-5); ’732 patent, Abstract. Each is reasonably pertinent to the problems of efficiencies of solar cell designs. *Id*. Both Yablonovitch and Kwark address the critical role of the polysilicon/SIPOS interface with silicon substrates and thin interfacial oxides in controlling carrier transport and device efficiency. Further, an author of Yablonovitch – R.M. Swanson of Stanford Electronics Laboratories – was

[2] In this section (Section X), I refer to exhibits other than those identified prior art reference(s) that disclose and/or suggest the claimed limitations. Such exhibits reflect the state of the art known to a person of ordinary skill in the art at the time of the alleged invention.

the advisor of the Kwark thesis. *See* Ex. 1005 (Yablonovitch); Ex. 1017 (Kwark), p. iii.

89. The combination of Yablonovitch and Kwark requires no modification to Yablonovitch – Kwark's teachings supply details about the physical phenomenon occurring during Yablonovitch's process that, while understood by a POSITA, Yablonovitch omitted. A POSITA would have been motivated to look to Kwark to understand the physical phenomenon occurring during Yablonovitch's process, which would be necessary to determine implementation details and design considerations omitted from Yablonovitch. These considerations would have been important to a POSITA looking to implement and optimize Yablonovitch's process because others taught and understood that there were important design considerations for forming interfacial oxides that affected the performance of the solar cell.

90. Yablonovitch teaches a SIPOS-Si heterojunction and provides important explanation on the basic mechanism for interface passivation, explaining that "the interface states at the heterocontacts *must be passivated*." Yablonovitch, 1211. In order to do so, Yablonovitch teaches that for its solar cell design, "[t]he interface states between SIPOS and crystalline silicon (c-Si) seem to be passivated as well as the high quality interface between thermally grown SiO_2 and c-Si."

Yablonovitch, 1211. In other words, Yablonovitch recognizes that thin interfacial SiO_2 oxides passivate the interface of SIPOS and crystalline silicon.

91. Yablonovitch also recognizes that interfacial oxides "frequently occurs inadvertently," but does not explain the ways in which the interfacial oxides may form. Yablonovitch, 1212. Yablonovitch further recognizes that the functioning of the interfacial oxide structures is "complex," but omits a complete analysis of the physical phenomenon underlying formation of the interfacial oxide. Knowledge of such physical phenomenon would have been sought after by a POSITA in order to implement Yablonovitch, particularly in order to implement Yablonovitch according to the design considerations, such as the electrical and optical characteristics of a solar cell. Kwark provides such knowledge of physical phenomenon. For example, Kwark explains how the presence or absence of an interfacial chemical oxide, as well as the thermal treatment impacts the reverse saturation current, J_{oe}, which impacts cell efficiency.

92. For example, "[d]ifferential tunneling probability between electrons and holes... [is] **very sensitive to oxide thickness**." Yablonovitch at 1213 (emphasis added). It is therefore important to know the physical nature of an interfacial oxide in a solar cell in order to optimize its properties for particular design considerations.

93. While Yablonovitch generally acknowledges that oxide thickness plays a crucial role in carrier transport properties, Kwark explains further the physical

properties and phenomenon that result in such properties. In particular, Kwark provides explanation and experimentation data that describe and quantify the trade-off between current density (J_o) and contact resistivity. Ex. 1017 (Kwark) at 41-84. These properties represent a known design consideration that a POSITA would optimize for a given application by tailoring the interfacial oxide thickness. *See Electrical Characterization of Polysilicon-To-Silicon Interfaces* (1988)(Ex. 1008)("Crabbe") at ("The structure of the interfacial layer at the polysilicon-to-silicon interface can dominate the carrier transport properties of polysilicon contacts... there is a **fundamental trade-off** between base current (i.e. gain) and emitter resistance... Within the base current/emitter resistance constraint, **the interface can be taylored [sic] for specific applications depending on the device requirements**"). In other words, a thicker interfacial oxide will provide better passivation qualities but suffer from higher resistance, while a thinner interfacial oxide will provide worse passivation qualities but will benefit from lower resistance.

94. As Kwark explains, SIPOS with an interfacial oxide can yield solar cells with high open circuit voltage and efficiency.

95. A POSITA would understand that optimizing these parameters are crucial for achieving the desired balance between low contact resistance and high open circuit voltage, which has concomitant benefits for efficiency.

96. The teachings of Yablonovitch and Kwark are highly complementary, as Kwark provides insights regarding complex interface design considerations. The combined teachings of Yablonovitch and Kwark would provide a POSITA a comprehensive understanding of the interface engineering at work in Yablonovitch's process, moving beyond Yablonovitch's general disclosure of the "complex" processes affecting the structure. With knowledge of such design considerations, as taught by Kwark, a POSITA would have been able to optimize the thin oxide to the design constraints of any given application.

97. A POSITA would have had the skills, knowledge and rationale to design and implement Kwark's teachings in Yablonovitch's process that would have predictably resulted in optimized parameters to form the interfacial oxide. A POSITA would have considered fabrication parameters, such as anneal time, anneal temperature, and dopant concentration to facilitate such an optimization. As one example, the resulting optimization, would have resulted in tailored contact resistivity (ρ_c) and emitter saturation current density (J_o) to meet the design constraints of a particular application for the solar cell.

98. It would have been well within the skill of a POSITA in 2009 to consider the design benefit/tradeoffs in designing/implementing such modification. Here, guided by Kwark, a POSITA would have balanced tradeoffs between contact resistivity (ρ_c) and emitter saturation current density (J_o) to warrant consideration

and implementation of the above modification. (*Id.,* 3) Moreover, a POSITA would have appreciated that such a modification would have involved applying known technologies/techniques (*e.g.*, Kwark's implementation details) and thus would have had the motivation and reasonable expectation of success in implementing them in Yablonovitch's process. (*Id.*, 3) Considering and implementing such knowledge, techniques, and teachings would have yielded the predictable result of optimized contact resistivity (ρ_c) and emitter saturation current density (J_o). (*Id.*).

b) Reasonable Expectation of Success

99. It is my opinion that a POSITA would have had a reasonable expectation of success in implementing the combination of Yablonovitch and Kwark.

100. The art was mature and predictable. Fabrication of polysilicon/SIPOS emitters and silicon oxide layers for semiconductor devices (including solar cells), including techniques for dopant diffusion, thermal annealing, and interface engineering, was a mature and well-understood discipline well before the relevant timeframe (2009). The behavior of thin oxide layers under high-temperature processing, especially in the presence of dopants, was an area of extensive research and optimization. R.M. Swanson (author of Yablonovitch and advisor to Kwark), known as "the father of solar in U.S." (see Ex. 1033, 1), and his colleagues at Stanford (which set multiple contemporary solar cell efficiency records in the 1980's

and early 1990's before leaving to found SunPower in 1991) focused the industry towards this subject matter throughout the mid to late 1980's. *See*, *e.g.*, Ex. 1020 ("On another front, the author supervised a PhD student in 1985 who developed oxygen doped poly silicon emitters (SIPOS) with J_o less than 10 fA/cm^2."). *See also* EX1006 (recognizing in 1971 the "intense interest" in "thin films of silicon dioxide due to their extensive use as passivating and insulating layers in the silicon planar technology," specifically due to the "interface states" formed between silicon dioxide and silicon). The keen interest and research activity in the subject matter more than 20 years before the effective filing date of the '732 patent highlights the degree to which the subject matter had been researched and characterized decades before 2009.

101. The consistent findings across multiple contemporaneous papers, including Exs. 1007-1010, Exs. 1014-1019, and Exs. 1024-1032, demonstrate a comprehensive and mature understanding of the complex polysilicon/SIPOS interface with silicon and the role of interfacial oxides. This collective body of knowledge indicates a predictable art where combining known phenomena would yield anticipated results. The concentration of research on polysilicon/SIPOS emitters, evidenced by these publications, further supports the robustness and predictability of these phenomena. Kwark's findings, which for example, explain the effects of oxygen dopant on interfacial oxide formation demonstrates a

systematic and predictable understanding of these phenomena. This strong corroborating evidence from the above multiple independent studies reinforces the predictability and reliability of the phenomenon.

102. The POSITA would have considered the Yablonovitch / Kwark combination to be simply an arrangement of old elements (and their corresponding fabrication steps) with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement (a solar cell with improved performance).

103. The understanding of the trade-offs, such as between contact resistivity (ρ_c) and emitter saturation current density (J_o), as discussed by Kwark, Gan and Neudeck, further support a high expectation of success. A POSITA would understand that by controlling dopant concentration and other conditions (such as annealing), they could predictably influence the oxide thickness and degree of oxide break-up, and thus optimize the balance between achieving low contact resistance (for efficient carrier flow) and maintaining high emitter efficiency by providing interface passivation and reducing J_o (for minority carrier blocking). Such routine experimentation would have been a matter of engineering optimization within known parameters, not discovery of new phenomena.

104. I do not believe that applying the teachings of Kwark to Yablonovitch's SIPOS emitter structure would be unworkable, lead to undesirable results, or

otherwise discourage the proposed combination. Instead, these references build on each other's teachings of interface engineering for improved device performance. Indeed, the results are presented as a beneficial outcome for achieving low-resistance contacts and efficient carrier transport, which indicates that a POSITA would actively pursue conditions that optimize this oxide thickness and break-up, to achieve desired device characteristics. Ex. 1005 (Yablonovitch), p. 1211 (discussing "good performance in SIPOS-crystalline silicon-SIPOS double heterostructure solar cells"); Ex. 1016 (Kwark). Identifying negatives (in addition to positives) in trade-offs (*e.g.*, between contact resistivity (ρ_c) and emitter saturation current density (J_o)) are design considerations for optimization, not teachings away from the fundamental concept of oxide thickness and break-up. A POSITA would understand that essentially any design decision in engineering comes with costs and benefits (i.e., positives and negatives), and that weighing those costs and benefits is part of the design process.

105. Combining Yablonovitch and Kwark as described herein would have been well within the level of ordinary skill in the art. It would not have resulted in any unpredictable results and could have been readily accomplished without undue experimentation and with a reasonable expectation of success. The combination would simply have been the combination of well known prior art steps in solar cell and semiconductor fabrication to yield predictable results. Likewise, implementing

Yablonovitch's interfacial oxide according to the design considerations of Kwark would have been a simple use of a known technique to improve similar devices (Yablonovitch's process) in the same way. It is nothing more than applying a known technique to a known device ready for improvement to yield predictable results.

2. Application to the Challenged Claims

106. In my opinion, Yablonovitch, in view of Kwark, teaches the limitations of claim 1. The mapping below provides my analysis on a limitation-by-limitation basis, with relevant citations to the teachings of Yablonovitch.

a. Claim 1

(1) Element [1.pre] A method of fabricating a solar cell, comprising;

107. I understand that this limitation is a preamble of the claim, and I have been asked to assume that the preamble of claim 1 is not limiting. But even if it were limiting, Yablonovitch discloses the preamble of claim 1.[3] As shown in the following limitations of claim 1, Yablonovitch teaches ***[a] method of fabricating a solar cell***.

108. Yablonovitch's fabrication method is for "[a] 720 mV open circuit voltage SiO_x:c-Si:SiO_x double heterostructure **solar cell**." Yablonovitch at Title.

[3] I understand that Petitioner does not acquiesce that the preambles are limiting.

For example, Table II of Yablonovitch below discloses the processing sequence (i.e., method of fabrication) for the double heterostructure solar cell. Yablonovitch, Table II.

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2.
5. Ramp up to 650 °C while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2.
7. Deposit SIPOS from 1000 ppm SiH_4, 50 ppm PH_3, and 10 ppm O_2.
8. Ramp furnace to 900 °C.
9. Anneal for 15 min.
10. Ramp furnace down to 450 °C.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

Yablonovitch, Table II

(2) Element [1.a] *providing a substrate,*

109. Yablonovitch discloses this limitation.

110. Yablonovitch provides a "crystalline silicon wafer" as **a substrate** for the **solar cell**. Yablonovitch at 1211 (discussing the "silicon wafer"), 1212 (discussing properties of the silicon wafer and showing the p-Si silicon wafer in Figure 2), 1213 (showing the "crystalline silicon wafer" in Figure 3). A crystalline

silicone wafer is the foundation layer, or **a substrate** on which the rest of the solar cell is built. Table I below summarizes the material properties of the wafer.

TABLE I. Properties of silicon wafer material.

Orientation	⟨100⟩
Resistivity	0.5 Ω cm *p*-type
Doping concentration	$2.5\times10^{16}/cm^3$
Bulk minority-carrier lifetime	450 μs
Minority-carrier mobility	700 cm^2/Vs
Diffusion length	0.9 mm
Thickness	50 μm
J_0 of n^+-SIPOS heterocontact	10^{-14} A/cm^2 at 27 °C
Emitter Gummel number	3.3×10^{15} s/cm^4

Yablonovitch, Table I

111. According to the process sequence such as in Table II (reproduced below) Yablonovitch uses a "float-zone p-type silicon wafers of 0.5 Ω cm resistivity… [which] were chemically thinned to 50 µm" as **a substrate** for fabricating the solar cell, as shown in Table 1I. Yablonovitch at 1212.

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2.
5. Ramp up to 650 °C while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2.
7. Deposit SIPOS from 1000 ppm SiH_4, 50 ppm PH_3, and 10 ppm O_2.
8. Ramp furnace to 900 °C.
9. Anneal for 15 min.
10. Ramp furnace down to 450 °C.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

Yablonovitch, Table II

112. Figure 3 below shows the wafer as the base for other layers during fabrication of the solar cell, meaning that the wafer is **a substrate**.

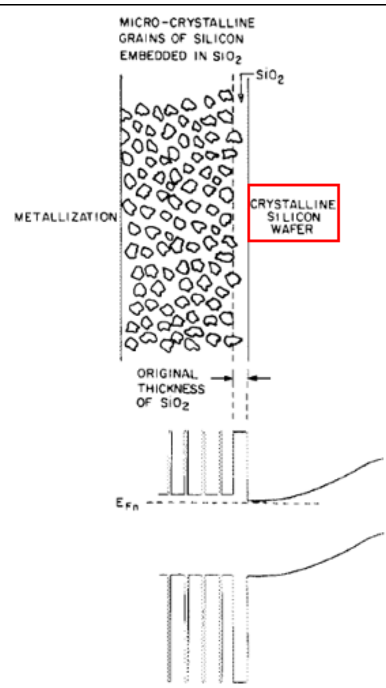


FIG. 3. Model for the metallurgical configuration of the SIPOS-Si heterojunction. Electron conduction is thought to proceed via the microcrystalline grains which protrude into the thin oxide layer.

Yablonovitch, FIG. 3

113. Further, Figure 2 shows the test configuration of the semiconductor structure for the solar cell. There, it can be seen that the wafer is **a substrate**.

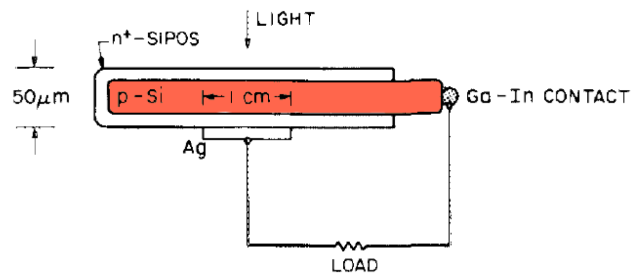


FIG. 2. Test configuration for the SIPOS : *c*-Si : SIPOS double heterostructure solar cells. In this design the fill factor was limited by the bulk resistance of the *p*-Si wafer itself.

Yablonovitch, FIG. 2

(3) Element [1.b] providing an interface passivation layer over the substrate,

114. Yablonovitch discloses this limitation.

115. Yablonovitch deposits n^+ SIPOS layer that is oxygenated poly-Si (polysilicon), which can also be thought of as a "mixture of microcrystalline silicon and silicon dioxide (SiO_x)." Yablonovitch at 1211. Yablonovitch at 1211-13.

116. As shown in Step (7), the n^+ SIPOS layer is formed with 10 ppm O_2, which results in a "5% oxygen concentration." Yablonovitch at 1213. As shown in Step (9), the n^+ SIPOS layer is then annealed at 900 C for 15 minutes.

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2.
5. Ramp up to 650 °C while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2.
7. Deposit SIPOS from 1000 ppm SiH_4, 50 ppm PH_3, and 10 ppm O_2.
8. Ramp furnace to 900 °C.
9. Anneal for 15 min.
10. Ramp furnace down to 450 °C.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

Yablonovitch, Table II

117. Kwark recognizes that while "SIPOS in the as deposited form consists of amorphous silicon islands embedded in a silicon rich matrix," "[a]nnealing promotes the crystallization of the α-Si islands with accompanying rejection of oxygen from the crystals to the surrounding matrix." Kwark at p. 178. As Kwark further explains, "[t]he expulsion of oxygen outside the grains also *causes the formation of an oxide layer at the Si-SIPOS interface*" that "acts much like the intentionally introduced chem oxide in blocking hole injection into the SIPOS." Kwark at p. 178. This "oxide layer at the Si-SIPOS interface" (**an interface passivation layer over the substrate**) is indicated as an "interfacial oxide" in Kwark's Figure 7.19 below. *See also* Kwark at p. 180 (referring to the interfacial oxide as a "thin tunnelable oxide at the Si-SIPOS interface").

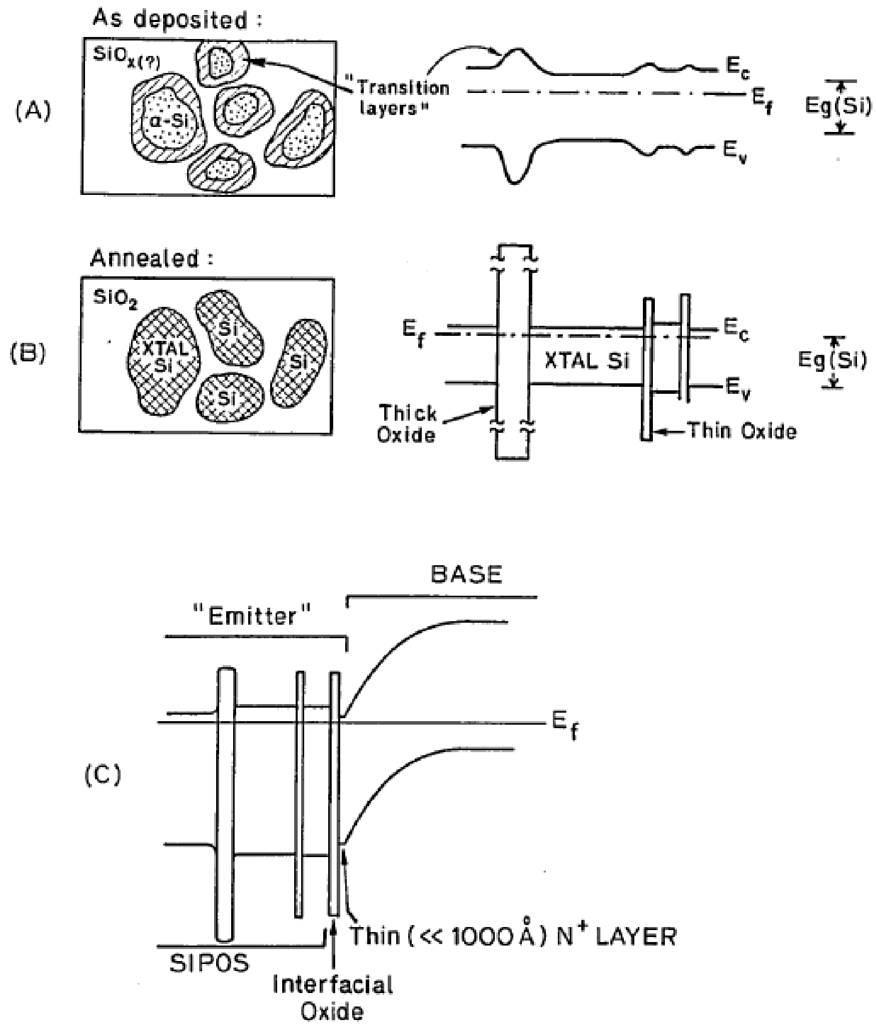


Figure 7.19: influence of annealing on SIPOS microstructure

Kwark, FIG. 7.19

118. This property of SIPOS has been well understood for many years. As explained in "*Electrical conductivity of semi-insulating polycrystalline silicon and its dependence upon oxygen content*" (Ex. 1031, "Ni")(1981), "[t]he oxygen

concentration in SIPOS greatly exceeds its solubility in silicon, so that when silicon crystallites begin to form during annealing *the excess oxygen must segregate outside the grains*." See p. 554.

119. Yablonovitch also discloses thermally growing a very thin silicon oxide, SiO_2, on the silicon wafer. *See* Yablonovitch at 1211 (describing "thermally grown SiO_2"), 1213 (showing "thin oxide layer" of SiO_2 in Figure 3). In particular, step (6) describes growing the thin layer. Yablonovitch at 1212.

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2.
5. Ramp up to 650 °C while maintaining N_2 purge.
6. $\boxed{\text{Oxidize for 5 min with 100 ppm } O_2.}$
7. Deposit SIPOS from 1000 ppm SiH_4, 50 ppm PH_3, and 10 ppm O_2.
8. Ramp furnace to 900 °C.
9. Anneal for 15 min.
10. Ramp furnace down to 450 °C.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

Yablonovitch, Table II

120. Step (6) is a typical process for growing thin oxides for interface passivation. After using N_2 to purge the chamber, the silicon wafer is exposed to oxygen for a short time (for example, 5 minutes), which forms a thin film of oxide on the surface of the wafer. The thin oxide formed is a very thin (25–40 Å, or 2.5-4

nm) amorphous layer of SiO_2 (silicon dioxide), which forms on the silicon wafer, is depicted in Figure 3 below. Yablonovitch, 1212-13.

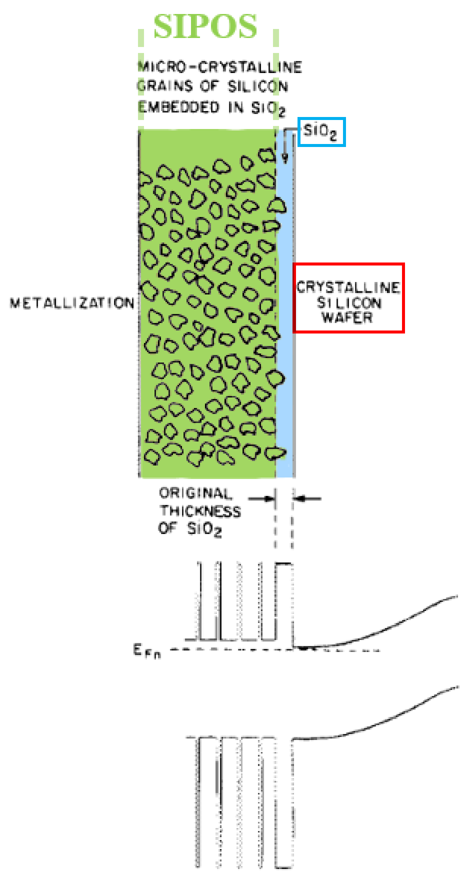


FIG. 3. Model for the metallurgical configuration of the SIPOS-Si heterojunction. Electron conduction is thought to proceed via the microcrystalline grains which protrude into the thin oxide layer.

Yablonovitch, FIG. 3

121. Kwark teaches that when an oxide layer is pre-formed (i.e., before annealing of SIPOS) on the interface between Si and SIPOS, the thin oxide formed from the SIPOS annealing process will form as an independent interfacial oxide, and both oxides together will form a "thicker composite oxide." Kwark at p. 180. As

Kwark explains, "adding the chem oxide layer to the SIPOS contact is therefore seen to result in two layers of interfacial oxide, one deliberately grown, the other, a by-product of the SIPOS annealing process," resulting in a "thicker composite oxide." Kwark at p. 180. This "thicker composite oxide" is also **an interface passivation layer over the substrate**.

122. A POSITA would have understood that the expelled oxygen from the SIPOS layer would also "aid[] in the formation" of the thermal thin oxide formed in Step (6). *See*, *e.g.*, Ex. 1018 (Kwark II) at 743. For example, Kwark II explains that "a thin tunnelable interfacial oxide" formed from the out-diffusion of oxygen from SIPOS during an anneal will "simply add[] an additional thickness" with a pre-formed thin oxide layer. Ex. 1018 (Kwark II) at 743. This thicker thermal thin oxide formed in Step (6) is also **an interface passivation layer over the substrate**.

123. Yablonovitch teaches that thin oxides at the interface between SIPOS and silicon substrates provide **interface passivation**. Yablonovitch teaches that when fabricating the solar cell, "the **interface** states at the heterocontacts *must be passivated*." Yablonovitch, 1211. In order to do so, Yablonovitch teaches that in its solar cell, "[t]he **interface** states between SIPOS and crystalline silicon (c-Si) seem to be **passivated as well as the high quality interface between thermally grown SiO_2 and c-Si**." Yablonovitch, 1211. In other words, thin interfacial SiO_2 oxides are explicitly recognized to passivate the interface of SIPOS and crystalline silicon.

124. Further, Yablonovitch notes that the "outstanding voltage performance" of a fabricated solar cell according to its method "is made possible" in part by "the **excellent surface passivation** of the n^+-SIPOS heterocontact." Yablonovitch, 1212. While Yablonovitch recognizes that the outstanding performance of the cell was due in part to excellent interface passivation (see Yablonovitch, 1212) caused by the thermally grown SiO_2, Kwark further recognizes that the thermally grown SiO_2 was formed in part by expelled oxygen from the step (9) anneal, and that surface passivation was also aided by an interfacial oxide formed independently by the step (9) anneal.

125. Further, a POSITA would have recognized that interfacial SiO_2 on silicon is well known to provide excellent surface passivation, which is consistent with the '732 patent. See Ex. 1006 (*Electron Trapping Levels in Silicon Dioxide Thermally Grown on Silicon*) (recognizing in 1971 the "intense interest" in "thin films of silicon dioxide due to their extensive use as passivating and insulating layers in the silicon planar technology," specifically due to the "interface states" formed between silicon dioxide and silicon).

126. The '732 patent's descriptions of the **interface passivation layer** align with Yablonovitch and Kwark's teachings. All of the '732 patent's embodiments of the "passivating interface layer" describe it as having "<10 nm" thickness, and identifies "silicon oxide" as a primary example. See '732 patent at 5:56-57, 5:66-

67, 6:65-66, 7:8-9, 8:5-6, 8:16-17, 9:12-13, 10:8-9, 10:19-20, 11:21-22, 11:30-31, 12:28-29, 12:38-39, 12:30-31, 13:36-37, FIG. 1. The ’732 patent does not purport to teach any invention or novelty regarding these properties, and the omitted teachings are understood to be within the knowledge of a POSITA.

(4) Element [1.c] providing a passivating film over the interface passivation layer, the passivating film comprising a passivating material and a conductive dopant,

127. Yablonovitch discloses this limitation. **Over** the thermal oxide and diffused oxide, Yablonovitch **provid[es]** an n^+ SIPOS (“semi-insulating polycrystalline silicon”) layer (**providing a passivating film over the interface passivation layer**). Yablonovitch at 1211-13. As discussed, SIPOS is oxygenated poly-Si (polysilicon), which can also be thought of as a “mixture of microcrystalline silicon and silicon dioxide (SiO_x).” Yablonovitch at 1211.

128. Steps (7-9) discloses the deposition the n^+ SIPOS layer: *“Deposit SIPOS from 1000 ppm SiH_4, 50 ppm PH_3 and 10 ppm O_2,”* and then anneal, as shown below.

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2.
5. Ramp up to 650 °C while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2.
7. Deposit SIPOS from 1000 ppm SiH_4, 50 ppm PH_3, and 10 ppm O_2.
8. Ramp furnace to 900 °C.
9. Anneal for 15 min.
10. Ramp furnace down to 450 °C.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

Yablonovitch, Table II

129. The n^+ SIPOS (**passivating film**) **compris[es]** phosphorus (**a conductive dopant**). Yablonovitch, 1213. As shown in step (7), the n^+ SIPOS deposition includes phosphine (PH_3), which produces phosphorus in the SIPOS layer. Yablonovitch, 1213.

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2.
5. Ramp up to 650 °C while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2.
7. Deposit SIPOS from 1000 ppm SiH_4, 50 ppm PH_3, and 10 ppm O_2.
8. Ramp furnace to 900 °C.
9. Anneal for 15 min.
10. Ramp furnace down to 450 °C.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

Yablonovitch, Table II

130. Yablonovitch explicitly discloses that the SIPOS includes a "phosphorus **dopant**." Yablonovitch, 1213. The "phosphorus **dopant**" is an n-type dopant, which dopes the SIPOS layer to be n-doped, which is why it is referred to as an "n^+ SIPOS" layer. Yablonovitch, 1211. It is my opinion that phosphorus has been a very well known n-type dopant of silicon for many decades before the relevant date, if not one of the most commonly used n-type dopants of silicon. *See* Ex. 1022, 28, 109 (by 1982 "[p]hosphorus [was] the impurity generally used" to as the n-type dopant in "standard solar cell technology"); Ex. 1021, 118-22.

131. The anneal (step 9) serves to "activate the phosphorous **dopant**," which causes the n^+ SIPOS to be more **conductive**. Yablonovitch at 1212. When the phosphorous is "activated," it means the phosphorous dopant is incorporated into the lattice structure of the n^+ SIPOS, which makes it more conductive. Yablonovitch at 1212. Anneals "activate" dopants by incorporating them into the material's lattice structure, which changes its electrical properties. When dopants like phosphorus are introduced into a semiconductor, they might not immediately settle into the correct, "substitutional" positions within the crystal lattice where they can donate their extra electron. During an anneal, phosphorus atoms substitute silicon atoms in the crystal lattice. Four of its valence electrons form covalent bonds with the surrounding silicon atoms, and the fifth valence electron is then loosely bound to the phosphorus

atom. This extra electron can easily become a free electron, contributing to the material's conductivity by acting as a charge carrier.

132. As a result of the phosphorous dopant and annealing, the n^+ SIPOS layer becomes conductive. As a result, the n^+ SIPOS layer forms a "SIPOS emitter structure," shown in Figures 2 and 3. Yablonovitch at 1211-12. A POSITA would have understood that emitters in solar cells are **conductive** because carriers (i.e., electrons and holes) are generated in the emitter, and must be swept to a contact in order to generate current. *See* Sec. V (technical background). If an emitter was not conductive, the carriers could not be conducted through it, and the solar cell would not generate any current.

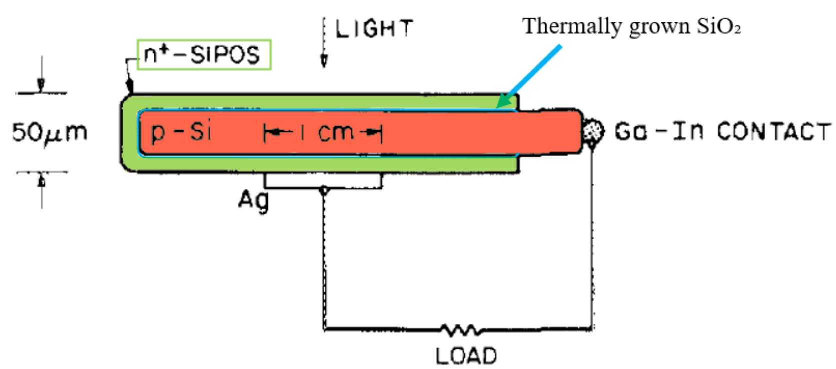


FIG. 2. Test configuration for the SIPOS : *c*-Si : SIPOS double heterostructure solar cells. In this design the fill factor was limited by the bulk resistance of the *p*-Si wafer itself.

Yablonovitch, FIG. 2

133. The n^+ SIPOS layer is also explicitly taught to be **conductive** after the phosphorous dopant and annealing. For example, as shown in Figure 3, in the

SIPOS-Si heterojunction, "**[e]lectron conduction** is thought to proceed via the microcrystalline grains which protrude into the thin oxide layer." Yablonovitch at 1213. As Yablonovitch further explains, this contact "provide[s] **more than enough conductivity** for majority-carrier electrons." Yablonovitch at 1213.

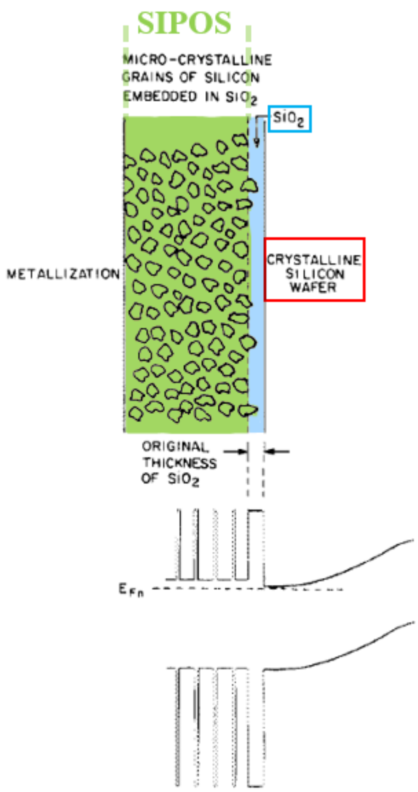


FIG. 3. Model for the metallurgical configuration of the SIPOS-Si heterojunction. Electron conduction is thought to proceed via the microcrystalline grains which protrude into the thin oxide layer.

Yablonovitch, FIG. 3

134. The '732 patent states that its "[e]lectrically passivating and conductive film" may be an "amorphous or polycrystalline silicon." '732 patent, 5:47-51. SIPOS is simply oxygenated poly-Si (polysilicon), which can also be thought of as

a "mixture of microcrystalline silicon and silicon dioxide (SiOx)." Yablonovitch at 1211. Further, Yablonovitch explains that the "electrical" properties of the n^+ SIPOS emitter is generally the same as a polysilicon emitter, which the '732 patent recognizes as conductive, and was known to be conductive. Yablonovitch, 1213. For example, Yablonovitch explains that the resistivity of the n^+ SIPOS of 10^{-3} $\Omega \cdot cm$ is "similar to that of doped polysilicon." Yablonovitch, 1213. Instead of electrical difference, Yablonovitch notes that the relevant difference provided by the 5% additional oxygen concentration in n^+ SIPOS as compared to poly-Si is that the oxygen content increases the density of grains protruding into the thin oxide layer, which increases conduction. As discussed above, n^+ SIPOS is essentially oxygenated poly-Si (polysilicon), and the '732 patent recognizes that its "[e]lectrically passivating and conductive film" may be an "amorphous or polycrystalline silicon." Yablonovitch at 1211. Polysilicon was a well known conductor used to form conductive emitters in solar cells. *See* '732 patent, 17:26-46 (describing how polysilicon is an exemplary material used for used to form conductive emitters).

135. The n^+ SIPOS layer is a **passivating** film that **compris[es] a passivating material**. Yablonovitch notes that the "outstanding voltage performance" of the solar cell fabricated according to its method "is made possible" in part by "the **excellent surface passivation** of the n^+ -SIPOS heterocontact."

Yablonovitch, 1212. Yablonovitch teaches that "the interface states at the heterocontacts *must be passivated*" and that in order to do so, Yablonovitch teaches that in the solar cell fabricated according to its method, "[t]he interface states between **SIPOS** and crystalline silicon (c-Si) seem to be **passivated** as well as the high quality interface between thermally grown SiO_2 and c-Si." Yablonovitch, 1211.

136. Thus, the n^+ SIPOS layer acts as a **passivating** heterojunction emitter with "excellent surface passivation" that enables an outstanding open-circuit voltage of 720 mV. Yablonovitch, 1212. The SIPOS/c-Si junction yields an extremely low saturation current ($J_0 \sim 1\times10^{-14}$ A/cm²) due to this passivation. Yablonovitch, 1212.

137. It was also well known that SIPOS emitters were **passivating**, and a POSITA would have also recognized Yablonovitch's SIPOS emitter as a **passivating layer**. *See*, *e.g.*, Ex. 1007 (an "application [of SIPOS] is the incorporation of a SIPOS emitter as a passivating layer in conventional silicon solar cell structures"), Ex. 1014 (SIPOS is "used as passivation films on silicon devices").

(5) Element [1.d] wherein providing the interface passivation layer and providing the passivating film comprise: [1d.1] providing an amorphous silicon-containing compound over an upper surface of the substrate, the compound comprising oxygen dopant and the conductive dopant,

138. Yablonovitch discloses this limitation.

139. Before annealing, the n^+ SIPOS layer is **an amorphous silicon-containing compound**. Yablonovitch at 1211-13. As discussed, SIPOS stands for "semi-insulating polycrystalline **silicon**," and is thus a **silicon-containing compound**. Yablonovitch at 1211.

140. Before annealing, the n^+ SIPOS layer is **amorphous**. Yablonovitch explains that the anneal is "necessary to precipitate microcrystalline silicon grains." Yablonovitch at 1211. Here, the term "precipitate" is referring to crystal precipitation, which is the process of transitioning from amorphous silicon to polycrystalline silicon. See Kwark III (Ex. 1019) at 1021 ("As deposited, SIPOS is usually amorphous... During annealing it has been found that the film morphology changes. Si precipitates into small grains of crystalline Si and the oxygen segregates as SiO_2 on the grain boundaries."). It was conventional and well known that a silicon compound formed from a deposition of SiH_4 at 650 C will be amorphous until it is annealed at a higher temperature (see step 7). *See* Kwark III (Ex. 1019) at 1021 ("As deposited, SIPOS is usually amorphous").

141. While the n^+ SIPOS layer being amorphous was well known before the relevant time, it is also explicitly recognized by Kwark. Kwark recognizes that while "SIPOS in the as deposited form consists of **amorphous silicon** islands embedded in a silicon rich matrix," "**[a]nnealing promotes the crystallization** of the α-Si

islands with accompanying rejection of oxygen from the crystals to the surrounding matrix." Kwark at p. 178.

142. As shown in Figures 2 and 3, the n$^+$ SIPOS is provided **over an upper surface of the substrate**.

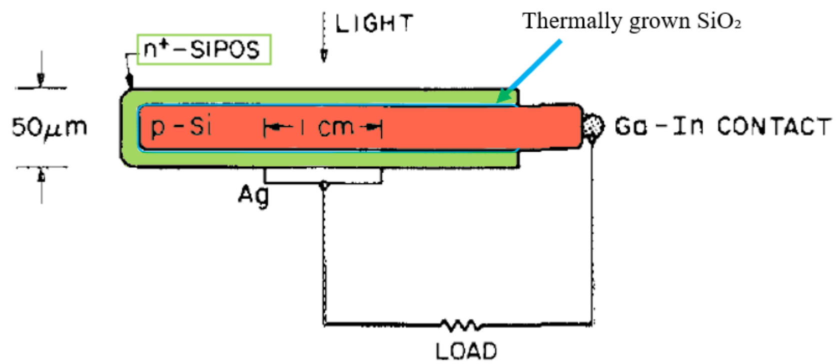


FIG. 2. Test configuration for the SIPOS : *c*-Si : SIPOS double heterostructure solar cells. In this design the fill factor was limited by the bulk resistance of the *p*-Si wafer itself.

Yablonovitch, FIG. 2

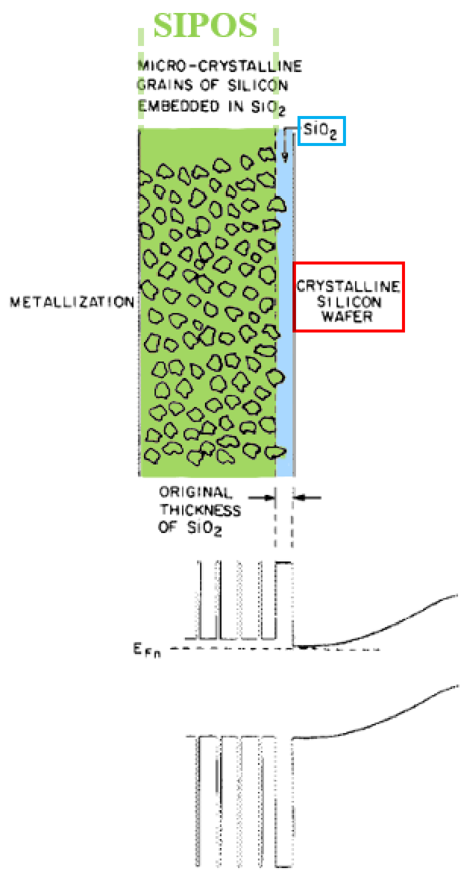


FIG. 3. Model for the metallurgical configuration of the SIPOS-Si hetero-junction. Electron conduction is thought to proceed via the microcrystalline grains which protrude into the thin oxide layer.

Yablonovitch, FIG. 3

143. The n+ SIPOS comprises **oxygen dopant and the conductive dopant**. As discussed, SIPOS, by definition, is polycrystalline silicon doped with oxygen. Yablonovitch, 1211. In the case of Yablonovitch, a "5% oxygen concentration" of **oxygen dopant** is used. Yablonovitch at 1213. As discussed in element [1c] (incorporated by reference), Yablonovitch discloses that the SIPOS includes a "phosphorus dopant" (**the conductive dopant**). Yablonovitch, 1213.

(6) Element [1.d] wherein providing the interface passivation layer and providing the passivating film comprise: ... [1d.2] thermally treating the amorphous silicon-containing compound to diffuse the oxygen dopant, at least in part, into the upper surface of the substrate to form an oxide layer over the substrate, the oxide layer defining the interface passivation layer; and,

144. Yablonovitch, in view of Kwark, discloses this limitation.

145. After depositing the SIPOS in step (7), Yablonovitch anneals at high temperature. Yablonovitch, 1212. As shown in steps 8-9 of Table II, after deposition at 650 °C, the furnace is ramped up to 900 °C and the wafer is annealed for 15 minutes (**thermally treating the amorphous silicon-containing compound**). Yablonovitch, 1212.

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2.
5. Ramp up to 650 °C while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2.
7. Deposit SIPOS from 1000 ppm SiH_4, 50 ppm PH_3, and 10 ppm O_2.
8. Ramp furnace to 900 °C.
9. Anneal for 15 min.
10. Ramp furnace down to 450 °C.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

Yablonovitch, Table II

146. As I discussed in element [1.b] (which I incorporate by reference), Kwark recognizes that while "SIPOS in the as deposited form consists of amorphous silicon islands embedded in a silicon rich matrix," (corresponding to **the amorphous silicon-containing compound**), annealing (**thermally treating**) causes "rejection of oxygen from the crystals to the surrounding matrix" (i.e., **to diffuse the oxygen dopant**). Kwark at p. 178. As Kwark further explains, "[t]he expulsion of oxygen outside the grains also *causes the formation of an oxide layer at the Si-SIPOS interface*" meaning the anneal causes the SIPOS layer **to diffuse the oxygen dopant, at least in part, into the upper surface of the substrate to form an oxide layer over the substrate**. As further discussed in element [1.b] (which I incorporate by reference) this SIPOS-formed oxide is an **oxide layer defining the interface passivation layer** both alone and in combination with the "composite oxide" formed with the thermally grown oxide from Step (6). Kwark at p. 178-80.

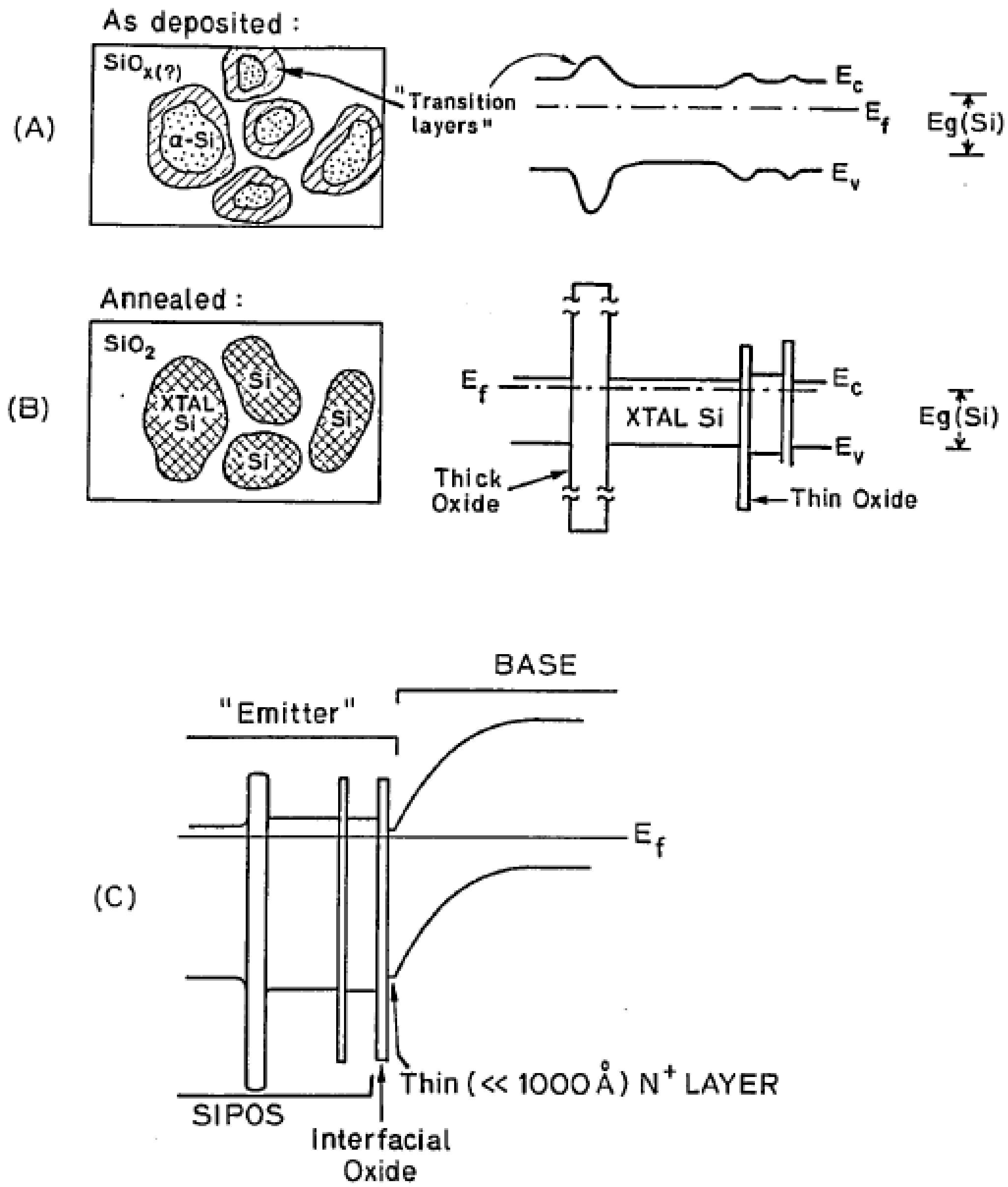


Figure 7.19: influence of annealing on SIPOS microstructure

Kwark, FIG. 7.19

(7) Element [1.d] wherein providing the interface passivation layer and providing the passivating film comprise: ... [1d.3] wherein remaining amorphous silicon-containing compound above the oxide layer defines the passivating film; and,

147. Yablonovitch discloses this limitation. As discussed in element [1c] (incorporated by reference), after the anneal (**thermally treating the amorphous silicon-containing compound**) and accompanying oxygen dopant diffusion of the amorphous SIPOS (**remaining amorphous silicon-containing compound above the oxide layer**), the annealed SIPOS **defines the passivating film**.

(8) Element [1.d] wherein providing the interface passivation layer and providing the passivating film comprise: ... [1d.4] wherein the thermally treating also diffuses at least a portion of the conductive dopant throughout the interface passivation layer to facilitate electrical connection to the substrate; and,

148. Yablonovitch, in view of Kwark, discloses this limitation in at least two ways.

149. First, Yablonovitch explains that "during [the annealing] step the phosphorus **diffuses** about 20-50 Å into the silicon wafer as measured by secondary ion mass spectrometry." Yablonovitch, 1212. In other words, the anneal step (9) (**the thermally treating**) **diffuses at least a portion of the** phosphorus dopant (**conductive dopant**) **throughout the interface passivation layer** and into the c-Si substrate by roughly 2–5 nm, which is on the other side of the SIPOS layer.

Yablonovitch, 1212. The result is a "shallow n^+ accumulation layer" at the wafer surface, essentially forming an n^+ region (cause by the presence of phosphorus dopant) in the wafer directly beneath/through the interface oxide. Yablonovitch, 1212.

150. As the silicon wafer is on the opposite side of the interfacial oxide as the SIPOS layer, the phosphorous must diffuse **throughout the interface passivation layer** that sits between the SIPOS layer (green) and silicon wafer (red), as shown in Figure 3. Yablonovitch, 1212.

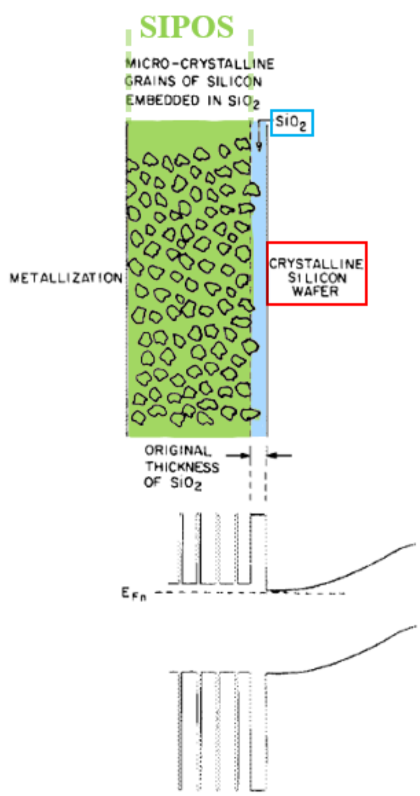


FIG. 3. Model for the metallurgical configuration of the SIPOS-Si heterojunction. Electron conduction is thought to proceed via the microcrystalline grains which protrude into the thin oxide layer.

Yablonovitch, FIG. 3

151. The anneal causing the phosphorous dopant diffused through the interfacial oxide and "*n* + accumulation layer" at the wafer surface (i.e., the surface interfacing the interfacial oxide) serves **to facilitate electrical connection to the substrate**. Such a diffusion makes the wafer surface more strongly n-type and matching the SIPOS layer, meaning that the surface will have higher conductivity, and in particular, a higher conductivity path (i.e., **electrical connection**) **to the substrate**. The anneal further aids in such diffusion by breaking up the oxide(s), which allows the phosphorous dopant to diffuse more freely. *See*, *e.g.*, Ex. 1024 ("*Poly silicon Contacted Emitter Bipolar Transistors: Fabrication Development*" (1988)) at 36-37 ("Annealing at high temperatures can reduce the emitter resistance and the leakage by breaking up the chemical oxide and diffusing the junction deeper into the substrate.").

152. For very thin oxides, such as under 5nm, it is easy for the dopant to enter throughout and pass through the oxide. *See*, *e.g.*, Ex. 1030 at 956-57 (performing various studies on the "diffusion of phosphorous in ultra-thin oxides from a doped polysilicon" into a silicon substrate and finding "very high" concentrations of dopants in the silicon substrate "[e]ven with a short diffusion time."); Ex. 1029 at 292 ("Thus, increasing amounts of phosphorus pass through the silicon oxide/silicon interface as the oxide layer gets thinner.").

153. In Yablonovitch, just as described by the Asserted Patent, phosphorus is incorporated into the interfacial oxide and substrate forms low resistance pathways through those layers along which electrons can more easily travel. Yablonovitch, 1212 ("the phosphorous diffuses… [to] produce a very shallow n^+ accumulation layers which is transparent to minority carriers); '732 patent 9:39-40 (teaching a phosphorous layer for resistance pathways), 15:7-11 (describing how phosphorous can be used to enhance electrical conductivity among layers). The diffusion of dopant into these layers thus increases the conductivity of the solar cell near the surface of the silicon substrate, i.e., through the interfacial oxide, such that its conductivity is more similar to the conductivity of the n^+ SIPOS. Yablonovitch, 1212 (describing how interfaces have shown the diffusion is consistent with the SIPOS emitter structure); '739 patent 15:5-11 (describing how the diffusion of the dopant "can be used to enhance the electrical conductivity between the metal electrodes and the surface of outer layers"). As a result, charges follow a lower resistance route from the substrate toward the electrodes than they otherwise would without the diffusion of the dopant. Yablonovitch, 1212 (finding "outstanding" voltage performance toward the electrodes due to n^+ SIPOS heterocontact); '732 patent, '739 patent 15:5-11 (describing how the diffusion of the dopant follows a lower resistance route, enhancing the electrical conductivity).

154. The diffusion of phosphorus from the n^+ SIPOS layer through the interfacial oxide (**interface passivation layer**) creates such conductive paths. It has been well known for many decades before the relevant date that diffusion of phosphorous through an SiO_2 layer and through its interface with a silicon substrate **facilitate[s] electrical connection to the substrate**.

155. For example, in 1961, *Diffusion of impurities into Silicon through an Oxide Layer* ("Thurston"; Ex. 1032) explained and provided experiments to show that "the distribution of phosphorus across the oxide-silicon interface is continuous." See p. 5.

156. As another example, in 1975, *Silicon dioxide masking of phosphorus diffusion in silicon* ("Ghoshtagore"; Ex. 1009) explained that there is a "continuity of impurity [phosphorous] distribution through th[e] interface" of SiO_2 and silicon.

157. As another example, "*TEM investigation of the effect of anneal temperature and arsenic concentration on the polysilicon/thin oxide/single-crystal-silicon emitter of a new high-performance bipolar transistor*" (1985) explains that an anneal causes dopants "to diffuse rapidly down the grain boundaries of the polysilicon, through the oxide film and into the underlying single-crystal Si to form the e/b junction." Ex. 1027 at 471.

158. Further, the anneal (**the thermally treating**) **also diffuses at least a portion of the conductive dopant throughout the interface passivation layer** by

embedding phosphorous and phosphorous-containing microcrystals into the interfacial oxide, which perforates the interfacial oxide **to facilitate electrical connection to the substrate**.

159. As Yablonovitch explains, the anneal (**the thermally treating**) causes phosphorus (**the conductive dopant**) in the microcrystalline grains to **diffuse[]** from the SIPOS layer to be "embedded in"/ "protrude into" the thin oxide (**throughout the interface passivation layer**). Yablonovitch, 1212. The phosphorous-containing microcrystalline grains are embedded into and **throughout** the thin oxide, as they form a "thin spots and pinholes in the $Si0_2$." Yablonovitch, 1213.

160. Yablonovitch explains that because of the incorporation of oxygen, the SIPOS grains are smaller but have a "significant surface density," in contrast to the "much larger" polysilicon grains that are fewer in number. Yablonovitch, 1213. A POSITA would understand that in order to "significant surface density of individual" phosphorous-containing microcrystalline grains, they must be **throughout** the thin oxide.

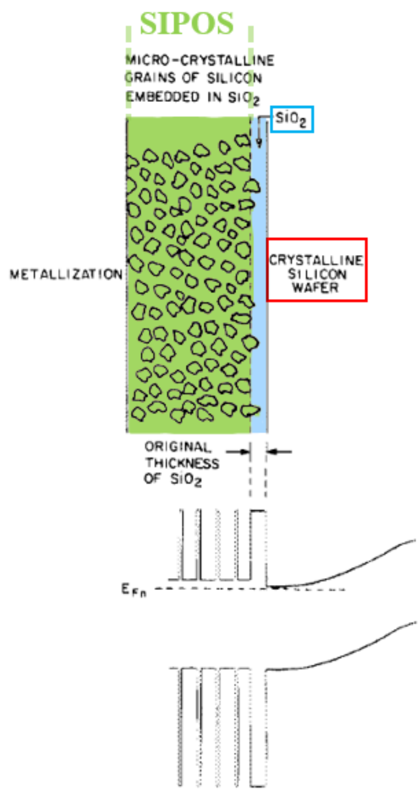


FIG. 3. Model for the metallurgical configuration of the SIPOS-Si heterojunction. Electron conduction is thought to proceed via the microcrystalline grains which protrude into the thin oxide layer.

Yablonovitch, FIG. 3

161. Due to the anneal, the interface is not a uniform insulating barrier but instead contains pinholes of doped material that let carriers through locally. Figure 3 of Yablonovitch illustrates this feature and explains that "**[e]lectron conduction** is thought to proceed via the microcrystalline grains which protrude into the thin oxide layer," which means it is **to facilitate electrical connection to the substrate**. Yablonovitch at 1213 ("the majority-carrier electrical contact is by individual

microcrystalline grains which occasionally protrude into the oxide as shown in Fig. 3, i.e., *electrical contact is via thin spots and pinholes in the SiO_2*.”).

162. Further, those n^+ SIPOS microcrystalline grains include the phosphorous dopant in their lattice, which makes them more conductive because the anneal serves to “activate the phosphorous dopant” (second effect mentioned above). Yablonovitch at 1212. Anneals “activate” dopants by incorporating them into the material’s lattice structure, which changes its electrical properties. When dopants like phosphorus are introduced into a semiconductor, they might not immediately settle into the correct, “substitutional” positions within the crystal lattice where they can donate their extra electron. During an anneal, phosphorus atoms substitute silicon atoms in the crystal lattice. Four of its valence electrons form covalent bonds with the surrounding silicon atoms, and the fifth valence electron is then loosely bound to the phosphorus atom. This extra electron can easily become a free electron, contributing to the material’s conductivity by acting as a charge carrier. *See* Ex. 1023, 12-13; Ex. 1022, 28; Ex. 1021, 118-22.

163. In other words, the high-temperature anneal causes phosphorous-doped microcrystalline Si grains in the SIPOS to poke through the interfacial SiO_2, and electrical contact between the n^+ layer and the wafer occurs at these numerous microscopic points. Yablonovitch explicitly notes that *“electrical contact is via thin spots and pinholes in the SiO_2”* at the interface. Yablonovitch, 1213. These highly

conductive phosphorous-doped microcrystalline Si grains **facilitate electrical connection to the substrate** for majority carriers (electrons, in the n^+ region of the n^+/p junction) to flow from the silicon substrate through the thin oxide and SIPOS layer and to the metal electrode. Thus, for majority carriers the electrical connection to the substrate is facilitated and low resistance as compared to if the microcrystalline grains did not form the pinhole "contacting points."

164. It was well known that anneals caused thermally grown interfacial oxides to perforate or "break-up," which allowed current paths through the oxide. For example *Electrical characterization of polysilicon-to-silicon interfaces* (1988)(Ex. 1008; "Crabbé") explained that after "native oxide interface" break-up from annealing, "[t]he electrons flow preferentially through the openings in the native oxide interface, which are **paths of least resistance**."

165. As another example, *Polysilicon emitters for silicon concentrator solar cells* (Gan & Swanson 1990) explains that "[a]s the oxide starts to break up [due to the anneal], additional **highly conductive channels are created due to the intimate contacts formed between the polysilicon and the substrate in the broken regions**. See Ex. 1016 at 249.

166. As another example, "*Poly silicon Contacted Emitter Bipolar Transistors: Fabrication Development*" (1988) explains that annealing for 1000 C for 10 minutes "is long enough to obtain a uniform doping level in the polysilicon

and the temperature is high enough to break up a large portion of the interface oxide **resulting in a low emitter resistance**." *See*, *e.g.*, Ex. 1024 ("Neudeck") at 47. While Neudeck refers to 1000C instead of Yablonovitch's 900 C, a POSITA would understand that oxide break-up would also occur at 900 C. See, e.g., Ex. 1025 ("Wolstenholme") at 228 ("significant breakup of the oxide layer [] was observed occurred during the 900 °C drive-in").

(9) Element [1.e] providing at least one electrode over the passivating film, wherein the conductive dopant within the passivating film and throughout the interface passivation layer provides direct electrical connection between the at least one electrode and the substrate.

167. Yablonovitch discloses and/or suggests this limitation.

168. Yablonovitch discloses that "[t]he n^+ -SIPOS was contacted with a 0.5 cm x 1 cm evaporated silver electrode" (**providing at least one electrode over the passivating film**), as shown in Figure 2. Yablonovitch, 1212. As shown in Figure 2, the **provid[ed]** silver **electrode** is **over the** n^+ -SIPOS (**the passivating film**). Yablonovitch, 1212.

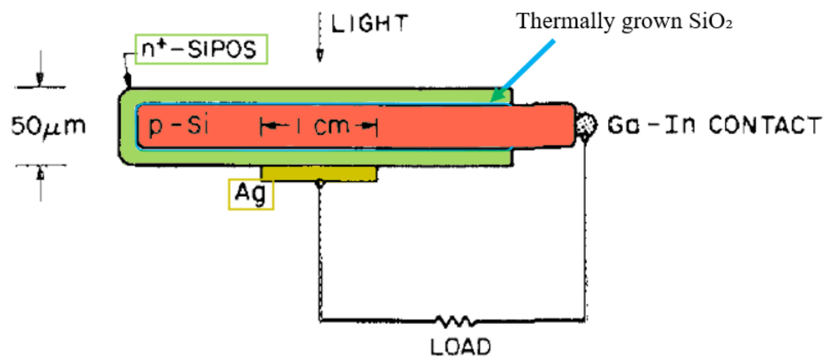


FIG. 2. Test configuration for the SIPOS : *c*-Si : SIPOS double heterostructure solar cells. In this design the fill factor was limited by the bulk resistance of the *p*-Si wafer itself.

Yablonovitch, FIG. 2

169. Yablonovitch's teaching that by diffusing phosphorus into the wafer and crystallizing the SIPOS, Yablonovitch creates an n^+/p "high-low" junction at the interface, which increases conductivity in the interface region and aligns the Fermi levels. Yablonovitch, 1212. As a result, carriers are able to take a direct route using these phosphorous dopant-created conductive pathways from the silicon wafer to the electrode through the composite layers. As discussed above in element [1.d3] (which I incorporate by reference), phosphorous diffusion from the n^+ SIPOS throughout the interfacial oxide and into the surface of the silicon wafer **to facilitate electrical connection to the substrate**, both by diffusion of phosphorous atoms and diffusion of phosphorous-containing micro crystallites that perforate the interfacial oxide. Accordingly, this phosphorous (**conductive dopant**) **within the** n^+ SIPOS (**passivating film**) and **throughout the** interfacial oxide (**interface passivation**

layer) **provides direct electrical connection between the at least one electrode and the substrate**.

170. Yablonovitch's device produces electric current from sunlight by a resulting direct electrical path that electrons travel from the crystalline silicon wafer to the silver electrode, meaning that the path of electrons in Yablonovitch's device travels along a **direct electrical connection between the at least one electrode and the substrate**. This occurs as follows.

171. First, electrons originate in the crystalline silicon wafer. Electrons, as minority carriers in the p-Si, are generated within the p-type crystalline silicon wafer by photon absorption. The fundamental operation of a solar cell involves the generation of electron-hole pairs in the semiconductor material when exposed to light. For the p-n junction of n^+-SIPOS and p-Si, holes are the majority carriers in the p-Sio substrate (or base) that need to be collected from the p-Si base.

172. Second, electrons are swept from the silicon wafer through an electrical connection across the interfacial oxide and thermal oxide to the n^+ SIPOS layer, as discussed in element [1.d3] (which I incorporate by reference). As discussed, phosphorous diffusion from the n^+ SIPOS throughout the interfacial oxide and thermal oxide and into the surface of the silicon wafer serves **to facilitate electrical connection to the substrate**, both by diffusion of phosphorous atoms and by diffusion of phosphorous-containing micro crystallites that perforate the interfacial

oxide. Accordingly, this phosphorous (**conductive dopant**) **within the** n^+ SIPOS (**passivating film**) and **throughout the** interfacial oxide (**interface passivation layer**) **provides direct electrical connection between the** silicon wafer and silicon wafer-facing surface of the n^+ SIPOS layer.

173. Third, electrons pass into and through the n^+-SIPOS layer. As discussed in element [1.c] (which I incorporate by reference), the n^+-SIPOS layer is highly conductive after annealing.

174. Fourth, electrons reach other side of the n^+-SIPOS layer and are collected by the silver electrode (described above).

175. Accordingly, phosphorous dopant-created conductive pathways **within the** n^+ SIPOS (**passivating film**) and **throughout the** interfacial oxide (**interface passivation layer**) **provides direct electrical connection between the at least one electrode and the substrate**.

b. Claim 2: The method of claim 1, wherein the thermally treating crystallizes, at least in part, the passivating film to establish a crystallized passivating film.

176. Yablonovitch explains that "[t]he annealing step (9)... is necessary to precipitate microcrystalline silicon grains within the material" (**the thermally treating crystallizes, at least in part, the passivating film to establish a crystallized passivating film**). Yablonovitch, 1212. This means the high-temperature anneal at 900 °C causes the initially deposited (amorphous) SIPOS to

become **a crystallized passivating film,** i.e., polycrystalline (with embedded microcrystals). Yablonovitch, 1212-13, FIG. 3 (showing the "microcrystalline silicon grains").

177. A POSITA would have understood that "precipitate microcrystalline silicon grains" means the SIPOS **crystallizes at least in part** because "precipitate" is referring to crystal precipitation. Yablonovitch, 1211. Crystal precipitation is one way to perform crystallization. *Id.*

178. SIPOS and polysilicon were well known to crystallize at an anneal temperature around 900 °C, and a POSITA would have recognized that Yablonovitch's SIPOS layer would have crystallized during the 900 °C anneal. *See*, *e.g.*, Ex. 1013 (*Fundamentals of Semiconductor Fabrication*) at 166 ("When phosphorous is diffused at 950 °C, the structure changes to crystallite, and grain size increases to a size between 0.5 and 1.0 μm.").

179. As another example, in 1994 *Characterization of SIPOS films by spectroscopic ellipsometry and transmission electron microscopy* ("Kragler") (Ex. 1007) provided a characterization analysis of SIPOS, and showed how "[a]fter annealing the amorphous films become polycrystalline whereby the volume fraction of c-Si increases with annealing temperature." Kragler at 79. This is shown in Figure 2, which shows the percent crystallization of silicon in SIPOS as deposited, and after subsequent anneal steps at various anneal temperatures. As shown,

Yablonovitch's high-temperature anneal of 900 °C (see Yablonovitch, 1212) would result in significantly increased percent crystallization of silicon in SIPOS, and therefore the SIPOS **crystallizes, at least in part** as a result of the anneal.

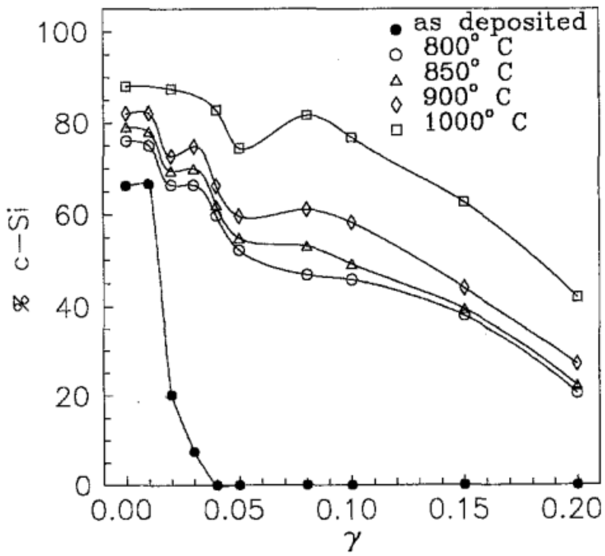


Fig. 2. Volume percentage of crystalline silicon in SIPOS deposited on quartz as a function of the N_2O to SiH_4 ratio γ in the gas flow for as deposited samples and after annealing at 800° C, 850° C, 900° C and 1000° C

Kragler, FIG. 2

180. In other words, "SIPOS can be regarded as a three component mixed phase consisting of crystalline and amorphous silicon as well as voids or SiO_2," and the anneal step results in a phase separation of amorphous silicon into crystalline Si grains. Kragler at 77-79.

181. As another example, in 1978 *Crystallographic study of semi-insulating polycrystalline silicon (SIPOS) doped with oxygen atoms* ("Hamasaki") (Ex. 1014)

provided a characterization analysis of the micro-crystals in SIPOS layers under various conditions. A shown in Figures 1 and 2, under identical thermal conditions as (650 °C deposition and 900 °C anneal –see Yablonovitch, 1212), Hamasaki shows that the annealing crystallizes SIPOS:

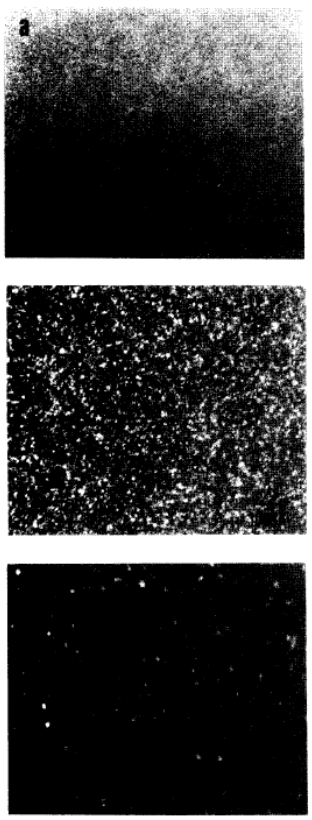


FIG. 1. Dark-field images of SIPOS with 15 at.% oxygen and deposited at 650°C. Specimens are (a) as-deposited (b) annealed at 900°C, and (c) annealed at 1100°C.

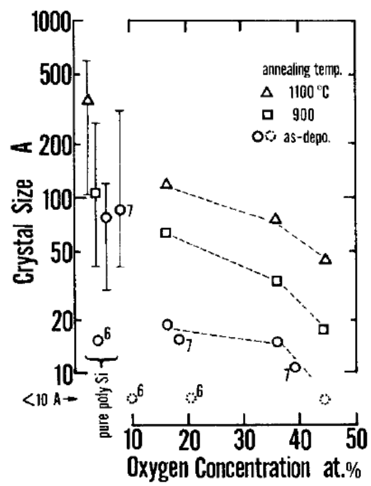


FIG. 2. Size of silicon micro-crystals in SIPOS evaluated from bright spots in dark-field images. Small numerals 6 and 7 indicate the deposition temperatures to be 600 and 700°C, respectively. Others were deposited at 650°C.

Hamasaki, FIGS. 1, 2

c. **Claim 3: The method of claim 2, wherein the crystallized passivating film is a transparent film.**

182. Yablonovitch discloses this claim.

183. The annealed n$^+$ SIPOS layer (**the crystallized passivating film**) **is a transparent film**. For example, this is why SIPOS can cover the light-facing side of the silicon substrate, and yet light is able to enter the silicon substrate to generate electrons.

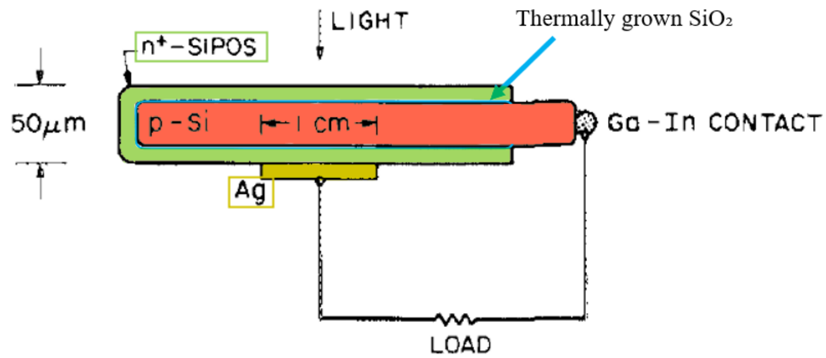


FIG. 2. Test configuration for the SIPOS : *c*-Si : SIPOS double heterostructure solar cells. In this design the fill factor was limited by the bulk resistance of the *p*-Si wafer itself.

Yablonovitch, FIG. 2

184. It is also my opinion that it was further known to a POSITA in the art before the relevant time that SIPOS was transparent. Yablonovitch, 1212 (noting that the SIPOS layer is transparent to light); *see also Id.* (noting that studies at the time predating the relevant time involve transparent SIPOS layers).

d. Claim 4: The method of claim 2, wherein the crystallization of the passivating film improves a passivation of the passivating film.

185. Yablonovitch discloses this limitation. I incorporate by reference my analysis for claim limitations [1.b] and [1.d2], which explain that **the crystallization**

of the SIPOS layer (**the passivating film**) expels oxygen to form an interfacial oxide and to form a thicker composite interfacial oxide with the existing thermal oxide, which **improves a passivation of the passivating film**.

e. Claim 6: The method of claim 1, wherein the interface passivation layer has a thickness selected to permit tunneling of electrical carriers through the interface passivation layer into the substrate.

186. Yablonovitch, in view of Kwark, discloses this limitation. I incorporate by reference my analysis of element 1b explaining Yablonovitch's disclosure of a "thin" (**thickness selected**) **interface passivation layer**. See, supra, Section X.A.2.a.(3).

187. How it **permits tunneling of electrical carriers through the interface passivation layer into the substrate** is a known phenomenon. As Kwark explains, the interfacial oxide (**the interface passivation layer**) is a "thin tunnelable oxide at the Si-SIPOS interface" (**has a thickness selected to permit tunneling of electrical carriers through the interface passivation layer into the substrate**). Kwark at p. 180. More specifically, Kwark explains that the physical properties and phenomenon that result in carrier transport properties are in relation to oxide thickness. Kwark at p. 181 (noting that oxide thickness is crucial to achieve a proper balance between low majority carrier series resistance and low hole tunnelling probabilities to avoid bulk resistivity).

f. Claim 7: The method of claim 1, wherein the thermally treating diffuses a portion of the conductive dopant through the interface passivation layer into the substrate.

188. Yablonovitch, in view of Kwark, discloses this limitation.

189. Claim 7 requires that the **thermally treating diffuses the conductive dopant through the interface passivation layer**, which corresponds to element 1d4. I incorporate by reference my analysis for element 1d4. *See, supra*, Section X.A.2.a.(8). Claim 7 additionally requires that "a portion" of that conductive dopant diffuses "into the substrate," and my analysis above showed Yablonovitch's disclosure of these features as well. See id.

190. Specifically, during Yablonovitch's anneal step (9), the phosphorus dopant (**conductive dopant**) diffuses throughout the interface passivation layer and also into the c-Si substrate by roughly 2–5 nm (**diffuses a portion of the conductive dopant through the interface passivation layer into the substrate**). Yablonovitch, 1212; *see also*, id. The result is a "shallow n^+ accumulation layer" at the wafer surface, essentially forming an n^+ region (caused by the presence of phosphorus dopant) in the wafer directly beneath/through the interface oxide. Yablonovitch, 1212.

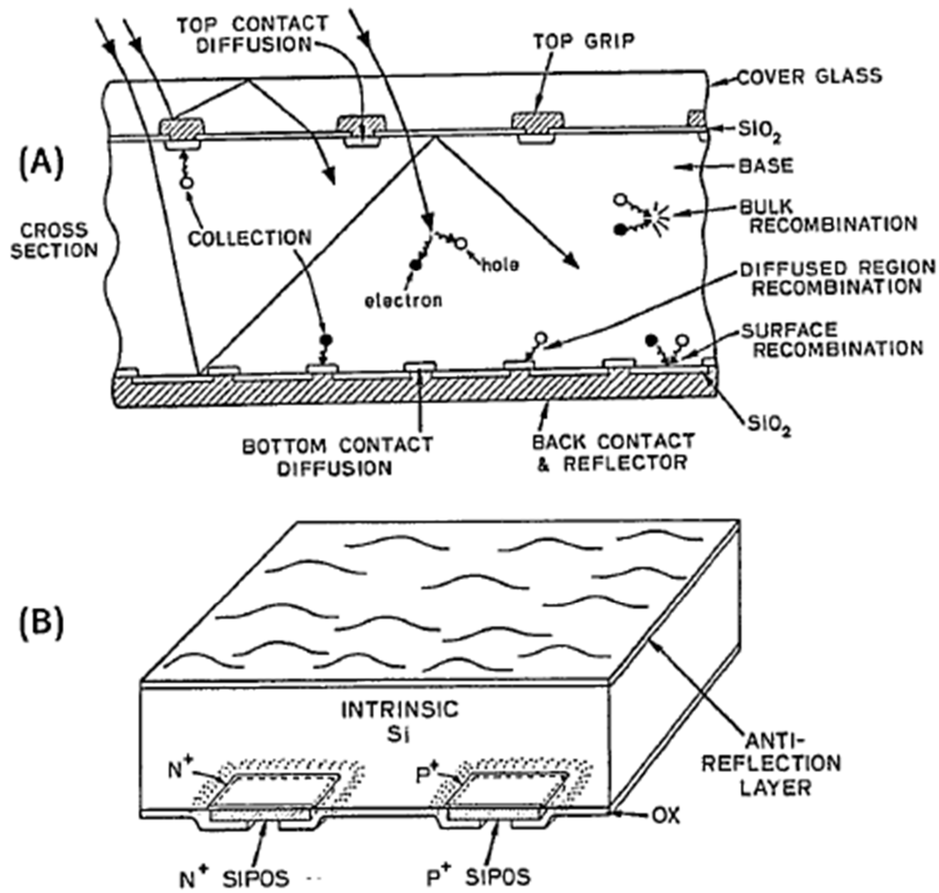
g. Claim 8: The method of claim 1, further comprising providing an anti-reflective film over the conductive upper surface of the passivating film.

191. Yablonovitch, and alternatively in view of Kwark, discloses this limitation.

192. Yablonovitch states, "The open circuit voltage was measured under a simulator at 1.3 suns. The light intensity was calibrated by two separate standard solar cells obtained from SERI. An intensity slightly above one sun was chosen in order to partially compensate for the absence of **an antireflection coating on the silicon wafer.**" Yablonovitch, 1211. However, a POSITA would understand this to mean that an anti-reflection film is present in Yablonovitch's solar cell design because Yablonovitch assumes that it would be present and adjusts the sun intensity during simulation to account for the anti-reflection film in the solar cell design.

193. Moreover, a POSITA would understand that providing an anti-reflection field would provide more accurate results and the actual sun intensity can be applied, instead of adjusting for it numerically. In fact, as Kwark explains, "the use of anti-reflection coatings (**an anti-reflective film**) and surface texturizing techniques [1] are common techniques employed to ensure that the incident light is tightly coupled to the bulk of the cell where generation takes place." Kwark, 10. A POSITA would understand that such teachings provide **an anti-reflective film over the conductive upper surface of the passivating film** because doing so minimizes the light coupled into the cell while maintaining the passivating layer and results in

more accurate simulation in Yablonovitch. Kwark depicts an anti-reflection layer below in Fig. 2.3 below.



Kwark, FIG. 2.3

h. Claim 9: The method of claim 1, wherein the at least one electrode only electrically connects to the substrate through the passivating film via the conductive dopant.

194. Yablonovitch discloses this limitation. I incorporate by reference my analysis for element [1.e], which explains how the phosphorous dopant (**the conductive dopant**) conductive pathways **provides direct electrical connection**

between the at least one electrode and the substrate. The electrode **only** electrically connects to the substrate as a result of the phosphorous dopant, as there are no other electrical connections between the substrate and electrode, and the electrical connection would not occur without the phosphorous dopant.

B. Yablonovitch in View of Kwark and Batra Renders Obvious Claim 5

1. Combined Teachings of Yablonovitch in View of Kwark and Batra

a. Motivation to Combine

195. It is my opinion that a POSITA would have been motivated to apply the teachings of Batra to Yablonovitch in view of Kwark. I incorporate by reference Section X.A.1 concerning the combination of Yablonovitch and Kwark.

196. It is my opinion that a POSITA would have been motivated to look to Batra to understand details about Yablonovitch's solar cell design. Specifically, Yablonovitch provides an interface passivation layer over the substrate with Step (6) of Yablonovitch's processing sequence. *See, supra*, Section X.A.2.a.(3). Yablonovitch provides a passivating film over the interface passivating layer with Steps (7)-(9). *See, supra*, Section X.A.2.a.(4). Yablonovitch illustrates the resulting structure in Figure 3, reproduced below.

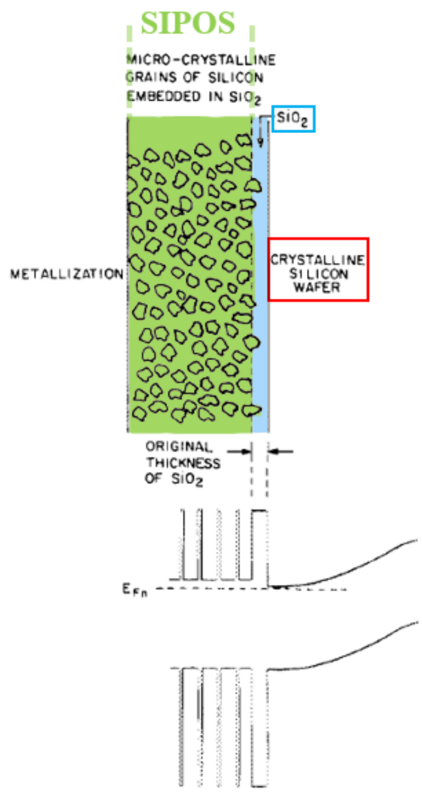


FIG. 3. Model for the metallurgical configuration of the SIPOS-Si heterojunction. Electron conduction is thought to proceed via the microcrystalline grains which protrude into the thin oxide layer.

Yablonovitch, FIG. 3

197. In addition, the thermal anneal of steps (8) and (9) "crystallizes, at least in part, the passivating film to establish a crystallized passivating film," which is also seen in Yablonovitch's Figure 3 above. *See also, supra*, Section X.A.2.b (claim 2). In its Figure 3 and description, Yablonovitch omits details of the effect of the passivating layer formed on the substrate. Indeed, Figure 3 of Yablonovitch does not depict the substrate ("crystalline silicon wafer") layer and interface passivation layer ("SiO_2"). A POSITA would understand that information is necessary to

understand whether the interface passivation layer **protects the substrate from crystallization or re-crystallization** during thermal annealing.

198. A POSITA reviewing Yablonovitch would therefore understand the importance of determining the effect of the interface passivation layer ("SiO_2") on the substrate ("crystalline silicon wafer") during anneal and would look to Batra for those details. A POSITA would look to Batra to understand the details missing from Yablonovitch because Batra taught and understood those details. A POSITA would have understood Batra's teachings to be beneficial to Yablonovitch since it teaches methods applicable to the passivation layer that enhance efficiency and uniformity of dopant diffusion.

b. Reasonable Expectation of Success

199. It is my opinion that a POSITA would have a reasonable expectation of success combining the teachings Batra with Yablonovitch. I incorporate by reference Section X.A.1 concerning the combination of Yablonovitch and Kwark.

200. Batra is also in the same field. *See* Sec. IX (overview of the prior art). As I further discussed above, Batra's teachings on nonuniformity in junctions, and thus it would have been obvious to a POSITA to rely on these teachings for Yablonovitch's interface passivation layer. A POSITA would have also had the skill to implement and reasonable expectation of success in achieving such a modification

because would naturally be a consideration in implementing Yablonovitch to ensure efficiency.

2. Application to the Challenged Claims

a. Claim 5: The method of claim 2, wherein the interface passivation layer protects the substrate from crystallization or re-crystallization during the thermally treating and crystallization of the passivating film.

201. Yablonovitch, in view of Kwark, and further in view of Batra renders obvious this limitation.

202. First, Yablonovitch, in view of Kwark, renders obvious claim 2, on which claim 5 depends. I incorporate by reference my analysis for claim 2 from ground 1 above, which explains how thermally treating the substrate crystallizes the passivating film to establish a crystallized passivating film. *See* Sec. X.A.2.b.

203. Second, a POSITA would have found it obvious to apply the teachings of Batra to Yablonovitch for the properties of an interface passivation layer formed over the substrate in Yablonovitch after annealing has completed. Specifically, Yablonovitch discloses that an interface passivation layer is formed over the substrate and a passivating film is formed over the interface passivation layer, and a thermal treatment (i.e., anneal) is performed to crystalize the passivating film. *See, supra*, Sections X.A.2.a.(3), X.A.2.a.(4), X.A.2.b. Batra provides further details teaches how thermal annealing affects the substrate's crystal structure and dopant diffusion. Batra, 955 (describing how higher-temperature or longer anneals cause

dopants to diffuse deeper in the substrate making the junctions more uniform). Batra's Figures 3 and 5 reproduced below illustrate that the crystallization of the Poly Si does not to create damage in the substrate and vice versa which a POSITA would understand is due to an interfacial oxide. In other words, the interface passivation layer **protects the substrate from crystallization or re-crystallization** during the thermally treating and crystallization of the passivating film.

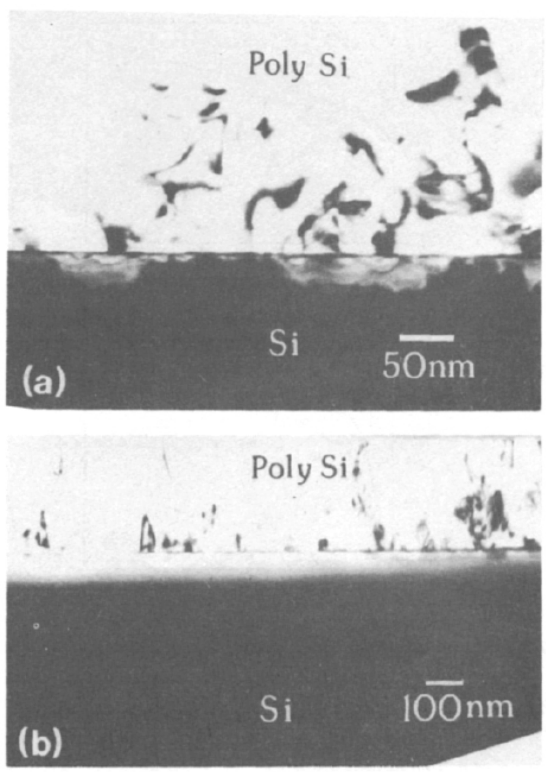


Fig. 3. XTEM micrographs of arsenic-implanted, (a) as-deposited amorphous Si; and (b) as-deposited polycrystalline Si films after at 60 s, 950°C RTA. A concentration-dependent etch was used to delineate the diffusion fronts.

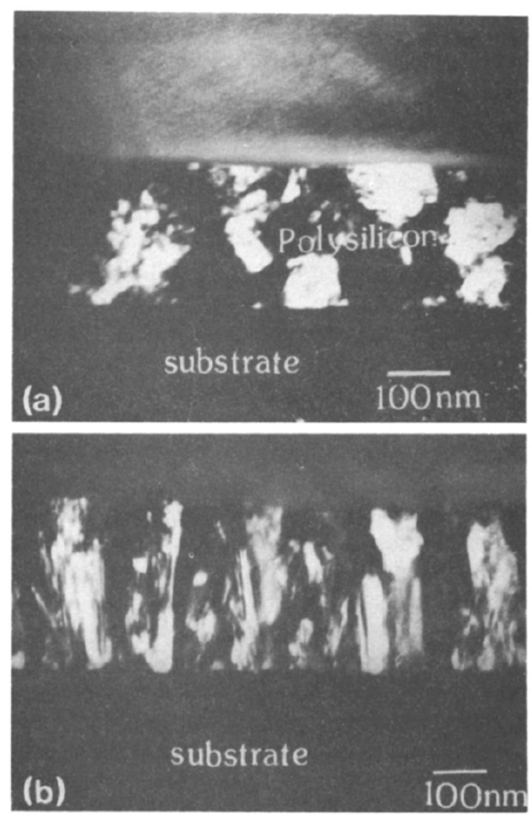


Fig. 5. XTEM micrographs of BF_2-implanted, (a) as-deposited amorphous Si, and (b) as-deposited polycrystalline Si films after a 60 s, 950°C RTA.

Batra, FIGS. 3, 5

204. Further Batra teaches that annealing changes the crystal structure and dopant distribution such that higher-temperature or longer anneals lead to a more

uniform junction, which resolves the underlying problem caused by crystallization or re-crystallization of the passivating film since the even dopant distribution reduces pn junction lateral non-uniformity. Lateral uniformities of the junction or other structural defects in the substrate can lead to an increase of the leakage current (i.e. J_o). *Id*, 959-960 ("for higher thermal budget anneals the leakage current decreases… not only because the junctions become deeper, but also because they become more uniform laterally as any doping inhomogeneities in the substrate get averaged out as the dopants diffuse in further", "higher-thermal-budget anneals result in lower leakage currents… because any doping inhomogeneities get smeared out, and also because the depletion region cannot probe the polycrystalline Si-single crystal Si interface as the junction gets deeper"). A POSITA would have recognized that the junctions are affected by the crystallization or re-crystallization structural changes occurring to the substrate.

XI. SECONDARY CONSIDERATIONS

205. I have seen no evidence of, and I am unaware of, any secondary indicia or considerations that would support non-obviousness of the features of the '732 patent, including commercial success, long-felt need, failure of others, skepticism, praise, teaching away, recognition of a problem or copying competitors. However, to the extent Patent Owner subsequently present such evidence, I respectfully reserve the right to respond at the time.

XII. CONCLUSION

206. For the foregoing reasons, I am of the opinion that claims 1-9 of the ’732 patent would have been obvious based on the prior art cited herein.

I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made arc punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: 8/15/2025

Respectfully Submitted

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Prof. Sanjay Banerjee, Ph.D.