UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,
Petitioner,

v.

138 EAST LCD ADVANCEMENTS LIMITED,
Patent Owner.

Case No. IPR2025-01396
U.S. Patent No. 7,636,146

PATENT OWNER'S PRELIMINARY RESPONSE

TABLE OF CONTENTS

TABLE OF AUTHORITIES

Page(s)

Cases

Statutes

Regulations

TABLE OF EXHIBITS

Number	Description
2001	Complaint for Patent Infringement, *Longitude Licensing Limited et al. v. BOE Technology Group Co., Ltd. et al.*, Dkt. 1, Case No. 2:25-cv-00358 (E.D. Tex.) (April 8, 2025)
2002	Complaint for Patent Infringement, *Longitude Licensing Limited et al. v. BOE Technology Group Co., Ltd. et al.*, Dkt. 1, Case No. 2:25-cv-00440 (E.D. Tex.) (April 25, 2025)
2003	Consolidation Order, *Longitude Licensing Limited et al. v. BOE Technology Group Co., Ltd. et al.*, Dkt. 23, Case No. 2:25-cv-00440 (E.D. Tex.) (August 14, 2025)
2004	Order Setting Scheduling Conference, *Longitude Licensing Limited et al. v. BOE Technology Group Co., Ltd. et al.*, Dkt. 15, Case No. 2:25-cv-00440 (E.D. Tex.) (August 15, 2025)
2005	Order Resetting Scheduling Conference, *Longitude Licensing Limited et al. v. BOE Technology Group Co., Ltd. et al.*, Dkt. 30, Case No. 2:25-cv-00440 (E.D. Tex.) (September 11, 2025)
2006	Defendant BOE Technology Group Co., Ltd.'s Amended Answer and Defenses to Plaintiffs' Complaint for Patent Infringement, *Longitude Licensing Limited et al. v. BOE Technology Group Co., Ltd. et al.*, Dkt. 32, Case No. 2:25-cv-00358 (E.D. Tex.) (September 16, 2025)
2007	Defendant BOE Technology Group Co., Ltd.'s Amended Answer and Defenses to Plaintiffs' Complaint for Patent Infringement, *Longitude Licensing Limited et al. v. BOE Technology Group Co., Ltd. et al.*, Dkt. 39, Case No. 2:25-cv-00440 (E.D. Tex.) (October 14, 2025)
2008	Declaration of E. Fred Schubert, Ph.D.
2009	Defendant LG Electronics Inc.'s Answer to Plaintiffs' Complaint for Patent Infringement, *Longitude Licensing Limited et al. v. BOE Technology Group Co., Ltd. et al.*, Dkt. 21, 2:25-cv-00440 (E.D. Tex.) (September 8, 2025)

I. PRELIMINARY STATEMENT

Pursuant to 37 C.F.R. § 42.107, Patent Owner 138 East LCD Advancements Limited ("138 East" or "Patent Owner") submits its Preliminary Response to the Petition for *Inter Partes* Review of U.S. Patent No. 7,636,146 ("the '146 patent"). Paper 2 ("Petition" or "Pet."). Petitioner BOE Technology Group Co., Ltd., challenges the validity of claims 1-23 of the '146 patent.

Petitioner's lead reference—Kitawada—does not disclose the claimed inventions. The '146 patent describes and claims particular LCD panel terminal arrangements—specifically, clock signal input terminals, image signal input terminals, and power source terminals having particular areas and relative sizes. Kitawada discloses nothing about terminal areas or relative sizes. The Petition's suggestion that Kitawada discloses all but a few claim limitations is misleading, because Kitawada does not disclose the key aspect of the claimed inventions.

Neither does any other asserted reference. Minami does not disclose a clock signal input terminal on an LCD panel *at all*, much less one having a particular width, area, or relative size. Minami does *not* disclose (1) clock signal input terminals on an electro-optical panel, (2) power source terminals on an electro-optical panel, or (3) any particular type of terminal having a larger width or area than others. And Sano teaches *away* from the claimed inventions because it discloses clock signal input terminals and image signal input terminals having the

same size, wider relative to *other* external connection terminals. No asserted combination discloses the claimed inventions. The Board should deny institution.

II. THE '146 PATENT

The '146 patent, titled "Electro-Optical Panel, System with Terminals Having Different Corresponding Characteristics," is directed to an improved liquid crystal display (LCD) panel including particular input terminals having larger areas than others. *See generally* Ex. 1001. The '146 patent claims priority to two Japanese patent applications, filed August 8, 2003, and June 30, 2004. *Id.* at 1.

The '146 patent explains that a "scanning-line drive circuit, which drives scanning lines, and a data-line drive circuit, which drives data lines, are sometimes formed on the electro-optical panel." *Id.* at 1:53-55. Thus, input terminals are provided on the panel to receive and supply power and signals to the drive circuits. *Id.* at 1:55-62 ("A power source, a driving signal, an image signal, etc. are supplied to the electro-optical panel having drive circuits.").

The '146 patent explains that, in general, "it is desirable that the size of the input terminal is large," because "the resistance of an input terminal becomes smaller as the area thereof becomes larger." *Id.* at 1:63-66. If "the area of the input terminal is made small in terms of the reduction of the mounting area, the contact resistance increases, and there has been a problem in that the driving signal cannot be input at a proper timing." *Id.* at 2:10-14. But the '146 patent balances resistance

optimization with space restrictions. Space is limited on an LCD panel, and a POSITA cannot enlarge the input terminals to decrease resistance and still dispose the terminals in a limited area in the panel's periphery. *Id.* at 1:66-2:2. The number of image signal input terminals, for example, may be too large. *Id.* at 2:3-20 ("In particular, in an electro-optical panel of the type which does not contain a data-line drive circuit, or an electro-optical panel of the type which contains a multiplexer, it is necessary to take a plurality of image signals into the electro-optical panel, and thus the number of the input terminals becomes large.").

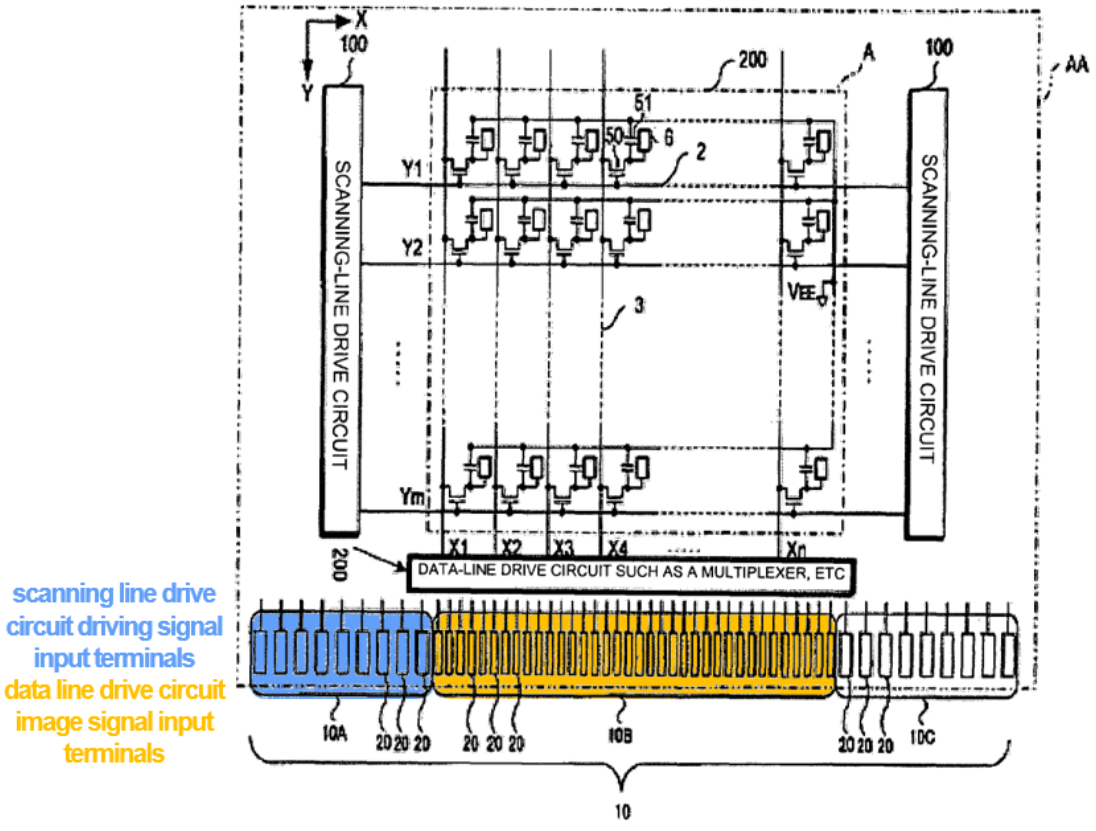
In particular, the '146 patent describes and claims clock signal input terminals having a larger area than image signal input terminals. The '146 patent explains that higher-frequency terminals should have a larger area than lower-frequency terminals. *Id.* at 2:24-41. "[T]hus it is possible to make smaller the area of the input terminal capable of sufficiently transmitting the signal in spite of a large time constant," and "it is preferable that the area of the input terminal supplied with the plurality of input signals is set in accordance with the frequency characteristics of the input signal." *Id.* at 2:44-52. In particular, the '146 patent describes and claims providing driving signal input terminals (e.g., clock signal input terminals) having a larger area than image signal input terminals. *Id.* at 2:59-67; *see also id.* at 7:30-32 ("the driving signal includes a Y transmission start pulse DY, a Y clock signal YCK, an inverted Y clock signal YCKB, and the like").

"[I]n order for the driving signal to be transmitted without becoming dull, it is necessary to decrease the time constant of the equivalent low-path filter," in other words, decrease resistance. *Id.* at 7:41-43. "Thus, in this embodiment, the area of the input terminal to which the driving signal is supplied is made larger compared with that of the input terminal to which the image signal is supplied." *Id.* at 7:48-51. "In this case, the waveform of the driving signal is captured into the electro-optical panel without becoming dull, and thus an erroneous operation of displaying an image can be prevented." *Id.* at 2:67-3:3. And "[a]t the same time, the area of the input terminal of the image signal can be made small, and thus multiple input terminals can be disposed in a limited area." *Id.* at 3:3-5. Thus, the invention optimizes signal functionality within a limited space on the LCD panel. The prior art does not disclose adjusting and prioritizing input terminal size in this way.

The '146 patent also explains that disposing the larger input terminals at the outer side of the LCD panel substrate provides the added advantage of "prevent[ing] a connection failure because of the difference in the contraction rates" when connecting the input terminals using anisotropic conductive film (ACF). *Id.* at 3:10-22 ("Therefore, by disposing an input terminal having a wider area at a more outer side than the input terminal having a smaller area, it is possible to prevent a connection failure because of the difference in the contraction rates as

long as the input terminal is a large one even if a slight misalignment of the connection arises.").

The '146 patent further describes and claims providing larger-area power source terminals. "In general, if a power source, which is input into a power terminal, has a high resistance, the voltage is trapped, and there is a strong possibility that a predetermined voltage cannot be obtained." *Id.* at 3:27-30. "Therefore, the power source preferably has as low a resistance as possible. Accordingly, in the above-described panel, the power terminal to which power is supplied preferably has the same area or more as the area of the input terminal to which the driving signal is supplied." *Id.* at 3:30-35.



Id. at Fig. 10 (annotations added, blue showing larger-area clock signal input terminal, orange showing smaller-area image signal input terminal).

The ’146 patent has three independent claims. Claim 10 recites:

> 10. An electro-optical panel comprising:
>
> a first substrate;
>
> data lines;
>
> scanning lines intersecting the data lines;
>
> pixels disposed corresponding to intersections between the data lines and the scanning lines;
>
> a clock-signal input terminal supplied with a clock signal and connected to a mounting member through anisotropic conductive film;
>
> image-signal input terminals supplied with image signals and connected to the mounting member through anisotropic conductive film, the clock-signal input terminal and the image-signal input terminals being disposed along one side of the first substrate, the image signals being supplied from an external data drive circuit and being supplied simultaneously to all of the data lines; and

a scanning-line drive circuit that is formed on the first substrate and that sequentially transmits a transmission start pulse in synchronization with the clock signal,

wherein the clock-signal input terminal overlaps a first wiring of the mounting member through said anisotropic conductive film by a larger area than an area at which at least one of the image-signal input terminals overlaps a second wiring of the mounting member through said anisotropic conductive film.

Id. at 14:13-38. Claim 23 recites:

23. An electro-optical panel comprising:

a substrate;

data lines;

scanning lines intersecting the data lines;

pixels disposed corresponding to intersections between the data lines and the scanning lines;

a clock signal input terminal supplied with a clock signal;

an image signal input terminal supplied with an image signal;

a scanning line drive circuit that outputs scanning signals to the scanning lines, image signals from the data lines supplied to the pixels are selected by the scanning signals;

wherein the data lines, the scanning lines, the pixels, the clock signal input terminal and the image signal input terminal are implemented on the substrate; and

a mounting member that is distinct from and connected to the substrate, the mounting member comprising:

a first wiring that is connected to the clock signal input terminal; and

a second wiring that is connected to the image signal input terminal,

wherein the clock signal input terminal overlaps the first wiring of the mounting member by a larger area than an area at which at least one of the image signal input terminals overlaps the second wiring of the mounting member.

Id. at 15:17-16:21. And claim 1 recites:

1. An electro-optical panel comprising:

a plurality of data lines;

a plurality of scanning lines intersecting the plurality of data lines;

a plurality of pixels disposed corresponding to the intersections between the data lines and the scanning lines;

a clock signal input terminal supplied with a scanning line clock signal;

an image signal input terminal supplied with an image signal;

a scanning line drive circuit that sequentially transmits a transmission start pulse in synchronization with the scanning line clock signal and outputs a scanning signal to each of the plurality of scanning lines, image signals from the plurality of data lines are supplied to pixels selected by the scanning signals;

a drive circuit which controls a grayscale of the pixels based on the scanning line clock signal and the image signal; and

a third input terminal, wherein the third input terminal comprises a power source terminal supplied with a power source, and the area of the third input terminal is not smaller than that of the first clock signal input terminal, wherein the clock signal input terminal has a larger area than the image signal input terminal, and

wherein a plurality of the power source terminals, a plurality of the first clock signal input terminals, and a plurality of the second image signal input terminals are included;

the plurality of the power source terminals, the plurality of the first clock signal input terminals, and the plurality of the second image signal input terminals are formed in line on a substrate; and

a pitch interval of the adjacent first clock signal input terminals is an integer multiple of a pitch interval of the adjacent second image signal input terminals.

Id. at 13:2-39.

III. CLAIM CONSTRUCTION

No claim term requires express construction to determine that the Petition does not establish a reasonable likelihood of unpatentability of any challenged claim. For purposes of this Preliminary Response, Patent Owner contends that the claim terms should receive their ordinary and customary meaning in light of the specification and prosecution history, as understood by a person of ordinary skill in the art. 37 C.F.R. § 100(b); *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005).

IV. LEGAL STANDARD

The Board may not institute *inter partes* review unless the Petition demonstrates a reasonable likelihood that the petitioner would prevail with respect to at least one of the claims challenged in the petition. 35 U.S.C. § 314(a).

V. LEVEL OF ORDINARY SKILL IN THE ART

For purposes of this Preliminary Response only, Patent Owner does not dispute the level of skill for a person of ordinary skill in the art ("POSITA"), set forth in the Petition. Pet. at 15-16; Ex. 2008 ¶¶ 19-22. The level of skill in the art does not affect whether to deny institution. Patent Owner does not waive, however, any argument regarding the proper level of skill and reserves the right to later advance additional arguments.

VI. THE PETITION DOES NOT ESTABLISH A REASONABLE LIKELIHOOD THAT THE ASSERTED COMBINATIONS RENDER OBVIOUS ANY CHALLENGED CLAIM.

A. The Petition does not establish a reasonable likelihood that Kitawada in view of Kawaguchi, Matsumoto, and Minami or Sano renders obvious claims 10-23 (Ground 1).

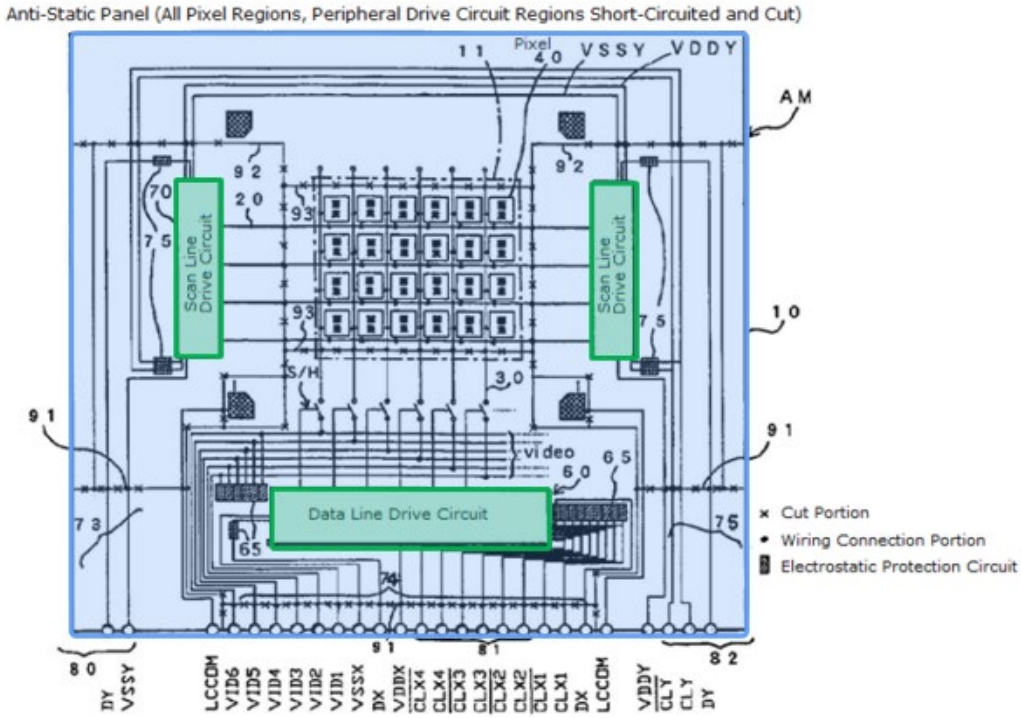
1. Kitawada: Overview

Kitawada discloses nothing about input terminal areas or relative sizes—it addresses a different problem regarding electrostatic damage, unrelated to input terminal size. Kitawada, titled "Method for Manufacturing Active Matrix Substrate and Liquid Crystal Display Device," describes "a method for manufacturing an active matrix substrate able to flatten unevenness and expose the short-circuit wiring without increasing the number of steps even when pixel electrodes and drain regions are electrically connected via a drain electrode." Ex. 1004 at Abstract. Kitawada "relates more specifically to a technique for protecting drive circuits from static electricity generated during the manufacturing process for active matrix substrates and from charges that have accumulated on insulating substrate surfaces." *Id.* ¶ [0001].

Relevant here, Kitawada describes "an active matrix substrate with built-in drive circuits." *Id.*; *see also id.* ¶ [0002] ("The outer region of the pixel portion on the insulating substrate comprises a data line drive circuit unit that supplies video signals to each of the data lines, and scan line drive circuits that supply scanning

signals to each of the scan lines."). "A data line drive circuit 60 is configured in the outer region (peripheral portion) of the pixel portion 11 on the insulating substrate 10 to supply video signals to each of the data lines 30. In addition, scan line drive circuits 70 are configured at the ends of each scan line 20 to supply scan signals for pixel selection to each scan line 20." *Id.* ¶ [0018].

[FIG. 2]



Id. at Fig. 2 (annotations added, blue identifying active matrix substrate and green identifying built-in drive circuits).[1]

[1] Kitawada describes "data line drive circuit" 60 as including "an X-side shift register circuit, a sample hold circuit S/H equipped with TFTs that function as

"The data line drive circuit 60 comprises an X-side shift register circuit, a sample hold circuit S/H equipped with TFTs that function as analog switches based on signals outputted from the X-side shift register circuit, and six video signal lines corresponding to each of the video signals VD1 to VD6 expanded to six phases." *Id.* ¶ [0019]. Start signal DX, clock signals CLX1 through CLX4, and inverted clock signals CLX1 bar through CLX4 bar are provided to the shift register circuit. *Id.* And "start signal DY, clock signal CLY, and inverted clock signal CLY bar are supplied from outside via terminals to the scan line drive circuits 70, and the scan line drive circuits 70 are driven by these signals." *Id.* The drive circuits are also connected to "power supplies VDDX, VSSX, VDDY, VSSY." *Id.* ¶ [0020].

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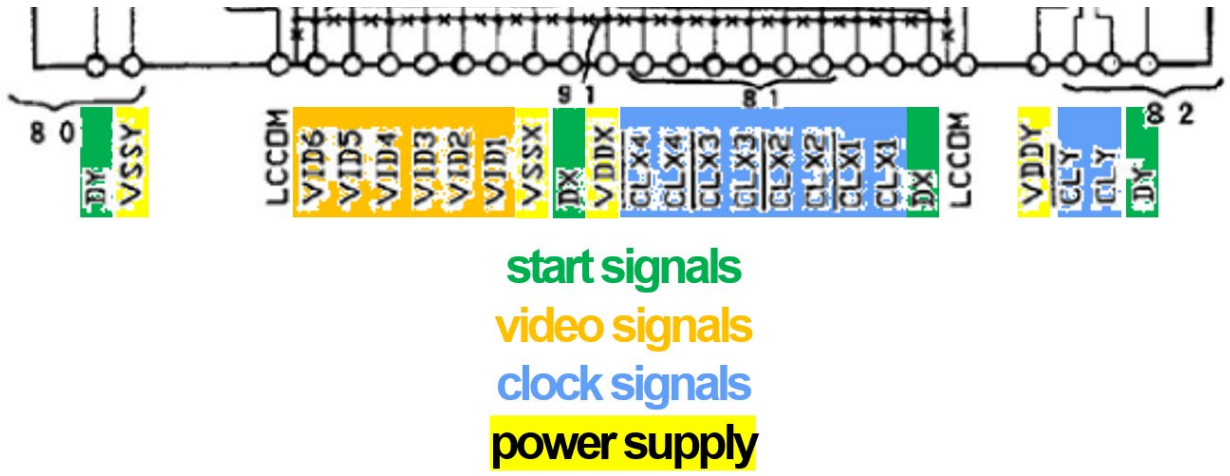
analog switches based on signals outputted from the X-side shift register circuit, and six video signal lines corresponding to each of the video signals VD1 to VD6 expanded to six phases," Ex. 1004 ¶ [0019], and thus arguably the green box should extend around the VD lines and switches, too. For purposes of these POPR arguments, that annotation distinction is not material. Arguably box 60 in Fig. 2 captures only the shift register circuit.

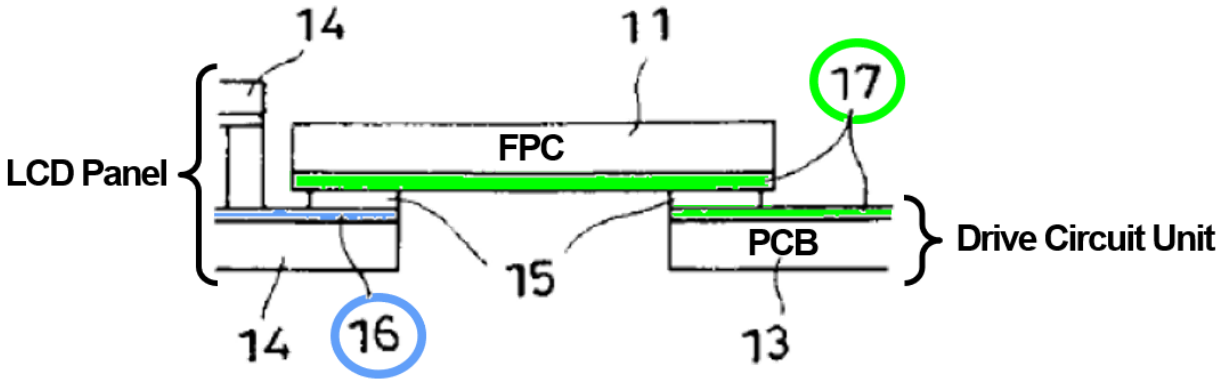


Id. at Fig. 2 (annotations added); *see also* Ex. 2008 ¶¶ 40-42.

2. Minami: Overview

Minami, titled "Liquid Crystal Display Device," describes a liquid crystal display unit and a separate drive circuit unit. Ex. 1007 at 13 ("As shown in FIG. 4, the liquid crystal display device (LCD) comprises an LCD panel 10 formed from a glass material, a drive circuit board 12 that drives the display, and an FPC board (flexible printed circuit board) 11 that electrically connects the LCD panel 10 and the drive circuit board 12."). Minami describes connecting the drive circuit unit on a printed circuit board to the liquid crystal display unit (or LCD panel) using a flexible printed circuit board, or FPC. *Id.* ITO electrodes (16, blue) on the LCD panel connect to FPC wiring electrodes (17, green), which connect to drive circuit unit wiring electrodes on a printed circuit board (PCB):

FIG. 5

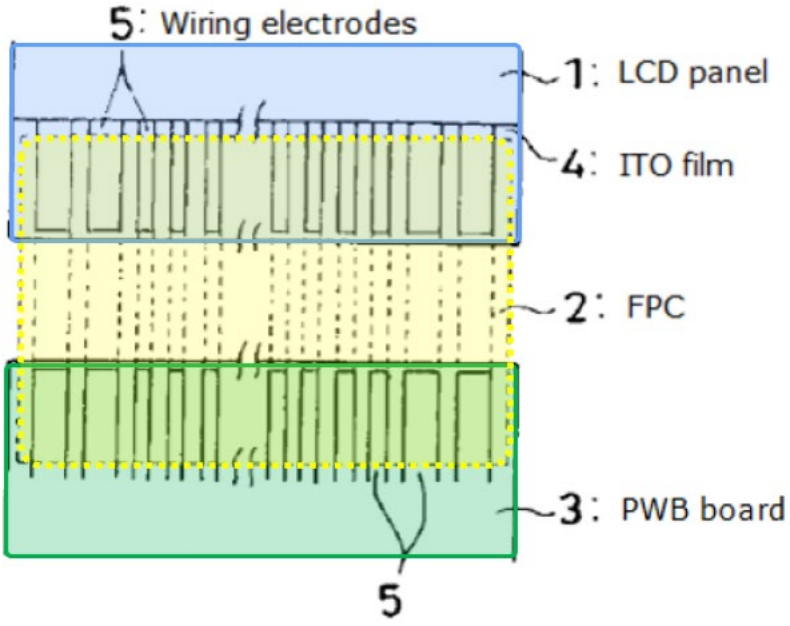


Id. at 13, Fig. 5 (annotations added).

Minami states that "[r]ecent large dot matrix displays require high-density terminal pitch connections . . . between the drive circuit board and the display unit." *Id.* at 13. Minami explains that "[w]hen the pitch is approximately 100 to 200 μm, the bonding area between the anisotropic conductive film and the LCD panel electrode terminals is small," which decreases bonding strength. *Id.* Further, "external pressure, vibrations, and other factors cause stress on both ends of the FPC board, resulting in frequent electrical connection failures at both terminals." *Id.*

Minami describes a purported solution to accommodate voluminous, densely packed terminals and effective FPC bonding. Specifically, Minami discloses an arrangement in which "the pattern width near both ends of the electrode terminals connecting the liquid crystal display unit and the drive circuit unit is wider than the pattern width near the center." *Id.* at 14.

FIG. 1



Id. at Fig. 1 (annotations added, blue identifying LCD panel, green identifying printed circuit board (drive circuit unit), and yellow identifying flex connecting the panel and the drive circuit unit).

Minami does *not* disclose (1) clock signal input terminals on an electro-optical panel, (2) power source terminals on an electro-optical panel, or (3) any particular type of terminal having a larger width or area than others. Minami's disclosed LCD arrangement confirms that the input terminals on the LCD panel receive drive circuit unit signals—i.e., data line signals and/or scanning line signals. Indeed, because Minami discloses only an arrangement in which the drive circuit unit is off-panel and connected to the LCD panel through an FPC and wiring electrodes, a POSITA would understand that the LCD panel does *not*

include clock signal input terminals. The ITO electrodes on the LCD panel are connected to the drive circuit unit *outputs*, for example, image signals supplying the LCD panel's data lines. The LCD panel would not receive a clock signal. *See generally* Ex. 1007; *see also* Ex. 2008 ¶¶ 43-47.

3. Sano: Overview

Sano, titled "Liquid Crystal Display Device," describes an LCD device in which "the terminal width and the pitch between adjacent external connection terminals that transmit high-frequency signals such as clock signals or data signals of the driving circuit are formed wider than those of other external connection terminals." Ex. 1006 at 6 (claim 1). "In order to prevent malfunctioning of the driving circuit due to high-frequency signals, the width . . . of the external connection terminal of the signal terminal for the high-frequency signal is made wider than the width . . . of other external connection terminals." *Id.* at 5 (Abstract).

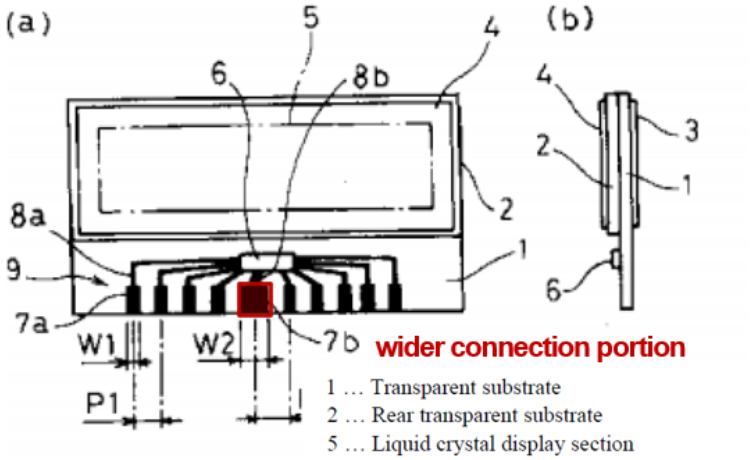
Sano explains that clock signals *and data signals* (i.e., image signals)[2] are high-frequency signals and that those external connection terminals may be wider

[2] A POSITA would understand that "data signals" of the driving circuit refers to and includes "image signals." Ex. 2008 ¶ 49. The Petition does not suggest otherwise.

than other external connection terminals. "[T]he connection portion 7b of the transparent substrate electrode 9, the wiring extension portion 8b, and the electrode portion 10b of the printed circuit board 10 serve as terminals for transmitting high-frequency signals such as clock signals or data signals of the liquid crystal panel driving circuit." *Id.* ¶ [0013]; *see also id.* ¶ [0006] ("signal waveforms may become distorted when transmitting high-frequency signals such as clock or data signals"). Thus, Sano does not disclose clock signal terminals having a larger area than data (i.e., image) signal input terminals. *See generally* Ex. 1006; Ex. 2008 ¶¶ 48-49.

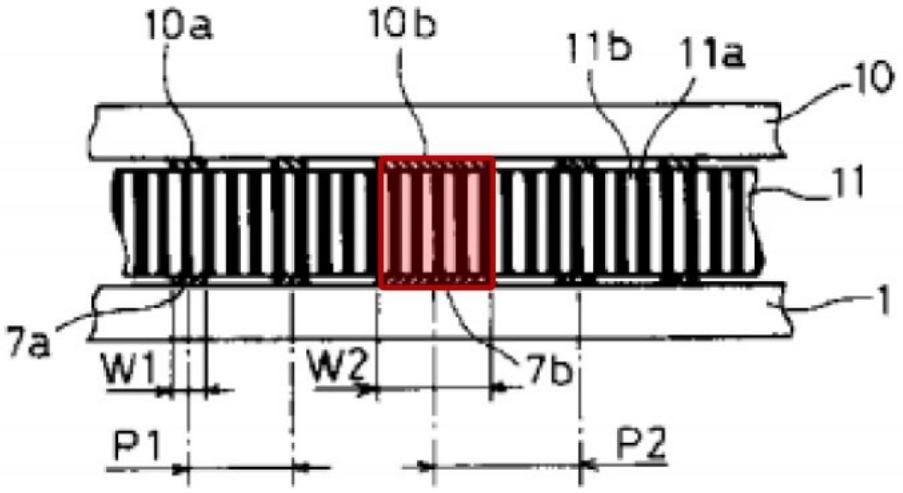
Sano also discloses providing the wider, high-frequency external connection terminals (7b) toward the center of the LCD substrate:

[Figure 1]



Ex. 1006 at Fig. 1 (annotations added).

[Figure 2]



Id. at Fig. 2 (annotations added). "Furthermore, as shown in Figure 1(a), the connection portion 7b of the transparent substrate electrode 9—which transmits high-frequency signals—may be arranged closer to the liquid crystal panel driving IC 6." *Id.* ¶ [0015]. "This enables the wiring lead-out portion 8b of the transparent substrate electrode 9 to be shortened, thereby further reducing wiring resistance, and also contributing to improved malfunction prevention." *Id.*

Sano also describes connecting a printed circuit board to the external connection terminals using a "zebra rubber connector." *Id.* ¶¶ [0004], [0012]. Sano's purported solution is directed to arrangements using a zebra connector, in which "the connection resistance through each conductive section 11a of the zebra rubber connector 11 is relatively high." *Id.* ¶¶ [0006] ("Due to this high connection

resistance from the electrode portion 10a of the printed circuit board 10 through the conductive section 11a of the zebra rubber connector 11 to the connection portion 7a of the transparent substrate electrode 9, signal waveforms may become distorted when transmitting high-frequency signals such as clock or data signals."), [0014] ("As a result of adopting such an electrode structure, the number of conductive sections 11a in the zebra rubber connector (11) that connect the connection portion 7b of the transparent substrate electrode (9) to the electrode portion 10b of the printed board (10) becomes greater than the number used in connecting the other portions (7a and 10a)."). *See also* Ex. 2008 ¶¶ 50-52.

4. The Petition fails to show that Kitawada in view of Kawaguchi, Matsumoto, and Minami or Sano discloses or renders obvious all limitations of any of challenged claims 10-23.

Kitawada in view of Kawaguchi, Matsumoto, and Minami or Sano does not render obvious any challenged claim. In particular, no asserted reference—and thus, no asserted combination—discloses a key aspect of the claimed inventions: clock signal input terminals having a larger area than image signal input terminals. *Id.* ¶ 53 *et seq.*

a. Claim 10

i. The Petition does not show that Kitawada in view of Kawaguchi, Matsumoto, and Minami or Sano discloses or renders obvious "wherein the clock-signal input terminal overlaps a first wiring of the mounting member through said

anisotropic conductive film by a larger area than an area at which at least one of the image-signal input terminals overlaps a second wiring of the mounting member through said anisotropic conductive film" (claim 10[j]).

The Petition concedes that its lead reference, Kitawada, "does not disclose [clock signal input terminal and image signal input terminal] relative areas," and that Kitawada does not "disclose larger area clock signal . . . terminals." Pet. at 6, 33. Indeed, Kitawada does not describe width, area, or other size information of its input terminals. Nor does Kitawada describe whether or how its input terminals overlap "mounting member" wiring, as recited in claim 10. Thus, the Petition relies on Minami or, in the alternative, Sano to disclose "wherein the clock-signal input terminal overlaps a first wiring of the mounting member through said anisotropic conductive film by a larger area than an area at which at least one of the image-signal input terminals overlaps a second wiring of the mounting member through said anisotropic conductive film." Ex. 1001, claim 10[j]. But neither Kitawada in view of Minami nor Kitawada in view of Sano discloses the limitation. Ex. 2008 ¶¶ 54-56.

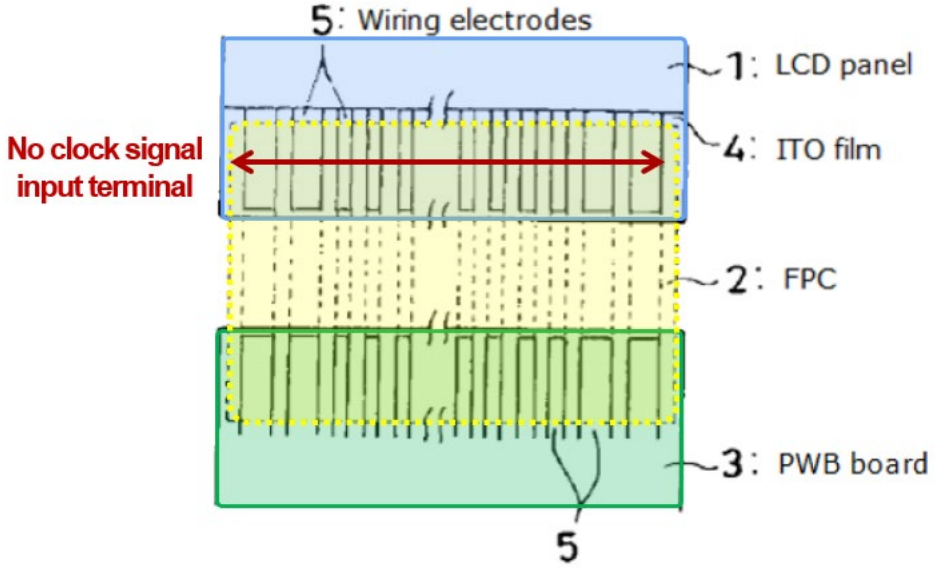
Minami

Minami does not disclose "wherein the clock-signal input terminal overlaps a first wiring of the mounting member through said anisotropic conductive film by a larger area than an area at which at least one of the image-signal input terminals

overlaps a second wiring of the mounting member through said anisotropic conductive film." Minami describes providing wider electrode terminals "near both ends of the electrode terminals." Ex. 1007 at 14. But Minami does *not* disclose a clock signal input terminal, much less a clock signal input terminal that is wider or otherwise larger than an image signal input terminal. Ex. 2008 ¶ 57.

Indeed, Minami describes only an LCD arrangement in which the drive circuit unit is off-panel, on a separate printed circuit board, and connected to the LCD panel through a flexible printed circuit board and wiring electrodes. *See* § VI.A.2, *supra*. Thus, a POSITA would understand that Minami's LCD panel does *not* include a clock signal input terminal. The LCD panel would not receive a clock signal—the drive circuit unit on the separate PCB would. And the drive circuit unit would not send that clock signal to the LCD panel—it would send data line and/or scanning line signals. A clock signal is required at the input of a driving circuit (e.g., a scanning line driving circuit) but would *not* be provided at the output of a driving circuit, because none of the data lines and scanning lines of an LCD panel's active matrix receive a clock signal. Ex. 2008 ¶ 58.

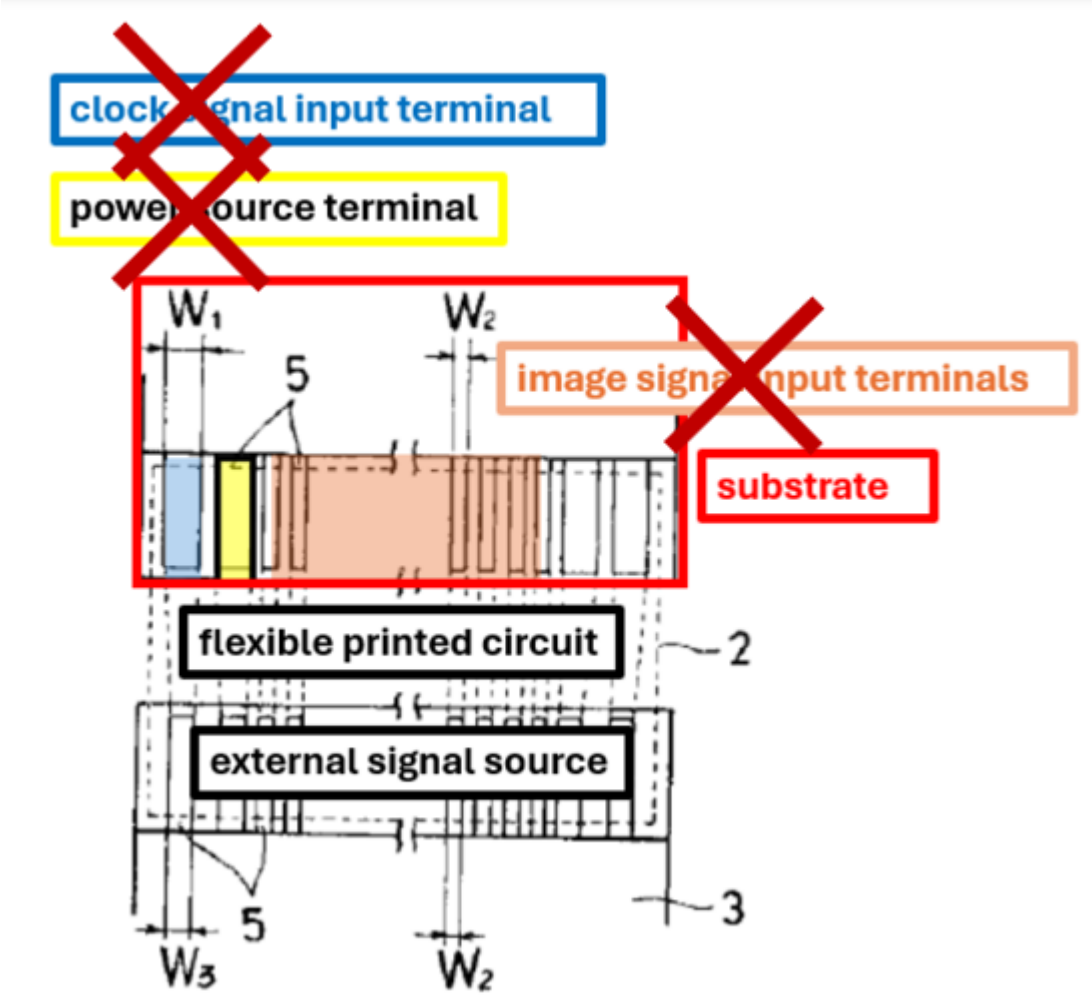
FIG. 1



Ex. 1007 at Fig. 1 (annotations added). Minami does not disclose or describe, and its teachings are not directed to, clock signal input terminals. Rather, Minami describes ITO electrodes/wiring on the LCD panel that connect to drive circuit unit wiring lines. A POSITA would understand that Minami's LCD panel receives signals from the drive circuit unit, for example, data line signals. *See generally* Ex. 1007; *see also* Ex. 2008 ¶ 58. A POSITA would understand that Minami's terminals correspond to data lines and scanning lines. Ex. 2008 ¶ 58.

Petitioner cites an annotated version of Minami Figure 3 throughout the Petition. Those annotations are not supported by, and are contrary to, Minami's disclosure. Minami discloses an LCD arrangement including an off-panel drive

circuit unit, such that the LCD panel could *not* include a clock signal input terminal as Petitioner has annotated:



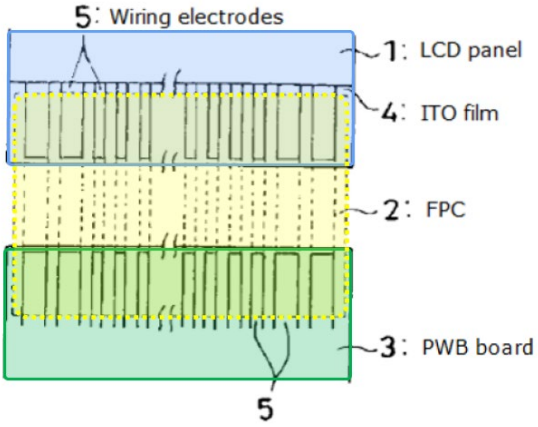
See, e.g., Pet. at 22 (Petitioner's annotations, red Xs added identifying unsupported annotations). Minami does not disclose clock signal input terminals or power source terminals on an LCD panel, much less those particular terminals in the particular arrangement and in the particular order that Petitioner shows (using the '146 patent as a guide). Minami's disclosure *contradicts* Petitioner's self-serving annotations. Minami does not disclose limitation 10[j]. And thus no reference in

Petitioner's proposed combination, alone or in combination—Kitawada in view of Kawaguchi, Matsumoto, and Minami—does. Ex. 2008 ¶ 59.

Moreover, the Petition does not show that a POSITA would have been motivated to apply Minami's teachings to Kitawada. To start, Minami and Kitawada disclose different LCD arrangements. Minami discloses off-panel drive circuit units, and Kitawada discloses scanning line drive circuits and a data line drive circuit on the LCD panel substrate. *Compare* Ex. 1007 at 13, Fig. 1 *with* Ex. 1004 ¶ [0001] ("The present invention relates to a method for manufacturing an active matrix substrate with built-in drive circuits . . . ."), Fig. 2.

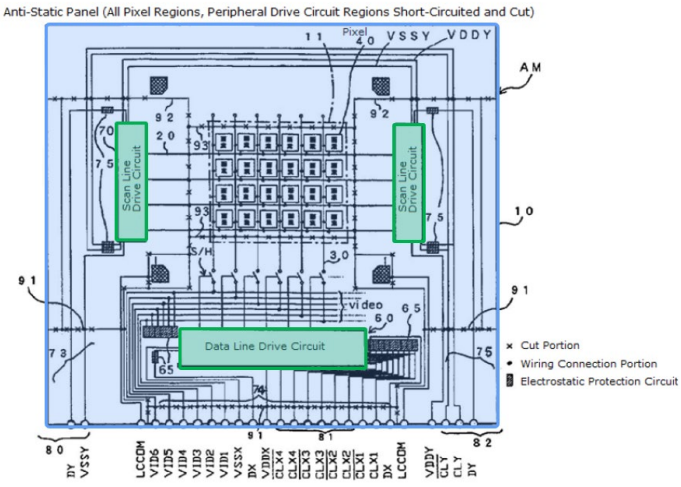
Minami

FIG. 1



Kitawada

[FIG. 2]



See also Ex. 2008 ¶ 60.

Relevant to its particular "off-panel" arrangement, Minami describes an LCD panel terminal arrangement for "displays [that] require high-density terminal

pitch connections . . . *between the drive circuit board and the display unit*." Ex. 1007 at 13. Kitawada does *not* disclose an LCD arrangement requiring connections *between a drive circuit board and a display unit*—Kitawada's drive circuits are built-in, and its terminals 80, 81, and 82 do not facilitate connections between a drive circuit board and a separate display unit. Kitawada discloses a discrete number of terminals, including only six VD lines. Indeed, Kitawada discloses a multiplexer / de-multiplexer drive circuit, which reduces the number of image data line inputs. Ex. 2008 ¶ 61. A POSITA would understand that Minami's disclosure contemplates more terminals—possibly as many terminals as data lines and/or scanning lines, because the panel terminals connect to the drive circuit unit's output lines. Minami's solution does not apply to and is incompatible with Kitawada's layout in which the panel accommodates far fewer input terminals. *Id.* The Petition does not address these aspects of the asserted references.

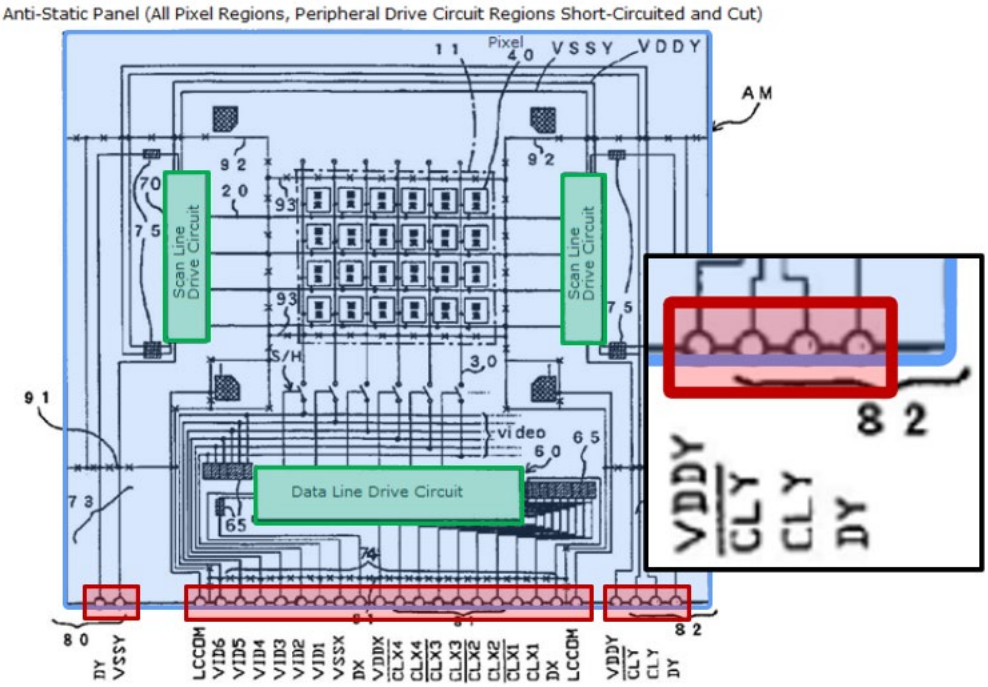
And to the extent that the Petition tries to apply Minami's teachings regarding connection mechanics outside of its particular application (i.e., dense connections between drive circuit board and display unit), Kitawada already discloses a particular terminal arrangement that ensures that "a flexible wiring substrate, etc., can be connected to the pads 9c (terminals) with a high degree of reliability." Ex. 1004 ¶ [0029]; Ex. 2008 ¶¶ 62-63.

The Petition does not contend with any of these disclosures or explain how or why a POSITA would be motivated to modify Kitawada's terminal arrangement in view of Minami.

In addition, the Petition does not explain how or why a POSITA would map Minami's "wider terminal" teachings to Kitawada's *clock* signal input terminals. The Petition uses hindsight and relies heavily (and exclusively) on Kitawada Figure 2, showing a clock signal input terminal near the end of the terminal arrangement. But Kitawada does not disclose how external signals (e.g., clock signal CLY, video signals VD) connect to its terminals, or whether the terminals would connect to external signals in more than one "group." Ex. 2008 ¶ 64.

For example, a POSITA would understand that Kitawada teaches several distinct terminal "groups" 80, 81, and 82. A POSITA would understand that those terminal groups could connect to external signals using more than one FPC and/or more than one PCB. Thus, Minami's teaching regarding "end" terminals and "central" terminals are not specific to Kitawada's clock or image signal input terminals, respectively. As just one example, Kitawada's clock signal input terminal connected to the scanning line driving circuit could be a *central* terminal rather than a wider *end* terminal, if terminal group 82 is connected to its own "mounting member":

[FIG. 2]



Ex. 1004 at Fig. 2 (annotations added); *see also* Ex. 2008 ¶ 65. The Petition relies on little more than impermissible hindsight to suggest that Minami's non-specific teachings must map to specific terminals.

The Petition cannot show that Kitawada in view of Minami discloses "wherein the clock-signal input terminal overlaps a first wiring of the mounting member through said anisotropic conductive film by a larger area than an area at which at least one of the image-signal input terminals overlaps a second wiring of the mounting member through said anisotropic conductive film." And the Petition does not contend with the material differences between Kitawada's built-in drive circuit arrangement and Minami's off-panel drive circuit unit arrangement and

does not show that a POSITA would have been motivated to combine Minami with Kitawada. Ex. 2008 ¶ 66.

Sano

Sano also does not disclose "wherein the clock-signal input terminal overlaps a first wiring of the mounting member through said anisotropic conductive film by a larger area than an area at which at least one of the image-signal input terminals overlaps a second wiring of the mounting member through said anisotropic conductive film." Sano discloses wider clock signal *and image signal* input terminals. *See, e.g.*, Ex. 1006 ¶¶ [0006], [0013]; Ex. 2008 ¶ 67. A POSITA would understand that "data signals" refers to "image data signals" or "image signals" for the data line drive circuit. Ex. 2008 ¶ 67. The Petition overlooks this disclosure, choosing to highlight only the portion of Sano's disclosure referencing clock signals. But Sano's express teaching does not disclose the different areas recited in the '146 claims and instead is *contrary* to the '146 patent claimed inventions: at most, Sano teaches clock signal input terminals and image signal input terminals having the same width.

Sano teaches away from the claimed invention in a second way. It proposes a purported solution in which external terminals are connected to a printed circuit board using a zebra connector. Ex. 1006 ¶¶ [0004], [0006], [0012], [0014]. Mr. Flasck explains that a zebra connector is distinct from the claimed anisotropic

conductive film. *See* Ex. 1002 ¶¶ 115, 118; Ex. 2008 ¶ 68. This solution does not apply in the context of the claimed inventions, which claim ACF.

Thus, Petition cannot show that Kitawada in view of Sano discloses "wherein the clock-signal input terminal overlaps a first wiring of the mounting member through said anisotropic conductive film by a larger area than an area at which at least one of the image-signal input terminals overlaps a second wiring of the mounting member through said anisotropic conductive film." And the Petition does not contend with the fact that Sano teaches away from the claimed invention. Ex. 2008 ¶¶ 69-70.

Other References Not Included in the Asserted Grounds

The Petition separately (and heavily) cites Nakanishi to support the argument that Kitawada in view of Minami or Sano discloses limitation 10[j]. But the Petition does not include Nakanishi in the asserted combination. Moreover, Nakanishi does not disclose limitation 10[j], either.

Nakanishi describes active matrix organic light emitting diode (AMOLED) arrangements—not LCD arrangements. *See, e.g.*, Ex. 1010 at 15 ("Provided is an electro-optical device comprising a display substrate on which are formed a plurality of light emitting elements . . . ."), ¶ [0001] ("The present invention relates to an electro-optical device and an electronic device, and in particular to an electro-optical device provided with an organic electroluminescent material and an

electronic device provided with the electro-optical device."). Nakanishi describes wirings having different widths and providing a plurality of external connection terminals for wider lines. *See, e.g.*, *id.* ¶ [0013] ("a first aspect of the present invention is an electro-optical device comprising first wiring connected to a first external connection terminal and second wiring formed so as to be wider than the width of the first wiring, the electro-optical device characterized in that a plurality of second external connection terminals are provided for the second wiring"). Thus, Nakanishi achieves "uniform" pressure bonding conditions. *Id.*; *see also* Ex. 2008 ¶ 72.

Nakanishi does not describe clock signal input terminals. Nakanishi describes only external connection terminals for "scanning line drive circuit control signal wiring"—a POSITA would understand that an AMOLED scanning line drive circuit control signal is different than a clock signal. *See, e.g.*, Ex. 1010 ¶ [0053]; Ex. 2008 ¶ 73. A control signal might be, for example, a start signal. Ex. 2008 ¶ 73. Indeed, Petitioner's expert, Mr. Flasck, admits that Nakanishi does not disclose a clock signal input terminal. Ex. 1002 ¶ 133. Like Minami, the Petition's self-serving "clock signal" figure annotations find no support in the underlying reference.

Further, Nakanishi discloses an AMOLED display arrangement, not an LCD panel, and the Petition does not explain why Nakanishi is analogous prior art. Kitawada describes LCD arrangements. Ex. 2008 ¶ 74.

The Petition also cites a "Mismatch" report. *See* Ex. 1014. Again, the Petition does not assert that the Mismatch report is part of the asserted combination. Moreover, the Petition misrepresents the Mismatch report, which includes *no disclosure* regarding the size or pitch of input terminals on the LCD panel. *See, e.g.*, *id.* at 2 (noting changes to the outer lead bonds *on the tape automated bonding (TAB)* and that "the coordinates of the outer leads *on the glass panel remain unchanged*") (emphasis added). The Mismatch report at most discloses modified *locations* of leads on a *TAB* (not the panel) and otherwise provides leads of uniform size. *See id.* at Fig. 1; *see also* Ex. 2008 ¶ 75.

Thus, the Petition fails to show that Kitawada in view of Kawaguchi, Matsumoto, and Minami or Sano discloses or renders obvious "wherein the clock-signal input terminal overlaps a first wiring of the mounting member through said anisotropic conductive film by a larger area than an area at which at least one of the image-signal input terminals overlaps a second wiring of the mounting member through said anisotropic conductive film."

b. Claims 11-22

Because the Petition cannot show that Kitawada in view of Kawaguchi, Matsumoto, and Minami or Sano renders obvious claim 10, the Petition cannot show that the combination renders obvious any of claims 11-22, which depend from claim 10. Ex. 2008 ¶ 76.

c. Claim 23

i. The Petition does not show that Kitawada in view of Kawaguchi, Matsumoto, and Minami or Sano discloses or renders obvious "wherein the clock signal input terminal overlaps the first wiring of the mounting member by a larger area than an area at which at least one of the image signal input terminals overlaps the second wiring of the mounting member" (claim 23[l]).

For the same reasons that Kitawada in view of Kawaguchi, Matsumoto, and Minami or Sano does not disclose limitation 10[j], the combination does not disclose "wherein the clock signal input terminal overlaps the first wiring of the mounting member by a larger area than an area at which at least one of the image signal input terminals overlaps the second wiring of the mounting member" (limitation 23[l]). Specifically, neither reference on which the Petition relies to disclose limitation 23[l]—Minami and Sano—teaches clock signal input terminals having a larger area than image signal input terminals. Ex. 2008 ¶ 77.

B. The Petition does not establish a reasonable likelihood that Kitawada in view of Kawaguchi and Minami or Sano or Kato renders obvious claims 1-9 (Ground 2).[3]

1. The Petition fails to show that Kitawada in view of Kawaguchi and Minami or Sano or Kato discloses or renders obvious all limitations of any challenged claim.

a. Claim 1

i. The Petition does not show that Kitawada in view of Kawaguchi and Minami or Sano or Kato discloses or renders obvious "wherein the clock signal input terminal has a larger area than the image signal input terminal" (claim 1[i]).

For the same reasons that Kitawada in view of Kawaguchi, Matsumoto, and Minami or Sano does not disclose limitation 10[j], Kitawada in view of Kawaguchi and Minami or Sano or Kato does not disclose "wherein the clock signal input terminal has a larger area than the image signal input terminal" (limitation 1[i]).

[3] The Petition alternatingly refers to its Ground 2 combination as "Kitawada in view of Kawaguchi, and Minami or Sano or Kato" or "Kitawada in view of Kawaguchi, Matsumoto, and Minami or Sano or Kato." *Compare* Pet. at 5 *with* Pet. at 77. The Petition is not clear and frequently refers back to Ground 1 arguments to advance its Ground 2 arguments. Absent a clear articulation of its *combination* and motivations to combine the asserted references, the Petition cannot show a reasonable likelihood of prevailing on Ground 2.

Specifically, neither reference on which the Petition relies to disclose limitation 1[i]—Minami and Sano—teaches a clock signal input terminal having a larger area than an image signal input terminal. Ex. 2008 ¶¶ 78-79.

b. Claims 11-22

Because the Petition cannot show that Kitawada in view of Kawaguchi and Minami or Sano or Kato renders obvious claim 1, the Petition cannot show that the combination renders obvious any of claims 2-9, which depend from claim 1. *Id.* ¶ 80.

VII. PATENT OWNER DOES NOT WAIVE ADDITIONAL ARGUMENTS.

The Petition fails to establish a reasonable likelihood that any challenged claim is unpatentable, and the Board should deny institution. Patent Owner does not waive its right to address additional arguments in favor of validity and/or objective indicia of non-obviousness in its Patent Owner's Response, should the Board institute these proceedings.

VIII. PETITIONER'S *SOTERA* STIPULATION DOES NOT CHANGE THE FACT THAT RELEVANT FACTORS FAVOR DISCRETIONARY DENIAL.

Petitioner filed a *Sotera* stipulation on November 17, 2025. *See* Paper 7. First, Patent Owner notes that the stipulation suggests that it covers Petitioner's co-defendants in the related district court proceedings. *See id.* at 2 ("Petitioner and the defendants in the co-pending district court proceeding . . . will not advance

invalidity challenges under §§ 102 or 103 . . . ."). But the stipulation does not indicate that Petitioner has the authority to bind those co-defendants—separate LG and Hisense entities—and those co-defendants have not separately executed or otherwise joined the *Sotera* stipulation. Thus, it remains likely that the related district court proceedings will involve the validity of the '146 patent, including §§ 102 and 103 challenges by the defendants other than Petitioner. *See* Ex. 2009 at 28 (co-defendant LG Electronics Inc.'s Answer in related proceeding asserting counterclaim of invalidity of the '146 patent, including under §§ 101, 102, 103, and 112).

Second, Patent Owner stands on its discretionary denial brief, Paper 6, noting, in particular, settled expectations regarding the '146 patent and Petitioner's longstanding knowledge of the patent and of Patent Owner's infringement contentions. For that reason alone, the *Sotera* stipulation should not change the fact that current guidance and efficiency favor discretionary denial.

Date: November 19, 2025

Respectfully submitted,

s/ Cyrus A. Morton

Cyrus A. Morton (Reg. No. 44,954)
CMorton@RobinsKaplan.com
Lead Counsel
Samuel J. LaRoque (Reg. No. 68,542)
SLaRoque@RobinsKaplan.com
Back-Up Counsel

Robins Kaplan LLP
800 LaSalle Avenue, Suite 2800
Minneapolis, MN 55402
Direct Line: 612-349-8722
Fax: 612-339-4181

Attorneys for Patent Owner

CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATION

I certify that this Patent Owner's Preliminary Response complies with the word count limit and contains 6,516 words in 14-point Times New Roman font as calculated by the word count feature of Microsoft Office, in compliance with 37 C.F.R. § 42.24(a)(1)(i). This word count is inclusive of all text and footnotes but does not include the table of contents, table of authorities, certificate of service or word count, or appendix of exhibits or claim listing.

Date: November 19, 2025

Respectfully submitted,

s/ Cyrus A. Morton

Cyrus A. Morton (Reg. No. 44,954)
CMorton@RobinsKaplan.com
Lead Counsel
Samuel J. LaRoque (Reg. No. 68,542)
SLaRoque@RobinsKaplan.com
Back-Up Counsel
Robins Kaplan LLP
800 LaSalle Avenue, Suite 2800
Minneapolis, MN 55402
Direct Line: 612-349-8722
Fax: 612-339-4181

Attorneys for Patent Owner

CERTIFICATE OF SERVICE

I certify that on November 19, 2025, a copy of Patent Owner's Preliminary Response, including exhibits, was served in its entirety by electronic mail on Petitioner's counsel at the following addresses indicated in Petitioner's Mandatory Notices:

Amy E. Simpson, Reg. No. 54,688
Amy.Simpson@hklaw.com

Kristopher L. Reed, Reg. No. 58,694
kris.reed@hklaw.com

Edward J. Mayle, Reg. No. 65,444
edward.mayle@hklaw.com

boeiprservice@hklaw.com

Date: November 19, 2025

Respectfully submitted,

s/ Cyrus A. Morton

Cyrus A. Morton (Reg. No. 44,954)
CMorton@RobinsKaplan.com
Lead Counsel
Samuel J. LaRoque (Reg. No. 68,542)
SLaRoque@RobinsKaplan.com
Back-Up Counsel
Robins Kaplan LLP
800 LaSalle Avenue, Suite 2800
Minneapolis, MN 55402
Direct Line: 612-349-8722
Fax: 612-339-4181

Attorneys for Patent Owner