UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.

Petitioner

v.

138 EAST LCD ADVANCEMENTS LIMITED,

Patent Owner.

PTAB Case No. IPR 2025-01396

Patent No. 7,636,146

PETITION FOR *INTER PARTES* REVIEW OF PATENT NO. 7,636,146 CHALLENGING CLAIMS 1-23

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Ex. 1020	U.S. Publication 2003-0043105 ("**Hirakata**")
Ex. 1021	U.S. Pat. No. 7,002,545 ("**Osame**")
Ex. 1022	"*Liquid Crystal Display Technology*," with partial translation provided by the patent applicant, cited in September 17, 2008 Response to Office Action.
Ex. 1023	U.S. Pat. No. 5,155,065 ("**Schweiss**")

CHALLENGED CLAIM LISTING (CLAIMS 1-23)

Claim	Limitation No.	Limitation
1	[1pre]	An electro-optical panel comprising:
	[1a]	a plurality of data lines
	[1b]	a plurality of scanning lines intersecting the plurality of data lines
	[1c]	a plurality of pixels disposed corresponding to the intersections between the data lines and the scanning lines
	[1d]	a clock signal input terminal supplied with a scanning line clock signal
	[1e]	an image signal input terminal supplied with an image signal
	[1f]	a scanning line drive circuit that sequentially transmits a transmission start pulse in synchronization with the scanning line clock signal and outputs a scanning signal to each of the plurality of scanning lines, image signals from the plurality of data lines are supplied to pixels selected by the scanning signals
	[1g]	a drive circuit which controls a grayscale of the pixels based on the scanning line clock signal and the image signal; and
	[1h]	a third input terminal, wherein the third input terminal comprises a power source terminal supplied with a power source, and the area of the third input terminal is not smaller than that of the first clock signal input terminal,
	[1i]	wherein the clock signal input terminal has a larger area than the image signal input terminal, and
	[1j]	wherein a plurality of the power source terminals, a plurality of the first clock signal input terminals, and a

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Claim	Limitation No.	Limitation
		plurality of the second image signal input terminals are included
	[1k]	the plurality of the power source terminals, the plurality of the first clock signal input terminals, and the plurality of the second image signal input terminals are formed in line on a substrate; and
	[1l]	a pitch interval of the adjacent first clock signal input terminals is an integer multiple of a pitch interval of the adjacent second image signal input terminals.
2		An electro-optical panel according to claim 1, wherein the first clock signal input terminal has a smaller input resistance compared with the image signal input terminal.
3		An electro-optical panel according to claim 1, wherein a signal supplied to the clock signal input terminal comprises a driving signal supplied to the scanning-line drive circuit.
4		An electro-optical panel according to claim 1, wherein the clock signal input terminal and the image signal input terminal, which are disposed along an edge of a substrate, are formed in line, the image signal input terminal is disposed in the central part of the substrate, and the clock signal input terminal is disposed at the outer side of the substrate.
5		An electro-optical apparatus comprising: an electro-optical panel set forth in claim 1; power source means for supplying the power source; and signal generation means for supplying the input signals.
6		An electro-optical apparatus comprising: an electro-optical panel set forth in claim 5; an external substrate which includes power source means for supplying the power source and signal generation means for supplying

Claim	Limitation No.	Limitation
		the input signals; and a flexible substrate which connects the external substrate and the electro-optical panel, wherein the flexible substrate is connected to the plurality of power source terminals, the plurality of clock signal input terminals and the plurality of image signal input terminals through an anisotropic conductive film.
7		An electro-optical apparatus according to claim 6, wherein wiring lines are formed corresponding to a reference pitch interval of the image signal input terminals on the flexible substrate.
8		An electronic system comprising the electro-optical apparatus set forth in claim 1.
9		The electro-optical panel according to claim 1, further comprising a substrate, the clock signal input terminal and the image signal input terminal arranged in a line on an edge of the substrate, and the image signal input terminal disposed closer to a center of an edge of the substrate than the clock signal input terminal.
10	[10pre]	An electro-optical panel comprising:
	[10a]	a first substrate
	[10b]	data lines
	[10c]	scanning lines intersecting the data lines
	[10d]	pixels disposed corresponding to intersections between the data lines and the scanning lines
	[10e]	a clock-signal input terminal supplied with a clock signal and connected to a mounting member through anisotropic conductive film

Claim	Limitation No.	Limitation
	[10f]	image-signal input terminals supplied with image signals and connected to the mounting member through anisotropic conductive film,
	[10g]	the clock-signal input terminal and the image-signal input terminals being disposed along one side of the first substrate,
	[10h]	the image signals being supplied from an external data drive circuit and being supplied simultaneously to all of the data lines
	[10i]	and a scanning-line drive circuit that is formed on the first substrate and that sequentially transmits a transmission start pulse in synchronization with the clock signal
	[10j]	wherein the clock-signal input terminal overlaps a first wiring of the mounting member through said anisotropic conductive film by a larger area than an area at which at least one of the image-signal input terminals overlaps a second wiring of the mounting member through said anisotropic conductive film.
11		The electro-optical panel according to claim 10, the clock-signal input terminal having a smaller resistance compared with resistance of the image signal input terminal.
12		The electro-optical panel according to claim 10 the clock-signal input terminal and the image-signal input terminal arranged in a line on an edge of the first substrate, the image-signal input terminal being disposed closer to a center of the edge of the first substrate than the clock-signal input terminal.
13		The electro-optical panel according to claim 10, the external data line circuit being formed on a second substrate other than the first substrate.

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Claim	Limitation No.	Limitation
14		The electro-optical panel according to claim 10, the clock-signal input terminal being disposed further out on the first substrate relative to a central part of an outer edge of the first substrate than the image signal input terminal.
15		The electro-optical panel according to claim 10, the pixels arranged on the first substrate.
16		The electro-optical panel according to claim 10, the mounting member comprising a flexible substrate and an external substrate that are different than the first substrate.
17		The electro-optical panel according to claim 10, wherein each of the first wiring and the second wiring comprise at least one wire.
18		The electro-optical panel according to claim 10, wherein contact area between the clock signal input terminal and the first wiring is greater than contact area between the at least one of the image signal input terminals and the second wiring.
19		The electro-optical panel according to claim 10, wherein the mounting member is distinct from and connected to the first substrate.
20		The electro-optical panel according to claim 19, wherein the mounting member is electrically and mechanically connected to a terminal group of the first substrate that comprises the clock signal input terminal and the image signal input terminals.
21		The electro-optical panel according to claim 10, wherein the clock signal input terminal and the at least one of the image signal input terminals are connected between the substrate and the mounting member.

Claim	Limitation No.	Limitation
22		The electro-optical panel according to claim 10, wherein the mounting member is implemented as a flexible cable that is connected to the substrate over the clock signal input terminal and over the image signal input terminals.
23	[23pre]	An electro-optical panel comprising:
	[23a]	a substrate
	[23b]	data lines
	[23c]	scanning lines intersecting the data lines
	[23d]	pixels disposed corresponding to intersections between the data lines and the scanning lines
	[23e]	a clock signal input terminal supplied with a clock signal
	[23f]	an image signal input terminal supplied with an image signal
	[23g]	a scanning line drive circuit that outputs scanning signals to the scanning lines, image signals from the data lines supplied to the pixels are selected by the scanning signals
	[23h]	wherein the data lines, the scanning lines, the pixels, the clock signal input terminal and the image signal input terminal are implemented on the substrate
	[23i]	a mounting member that is distinct from and connected to the substrate, the mounting member comprising:
	[23j]	a first wiring that is connected to the clock signal input terminal;
	[23k]	a second wiring that is connected to the image signal input terminal;

Claim	Limitation No.	Limitation
	[23l]	wherein the clock signal input terminal overlaps the first wiring of the mounting member by a larger area than an area at which at least one of the image signal input terminals overlaps the second wiring of the mounting member

BOE Technology Group Co., Ltd. ("BOE" or "Petitioner") requests IPR of claims 1-23 of U.S. Patent No. 7,636,146.

I. INTRODUCTION

Prior art LCD displays had circuits (*e.g.*, microchips) mounted externally to the display's glass substrate. These circuits supplied power source signals, image signals, clock signals, and other signals to control the display's pixels. Such signals travelled from the external circuits along wiring connected to the display's "terminals," which are connectors on the display's substrate and act as points where external wiring can be connected. The '146 patent's inventor's allegedly novel idea was to use clock signal input terminals having a "larger area" than the image signal input terminals. A related idea was to use power source terminals having an area "not smaller" than the clock signal terminal's area. Ex. 1001, Abstract, 2:24-3:42. Both of these ideas were known and used in the prior art for exactly the same reasons as used in '146 patent.

First, clock signal and power source terminals were often mounted near the corners of an LCD device's glass substrate, where heat and pressure were applied during manufacturing to connect fine pitch wiring from the external circuits to the input terminals (using something called anisotropic conductive film, "ACF"). Prior art publications teach the use of larger terminals at that location to mitigate the known risk of "misalignment" between wiring and terminals, weakened ACF bonding, and other related defects. In contrast, the image signal terminals were typically placed closer to the center of the LCD panel's substrate, and a POSITA knew that there was a lower risk of manufacturing-related defects at that location, and therefore the area for the image signal terminals could be smaller. The claims are obvious for this reason, standing alone.

Second, it is elementary that resistance and area vary inversely, and prior art publications teach that some terminals needed to have a lower resistance, and thus a larger area. Specifically, clock signal input terminals must allow high frequency components of the clock signal waveform—typically, a square wave—to pass, which requires a lower resistance. It was also known that power source terminals transmit high currents, which also requires a lower resistance. On the other hand, the higher frequency components of image signals are not critical, and image signals involve lower currents. Image signal terminals could therefore have a smaller area than clock signal and power source terminals in an LCD display. The claims are obvious for this second and ***independent*** reason.

For both reasons—one being of a simple mechanical nature related to bonding terminals to wiring through ACF, the other reflecting the elementary principle that electrical resistance varies inversely with area—prior art clock signal and power source terminals had larger areas than image signal terminals. As shown in detail below, because the ’146 patent improperly claims known concepts, Petitioner requests that claims 1-23 be found unpatentable.

II. MANDATORY NOTICES

A. Real Party-in-Interest

BOE is the RPI.

B. Related Matters

Patent Owner 138 East LCD Advancements Limited and its alleged exclusive licensee Longitude Licensing Limited (collectively “Patent Owner”) asserted that BOE infringes at least claim 23 of the ’146 patent and claims of other patents in *Longitude Licensing v. BOE*, No. 2:25-cv-440 (E.D. Tex.) and *Longitude Licensing v. BOE*, No 2:25-cv-358 (E.D. Tex.). In Case No. 2:25-cv-440, Patent Owner also sued LG Electronics, Inc.; in Case No. 2:25-cv-358, Patent Owner also sued Hisense Group Holdings Co. Ltd. *et al.*

C. Counsel and Service Information

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Petitioner consents to electronic service, which should be sent to boeiprservice@hklaw.com. A Power of Attorney is filed herewith.

III. REQUIREMENTS FOR *INTER PARTES* REVIEW

A. Grounds For Standing

Petitioner certifies that the '146 patent is available for IPR and that Petitioner is not barred from requesting IPR. This Petition is filed less than one year after Patent Owner filed BOE's waiver of service on May 15, 2025 in Case 2:25-cv-358.

B. Overview of Challenges and Requested Relief

Petitioner requests cancellation of claims 1-23.

1. Identification of Prior Art

Petitioner relies on the patents and publications listed in the Table of the Exhibits, including:

Exhibit No.	Prior Art Basis
Ex. 1004: ("**Kitawada**") JP H11282011A	Kitawada published on October 15, 1990 and is prior art least under pre-AIA 35 U.S.C. §102(b).
Ex. 1005: ("**Kawaguchi**") JP 2000231115A	Kawaguchi published on August 22, 2000 and is prior art at least under §102(b).
Ex. 1008: ("**Matsumoto**") *Electronic Display Devices*, Chapter 2, Liquid Crystal Displays	Matsumoto published no later than September 17, 1990 and is prior art at least under §102(b).
Ex. 1006: ("**Sano**") JP H10282516A	Sano published on October 23, 1998 and is prior art at least under §102(b).
Ex. 1007: ("**Minami**") JP H03-125334	Minami published on December 18, 1991 and is prior art at least under §102(b).

Exhibit No.	Prior Art Basis
Ex. 1009: ("**Kato**") U.S. 2002-0018169A1	Kato published on February 14, 2002 and is prior art at least under §102(b).

2. Grounds for Challenge

Claims 1, 10, and 23 are independent claims. The table below summarizes the grounds challenging claims 1-23.

Ground	Claims	Basis
Ground 1	Claims 10-23	Obvious over **Kitawada** in view of **Kawaguchi**, **Matsumoto**, and **Minami** or **Sano**
Ground 2	Claims 1-9	Obvious over **Kitawada** in view of **Kawaguchi**, and **Minami** or **Sano** or **Kato**

Ground 1: Petitioner relies on **Kitawada** which expressly discloses nine of eleven elements of claim 10, including [10pre]-[10g], and [10i].

Element [10h] requires an "external" data drive circuit; while Kitawada expressly teaches a data drive formed on the LCD panel's substrate, a POSITA would have known, understood, and expected the same results by using an external data drive. While obvious to a POSITA, Petitioner relies on **Kawaguchi** as expressly teaching the external data drive. Element [10h] also requires the data drive to supply image signals "simultaneously" to all data lines. Kitawada does not use the word "simultaneously," but this was conventional long before 2003 and

Patent Owner admits as much. Out of an abundance of caution, Petitioner relies on **Matsumoto** because it expressly teaches suppling image signals "simultaneously."

Finally, Kitawada discloses clock signal input terminals and image signal input terminals as recited in [10j], but does not disclose their relative areas. Petitioner alternatively relies in the alternative on **Minami *or* Sano**, each of which ***independently*** motivate making the clock signal input terminals have a larger area. As explained below and at Flasck, §X, Minami teaches that terminals located near the corners of the LCD panel's substrate—where Kitawada's clock and power source terminals are—should be made larger for mechanical reasons. If Patent Owner disagrees, then Sano teaches to make the area of clock terminals larger to reduce their resistance. Either way, this key element is obvious. Petitioner relies on the same prior art for independent claim 23, which closely tracks claim 10.

Ground 2: As with Ground 1, Petitioner relies on **Kitawada**, which expressly discloses almost all elements of claim 1, including [1pre]-[1g], [1j], [1k].

Kitawada discloses a "power source terminal" as recited in element [1h] but does not expressly teach that it is "not smaller" than the clock signal terminal. Petitioner relies in the alternative on **Minami *or* Kato**, each of which ***independently*** show that this was obvious. As discussed above, Minami teaches that Kitawada's power source terminals should have larger areas for mechanical reasons. If Patent Owner disagrees, Kato teaches that, because power terminals must transmit large currents, they need to have larger areas to lower their electrical resistance. Either way, [1h] is obvious. Similarly, Kitawada does not expressly teach that the clock signal input terminal "has a larger area" than the image signal input terminal as recited in [1i], but, just as with Ground 1, Petitioner relies in the alternative on **Minami *or* Sano**, each of which ***independently*** show that this was obvious.

Finally, Kitawada does not explicitly teach that the pitch interval of adjacent clock signal input terminals is an "integer multiple" of the pitch interval of image signal terminals as recited in [1l], but this was an obvious design choice, and Petitioner relies on **Minami** to show that this was the case.

Any discussion of prior art herein (including AAPA) other than Kitawada, Kawaguchi, Matsumoto, Minami, Sano, and Kato is referenced to support the knowledge of a POSITA.

IV. OVERVIEW OF THE '146 PATENT

A. The Invention

1. Applicant Admitted Prior Art

The specification admits that the majority of the claimed LCD elements were already known as conventional prior art. The Background section references Japanese Patent No. 2822558 admitting that as early as 1990, certain claimed technology was "known." Ex. 1001, 1:18-62. Japanese Patent No. 2822558 and admissions in the Background section of the '146 Patent all constitute AAPA.

Petitioner intends to rely on AAPA to further show what was within the knowledge of a POSITA at the time of the alleged invention.

LCD displays were admittedly "widely used" and had a "known" structure. Ex. 1001, 1:18-25. According to the AAPA, the structure of a "known electro-optical apparatus" included: (i) "pixel electrodes arranged in a matrix state"; (ii) "an element substrate on which switching elements, such as TFTs (Thin Film Transistors), connected to the pixel electrodes, are disposed"; (iii) "an opposing substrate on which opposing electrodes opposed to the pixel electrodes are formed"; and (iv) "a liquid crystal, which serves as an electro-optical material, filled between both of these substrates." Ex. 1001, 1:18-31.

The AAPA also establishes that a "pixel includes the switching element, the pixel electrode, the electro-optical material, and the opposing electrode, and is arranged in a matrix state." Ex. 1001, 1:31-50. Conventional elements for controlling the pixels included TFTs, scanning lines, data lines, and capacitors. "[W]hen a scanning signal is applied to the switching element through a scanning line, that switching element adopts a conductive state." *Id.* "In this conductive state, when an image signal having a voltage in accordance with grayscale is applied to the pixel electrode through a data line, a charge in accordance with the voltage of the image signal is stored in the liquid crystal layer between the pixel electrode and the opposing substrate." *Id.* "After the charge is stored, even if the switching element is turned to an off state, the storage of the charge in that liquid crystal layer is maintained by the capacitance of the liquid crystal layer itself, the storage capacitance, and the like." *Id.* "In this manner, when each switching element is driven, and the charge amount to be stored is controlled in accordance with grayscale, the alignment state of the liquid crystal is changed for each pixel, and thus the density changes for each pixel." *Id.* "It is, therefore, possible to display grayscale." *Id.*

The AAPA further establishes the following: "an electro-optical panel on which the above-described pixels are disposed in a matrix state" (Ex. 1001, 1:51-62); "[a] scanning-line drive circuit, which drives scanning lines, and a data-line drive circuit, which drives data lines, are sometimes formed on the electro-optical panel" (*id.*); "[a] power source, a driving signal, an image signal, etc. are supplied to the electro-optical panel having drive circuits" (*id.*); and "[a]s means for supplying the power source, etc. to the electro-optical panel, techniques which connect an input terminal formed on the electro-optical panel and a flexible substrate as a connection cable through an anisotropic conductive film are known." *Id.*

What's more, during prosecution, the applicant admitted that supplying image signals "simultaneously to all of the data lines" (as recited in claim 10) was known as the "line sequential method," a technique that was "well-known to those skilled in the art." Ex. 1003 (Response dated 9/17/2008).

In summary, the vast majority of the challenged claim elements are AAPA, and these admissions are "binding on the applicant and patentee for determinations of anticipation and obviousness." *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1570 (Fed. Cir. 1988). "AAPA can be important evidence of general background knowledge, and general knowledge can be used to supply a missing claim limitation." *Shockwave Med., Inc. v. Cardiovascular Sys., Inc.*, 142 F.4th 1371, 1378-79 (Fed. Cir. 2025) ("Permissible uses for general background knowledge in an IPR" include "for example, furnishing a motivation to combine, or supplying a missing claim limitation.") (cleaned up).

2. The Problem Addressed By the '146 Patent

The claims recite admittedly conventional structures, with the alleged novelty lying in the input terminals' relative areas.

The '146 patent expressly acknowledges that "the resistance of an input terminal becomes smaller as the area thereof becomes larger." Ex. 1001, 1:63-2:2. And, while it was "desirable" to make the input terminals large to reduce their resistance, there was simply not enough space and "all of the input terminals cannot be disposed in a limited area." *Id.* Further, when "the number of input terminals becomes large" and "when a flexible substrate, etc., are mounted, a problem of connection failure or the like has occurred." *Id.*, 2:3-14. On the other hand, if the area of all input terminals was "made small," their "contact resistance increases" as was well-known, and causes "a problem in that the driving signal cannot be input at a proper timing." *Id.*

The inventor solved this known dilemma in exactly the same way the prior art did before: by using "larger area" terminals for signals that need to utilize terminals having lower resistance (*e.g.*, power source signals or clock signals having a "higher frequency component"), while using smaller area image signals input terminals. Ex. 1001, Abstract ("The driving signal includes a higher frequency component than the image signal" so its input terminals "have a larger area"); 1:63-64 ("[T]he resistance of an input terminal becomes smaller as the area thereof becomes larger."); 3:23-42 (if the power source input terminal "has a high resistance, the voltage is trapped"); 3:5-9 ("[B]y . . . allocating the area of the input terminals, it becomes possible to appropriately dispose input terminals in a limited area."); 7:56-8:3 (area of input terminal "to which the image signal having a relatively low frequency component is supplied is made smaller"); 2:52-58 ("For an input signal which includes a high-frequency component, the input signal waveform can be captured without becoming dull by setting the time constant to a small value. Whereas for the input signal which consists of relatively low-frequency components, there is no problem even if the time constant is large, and thus the area of the input terminal can be made small.").

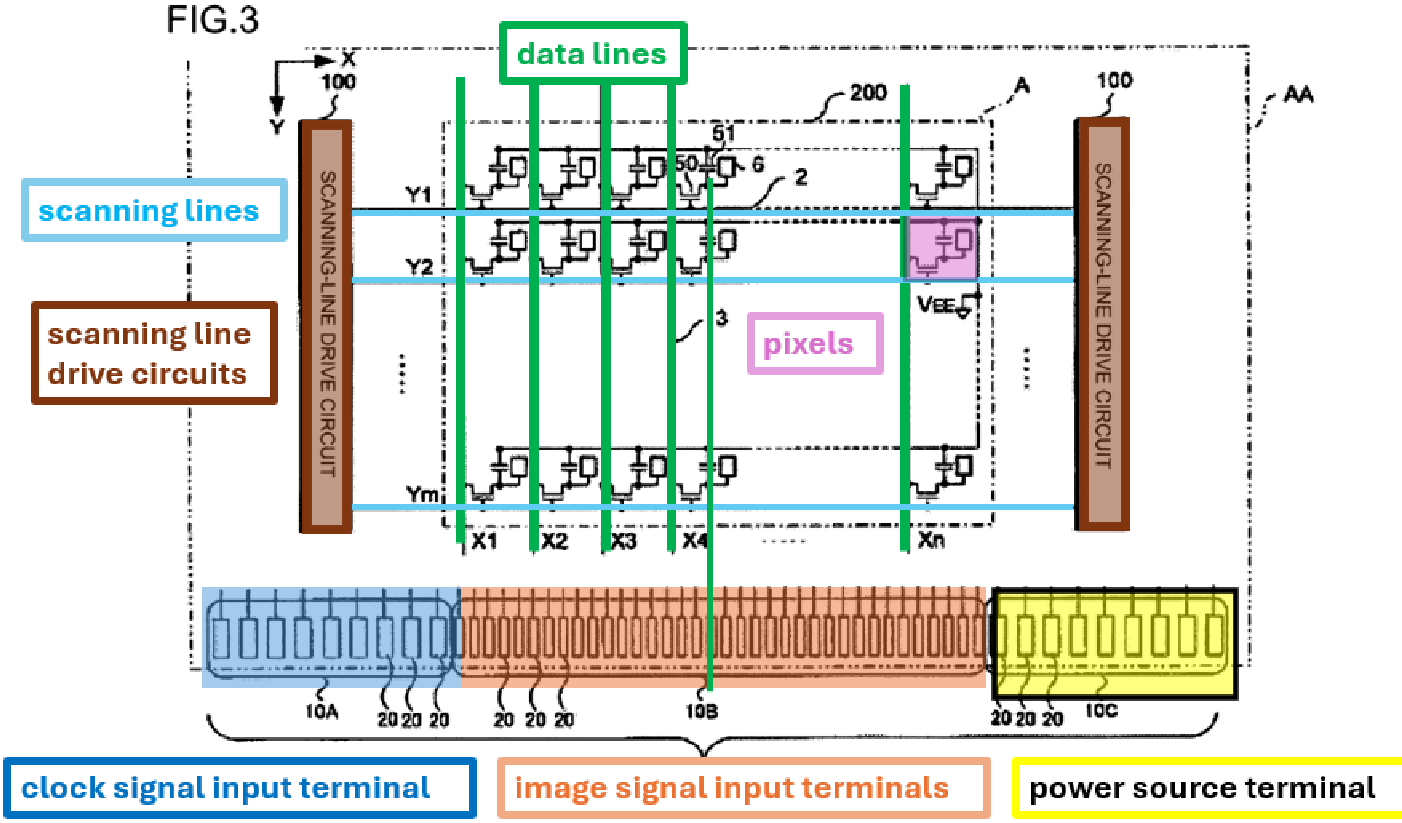
The inventor's "idea" that the clock signal input terminal has a "larger area" than the image signal terminals is recited in all three independent claims. *See* [1i],

[10j], [23l]. Limitation [1h] of claim 1 also recites the related concept that a "power source terminal" has an area that "is not smaller" than the clock signal input terminal.

Relying on basic design choices known to an LCD engineer, the patent states that it is "preferable" to put all of the input terminals "in line on a substrate" with the smaller area terminals "disposed in the central part of the substrate" and the larger area ones "disposed at the outer side of the substrate." Ex. 1001, 3:10-21. This is beneficial because when "connecting each terminal with ACF [anisotropic conductive film], heat and pressure are applied, and thus the outer side of ACF tends to have a larger extension rate than the central part." *Id*. "Therefore, by disposing an input terminal having a wider area at a more outer side than the input terminal having a smaller area, it is possible to prevent a connection failure because of the difference in the contraction rates as long as the input terminal is a large one even if a slight misalignment of the connection arises." *Id*.

The invention is illustrated in Figures 3:

FIG.3



B. Prosecution History

Seiko Epson was the original applicant. After rounds of rejections from the examiner and claim amendments from the applicant, the examiner allowed claim 1 on January 23, 2009, but did not provide any reasons for allowance. Ex. 1003 (Office Action of 1/23/2009). Other claims remained rejected.

The applicant then amended application independent claim 15 (which issued as claim 10) to require that the clock-signal input terminal "overlaps a first wiring of the mounting member through said anisotropic film by a larger area than an area at which at least one of the image-signal input terminals overlaps a second wiring of the mounting member through said anisotropic conductive film." Ex. 1003

(Response of 4/14/2009, underlining in original, text deleted by applicant omitted). The examiner then allowed independent claims 15 and 23—without explanation—with an examiner's amendment to claim 23 deleting language and adding that "the clock signal input terminal overlaps the first wiring of the mounting member by a larger area than an area at which at least one of the image signal input terminals overlaps the second wiring of the mounting member." Ex. 1003 (Notice of Allowance of 8/6/20089). *See* Flasck, §VII.B.

C. Priority Date

For purposes of this Petition only, Petitioner assumes the priority date is August 8, 2003. The critical date for pre-AIA §102(b) is August 6, 2003—one year before the "actual filing of the application in this country" of August 6, 2004. Pre-AIA 35 U.S.C. §119(a).

V. CLAIM CONSTRUCTION

At this time, Petitioner does not believe construction is necessary to resolve the Petition's challenges. *Vivid 10 Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999). Petitioner reserves the right to construe terms in the litigation and/or to respond to any constructions from Patent Owner. That said, two terms in claims 5 and 6 use the phrase "means for" and are addressed below.

A. "power source means for supplying the power source"

Under any construction, power sources were well-known, so there is no need to construe this term. Flasck, ¶96. Indeed, the specification admits that "means for supplying the power source, etc., to the electro optical panel … are known." Ex. 1001, 1:51-62. Further, a term that uses "means" is not governed by 35 U.S.C. § 112 ¶6 when the claim conveys "sufficient structure" to perform the recited function. *Lighting Ballast Control LLC v. Philips Elecs. N. Am. Corp.*, 790 F.3d 1329, 1339 (Fed. Cir. 2015). A "power source" was a known structure sufficient to supply power. Nonetheless, Petitioner identifies "portions of the specification that describe the structure, material, or acts corresponding to each claimed function" under 37 C.F.R. §42.104 (b)(3). Figure 5 discloses "power source circuit 500" mounted on external substrate ("C") that is connected to a liquid crystal panel ("AA") through a flexible substrate ("B"). Ex. 1001, Figure 5, 9:40-55, 10:9-13.

B. "signal generation means for supplying the input signals"

This term may not invoke §112 ¶6 because a signal generator is sufficient to supply input signals and such structures were well-known. Flask, ¶97. In Figure 5 of the patent, "the data-line drive circuit 200, the timing generation circuit 300, and the image processing circuit 400 function as signal generation means for supplying input signals to the liquid crystal panel AA." Ex. 1001, 10:13-17, 9:40-10:17.

VI. LEVEL OF ORDINARY SKILL

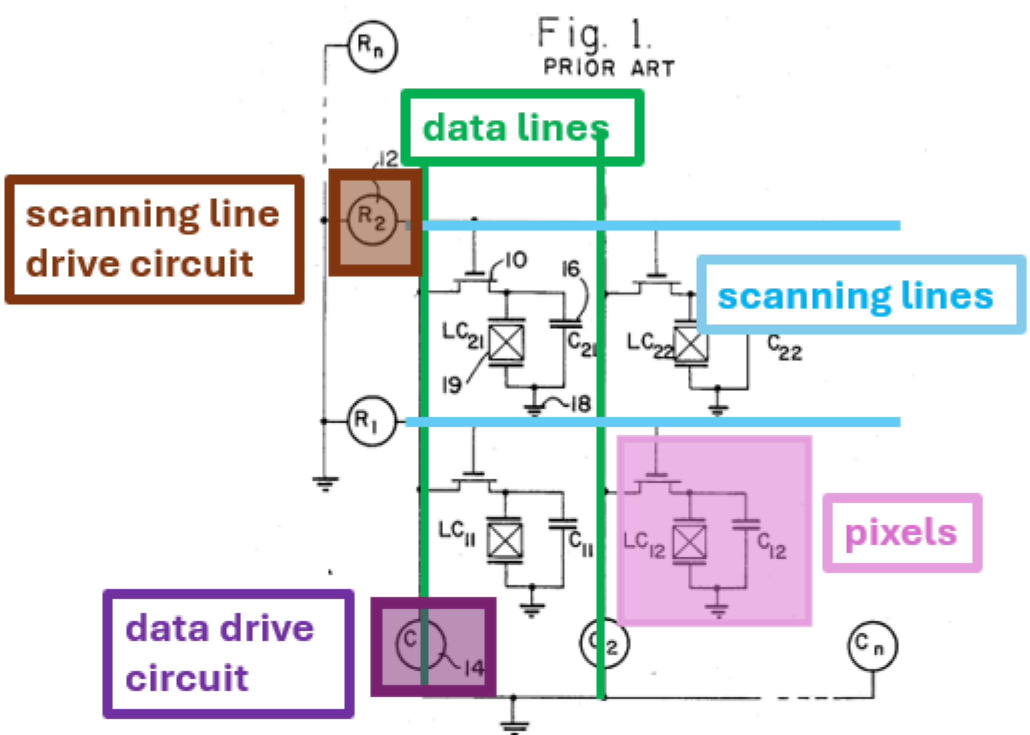
A POSITA had at least: i) a B.S. in electrical engineering, physics, or a related subject and two plus years of experience working in the field of LCD displays; ii) an M.S. degree in the aforementioned subjects, and at least 1 year of experience in the design/development of LCD displays; or iii) a Ph.D. in the aforementioned subjects, and at least some experience in the area of LCD displays. Additional education may substitute for professional experience, and significant work experience may substitute for formal education. Flasck, §V.

VII. STATE OF THE ART

As Mr. Flasck explains, the claimed technology was conventional long before the time of the invention in 2003. Flasck, §§VI, X.

A. Koda

Most elements of the claims were patented decades ago. For example, claim 1 of Pat. No., 3,824,003 recites elements of a typical active-matrix liquid crystal display device, which are illustrated below:



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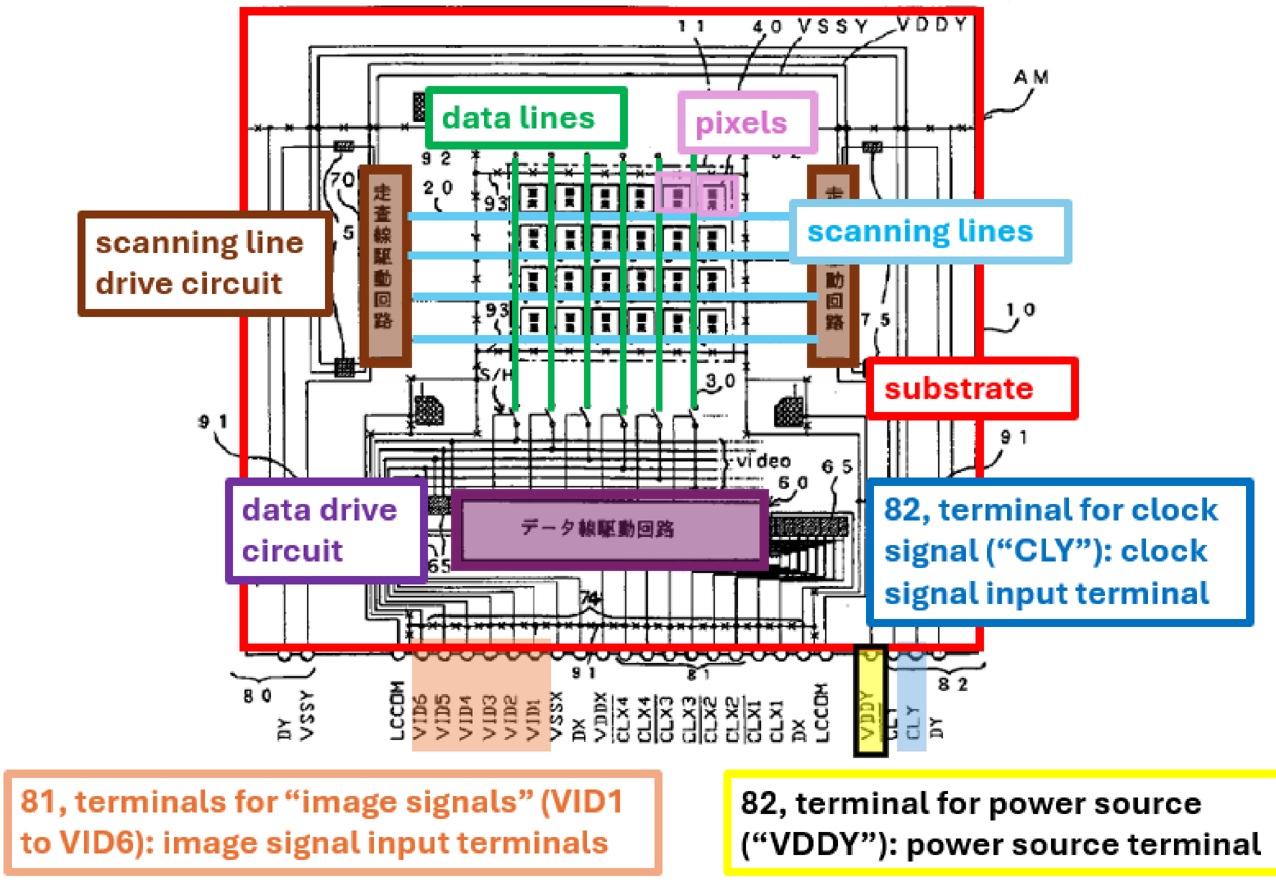
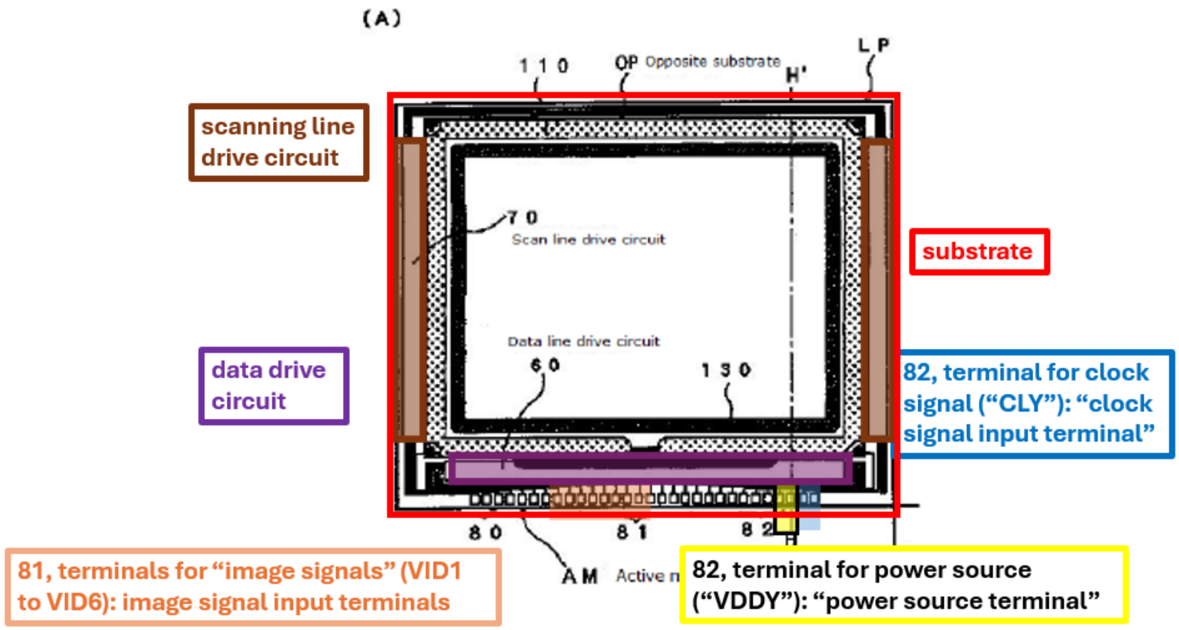
Ex. 1016, Figure 1 (all colored figures herein were annotated by Petitioner).

B. Kitawada

Kitawada discloses the same conventional elements and more:



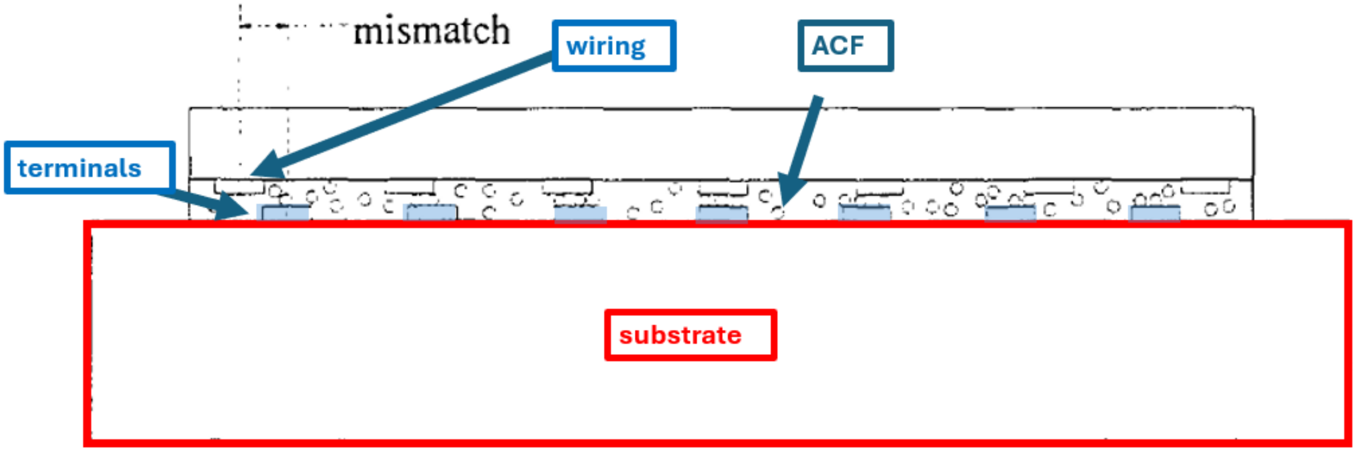
[FIG. 1]



Ex. 1004, Kitawada, Figure 2; Figure 1. Just like the invention of the '146 patent, Kitawada discloses input terminals arranged in a line on the edge of the substrate.

C. Mismatch Analysis Report

It was well-known that there could be a "mismatch" between input terminals having a "fine pitch" on an LCD substrate and wirings from an external "driver IC TAB" which are bonded using anisotropic conductive film ("ACF"). Ex. 1014 ("Mismatch Analysis Report"), first page. Like the '146 inventor later realized, the mismatch is most acute for the "outer lead bonds (OLBs)"—terminals near the outside of the LCD's substrate. *See id*:



Ex. 1014, Figure 1(b). This problem "will be inevitable if a uniform interconnection pitch is adopted in designing the TOG [tape on glass] connection." *Id*. at page 2 of 29. This "will be likely to cause early failure of the LCD panel" and so "methods for alleviating the adverse effects induced by OLB mismatch" were needed. *Id*. Similar to the claimed invention, Mismatch Analysis Report discloses "a nonuniform interconnection pitch" to mitigate these problems. *Id*.

As shown in detail below, Minami, Sano, Nakanishi, and Kato all disclose a nonuniform interconnection pitch, with certain terminals having larger areas. This (i) mitigates the problem of terminal-to-wiring "mismatch" and improves ACF bonding near the edges of an LCD panel's substrate; (ii) reduces resistance for the scanning signal drive clock signal input terminals so that they can transmit "high frequency" components with fidelity; and (iii) reduces resistance for the power source terminals so they can conduct large currents. *See* Flasck, §X.

D. Matsumoto

Matsumoto discloses an LCD device having pixels at the intersection of scanning lines and data lines:

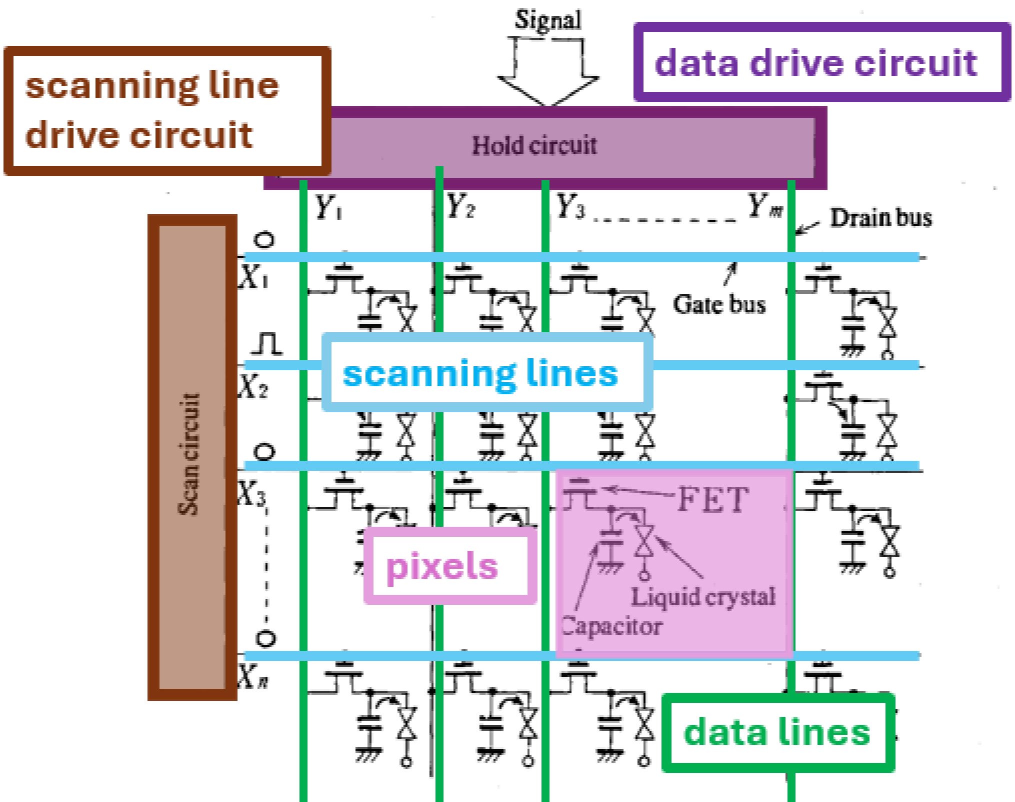
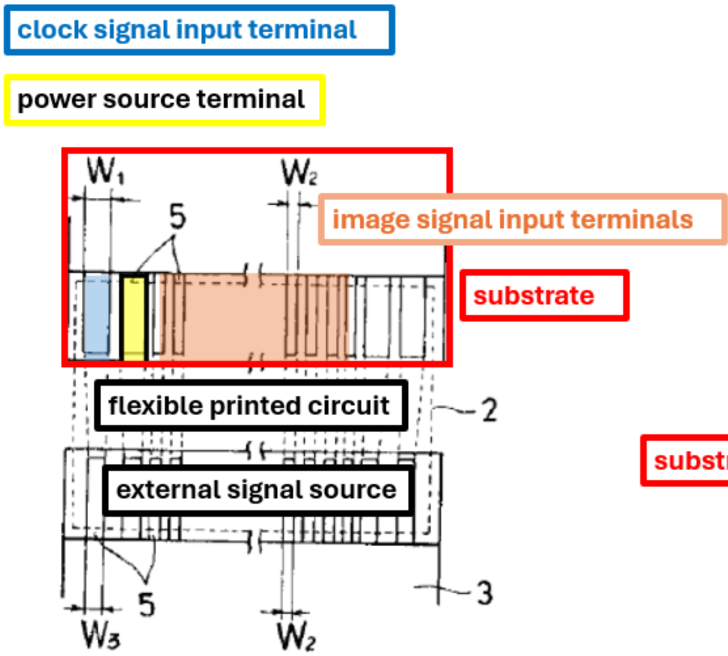


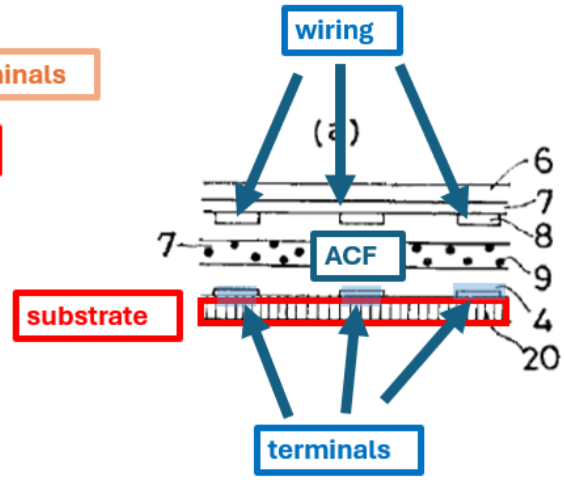
Figure 2.21 Operating principle of active matrix drive LCD

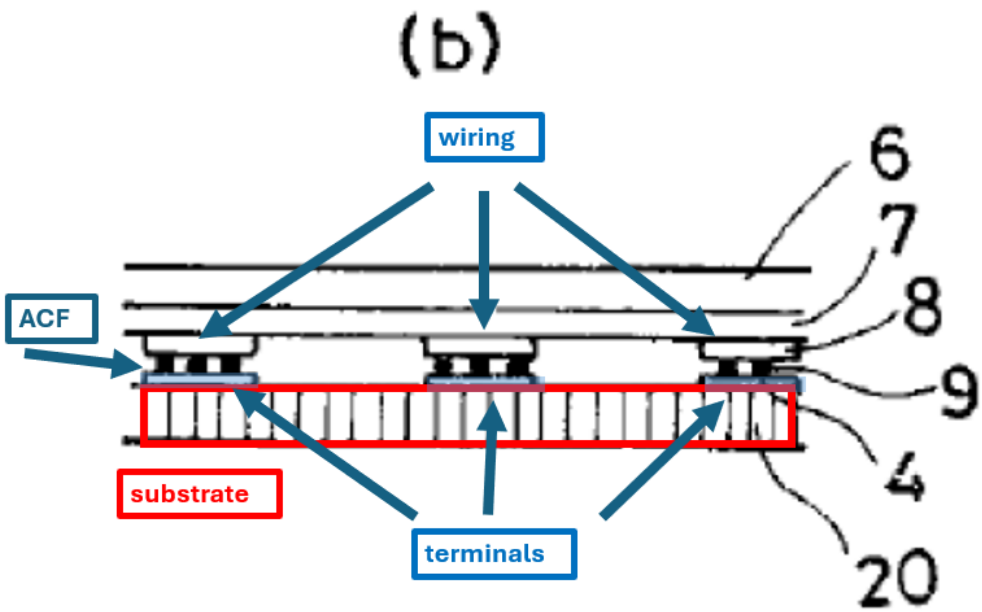
Ex. 1008, Fig. 2.21. A data line drive ("Hold circuit") supplies the image signals, and a scanning line drive ("Scan circuit") activates the pixel transistors in a row-sequential manner via a "Gate bus." The image signals are supplied from the Hold circuit to all data lines "simultaneously" (*id*., page 51 of 85), as recited in [10h].

E. Minami

Minami teaches that LCD panels may "require high-density terminal pitch connection . .. between the drive circuit board and the display unit." Ex. 1007 at page 13 of 18. When the "pitch is approximately 100 to 200 μm, the bonding area between the anisotropic conductive film and the LCD panel electrode terminals is small, resulting in a decrease in bonding strength and bond delamination due to external pressure after connection." *Id*. And "during assembly of the LCD panel unit or during transportation after connection, vibrations may cause a decrease in the reliability of electrical conductivity at the connection points." *Id*. "In particular, external pressure, vibrations, and other factors cause stress on both ends of the FPC board, resulting in frequent electrical connection failures at both terminals." *Id*. Just like the invention of the challenged claims, Minami discloses the solution, namely, "the pattern width near both ends of the electrode terminals connecting the liquid crystal display unit and the drive circuit unit is wider than the pattern width near the center." *Id*. Minami's Figure 3 (below on the left) shows that the outer terminals are wider ("W_1") and have a larger area than the narrower terminals ("W_2") near the center of the substrate:







Ex. 1007, Figures 3, 2a, 2b. Figure 2 shows an "anisotropic conductive film, such as one made of carbon fibers 9, is interposed between a glass substrate 20 on which an ITO film 4 has been formed and a polyimide film 6 on which a copper pattern 8 has been formed via an adhesive layer 7." *Id.*, page 14 of 18. "The connection portion is then subjected to thermal compression bonding at approximately 170 to 250°C, resulting in a state in which each material is connected as shown in FIG. 2 (b)." *Id*.

Since Minami's outer terminals have a larger area than the inner terminals (as shown in Figure 3), they overlap their respective wiring by a larger area through the ACF (as shown in Figure 2) as compared to the area that the (narrower) inner terminals overlap their respective wiring through the ACF. It is clear from Minami's Figures 1-3 that wiring electrodes 5 (*i.e.*, terminals) on LCD panel 1 (LCD panel 1 corresponds to glass substrate 20 in Figure 2) overlap the copper wiring pattern 8 shown in Figure 2, in the area bounded by dashed lines in Figures 1 and 3 (which includes flexible printed circuit 2), by a larger area at the edges (recall that Kitawada's clock signal input terminals are near the edges of Kitawada's substrate) than in the center (Kitawada's image signal input terminals are located near the center of Kitawada's substrate). Minami thus motivates and renders obvious elements [10j], [23l], [1h], [1i], and [1l]. Flasck, §§IX.E, X.

F. Sano

Sano teaches to increase the area of clock input terminals in LCD displays because they transmit a signal having "high frequency" components. Ex. 1006,

¶¶[0006]-[0008], [0018].[1] When an input terminal has a "high" resistance, "signal waveforms may become distorted" which "may cause malfunctioning of the liquid crystal panel driving IC 6 or the driving circuit of the panel." Ex. 1006, ¶[0006].

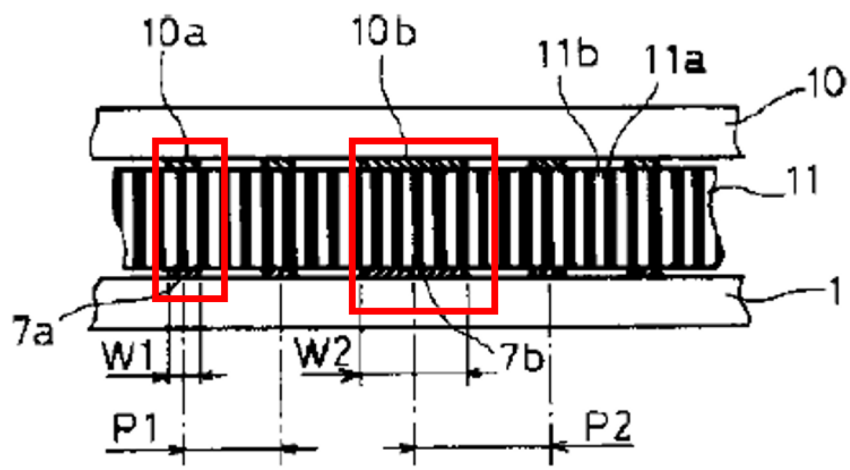
Just like the alleged point of novelty of the '146 patent,[2] Sano discloses that the "terminal width and pitch for external connection terminals that transmit high-frequency signals" are "made wider than those for other external connection terminals." ¶[0008]. "By adopting this structure, signal waveform distortion is

---

[1] *Cf.* Ex. 1019, ¶[0063] ("the clock signal YCK has a much higher frequency (by a factor of 1000, for example) than usual, and continues to have this high frequency for at least m periods or more"); Ex. 1020, ¶[0040] ("the maximum frequency of an input image signal is about 6 MHz in the NTSC standard, and about 20 MHz to 30 MHz in the HDTV standard. In order to accurately display this image signal, a clock signal is required to have a frequency (for example, about 50 MHz to 60 MHz) several times that of this image signal").

[2] Ex. 1001, 2:52-58 ("For an input signal which includes a high-frequency component, the input signal waveform can be captured without becoming dull by setting the time constant to a small value. Whereas for the input signal which consists of relatively low-frequency components, there is no problem even if the time constant is large, and thus the area of the input terminal can be made small.").

minimized even at high frequencies, thus preventing malfunctions of the liquid crystal panel driving circuit." *Id.*; ¶¶ [0009]-[0010], [0018]. Similar to Minami's Figures 2 and 3 shown above, Sano's Figure 2 shows clock input terminals 7b (of width "W_2") overlapping wirings 10b through an anisotropic connector by a larger area than input terminals 7a (of width "W1") overlap wirings 10a:



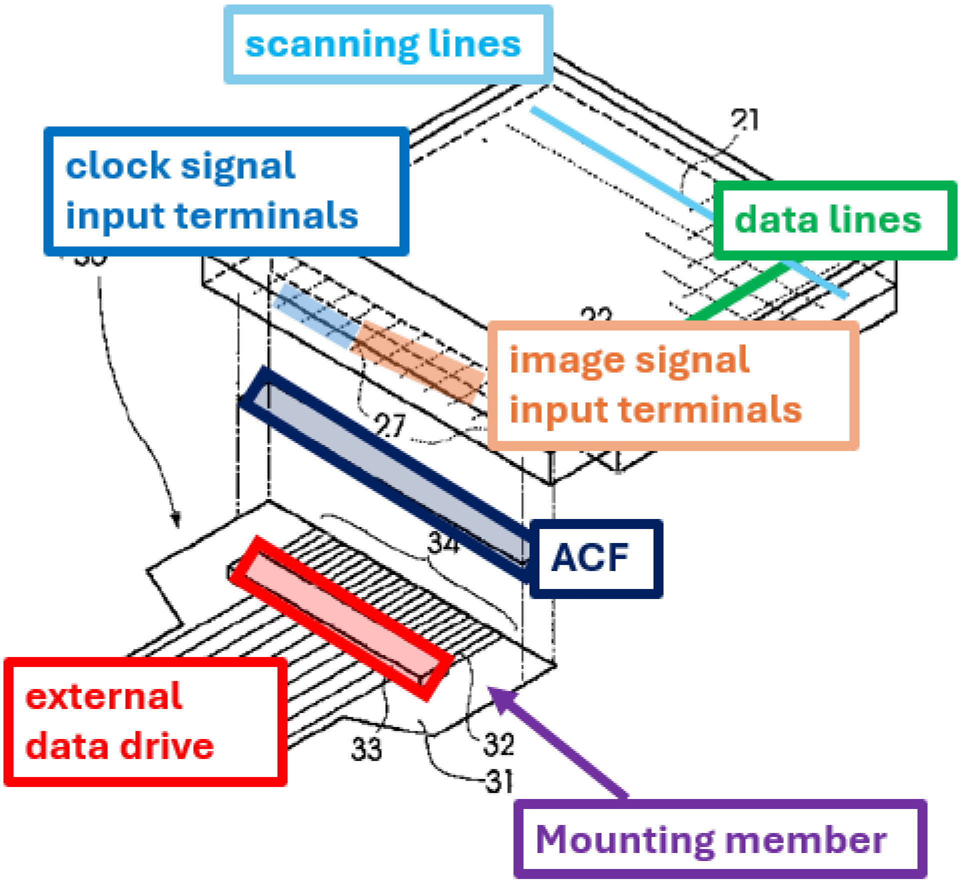
Ex. 1006, Figure 2. "Therefore, the connection resistance via the conductive sections 11a of the zebra rubber connector (11) at the terminals for transmitting high-frequency signals (i.e., between 7b, 8b and 10b) is lower than the connection resistance at other terminal portions of the transparent substrate electrode (9)." ¶[0014]. "As a result, distortion of the signal waveform for high-frequency signals is prevented, and malfunction of the liquid crystal panel driving circuit . . . can be effectively avoided." *Id.* "Moreover, at each connection point where high-frequency signals are transmitted . . . the terminal width is wider compared to other areas . . . This reduces wiring resistance and contributes effectively to the prevention of malfunctions." ¶[0015].

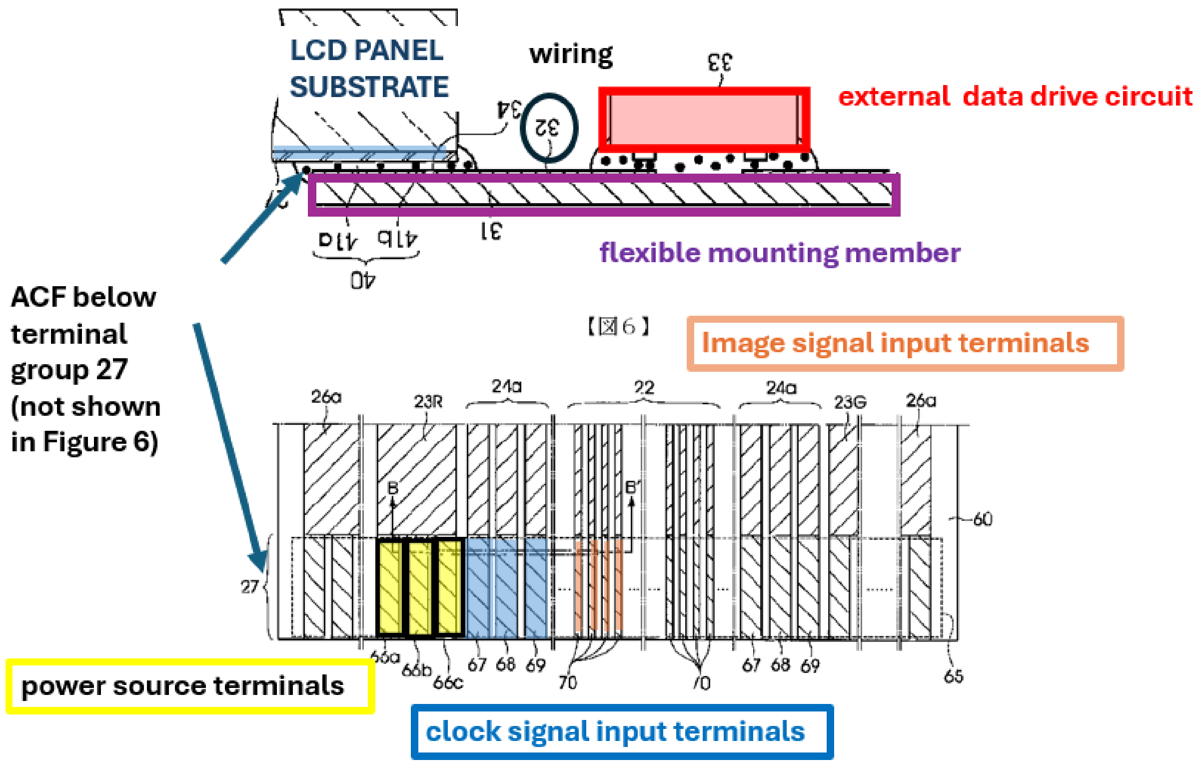
A POSITA would readily appreciate from Sano's teachings that an LCD panel's clock signal input terminals should have a larger area than its image signal input terminals. Flasck, §§VI.D.3, IX.F, X. Sano thus independently motivates and renders obvious claim elements [1i], [1l], [10j], and [23l].

G. Nakanishi

Nakanishi shows that POSITA's general knowledge included use of wider clock input terminals and power source terminals near the outer edges of a substrate, with narrower image signal input terminals near the center:

【図1】


scanning lines
clock signal input terminals
21
data lines
22
image signal input terminals
27
34
ACF
external data drive
33
32
31
Mounting member

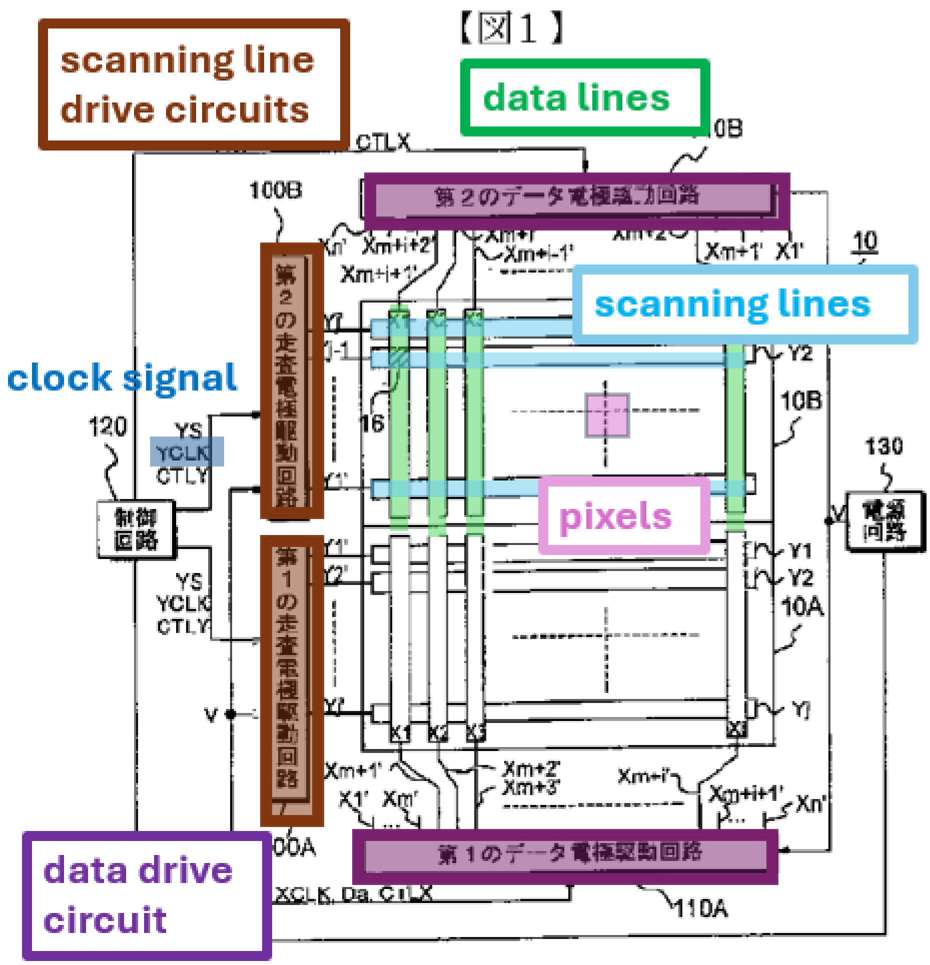


Ex. 1010, Figures 1, 2, 6.

Similar to Minami and Sano, Nakanishi's wider terminals overlap wiring in a mounting member (*e.g.*, flexible printed circuit) through ACF by a larger area than the narrower terminals overlap their wiring through the ACF. *See* Figures 1, 2 and 6. And like Minami, Nakanishi discloses that using larger area clock input terminals and power source terminals, nearer to the ends of the substrate (Ex. 1010, ¶¶[0052], [0053]), makes "the pressure application conditions as uniform as possible over the entire surface of the bonded portion." ¶[0054]. This "eliminates electrical resistance unevenness in the bonded portion, thereby preventing display defects such as display unevenness and contrast degradation caused by electrical resistance unevenness in the bonded portion." ¶[0013]. Thus Nakanishi underscores that [10j], [23l], [1h], [1i], and [1l] are obvious. Flasck, §§IX.G, X.

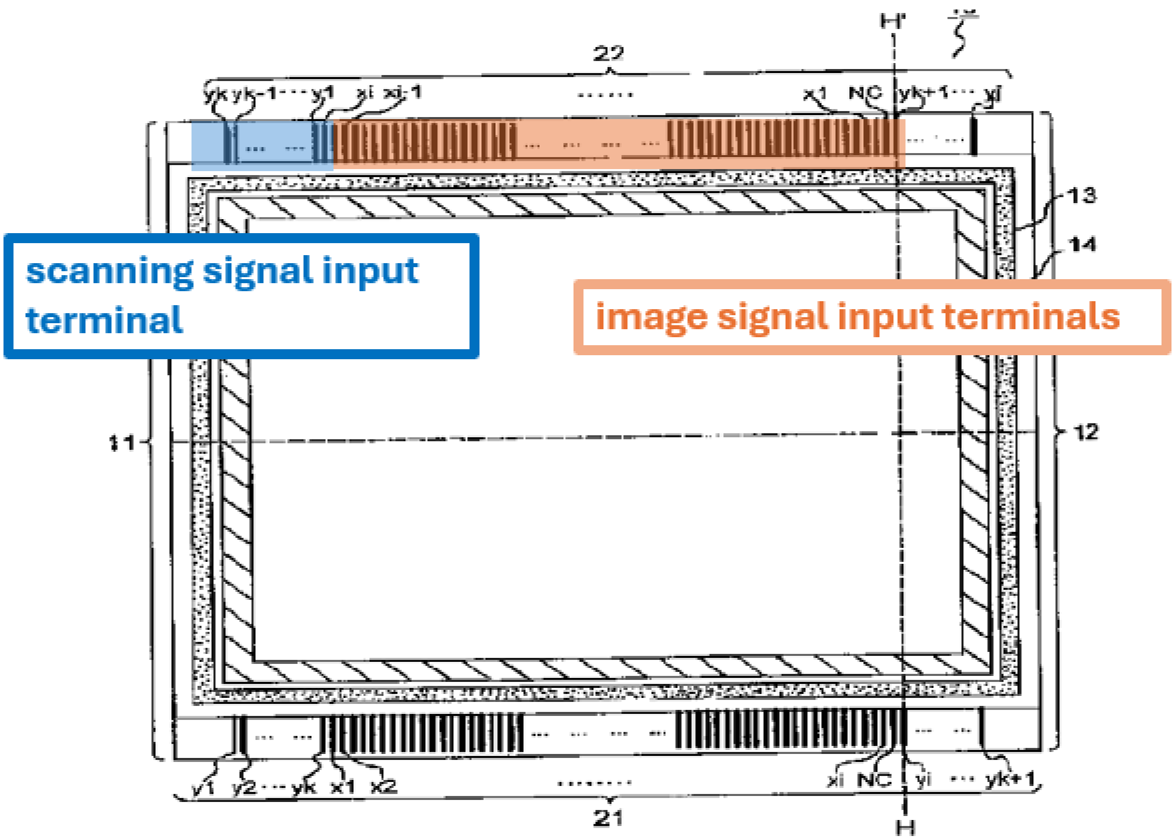
H. Kawaguchi

Kawaguchi also discloses most of the conventional technology recited in the challenged claims:



Ex. 1005, Figure 1. And like Nakanishi, Kawaguchi's data drive circuit is implemented on an external substrate; its wirings are in a mounting member (flexible circuit board) that is bonded to the LCD panel's image signal input terminals with

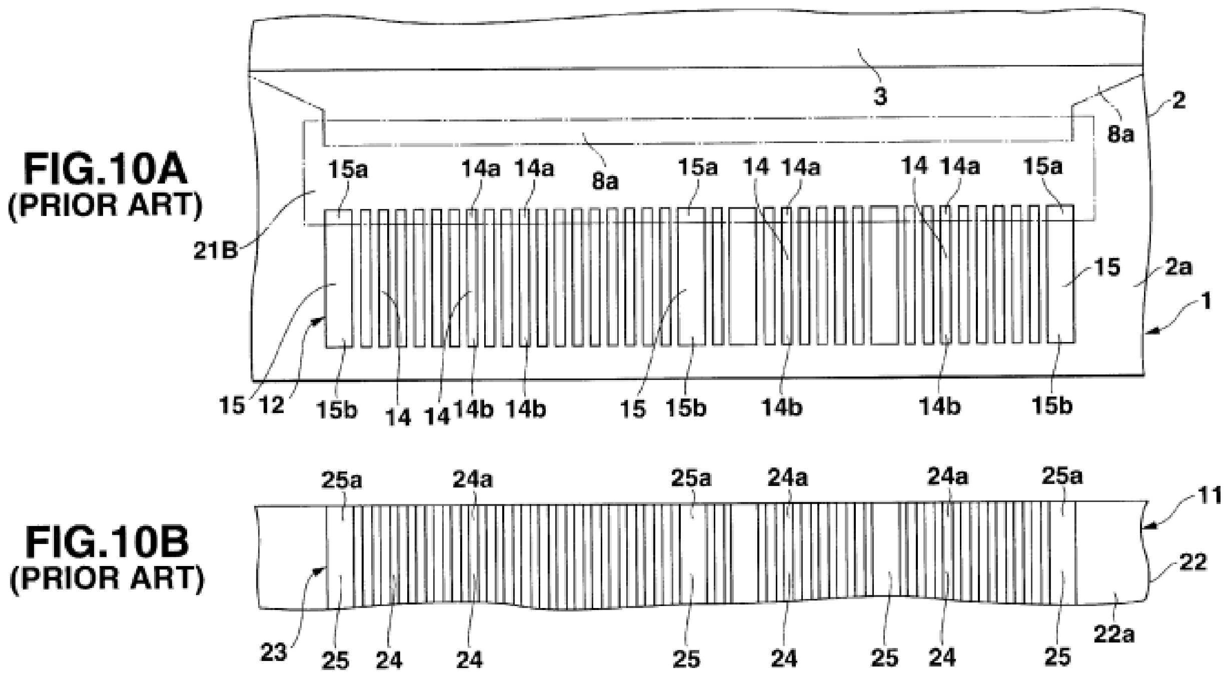
ACF. ¶[0055]. Kawaguchi also renders obvious forming input terminals on a line at the edge of the LCD panel's substrate, with image signal input terminals disposed closer to the substrate's center:



Id., Figure 2; Flasck, §IX.H.

I. Kato

Kato teaches that power supply wiring in an LCD display must be "made wider than the signal input wire" in order "to reduce the wire resistance, because a larger current flows through the power supply wire than through the signal input wire." Ex. 1009, ¶[0009]. The power supply input terminals (15b) therefore have a larger area than the image signal input terminals (14b), as shown in Figure 10A (illustrating input terminals on an LCD display panel (1)) and Figure 10B (illustrating wiring in a flexible wiring board (11) that is electrically connected to the input terminals of Figure 10A):

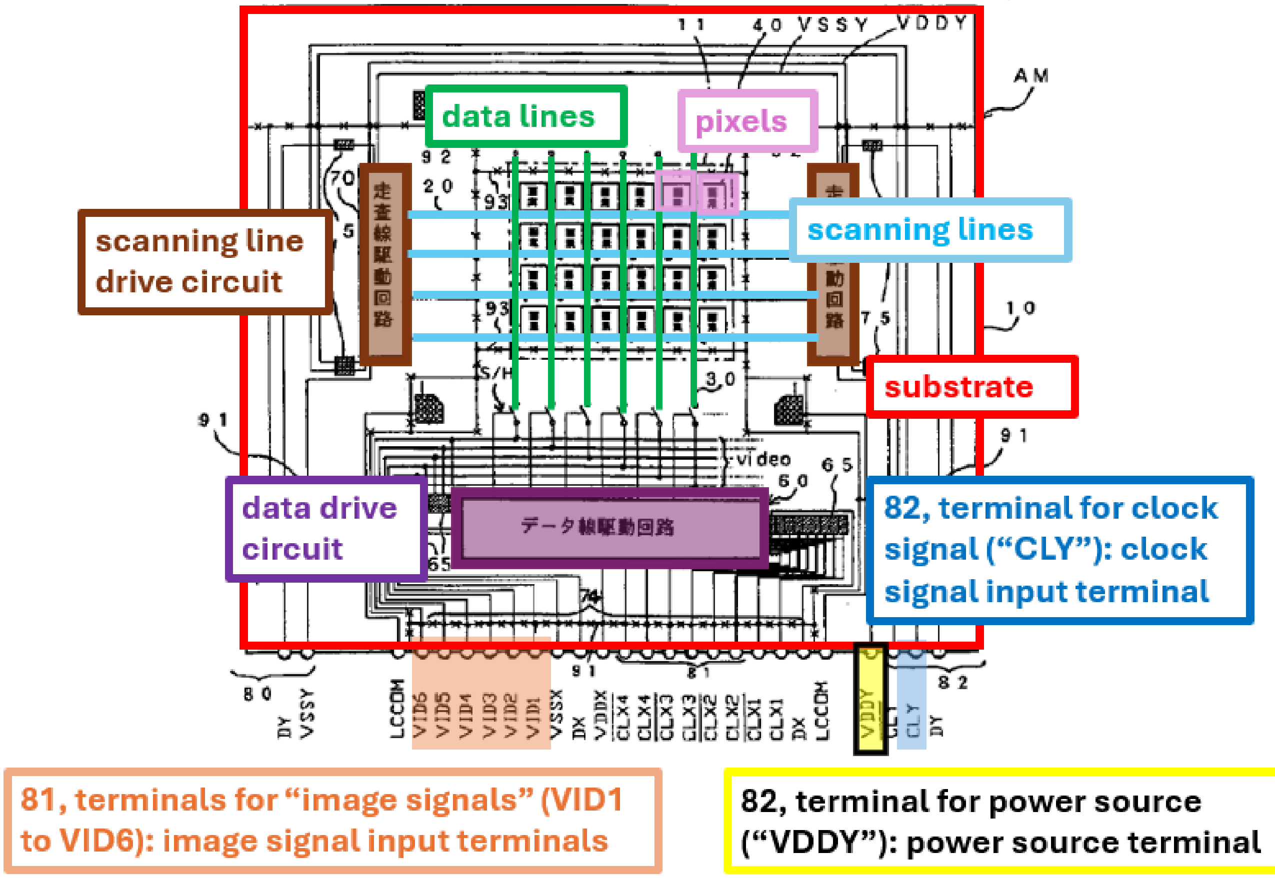


Ex. 1009, Figure 10 and ¶[0010]. A POSITA knew that power terminals conduct larger currents than clock signal input terminals, so it would have been obvious that the area of the power source terminals should be "not smaller than" than the clock input terminals' area, as recited in [1h]. Flasck, §§IX.I, X.

A POSITA knew that a high resistance power supply terminal would be problematic. First, the voltage drop is current times resistance ("IR drop"). Power supply signals use higher current than image signals, so the IR drop can be substantial. Any voltage drop at the terminal will be subtracted from the voltage intended to be delivered, thereby causing potential malfunctions in the LCD device. Ex. 1011, ¶[0070] (". . . the voltage drop at the upstream source driver ICs 20 becomes large because larger current flows through the power supply wiring line . . ."). Second, currents in a terminal generate heat (with wattage of current squared times resistance), and an overheated terminal could cause damage. Kato teaches that a larger area power supply terminal has lower resistance, making this an obvious choice. Flasck, §IX.I.

VIII. MOTIVATION TO COMBINE

The claims recite admittedly conventional technology that was used for decades before the '146 patent, including a "substrate"; "pixels"; "data lines" and "data line drive" circuits; "scanning lines" and "scanning line drive" circuits; signals with associated input terminals; and the "known" technique of connecting terminals to wiring through ACF. §IV.A.1, *supra*. Kitawada discloses all of this plus clock signal, image signal, and power source terminals formed in a line along one side of an LCD panel's substrate (as recited in [1k], [10g], [23g], and claims 4 and 12):



Ex. 1004, Kitawada, Figure 2. While Kitawada may not expressly disclose larger area clock signal and power source terminals, the prior art supplies independent reasons for modifying Kitawada in this manner, rendering obvious [11], [10j], [231], [1h], and [1i]. Flasck, §X.

First, Kitawada’s clock signal and power source terminals are lined up on the edge of the substrate near the outer side of the terminal block, with the image signal input terminals near the center. Ex. 1004, Figure 2. Per the teachings of **Minami** (and other art including Nakanishi and Mismatch Analysis Report), a POSITA would have known and been motivated to make the terminals on the outer side have a larger area to mitigate known problems of weakened ACF bonding, outer terminal "mismatch," and the like, rendering obvious [1i], [10j], and [23l]. §§VII, *supra*; Flasck, ¶¶161-163. Indeed, the '146 patent inventor later realized that clock signal input terminals and power source terminals can be "disposed at the outer side of the substrate" where "heat and pressure are applied" when "connecting each terminal with ACF," and he noted that "the outer side of ACF tends to have a larger extension rate than the central part." Ex. 1001, 3:10-22. So, he adopted the *same* solution that Minami and Nakanishi disclosed previously, for the *same* reasons: "by disposing an input terminal having a wider area at a more outer side than the input terminal having a smaller area, it is possible to prevent a connection failure because of the difference in the contraction rates as long as the input terminal is a large one even if a slight misalignment of the connection arises." *Id.*; 4:24-31.

Second, Sano independently motivates larger area clock input terminals, rendering obvious [1i], [10j], and [23l]. **Sano** teaches clock input terminals must transmit "high frequency" components to the scanning line driver with fidelity or else the LCD will malfunction. Ex. 1006, ¶¶[0017], [0014], [0018]; Flasck, §VI.D.3. Increasing the area of Kitawada's clock input terminals would involve ordinary skill. The '146 patent later adopted this *same* solution, for the *same* reason: when "the area of the input terminal of the driving signal having a high frequency component is larger than the area of the input terminal of the image signal having a lower frequency component," then "the contact resistance can be made low, and thus the signal can be prevented from becoming dull." Ex. 1001, 4:19-24; 2:42-58; 7:27-55; Flasck, ¶¶164-165.

Third, a POSITA would have known and been motivated to utilize power source terminals having an area "not smaller" than clock signal input terminals' area, rendering obvious [1 h], because, as **Kato** teaches, power source terminals transmit "larger currents" and so their resistance needs to be lower. *See* §§VII, IX; Flasck, ¶166. The '146 patent's inventor later adopted this *same* solution for the *same* reasons that Kato had previously disclosed it:

> In general, if a power source, which is input into a power terminal, has a high resistance, the voltage is trapped, and there is a strong possibility that a predetermined voltage cannot be obtained. Therefore, the power source preferably has as low a resistance as possible. Accordingly, in the above-described panel, the power terminal to which power is supplied preferably has the same area or more as the area of the input terminal to which the driving signal is supplied. With this arrangement, it becomes possible to decrease the resistance, and to supply a predetermined voltage.

Ex. 1001, 3:23-41.

Minami independently teach and motivate "not smaller" power source terminals. Kitawada's power terminals are adjacent to its clock signal terminals, all of which are located near the outer ends of the substrate. Ex. 1004, Figures 1-2. Per the teachings of Minami (like Mismatch Analysis Report and Nakashini), terminals there should have a larger area to mitigate known problems such as terminal-to-wiring mismatch and weakened ACF bonding strength. Since Kitawada's power terminals are adjacent to its clock signal terminals, a POSITA would have known that the power terminals are not smaller. Flasck, ¶167.

* * * * *

In summary, there are two reasons to use larger area clock signal terminals in Kitawada—one is of a simple mechanical nature related to bonding terminals to wiring through ACF, the other is simply to decrease resistance. First, Kitawada's clock signal terminals are near the outer side of the substrate, so according to Minami's (and Nakanishi's and Mismatch Analysis Report's) teachings, they should have a larger area than the image signal terminals near the center. Second, clock terminals should have a larger area to lower their resistance so they can pass the "high frequency" components of clock signals, per Sano. When the LCD display's input terminals are connected to wiring through ACF, the larger area terminals necessarily overlap their wiring by a larger area through the ACF than do the smaller image signal terminals. Flasck, ¶¶168-169.

Similarly, a POSITA would have known two reasons to use larger area power source terminals in Kitawada. First, Kitawada's power source terminals are also near the outer side of the terminal block and should thus have a larger area according to Minami (and Nakanishi and Mismatch Analysis Report)—and thus within POSITA's general knowledge. Second, power terminals should have a larger area to lower their resistance to conduct "larger currents"—a well-known, basic principle of engineering expressly taught by Kato. A power source terminal's currents are at least as large as a clock signal input terminal's are, so it would have been obvious that the former have "not smaller" areas. Flasck, ¶170.

The prior art's reasons to adjust the area of terminals are the exact *same* reasons that the '146 patent claims "larger area" clock signal terminals and "not smaller" power source terminals. Ex. 1001, 3:10-41; 4:24-31; §§VII and IV.A.2, *supra*.; Flasck, ¶171, §X. This is significant because the "motivation to modify a prior art reference to arrive at the claimed invention need not be the same motivation that the patentee had." *Alcon Rsch., Ltd. v. Apotex Inc.*, 687 F.3d 1362, 1368 (Fed. Cir. 2012). Indeed, to demonstrate a motivation to combine, it is "enough" for Petitioner to "show that there was a known problem" in the art, that one prior art reference "helped address that issue," and that "combining" prior art references "wasn't beyond the skill of an ordinary artisan." *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1381 (Fed. Cir. 2023). Here, there were known problems when terminals (i) were too small when located near the corners of an LCD display's substrate and/or (ii) had too high of a resistance. The prior art of the Grounds addressed both problems in a straightforward and obvious manner: using larger area clock signal and power source terminals with smaller area image signal input terminals. A "mere change in proportion" of the area of Kitawada's terminals—as explicitly taught by the prior art—"would involve no more than mechanical skill and would not amount to invention." *Powers-Kennedy Contracting Corp. v. Concrete Mixing & Conveying Co*., 282 U.S. 175, 185 (1930). Said another way, it is obvious to resize a component of a known device when, as here, doing so would improve the device's operation. *Novo Nordisk A/S v. Becton Dickinson and Co*., 304 F.3d 1216, 1218-19, (Fed. Cir. 2002) (affirming obviousness of claim reciting medical device having a specific "30 gauge" needle size where "the known pain reduction provided the requisite motivation to narrow the needle").

IX. GROUNDS

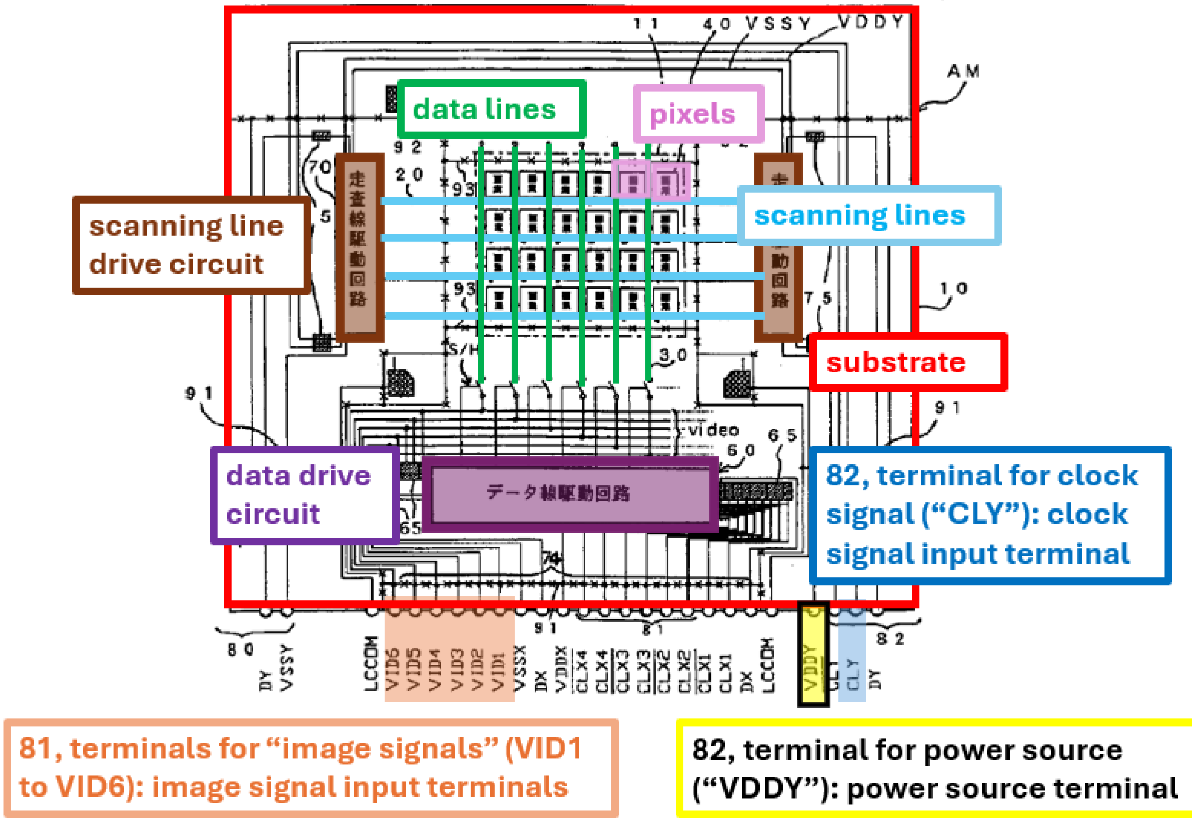
A. Ground 1: Claims 10-23 are Obvious over Kitawada in view of Kawaguchi, Matsumoto, and Minami or Sano

1. Claim 10[3]

a. [10pre]-[10d]

Kitawada discloses a "liquid crystal display device." Ex. 1004, ¶[0013]-[0014], Figures 1-2. It includes a first substrate ("substrate 10"), data lines ("data lines 30"), scanning lines intersecting the data lines ("scan lines 20") and pixels ("pixels 40") disposed corresponding to the intersections between the data lines and scanning lines:

[3] Given the length of the twenty-three claims, Petitioner does not repeat the claim elements, which are identified in the "Claim Listing" at pages vi-xii.



Ex. 1004, Figure 2; ¶[0017]; Flasck, ¶172, §§IX-XI.

b. [10e]

Kitawada discloses a clock-signal input terminal (82, terminals for "CLY" and/or inverted CLY) supplied with a clock signal ("CLY" and/or inverted CLY). Ex. 1004, ¶[0019] ("Meanwhile, start signal DY, clock signal CLY, and inverted clock signal CLY bar are supplied from outside via terminals to the scan line drive circuits 70, and the scan line drive circuits 70 are driven by these signals."); ¶[0014] ("various terminals 80, 81, 82, etc., data line drive circuit 60, and scan line drive circuits 70 are located to the outside of the opposing substrate OP."); ¶[0020].

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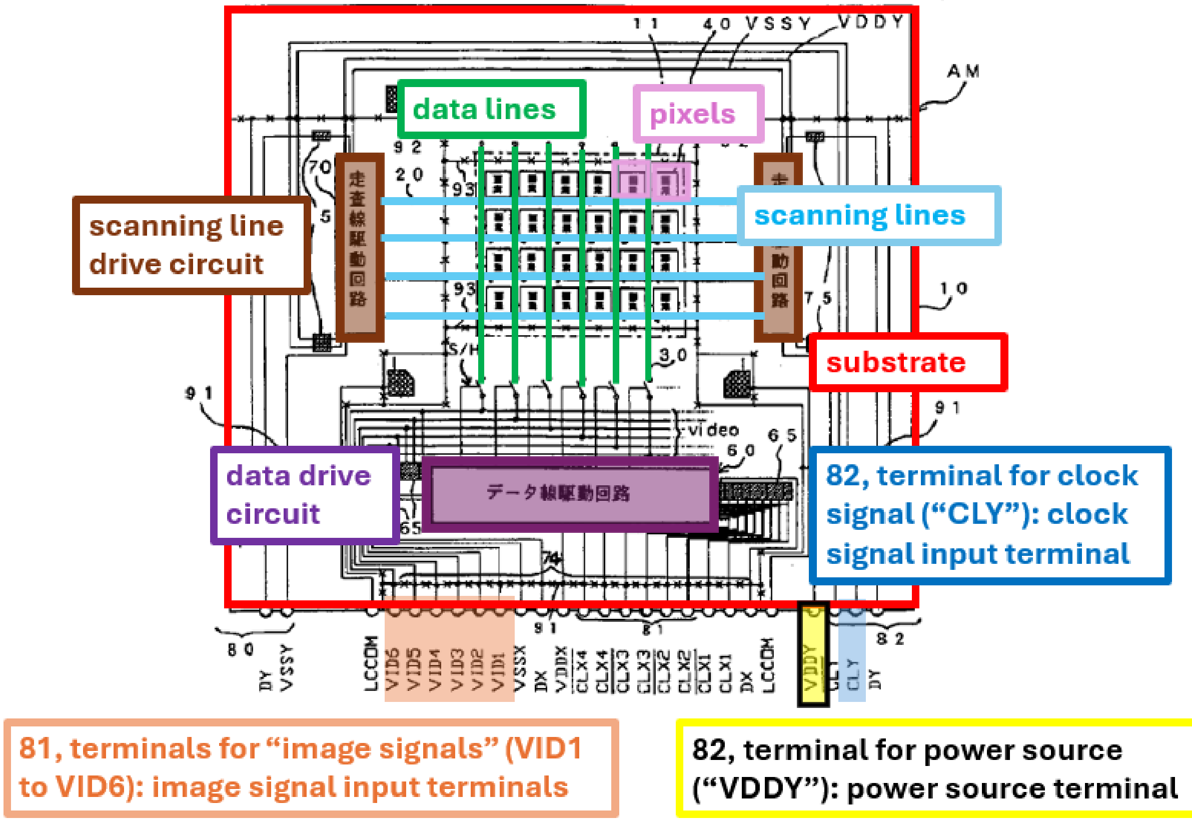
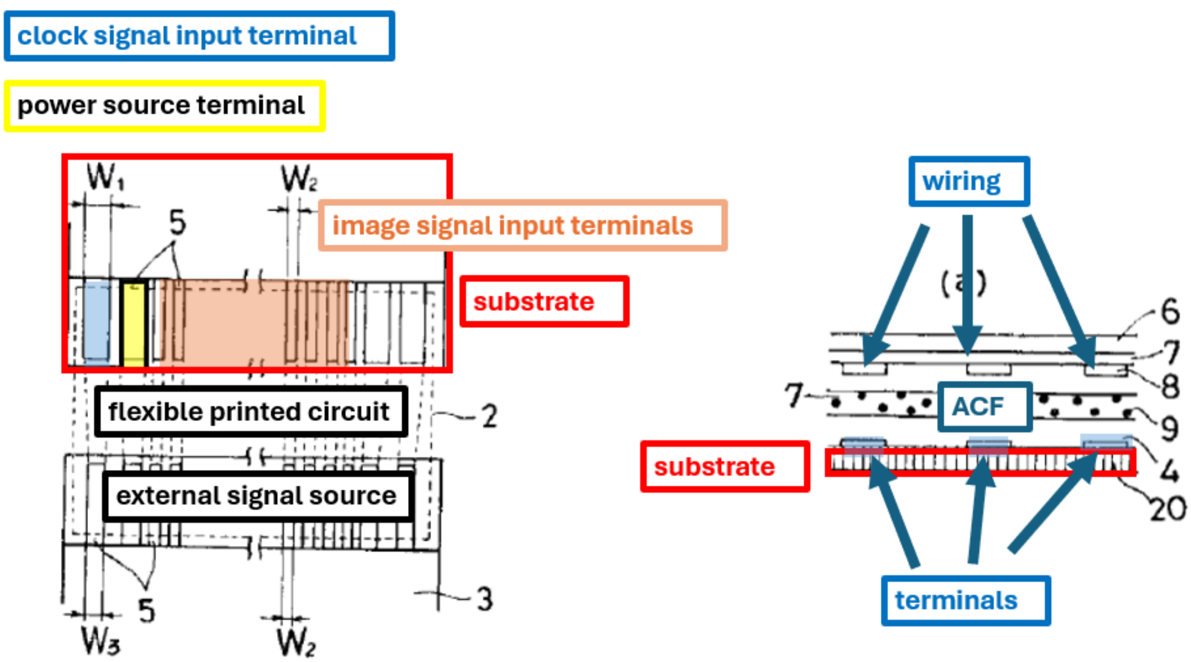


Ex. 1004, Figure 2. Kitawada renders it obvious that the clock-signal terminals are connected to a mounting member ("flexible wiring substrate, etc.") through anisotropic conductive film. *See* ¶[0029] ("a flexible wiring substrate, etc., can be connected to the pads 9c (terminals) with a high degree of reliability.").

Using ACF like this was conventional, within the general knowledge of a POSITA (Flasck, ¶¶175-176, 109-119) and the '146 patent admits that displays like those claimed were "known" (Ex. 1001, 1:17-62) and admits that "means for supplying the power source, etc. to the electro-optical panel, techniques which connect an input terminal formed on the electro-optical panel and a flexible substrate as a connection cable through an anisotropic conductive film are known." *Id*. at

1:51-62. These binding admissions underscore that it would have been obvious to connect Kitawada's clock signal input terminals to a "flexible wiring substrate," (Ex. 1004, ¶[0029]) through ACF—an *admittedly* known technique. *Shockwave*, 142 F.4th at 1378-79.

Minami is further evidence that connecting input terminals to a flexible printed circuit through ACF was well known to a POSITA:



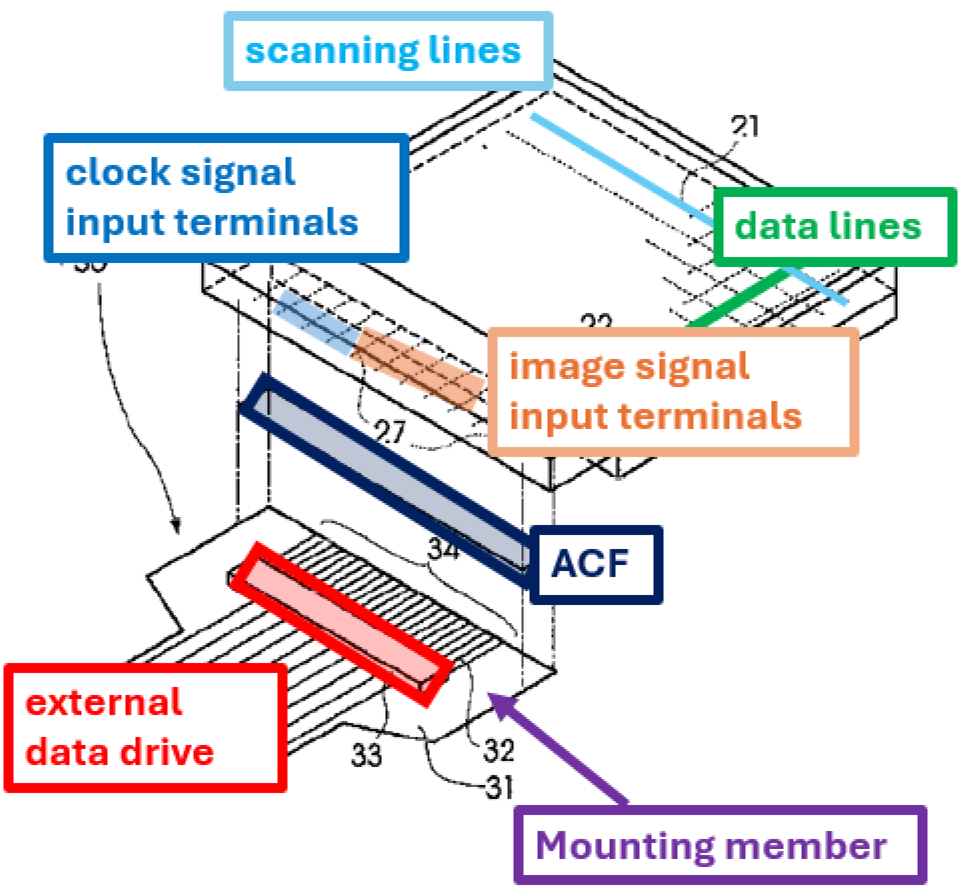
Ex. 1007, Figures 3 and 2a; see page 14 of 18 (describing Figure 2).

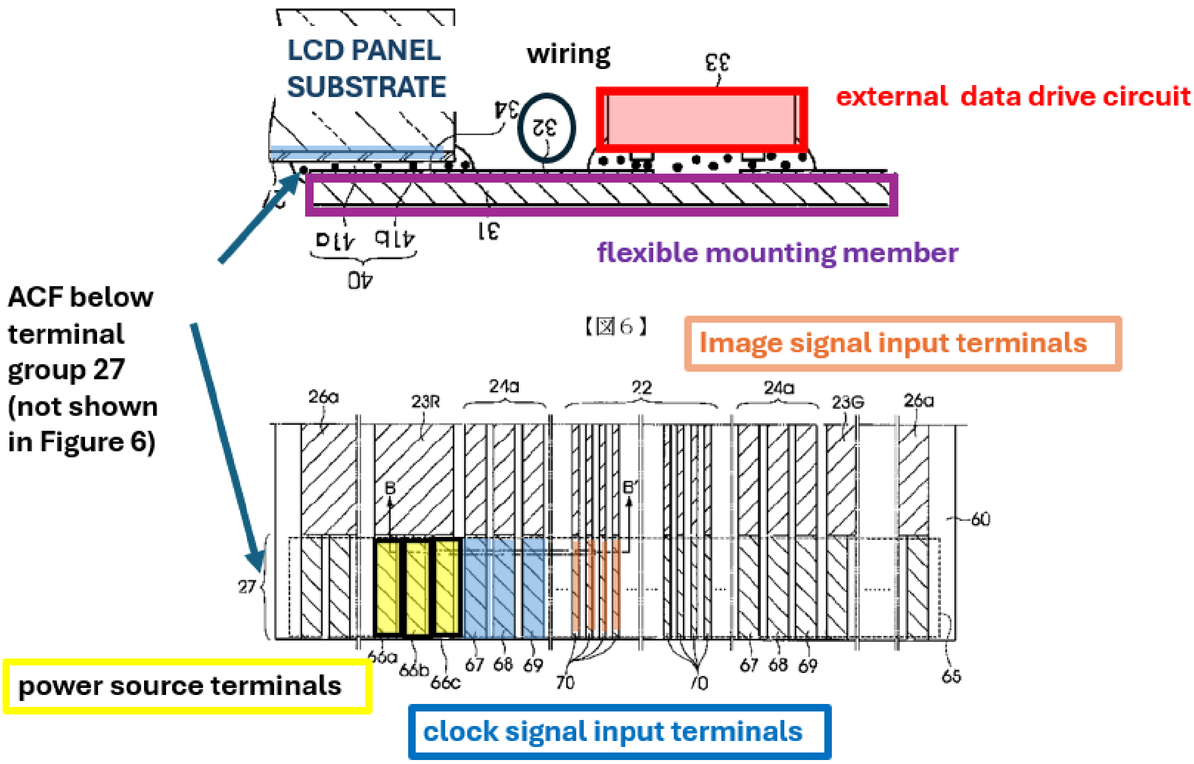
Further, **Kawaguchi** also discloses an LCD display similar to Kitawada's (Flasck, ¶¶173, 174), and uses ACF to connect terminals to mounting members. Kawaguchi, Ex. 1005, ¶[0055] ("The connection between the output terminal group 316 of the first TCP 31 and the input terminal group 21 of the first panel

10A is made using an anisotropic conductive film (ACF), which contains conductive microparticles in an adhesive.”). A POSITA would understand that ACF could be used in a similar way to, as Kitawada teaches, connect its “flexible wiring substrate, etc.” to the input terminals “with a high degree of reliability.” Ex. 1004, ¶[0029].

Nakanishi is yet another reference teaching connecting input terminals (for clock signals, image signals, and power sources) to a mounting member through ACF, demonstrating that this was within POSITA’s general knowledge:

【図1】



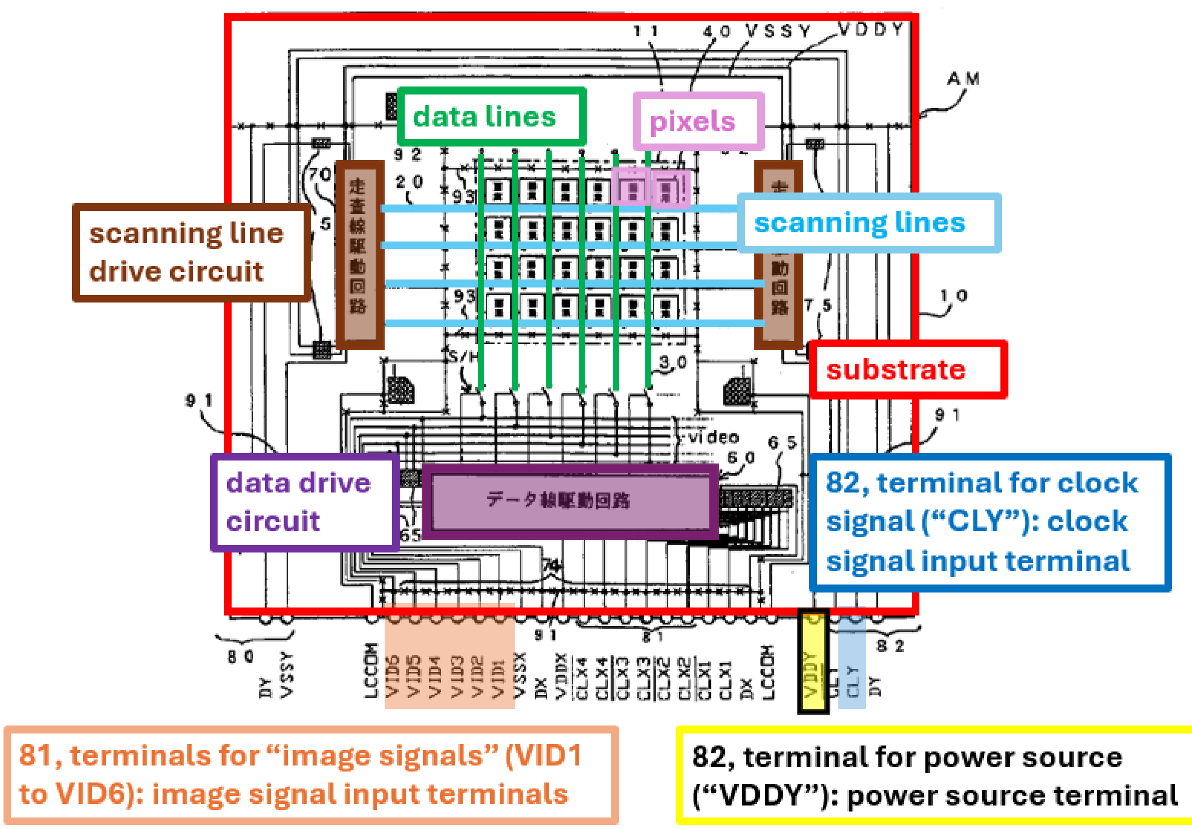


Ex. 1010, Figures 1, 2, 6; ¶[0019] ("As shown in FIG. 1, the intermediate substrate 30 is fixed to the display substrate 20 via an anisotropic conductive film 40. At this time, external connection terminals 34 on the intermediate substrate 30 are electrically connected to external connection terminals 27 on the display substrate 20 via the anisotropic conductive film 40. This anisotropic conductive film 40 is a conductive polymer film used to electrically connect pairs of terminals in an anisotropic manner and is formed, for example, by dispersing a plurality of conductive particles 41b in a thermoplastic or thermosetting adhesive resin 41a, as shown in FIG. 2.").

In summary, Kitawada teaches limitation [10e] which was also within the knowledge of a POSITA as evidenced by the teachings of Kawaguchi, Minami, and Nakanishi. Flasck, ¶¶173-178, §§IX, X, XI.

c. [10f]

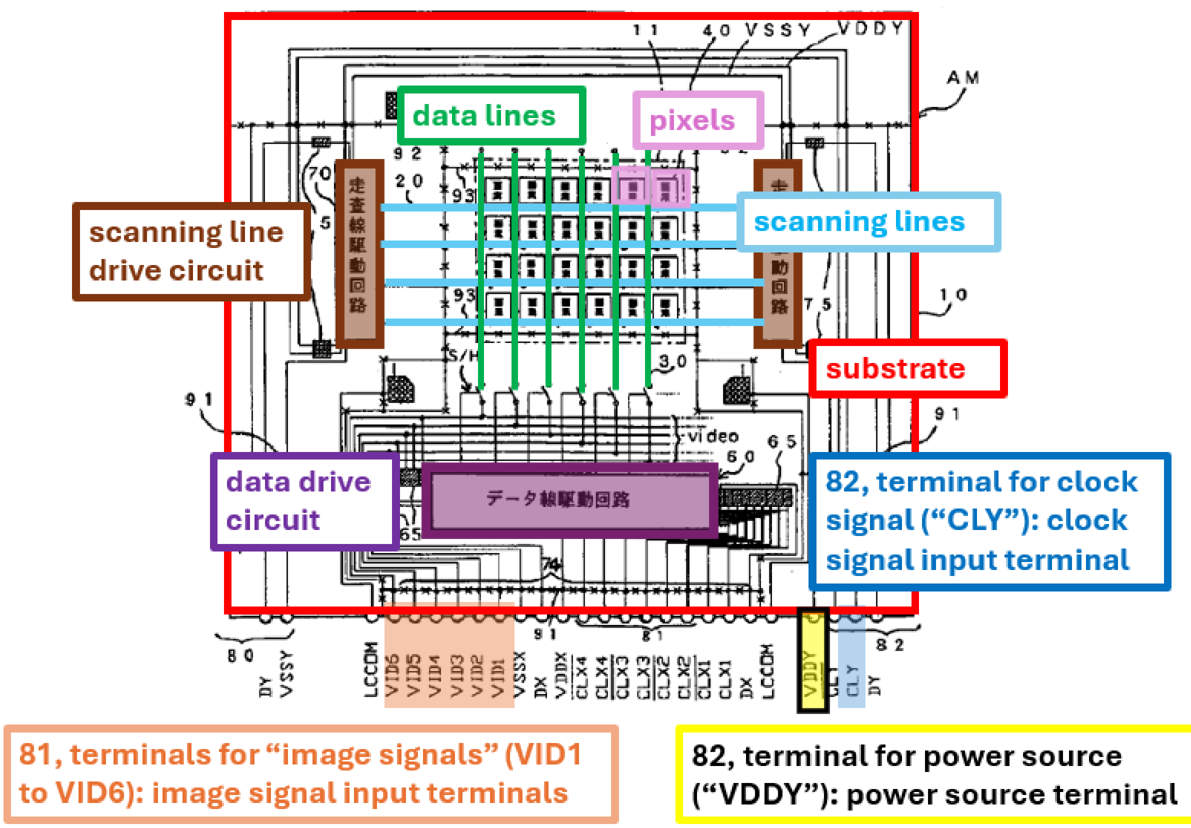
Kitawada discloses image-signal input terminals (81, terminals for "VID1" to "VID6") supplied with image signals ("VID1" to "VID6"). Ex. 1004, ¶[0020] ("[A]long the edges of the insulating substrate 10, the edge portion on the side with the data line drive circuit 60 includes constant power supplies VDDX, VSSX, VDDY, VSSY, and a plurality of terminals 80, 81, 82 . . . to which modulated video signals (image signals VD1 to VD6), and various drive signals, etc. are inputted.").



Ex. 1004 Figure 2. For the same reasons that [10e] is obvious, Kitawada teaches and renders it obvious that the image-signal input terminals are connected to a mounting member through anisotropic conductive film. ¶[0029] ("a flexible wiring substrate, etc., can be connected to the pads 9c (terminals) with a high degree of reliability."). Flasck, ¶179, §§IX, X, XI.

d. [10g]

Kitawada discloses clock signal input terminals and image signal input terminals disposed along one side of the substrate:



Ex. 1004, Figure 2; *also* Figure 1; ¶[0020]; Flasck, ¶180.

e. [10h]

Kitawada discloses a "data line drive circuit 60 is configured in the outer region (peripheral portion) of the pixel portion 11 on the insulating substrate 10 to supply video signals to each of the data lines 30." Ex. 1004, ¶¶ [0018]-[0020]. If it is argued that Kitawada fails to disclose supplying image signals "simultaneously to all of the data lines," simply because the word "simultaneously" does not appear in Kitawada, this is taught by **Matsumoto** and would have been obvious and within the general knowledge of a POSITA.

First, Figure 2.21 of Matsumoto discloses an LCD device that is remarkably similar to Kitawada's in that it has pixels disposed at the intersection of scanning lines (X1 … Xn) and data lines (Y1 … Yn):

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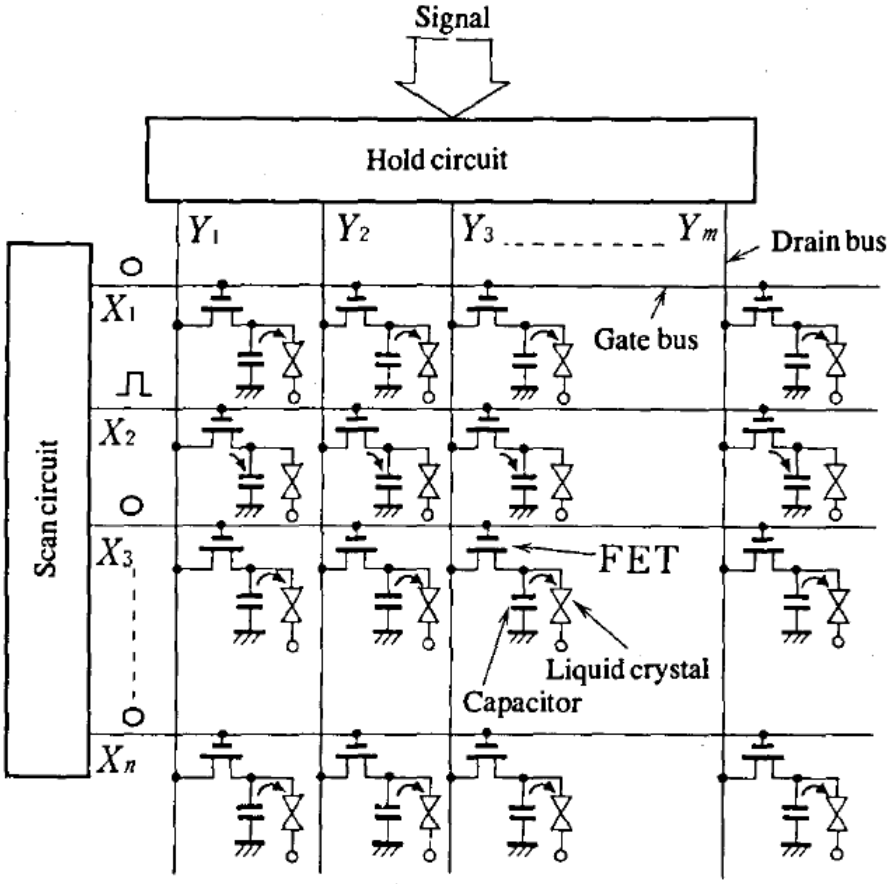

Figure 2.21 *Operating principle of active matrix drive LCD*

Ex. 1008. Like Kitawada's teachings, Matsumoto teaches a data line drive (*i.e.*, "Hold circuit") that supplies the image signals, and a scanning line drive (*i.e.*, "Scan circuit") that activates the pixel transistors in a row-sequential manner via a "Gate bus." *See* above. The '146 patent also admits that this structure was "known" and "widely used." Ex. 1001, 1:18-62.

Importantly, Matsumoto teaches that the image signals are supplied from the Hold circuit to all data lines "***simultaneously***." Ex. 1008, page 51 of 85 ("Figure 2.21 shows the operating principle of an active matrix drive LCD using FETs. Using a line scan technique, the row electrodes (gate buses) X 1, X 2, .. , X n are scanned sequentially, so that all of the FETs on one gate bus are turned on (conducting) ***simultaneously***, and the signals for the current row are supplied from the hold circuit through the drain buses Y1,Y2 , .. , Ym through the conducting FETs to the capacitors. The liquid crystal elements are sustained in their current state by the charge on the capacitor until the next scan.") (emphasis added).

Moreover, the original applicant admitted [10h] covers the "well-known" line sequential method. Ex. 1003, Response dated Sept. 17, 2008 at page 386 of 473. The applicant's translation of the discussed portion of the cited prior art (reproduced below) closely resembles the text of Matsumoto cited above:

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2008年 8月 7日 18時11分 NO. 1216 P. 7

EPSON
EXCEED YOUR VISION

SEIKO EPSON CORPORATION

Partial translation of Liquid Crystal Display Technology

Page 14, Fig. 1.11 and first paragraph

Fig. 1.11 shows the operating principle of an LCD using three-terminal elements by active matrix drive. The scanning row electrodes (gate bus) X_1, X_2, ... X_n are scanned one after the other using a line sequential drive method so that all of the three-terminal elements on one gate bus are temporarily turned ON all at once. In synchronization with this scanning, signal electrical charges from the hold circuit are supplied through the signal column electrodes (drain bus) Y_1, Y_2, ... Y_m to all of the capacitors connected to the three-terminal elements in this ON condition. These signal electrical charges continue to be applied to the liquid crystal of all pixels on the gate bus until the next frame of scanning.

Page 70, lines 12 to 14

Writing to the pixel electrodes is performed by a method wherein signals supplied simultaneously to the signal lines D_1, D_2, ...D_m are sampled using address signals sequentially supplied to the scanning lines G_1, G_2, ... G_n. This is called line sequential drive.

Ex. 1022. And Figure 1.1 of the applicant's cited reference (reproduced below) is virtually identical to Figure 2.21 of Matsumoto (shown previously):

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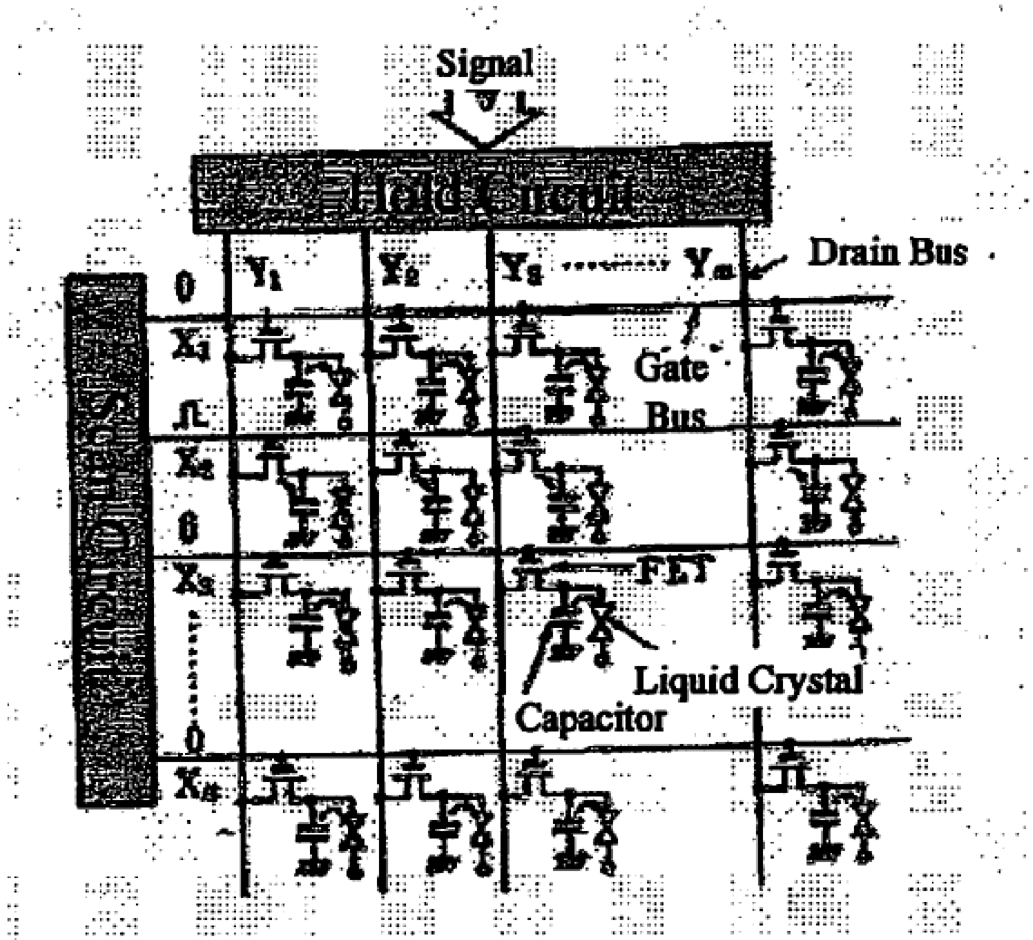


Fig. 1.11 Operating principle of three-terminal element type active matrix drive LCD

Ex. 1022. These admissions underscore that it would have been obvious to supply image signals simultaneously to all data lines. *Shockwave*, 142 F.4th at 1378-79. A POSITA would have known and been motivated to use this method, as evidenced by the teachings of Matsumoto and the AAPA, with the LCD display of Kitawada to increase the display's refresh rate, decrease motion blur, reduce flickering and dynamic distortion, increase the accuracy of motion detection and compensation, and decrease the response time. Flasck, ¶182.

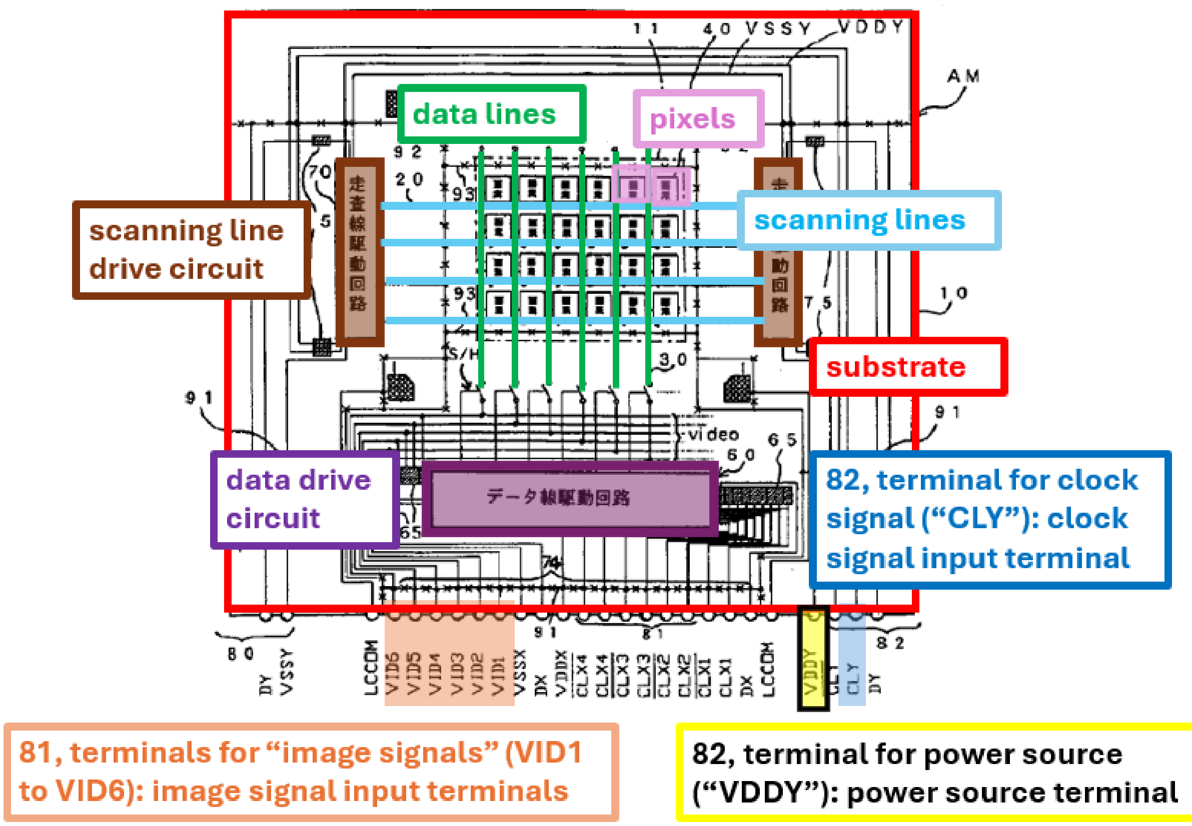
Element [10h] further recites an "external data drive circuit" but Kitawada's "data line drive circuit 60" is formed on the panel's substrate. Whether the data drive is external or on the substrate is a simple design choice between two conventional options known to a POSITA. **Kawaguchi** discloses an external data driver that is connected to the panel's image signal input terminals using a flexible mounting member bonded with ACF. Kawaguchi, Ex. 1005, ¶[0055]; Flasck, ¶¶183-186. This was within POSITA's knowledge as shown further by Nakanishi, Ex. 1010, Figures 1, 2; This was *admittedly* a "known" technique (Ex. 1001, 1:57-62), and there are a finite number of ways of implementing a data driver, *viz*., forming it on the substrate (like Kitawada) or using an external driver (like Kawaguchi). Both configurations were conventional; many other publications teach external data drives. Ex. 1012, Figure 1 and 18:31-38; Ex. 1015, ¶[0047].

A POSITA would understand the benefits of forming the *scanning* line drives on the LCD panel's substrate while using an external *data* drive to supply image signals to the data lines. Scanning signals generally involve only two voltage levels, one for "ON" (*e.g*., +15 to + 25 Volts), and one for "OFF (*e.g*., -5 to -30 Volts). It was easy for a POSITA to implement a scanning line driver on the LCD's substrate using semiconductor materials that were commonly used for displays at the time (amorphous silicon, polysilicon, oxide semiconductors). Flasck, ¶185, §VI.D.2. On the other hand, a POSITA would have known that image/data signals utilized a range of voltages (*e.g.*, -5 to + 5 Volts), divided into 256 subdivisions to control the grayscale of the pixels (*e.g.*, 8 bits = 2^8 = 256). Therefore, a POSITA would have known that such voltage levels required delicate fine tuning of the transistor characteristics and precise output of the voltage. A POSITA knew that this was relatively difficult to achieve on a TFT made of amorphous silicon, polysilicon, or oxide semiconductor—which are the materials that could be manufactured to form the TFT on the LCD's glass substrate. *Id*. So, a POSITA normally would have implemented an external image signal driver on silicon chips made of single crystalline silicon. It was well within the knowledge and would have been obvious to a POSITA (at least as supported by the teachings of Kawaguchi, Nakanishi, and many others) to modify Kitawada by using an "external" data driver. This was nothing more than a simple design choice.

Additionally, it would have been obvious to modify Kitawada to utilize an external data driver circuit that is, for example, connected to the panel's image signal input terminals using a flexible mounting member bonded with ACF (within POSITA's general knowledge as taught by Kawaguchi and confirmed by Nakanishi), and a POSITA would have seen the benefits in doing so for the reasons mentioned above. *Uber Technologies, Inc. v. X One, Inc.*, 957 F. 3d 1334, 1339-40 (Fed. Cir. 2020) (invention obvious where references taught "identified, predictable solutions"). A POSITA had a "simple design choice" between using an external data drive or forming the drive on the substrate; both were predictable. *CRFD Research Inc. v. Matal*, 876 F.3d 1330, 1347 (Fed. Cir. 2017) (claims obvious where "a person of ordinary skill would have two predictable choices"); Flasck, §§IX, X, XI.

f. [10i]

Kitawada discloses a scanning-line drive circuit ("scan line drive circuits 70") that is formed on the first substrate:



Ex. 1004, Fig. 2; ¶[0018] ("In addition, scan line drive circuits 70 are configured at the ends of each scan line 20 to supply scan signals for pixel selection to each scan line 20."). If it is argued that Kitawada's scanning-line drives are not on the first substrate, this would have been obvious. As discussed in [10h], scanning line drives are simpler than data drivers and can be fabricated using thin film transistors which can be formed on the substrate. Flasck, ¶187. **Matsumoto** teaches that "the peripheral drive circuitry can be integrated on the same substrate as that for the FET array for the display" and motivates this configuration because it "simplifies the connection between the drive circuit and the display." Ex. 1008 at page 52 of 85. Sano also motivates "mounting" drivers "on the transparent substrate" because it "simplifies the manufacturing process." Ex. 1006, ¶[0002].

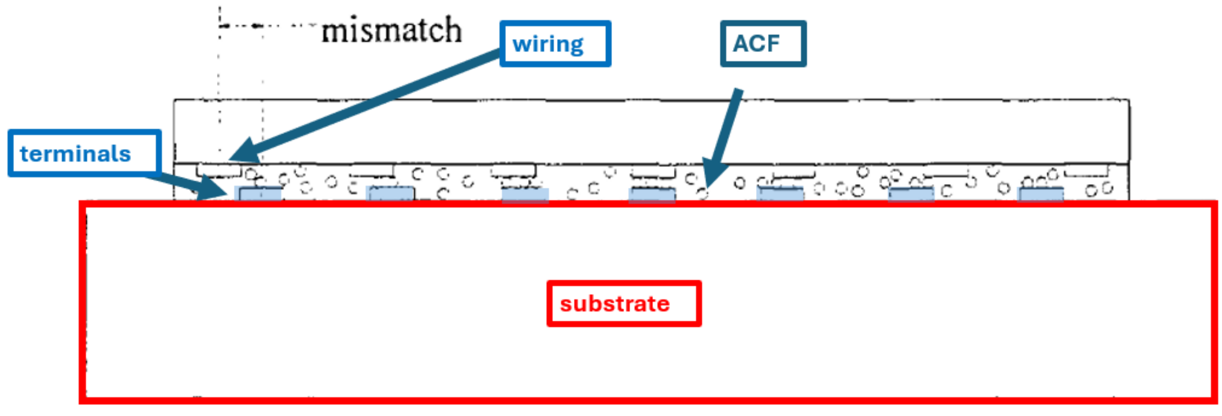
A POSITA would understand that Kitawada's scan line drive circuits sequentially transmit a start pulse ("start signal DY") in synchronization with the clock signal. Ex. 1004, ¶[0019] ("start signal DY, clock signal CLY, and inverted clock signal CLY bar are supplied from outside via terminals to the scan line drive circuits 70, and the scan line drive circuits 70 are driven by these signals"). Similarly, **Kawaguchi's** scanning line drive circuit sequentially transmits a transmission start pulse ("YS") in synchronization with its clock signal ("YCLK"). Ex. 1005, ¶[0032] ("Next, the first and second scan electrode drive circuits 100A and 100B include so-called bidirectional shift registers. Based on the power supply voltage V, Y shift start pulse YS, Y shift clock YCLK, and control signal CTLY, these bidirectional shift registers generate scan signals with a specified pulse width and timing. The scan signals are supplied sequentially line-by-line to the scan electrodes Y1, Y2, ..., Yj."); ¶[0033] ("At this time, the shift register starts shifting in response to the Y shift start pulse YS supplied every vertical scanning period and performs shifting operations in synchronization with the Y shift clock YCLK supplied every horizontal scanning period. As the shifting proceeds, the scan signals are sequentially generated in each horizontal scanning period."). This conventional technology is also disclosed by other patents. *E.g.*, Ex. 1021, 1:12-18 and Figures 2-3.

As shown, Kitawada, Matsumoto, and Kawaguchi render [10i] obvious. Flasck ¶187-190, §§IX, X, XI.

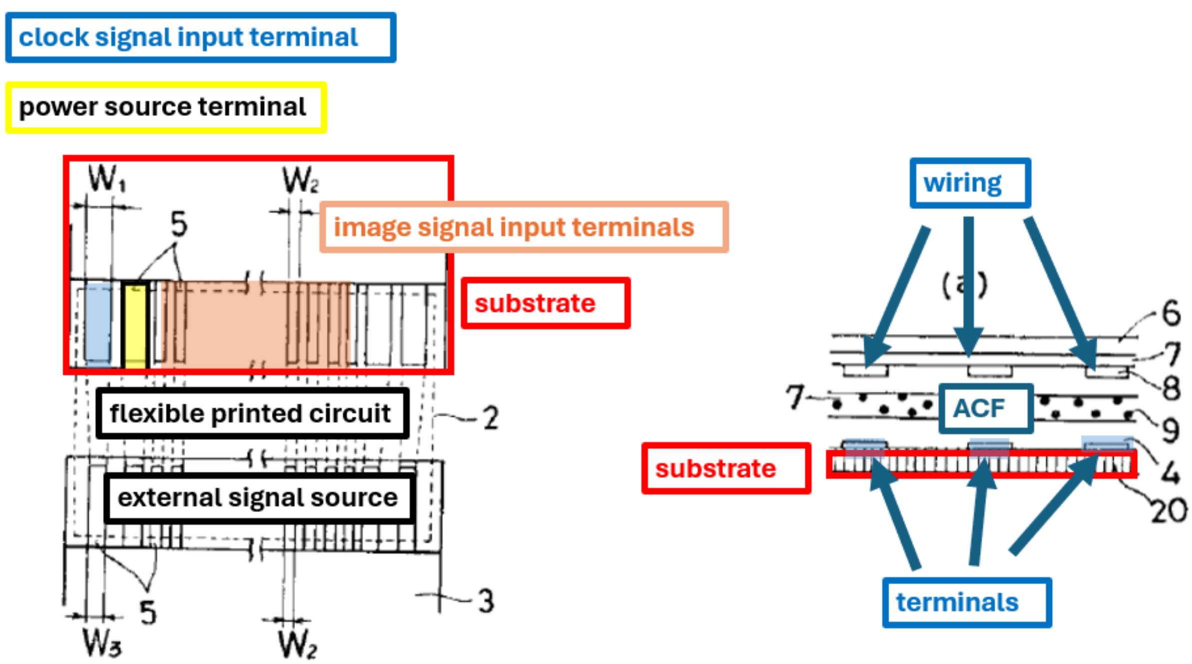
g. [10j]

It would have been obvious to modify Kitawada to use clock signal input terminals having a "larger area" than the area of the Kitawada's image signal input terminals; **Manami** and **Sano** ***independently*** teach this. Flasck, §X and ¶¶191-198; §VIII, *supra*. With this slight modification, Kitawada's clock signal input terminals would overlap a first wiring (supplying clock signals) in the mounting member (which Kitawada calls "a flexible wiring substrate, etc.") through the ACF by a larger area than an area at which at least one of Kitawada's image signal input terminals overlaps a second wiring (supplying image signals) of the mounting member through the ACF (*see* [10e] and [10f]).

By way of background, it was commonplace to connect terminals to wiring through ACF, which causes the terminals to "overlap" the wiring through the ACF:



Ex. 1014, Figure 1(b). And as discussed previously, Minami's Figure 3 (below on the left) shows that the outer terminals are wider (width "W_1") and have a larger area than the narrower terminals ("W_2") near the center of the substrate:



Ex. 1007. Since the outer terminals have a larger area, they will overlap their wiring by a larger area through the ACF. It is clear from Minami's Figures 1-3 that wiring electrodes 5 on LCD panel 1 (panel 1 corresponds to substrate 20 in Figure 2) overlap

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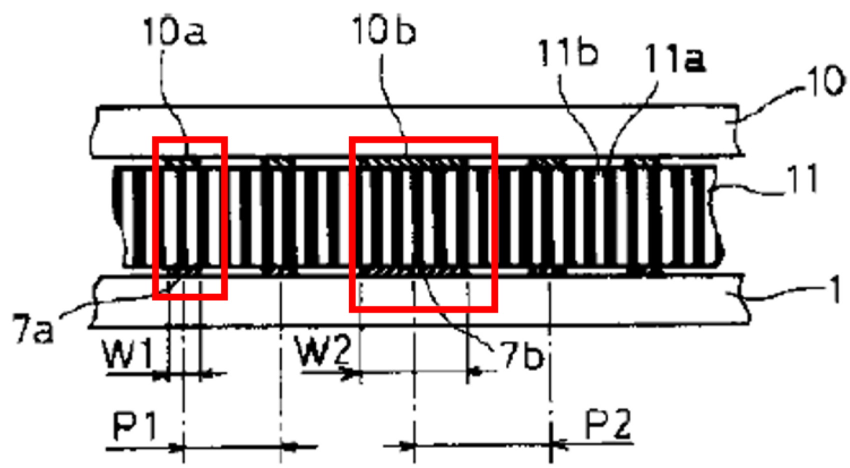
the copper wiring 8 shown in Figure 2 (corresponding to the dashed lines of FPC 2 in Figures 1 and 3) through the ACF by a larger area at the edges of the substrate (the location of Kitawada's clock signal input terminals) than in the center (where Kitawada's image signal input terminals are located). Flasck, ¶¶193-195.

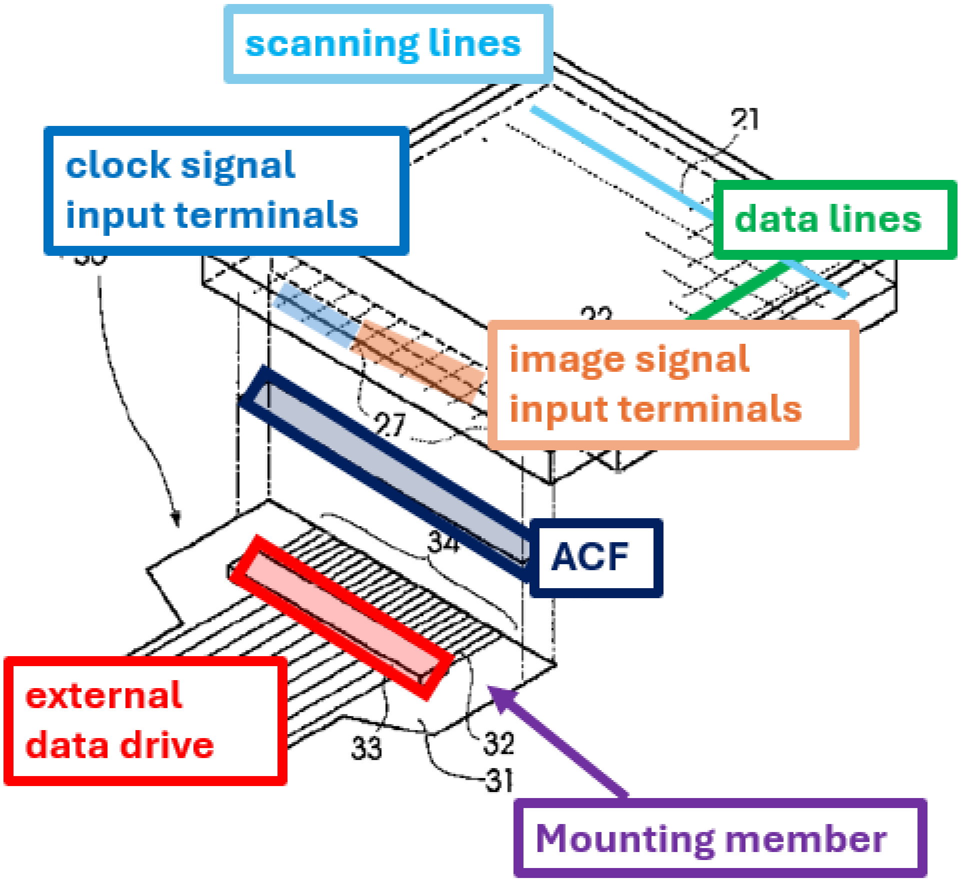
Alternatively, Sano's Figure 2 shows a side view of clock input terminals 7b (of width "W_2") overlapping wirings 10b through an anisotropic connector by a larger area than the other input terminals 7a (width "W_1") overlap wirings 10a through the anisotropic connector:

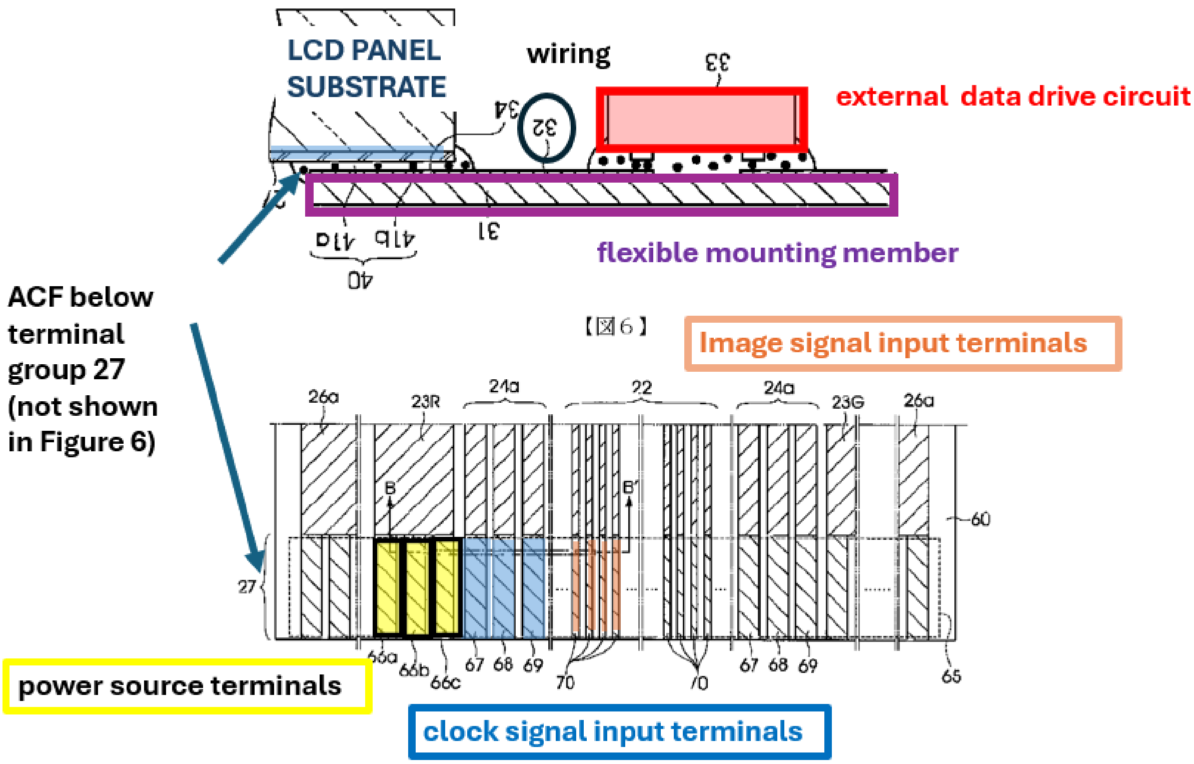


Ex. 1006, Figure 2; ¶¶ [0014]-[0015]. Sano's Figure 1(a) is a top view confirming that terminals 7b have a larger area than terminals 7a, such that the larger terminals overlap their wiring through the anisotropic connector by a larger area, which independently motivates [10j]. Flasck, ¶¶198, §§IX, X, XI.

Nakanishi is additional evidence that this concept was in the general knowledge of a POSITA. Like the '146 patent and Minami, Nakanishi discloses wider clock input terminals and power source terminals near the outer side of a substrate, with narrower image signal input terminals near the center:

【図1】





Ex. 1010, Figures 1, 2, 6. Nakanishi's clock signal input terminals (Figure 6 at 67, 68, 69) and their wiring (24a) have equal width, while its narrower image signal input terminals (70) and their wiring (22) have the same width. ¶[0053]; (Note: in Figure 6 "the anisotropic conductive film 40 and the intermediate substrate 30 are omitted from the drawing." ¶[0052]). Nakanishi shows that [10j] was within the level of ordinary skill, and would have been obvious. Flasck, ¶¶196-197.

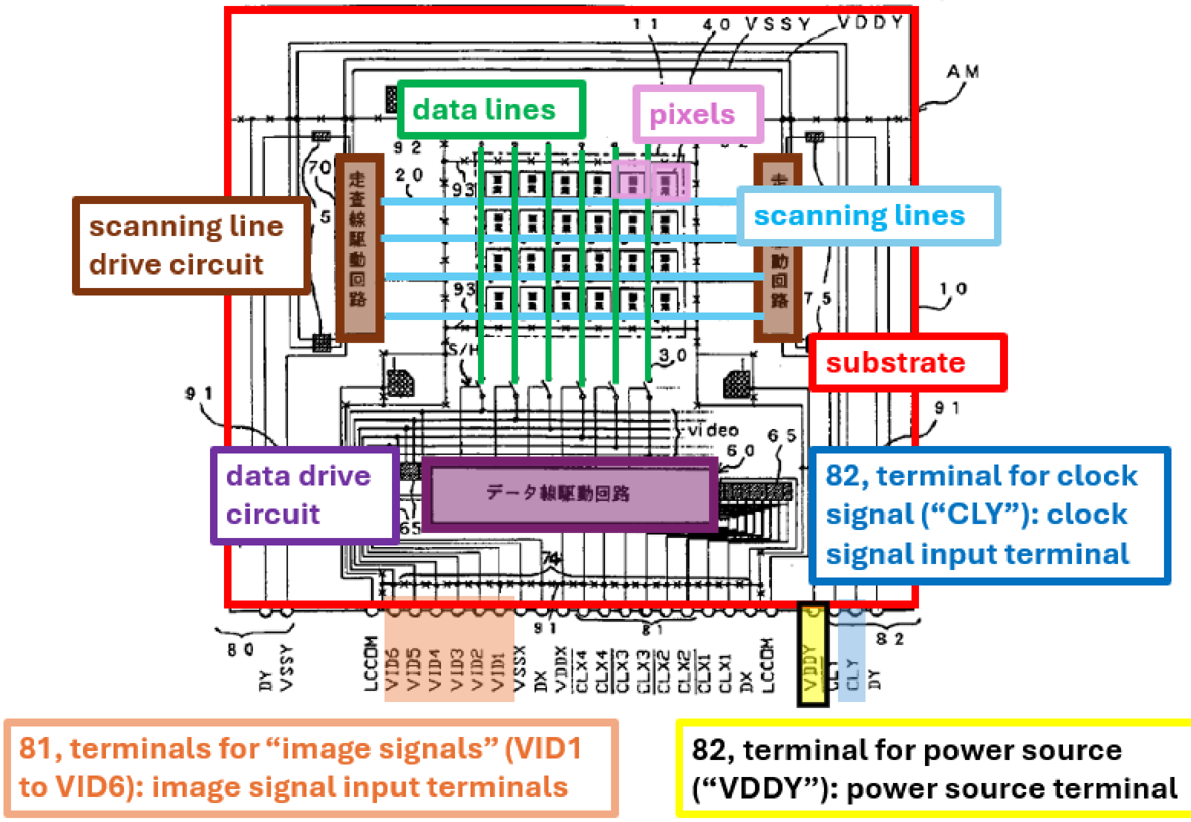
In sum, claim 10 is obvious over Kitawada in view of Kawaguchi, Matsumoto, and Minami or Sano.

2. Claim 11

A larger area terminal ***inherently*** has a smaller input resistance, a well-known fact taught by **Sano** (and confirmed by Kato). Flasck, ¶199, §§IX, XI.

3. Claim 12

Kitawada discloses claim 12:



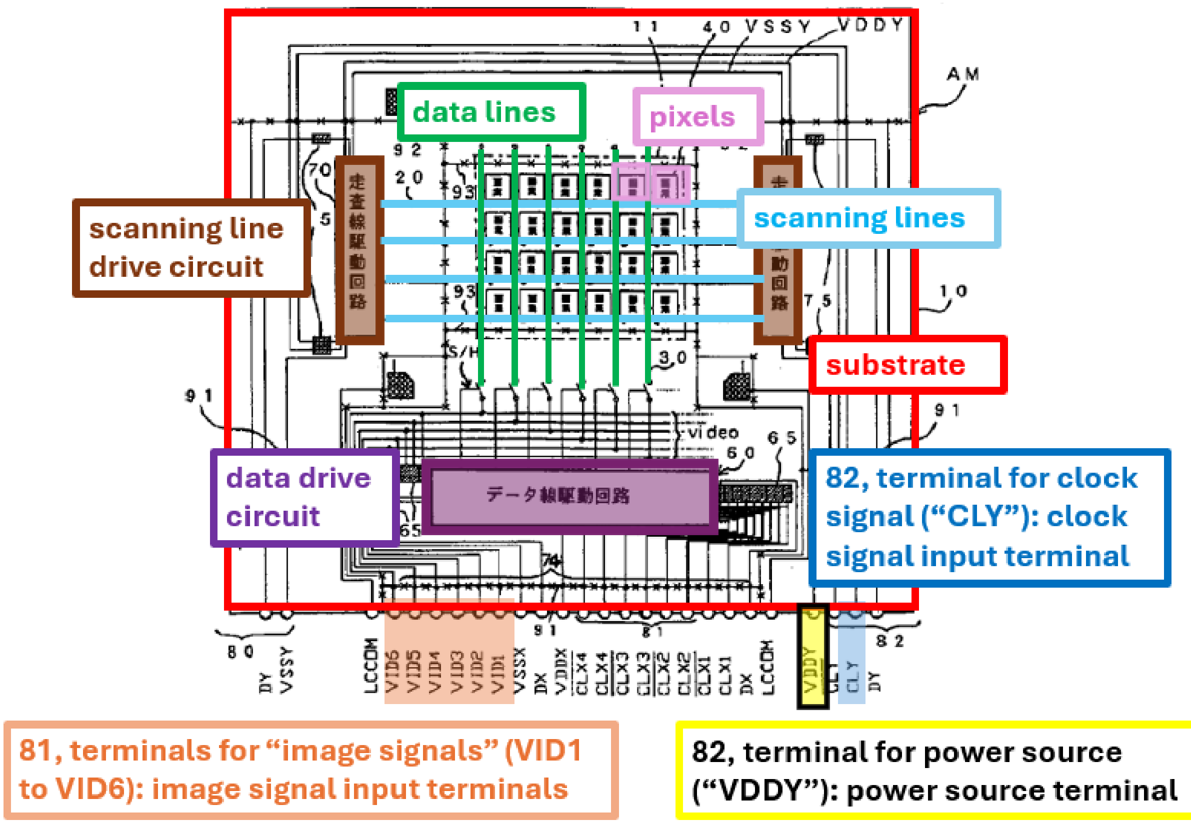
Ex. 1004, Figure 2; Figure 1; ¶[0020]; Flasck, §§IX, X, XI.

4. Claim 13

As discussed in [10h] it would have been obvious to modify Kitawada by using an external data drive that is formed on a mounting member separate from the first substrate. Again, **Kawaguchi** (and Nakanishi and many others) disclose an external data drive connected to the panel's image signal input terminals using a flexible mounting member bonded with ACF. Kawaguchi, Ex. 1005, ¶[0055]; Nakanishi, Ex. 1010, Figures 1-2. This admittedly was "known." Ex. 1001, 1:57-62. Flasck, ¶201, §§IX, X, XI.

5. Claims 14, 15

Kitawada discloses claims 14-15:



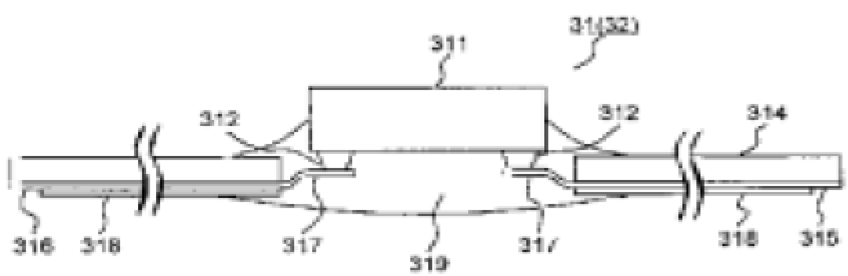
Ex. 1004, Figure 2; Figure 1; ¶[0020]; Flasck, §§IX, X, XI.

6. Claim 16

As discussed in [10h] and claim 13, it would have been obvious to modify Kitawada by using an external data drive formed on a mounting member separate from the first substrate. Again, **<u>Kawaguchi</u>** (and Nakanishi, among others) disclose such an external driver connected to the image signal input terminals using a flexible mounting member bonded with ACF. Kawaguchi, Ex. 1005, ¶[0055]. This was a "known" technique. Ex. 1001, 1:57-62.

Kawaguchi discloses a flexible substrate ("base substrate 314") and an external substrate ("mold 319") that are different than the LCD panel's first substrate:

Figure 7



Ex. 1005, Figure 7; ¶[0051].

Using ACF in this manner was conventional; the patent admits that LCD displays like those claimed were "known" (Ex. 1001, 1:17-62) and that "means for supplying the power source, etc. to the electro-optical panel, techniques which connect an input terminal formed on the electro-optical panel and a flexible substrate as a connection cable through an anisotropic conductive film are known." *Id*. at 1:51-62. These admissions underscore that it would have been obvious to connect

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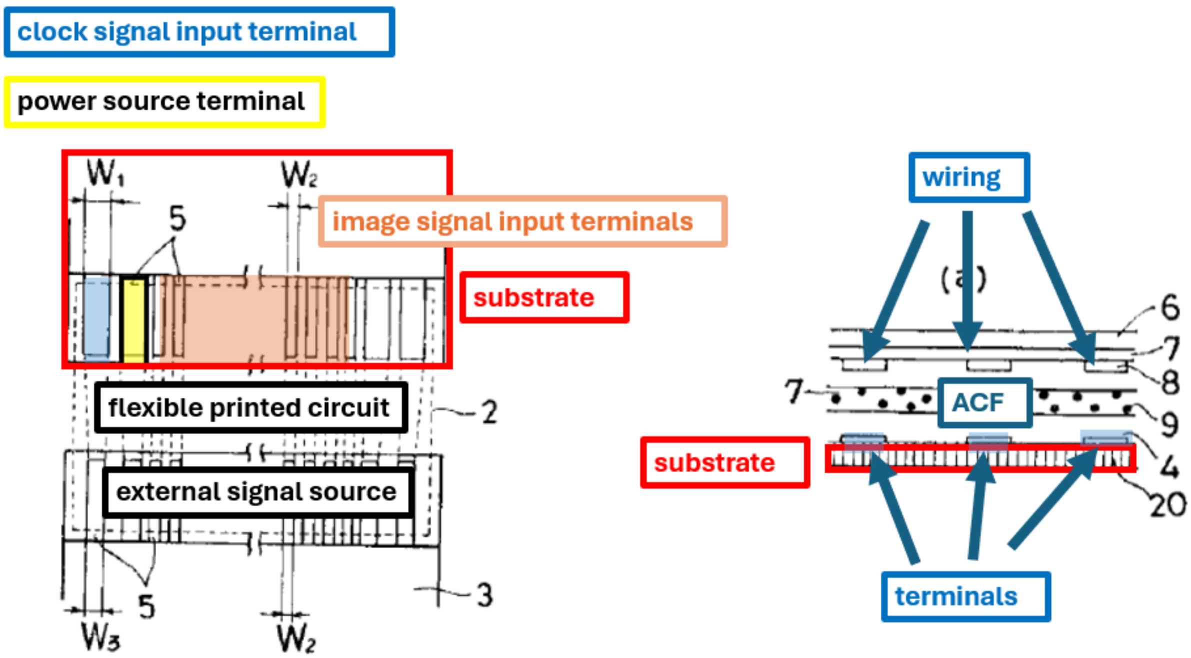
Kitawada's clock-signal input terminals to a "flexible wiring substrate," (Ex. 1004, ¶[0029]) through ACF. *Shockwave*, 142 F.4th at 1378-79; Flasck, §§IX, X, XI.

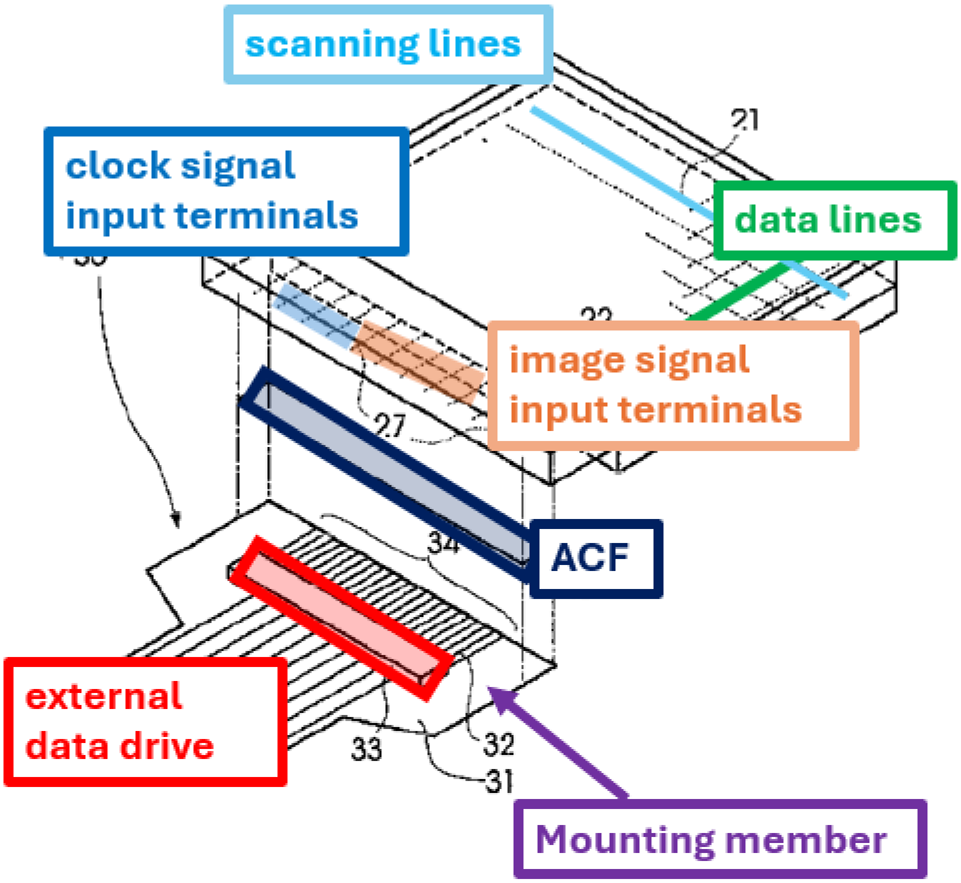
Similarly, Minami teaches using ACF to connect input terminals to a flexible printed circuit through ACF:



Ex. 1007, Figures 3 and 2a; *see* page 14 (describing Figure 2); Flasck, ¶206.

Confirming that this was within POSITA's general knowledge, Nakanishi discloses a flexible substrate ("flexible base substrate 31") and an external substrate ("intermediate substrate 30") that are different than the LCD panel's first substrate:

【図1】



Ex. 1010, Figure 1; ¶[0018] ("The intermediate substrate 30 has wiring 32 formed on a flexible base substrate 31 and has semiconductor chips 33 mounted at predetermined positions on the intermediate substrate 30. External connection terminals 34 are formed at one end of wiring 32 for electrical connection to wiring such as scanning lines 21 and signal lines 22 formed on display substrate 20.").

7. Claim 17

As shown in [10j] it would have been obvious to make Kitawada's clock signal terminal overlap a "first wiring" and its image signal input terminals overlap a "second wiring". Under plain meaning, a "wiring" comprises "at least one wire," and Minami, Sano, and Nakanishi teach wires. Flasck, ¶207, §§IX, X, XI.

8. Claim 18

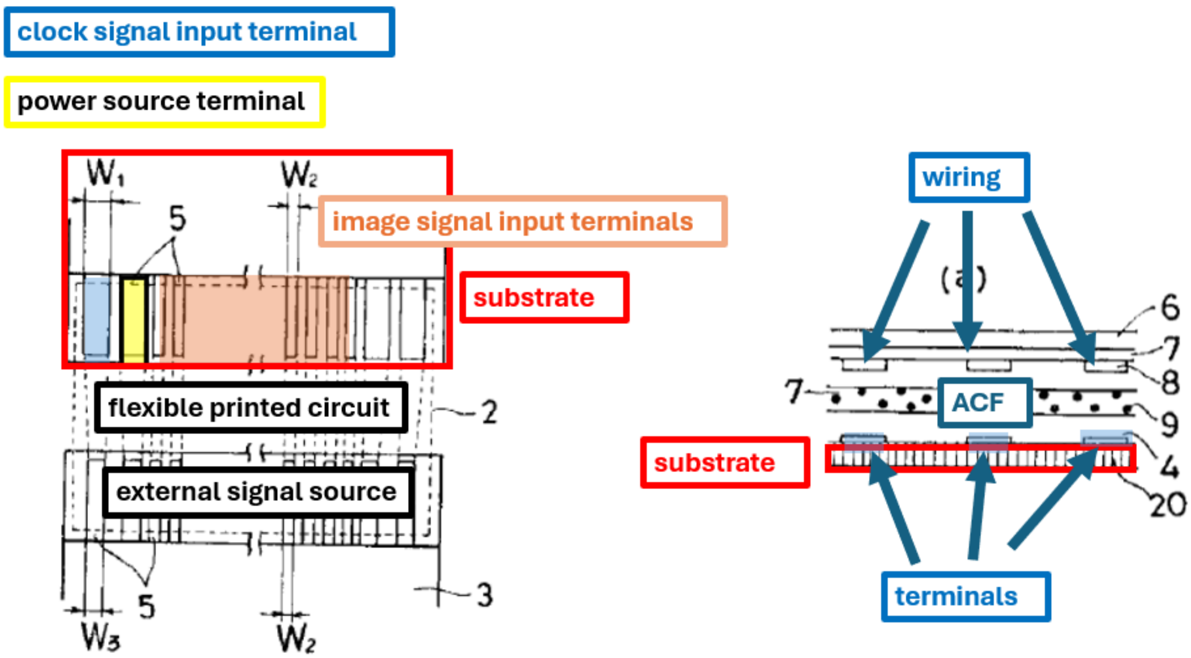
As shown above, it would have been obvious to modify Kitawada such that the contact area (*e.g.*, through ACF) between its clock signal input terminal and first wiring is greater than the contact area (*e.g.*, through ACF) between its image signal input terminals and the second wiring, as motivated and taught by Minami's Figures 1-3 and Sano's Figures 1-3 (and Nakanishi's Figures 1, 2 and 6 confirm that this technology was within POSITA's general knowledge). Flasck, ¶208, §X.

9. Claim 19

Claim 19 is obvious for the same reasons as claim 16. **Kawaguchi's** mounting member is connected to terminals on the panel's substrate through ACF. Ex. 1005, Figure 2 (showing terminal groups 21 and 22); ¶[0042] ("at the lower edge of the substrate 11, an input terminal group 21 for the first panel 10A is provided."); ¶[0055] ("The connection between the output terminal … and the input terminal group 21 … is made using an anisotropic conductive film (ACF)[.]").

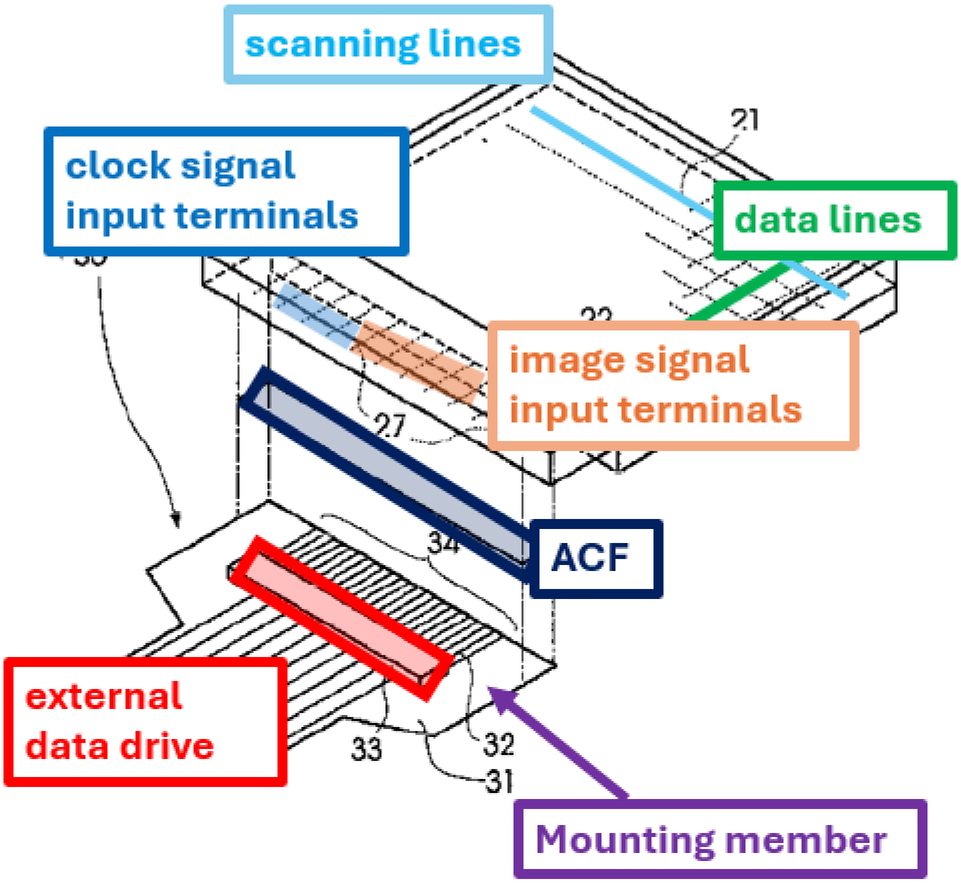
Using ACF like this was conventional. Flasck, ¶¶209-212. The '146 patent admits that displays like those claimed were "known" (Ex. 1001, 1:17-62) and that "means for supplying the power source, etc. to the electro-optical panel, techniques which connect an input terminal formed on the electro-optical panel and a flexible substrate as a connection cable through an anisotropic conductive film are known." *Id*. at 1:51-62. *Shockwave*, 142 F.4th at 1378-79; Flasck, §§IX, X, XI.

Similarly, **Minami** teaches using ACF to connect input terminals to a flexible printed circuit through ACF:



Ex. 1007, Figures 3 and 2a. Confirming this was within POSITA's knowledge, Nakanishi's mounting member is connected to terminals on Nakanishi's LCD panel's substrate through ACF:

【図１】



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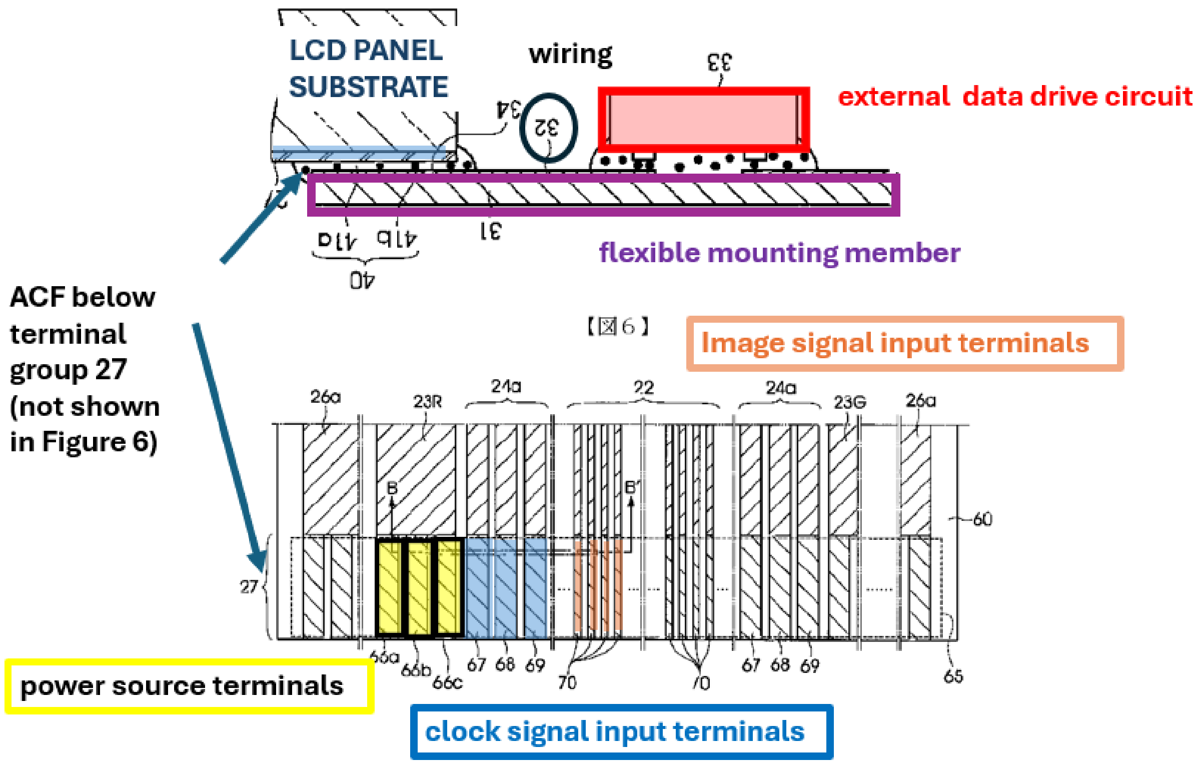

Ex. 1010, Figures 1, 2, 6; ¶¶[0019]-[0022].

10. Claim 20

Kitawada's terminal group 82 of the first substrate that comprises the clock signal input terminal and the image signal input terminals:

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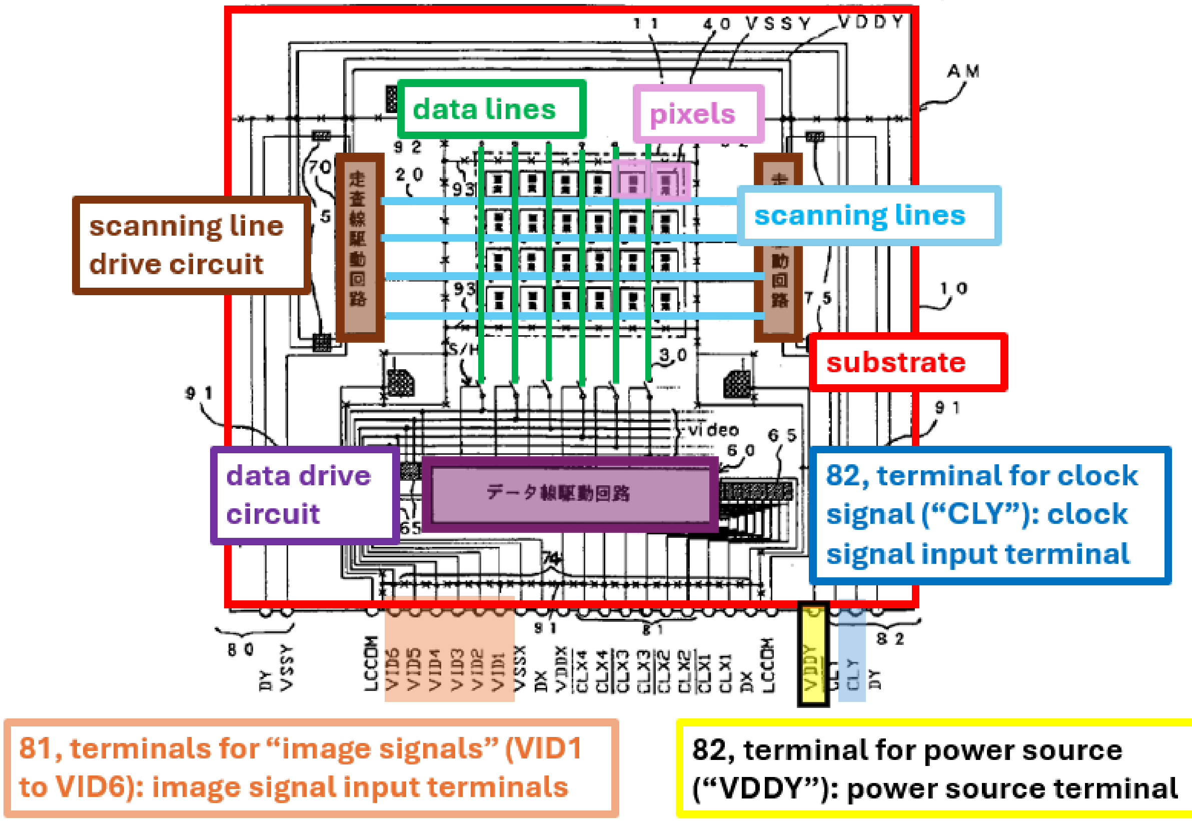


Ex. 1004, Figure 2; ¶[0020]. As discussed above with respect to [10e], [10f], [10h], and claims 16 and 19, it would have been obvious to connect a mounting member to Kitawada's terminal group using ACF, which would form an electrical and a mechanical connection. Flasck, ¶213, §§IX, X, XI.

11. Claim 21

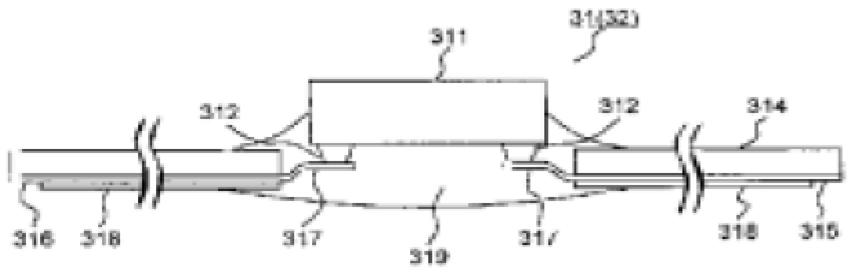
Claim 21 recites that "at least one of the image signal input terminals are connected between the substrate and the mounting member," which for purposes of this IPR, Petitioner interprets as "at least one of the image signal input terminals are connected <u>to wiring</u> between the substrate and the mounting member." As discussed above with respect to [10e], [10f], [10h], [10j] and claims 16, 19, and 22, it would have been obvious to connect a mounting member to Kitawada's terminal group using ACF. Thus, Kitawada's clock signal input terminal and at least one its image signal input terminals would be connected to wiring, through the ACF, between the LCD panel's substrate and the mounting member. Flasck, §§IX, X, XI.

12. Claim 22

This claim is obvious for the same reasons that [10e], [10f], [10h], [10j] and claims 16, 19, and 22 are. As discussed in [10h], it would have been obvious to modify Kitawada by using an external data drive circuit formed on a mounting member separate from the LCD panel's first substrate. Kawaguchi (and Nakanishi and others) disclose such an external data drive circuit connected to the panel's image signal input terminals using a flexible mounting member bonded with ACF. Nakanishi, Ex. 1010, Figures 1, 2; Kawaguchi, Ex. 1005, ¶[0055]. This was a "known" technique. Ex. 1001, 1:57-62.

Kawaguchi discloses a flexible substrate ("base substrate 314") and an external substrate ("mold 319") that are different than the LCD panel's first substrate:

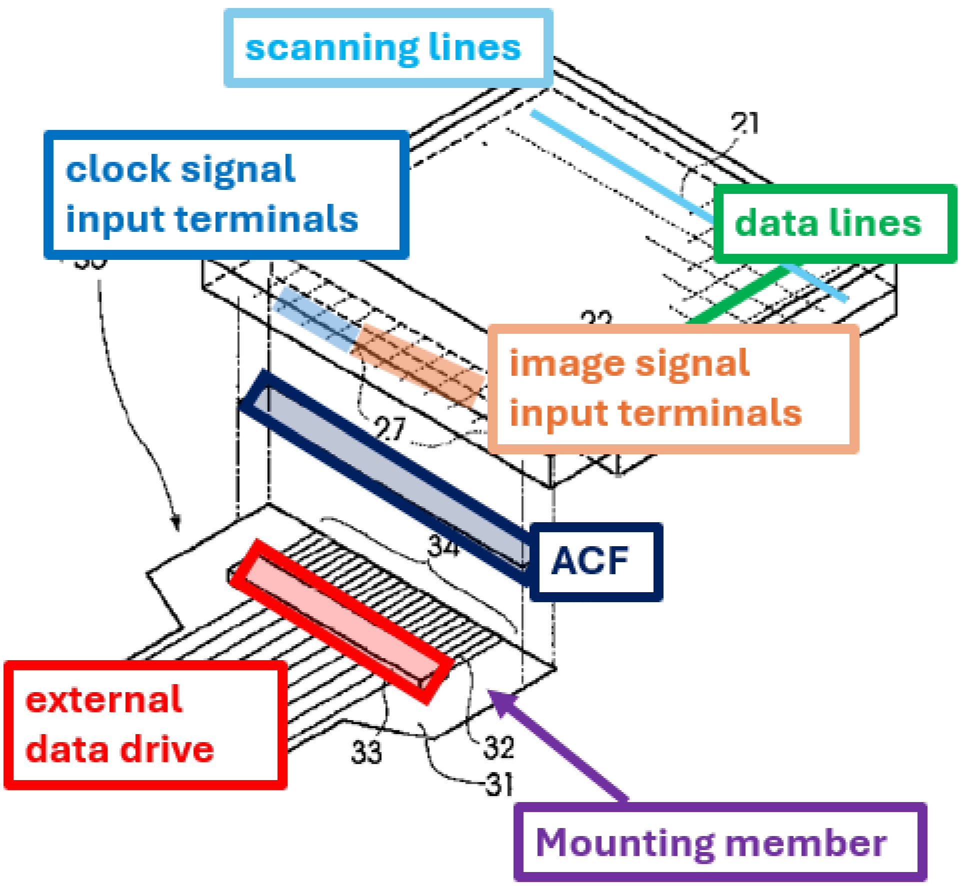
Figure 7

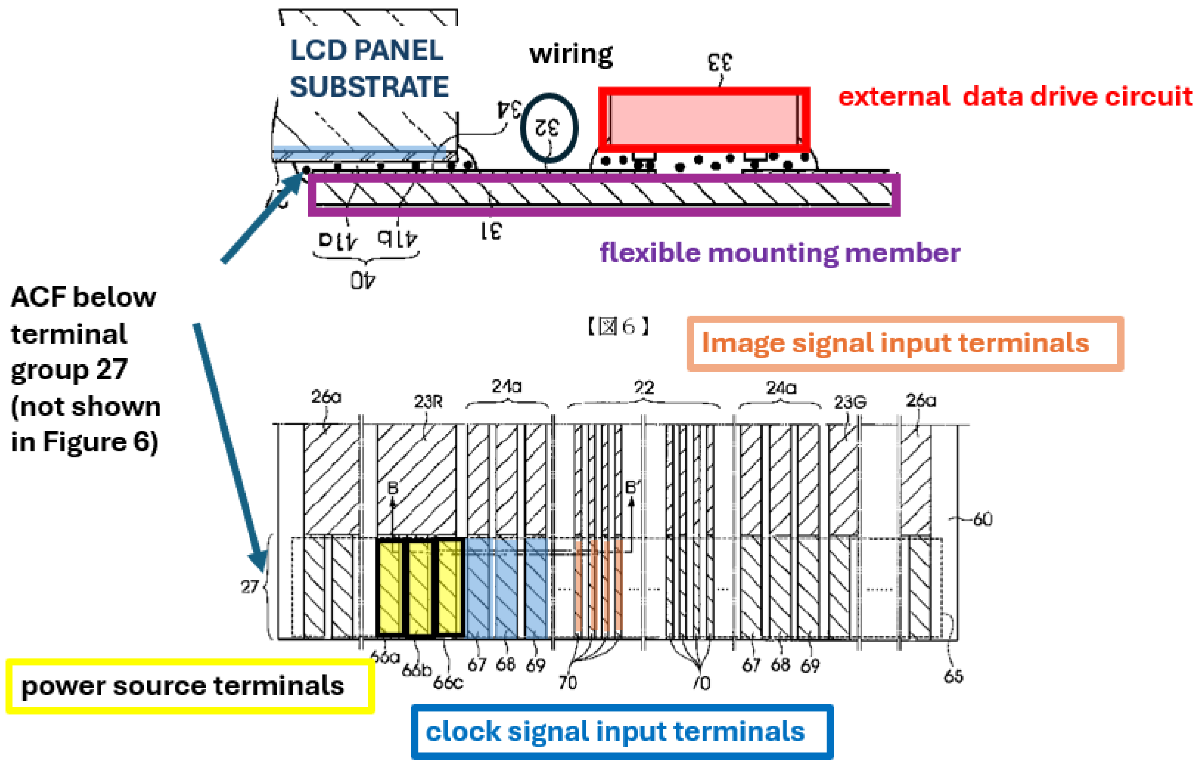


Ex. 1005, Figure 7; ¶[0051]. Kawaguchi's flexible mounting member is connected to Kawaguchi's LCD panel's substrate (through ACF) over the clock signal input terminal and over the image signal input terminals. Ex. 1005, Figure 2 (showing terminal groups 21 and 22, including 'x' terminals for image signals and 'y' terminals that could receive clock signals for the scanning line drive circuit); ¶[0042] ("[A]t the lower edge of the substrate 11, an input terminal group 21 for the first panel 10A is provided."); *id*. ("The input terminal group 21 includes: – Input terminals y1 to yk and input terminals yk+1 to yj, connected respectively to the scanning electrodes Y1 to Yk and Yk+1 to Yj of the first panel 10A, – Input terminals x1 to xi, connected respectively to the data electrodes X1 to Xi of the first panel 10A[.]"); ¶[0055] ("The connection between the output terminal group … and the input terminal group … is made using an anisotropic conductive film (ACF).").

Similarly, Nakanishi discloses a flexible substrate ("flexible base substrate 31") and an external substrate ("intermediate substrate 30") that are different than the LCD panel's first substrate. Ex. 1010, ¶[0018]. Nakanishi's flexible substrate is connected to Nakanishi's LCD panel's substrate (through ACF) over the clock signal input terminal and over the image signal input terminals:

【図1】





Ex. 1010, Figures 1, 2, 6; ¶¶[0019]-[0022].

As discussed above, Minami also discloses connecting terminals to wiring using ACF. Ex. 1007, Figure 2. Flasck, ¶¶215-218, §§IX, X, XI.

13. Claim 23

a. [23pre] – [23d]

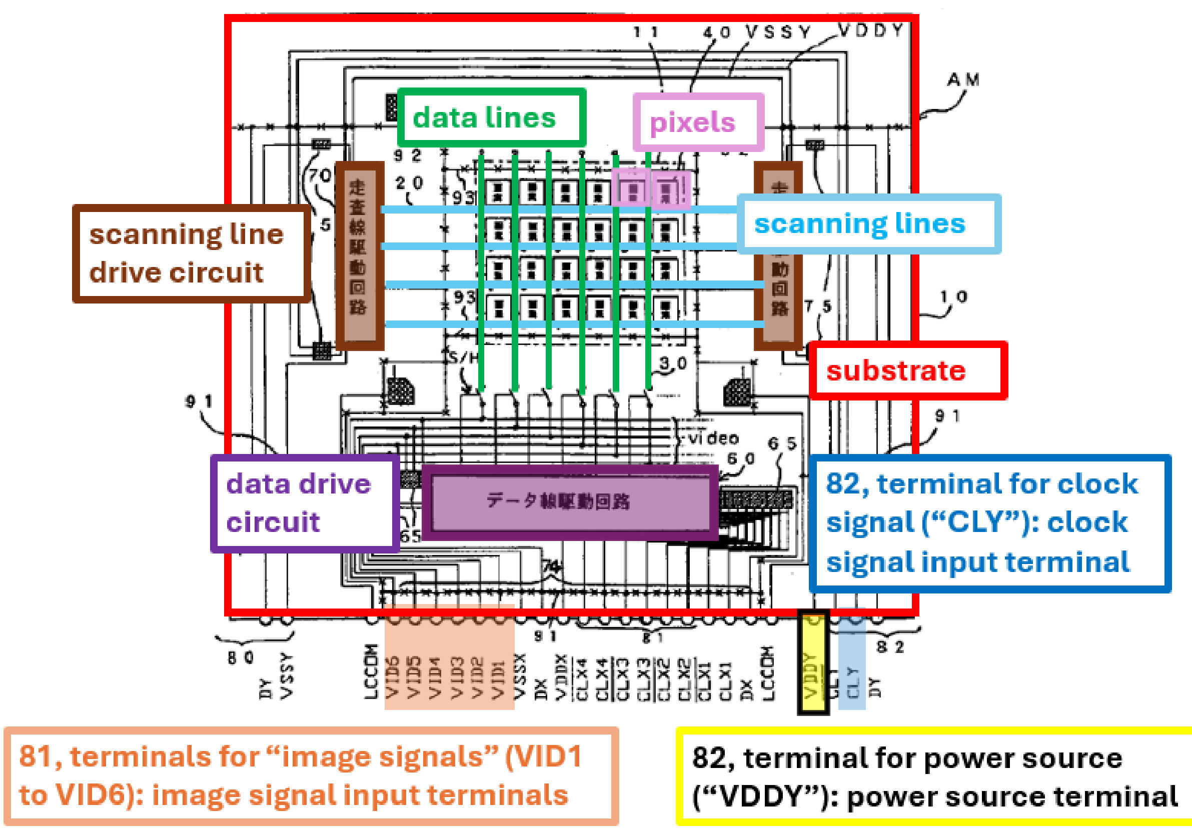
These elements are the same as claim 10's preamble through [10d], and are obvious for the same reasons. Additionally, this technology is AAPA. Flasck, §§IX, X, XI.

b. [23e], [23f]

[23e] and [23f] are the same as [10e] and [10f], respectively, without requiring connection to a mounting member through ACF, and they are obvious for the same reasons. Additionally, this technology is AAPA. Flasck, §§IX, X, XI.

c. [23g]

As shown above in [10h] and [10i], Kitawada discloses and renders obvious a scanning line drive circuit that outputs scanning signals to the scanning lines, image signals supplied from the data lines supplied to the pixels as selected by the scanning signals:



Ex. 1004, Figure 2; *see* ¶¶[0017]-[0020]; Flasck ¶¶221-222, §§IX, X, XI. Additionally, this technology is AAPA.

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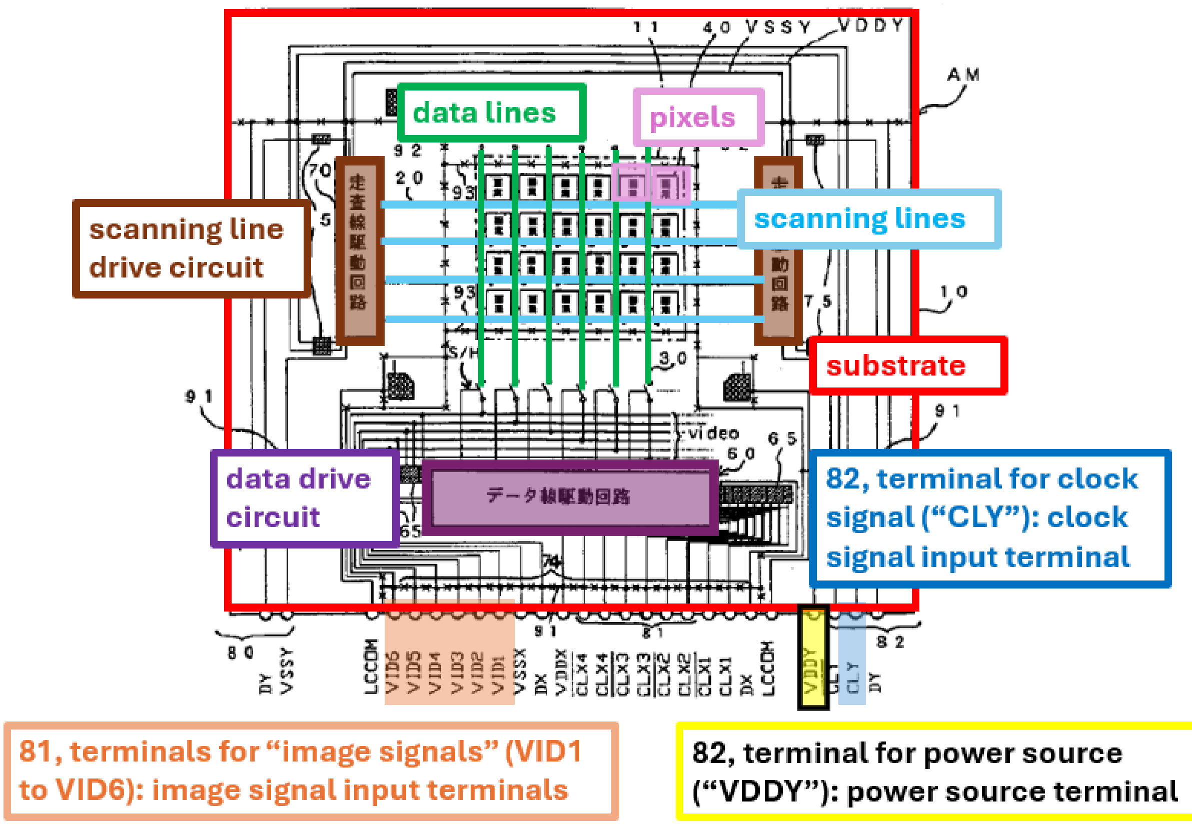
d. [23h]

As shown in [10a]-[10g], Kitawada's data lines, scanning lines, pixels, clock signal terminal, and image signal terminal are on the substrate.



Ex. 1004. Figure 2; ¶[0020]; Flasck, §§IX, X, XI.

e. [23i]-[23k]

As shown above in [10e], [10f], [10h], and claims 16 and 19, it would have been obvious to modify Kitawada to use a mounting member distinct from and connected to the LCD panel's substrate, with the mounting member comprising a first wiring (supplying clock signals) connected to the clock signal input terminal (*e.g.*, through ACF) and a second wiring (supplying image signals) connected to the image signal input terminal (*e.g.*, through ACF). Additionally, this technology is AAPA. Flasck, §§IX, X, XI

f. [23l]

This element is the same as [10 j], but does not require that the overlap be "through said anisotropic film," and is obvious. Flasck, §§IX, X, XI.

B. Ground 2: Claims 1-9 are Obvious over Kitawada in view of Kawaguchi, Matsumoto, and Minami or Sano or Kato

1. Claim 1

a. [1pre] – [1c]

The preamble through [1c] are like [10pre], and [10b]-[10d], respectively, and are obvious. Flasck, §§IX, X, XI.

b. [1d], [1e]

[1d] and [1e] are the same as [10e] and [10f], respectively, but without requiring connection through ACF, and are obvious. Flasck, §§IX, X, XI.

c. [1f]

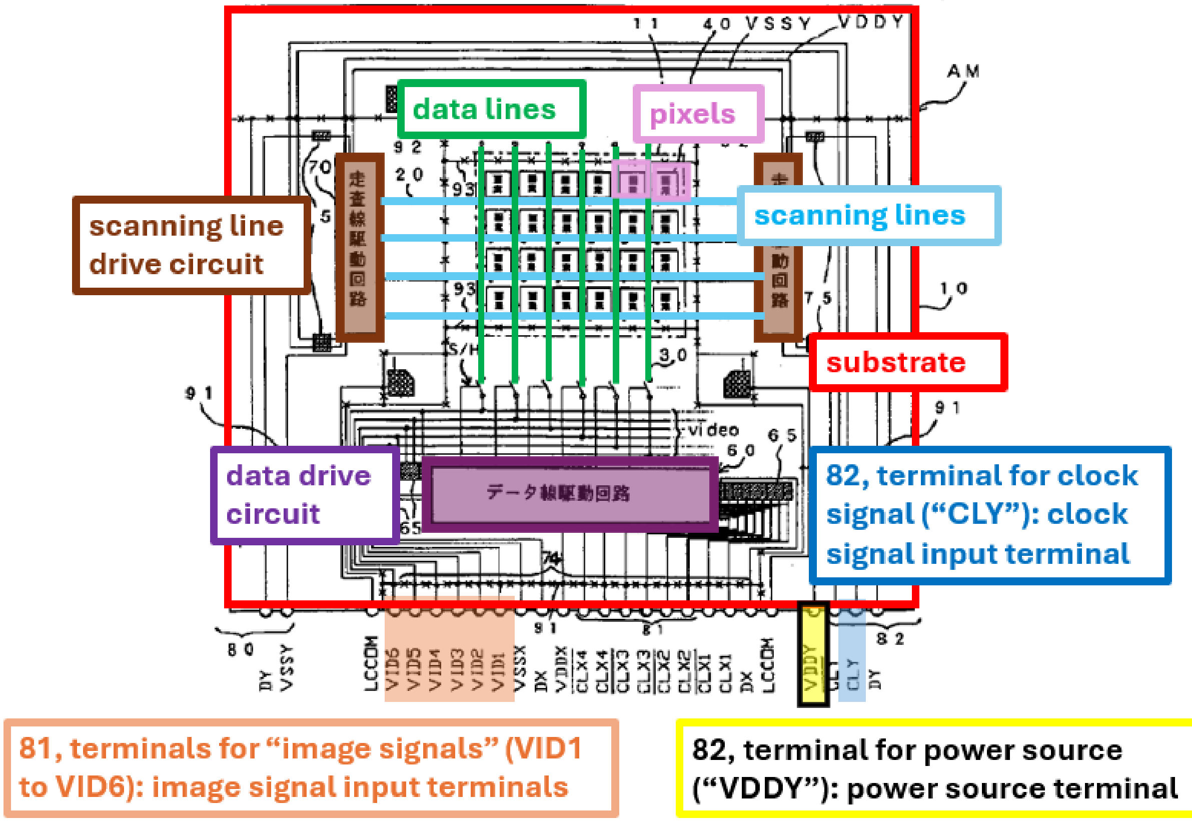
As shown in [10i] and [23g] in Ground 1, Kitawada discloses and renders obvious (alone and/or in view of Kawaguchi) a scanning-line drive circuit that is formed on the first substrate and sequentially transmits a transmission start pulse in synchronization with the clock signal. Kitawada's scanning-line drive outputs a scanning signal to each of the scanning lines. Ex. 1004, ¶¶[0017]-[0020]. Similarly, Kawaguchi's scanning-line drive outputs a scanning signal to each of the scanning lines. Ex. 1005, ¶¶[0032]-[0034]. And as shown in [10h], [10i], and [23g], Kitawada discloses and renders obvious image signals from the plurality of data lines are supplied to pixels selected by the scanning signals. Flasck, ¶228, §§IX, X, XI. Additionally, this technology is AAPA.

d. [1g]

As shown in [10h] and [10i] in Ground 1 and [1f] above, Kitawada discloses and renders obvious image signals being supplied from a data drive circuit and a scanning-line drive circuit that sequentially transmits a transmission start pulse in synchronization with the clock signal. As Mr. Flasck explains, a POSITA would understand that Kitawada's data drive circuit "controls a grayscale of the pixels based on the scanning line clock signal and the image signal" as claimed. Flasck, ¶229, §§VI.D.1, IX.B, X, XI; *also* Ex. 1018, ¶[0004] ("A conventional image display device … in which the direction of liquid crystal molecules is controlled by adjusting the applied voltage to achieve grayscale."). Additionally, this technology is AAPA.

e. [1h]

Kitawada discloses a power source input terminal (82, terminal for power source "VDDY") supplied with a power source ("VDDY"):



Ex. 1004, Figure 2; ¶[0020]. Kitawada does not expressly disclose the area of the power input terminal, but it would have been obvious that its area is not less than that of the clock signal input terminal. As discussed previously, **Minami** and **Kato** ***independently*** teach and motivate use of a power source terminal whose area “is not smaller than” that of the clock signal input terminal. *See* Flasck, §X.

Kitawada’s power source terminals are near the outer side of the substrate and should thus have a larger area according to **Minami** (and Nakanishi and Mismatch Analysis Report). Because Kitawada’s power source terminals are adjacent to its clock signal input terminals, it would be obvious that the former terminals should not be smaller than the latter. Flasck, §§X, XI, ¶231.

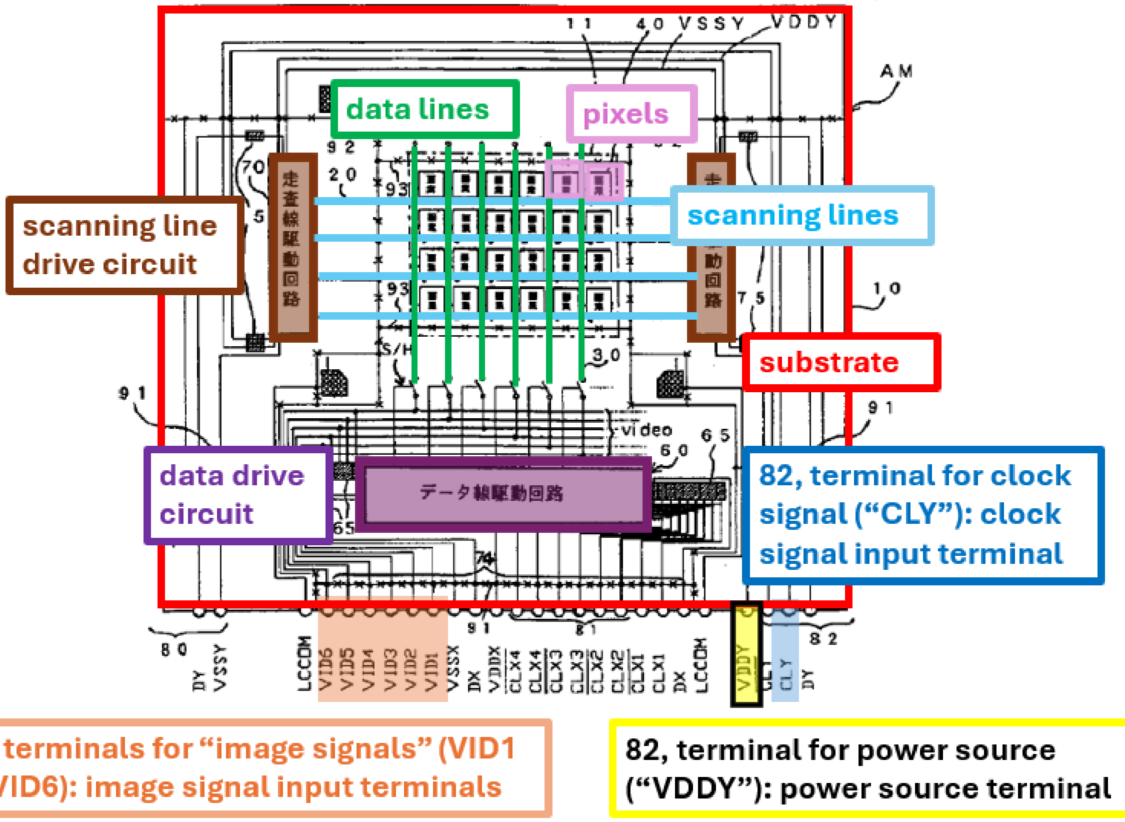
Further, power terminals should have a larger area to lower their resistance to conduct "larger currents" per **Kato**. A POSITA knew that a power source terminal's currents are at least as large as a clock signal input terminal's currents, so it would have been obvious that the former terminals have "not smaller" areas. Flasck, §§X, XI, ¶232.

f. [1i]

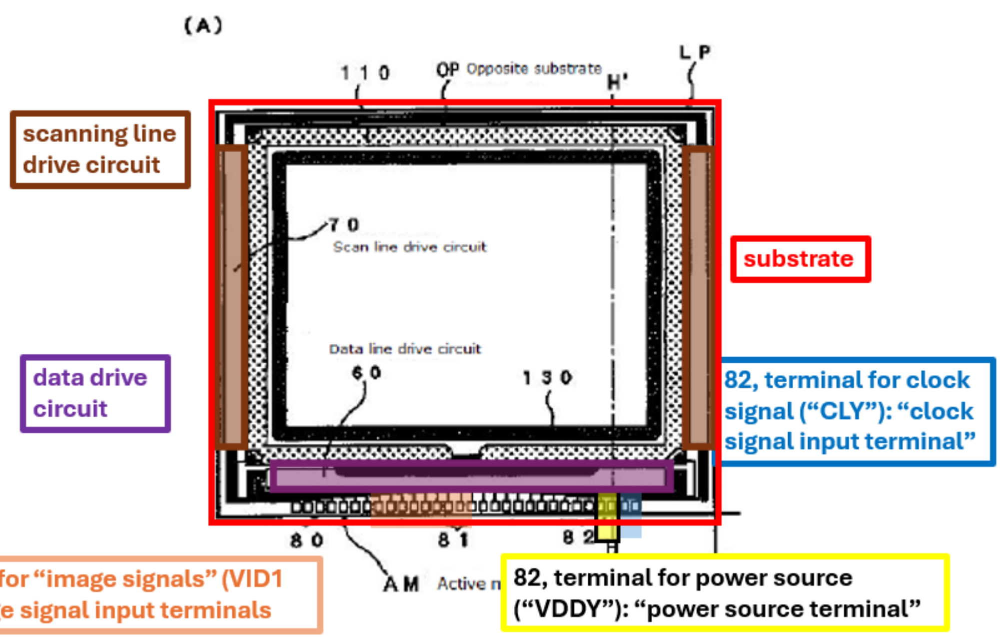
As shown in [10j] in Ground 1, it would be obvious to modify Kitawada so that its clock signal input terminal has a larger area than its image signal input terminal, according to the teachings of **Minami** or **Sanu**. Flasck, §§X, XI.

g. [1j], [1k]

Kitawada discloses a plurality of power source terminals (82, terminal for "VDDY"; 81, terminals for "VDDX" and "VSSX"), clock signal input terminals (82, terminals for "CLY" and inverted CLY), and image signal input terminals (81, terminals for "VID1"-"VID6") formed in line on the LCD panel's substrate:



[FIG. 1]

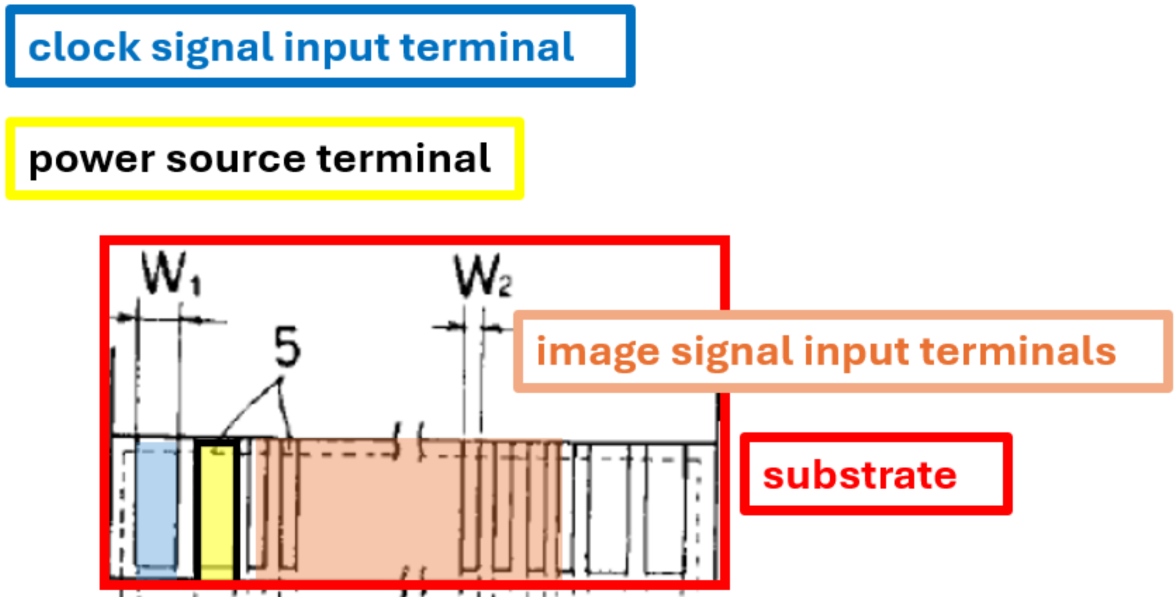


Ex. 1004, Figure 2 and Figure 1(A); ¶[0020]; Ground 1, [10g]; Flasck, §§X, XI.

h. [1l]

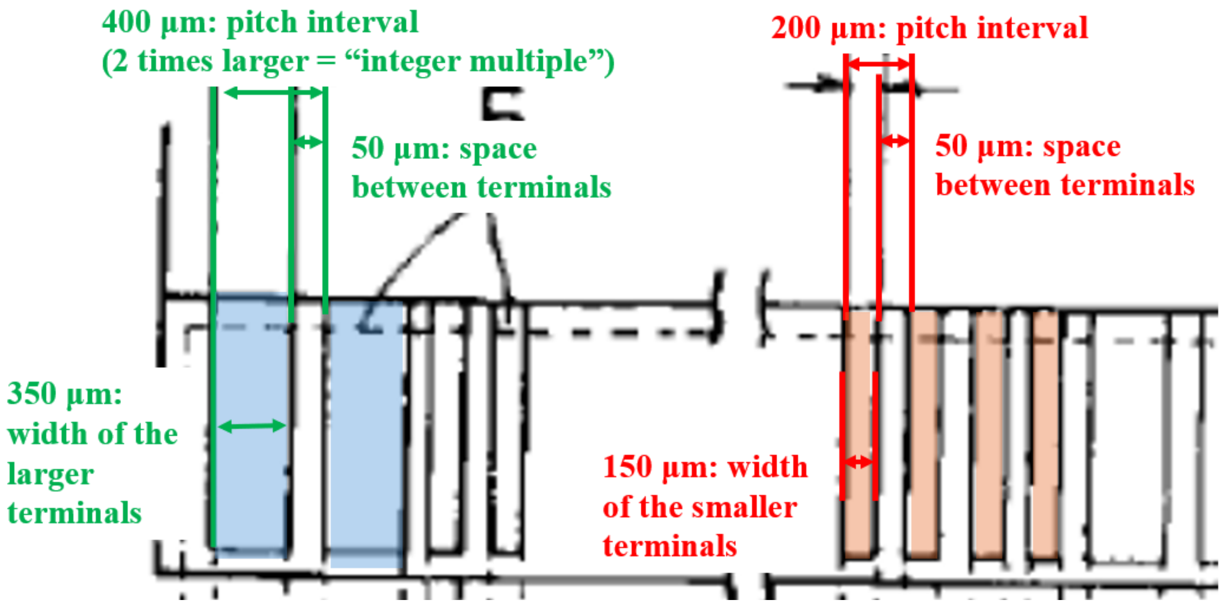
It would have been obvious to increase the area of Kitawada's clock signal terminals relative to the area of its image signal input terminals. *See* Ground 1 [10j]. It follows that it would have been an obvious to use a pitch interval for adjacent clock signal input terminals that is a multiple of the pitch interval of adjacent (smaller) image signal input terminals—whether that multiple be an integer or otherwise. In fact, the '146 patent does not disclose any reason for using an integer multiple. Ex. 1001, 9:9-11.

Further, **Minami** discloses that terminals located near the outside of the substrate (where Kitawada's clock signal input terminals are located) should have a larger area than the terminals closer to the center of the substrate (where Kitawada's image signal terminals are lcoated) when a display requires "high-density terminal pitch connections . . . between the drive circuit board and the display unit." Ex. 1007, at 13. "When the pitch is approximately 100 to 200 µm, the bonding area between the anisotropic conductive film and the LCD panel electrode terminals is small, resulting in a decrease in bonding strength and bond delamination due to external pressure after connection." *Id.* In Figure 3, the "width of the connection pattern is 150 µm for the pattern width W_2 at the center, and the pattern width W_1 near both ends on the LCD panel 1 side is 2 to 5 times the width of the connection pattern at the center, for example 500 µm." *Id.* at 2:



Ex. 1007, Figure 3.

Since the pitch interval can be "200 µm" and the "width of the connection pattern is 150 µm for the pattern width W_2 at the center," the space between the narrow terminals is 50 µm (*i.e.*, 200 µm – 150 µm = 50 µm). Therefore, if the wider terminals near the ends of the panel are 350 µm wide (within the range of "2 to 5 times the width of the connection pattern at the center"), then the pitch interval of the adjacent wider terminals is 400 µm:



Ex. 1007, Figure 3. Thus, the pitch interval of the wider terminals (400 µm) would be twice the pitch interval of the narrower terminals (200 µm), which is an "integer multiple" as claimed. Flasck, ¶¶235-237. *Galderma Lab'ys, L.P. v. Tolmar, Inc.*, 737 F.3d 731, 738 (Fed. Cir. 2013) (claim presumptively obvious "where there is a range disclosed in the prior art, and the claimed invention falls within that range[.]").

In the field of semiconductor chip pads, "varying pad pitch between pads" was known. Ex. 1023, 2:37-45. Similar to terminals used in an LCD display, a pad array "is an external interface of a semiconductor chip for coupling signals to the semiconductor chip. *Id.*, 1:8-10. This technology is analogous to the claimed technology; the active matrix display industry grew out of the semiconductor industry. And almost all design and manufacturing processes for AMLCD were ported over from the semiconductor industry. Further, active matrix design rules (including pad width and spacing rules) were conceptually ported over from the semiconductor industry. Among other benefits of varying pad pitch, it could "shorten development time, minimize need for customization, reduce cost, allow current developments to be used with next generation process flows, and give customers a choice on using different package technologies." Ex. 1023, 2:25-34. The same benefits would apply to varying terminal pitch interval in an LCD display. Adjustable pad pitch was achieved using a reference "grid size" where "pad widths and pad spacings are integer multiples of the grid size." Ex. 1023, 6:22-33 and claim 1 (". . . defining an incremental pad pitch, wherein predetermined pads in the row of pads can be contacted at pad pitch equal to the minimum pad pitch plus an integer multiple of the incremental pad pitch . . ."). This would result in some pad pitch intervals being an integer multiple of other pad pitch intervals. The pitch interval of LCD terminals could easily be adjusted in the same way, and a POSITA would have been motivated to do so because this could make manufacturing easier while satisfying design rules and allowing for varying pitch intervals. Flasck, ¶238.

2. Claim 2

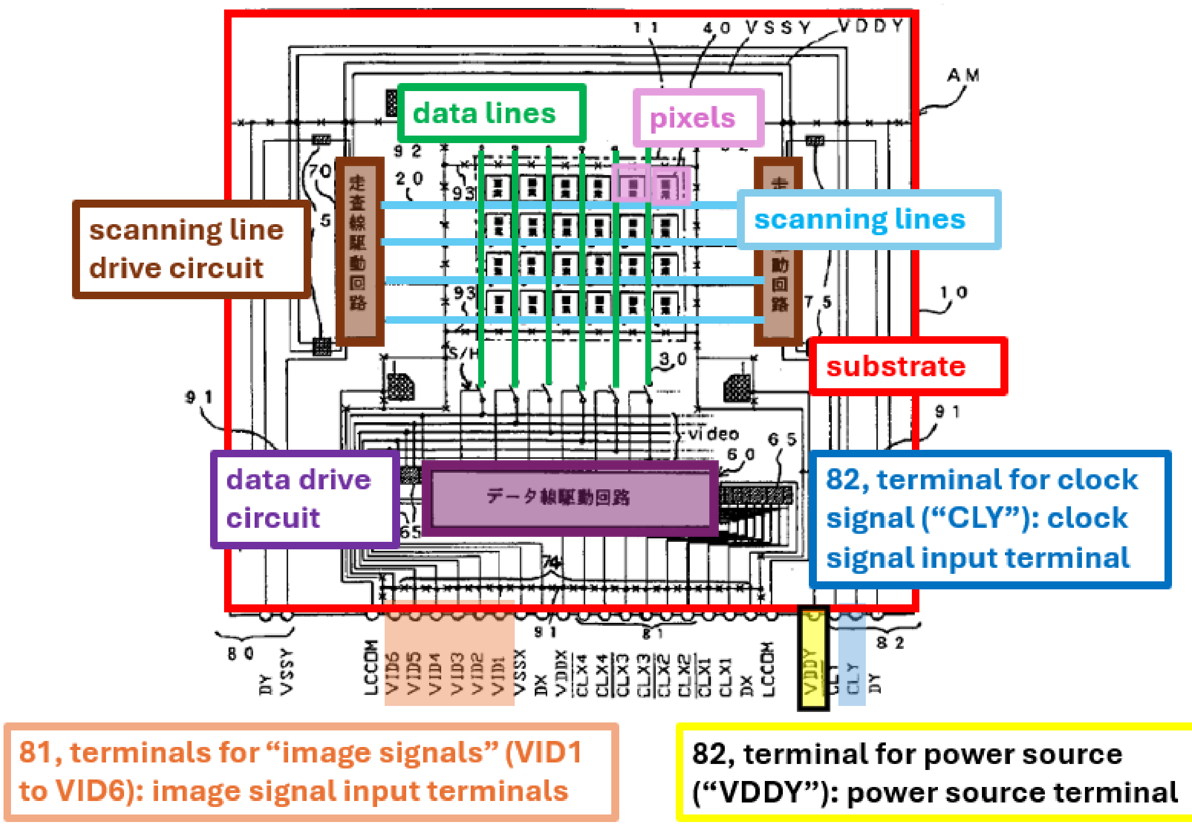
See Ground 1, claim 11. Flasck §§X, XI.

3. Claim 3

Kitawada discloses "start signal DY, clock signal CLY, and inverted clock signal CLY bar are supplied from outside via terminals to the scan line drive circuits 70, and the scan line drive circuits 70 are driven by these signals." Ex. 1004, ¶[0019]; ¶[0020] and Figure 2; [10i] in Ground 1; Flasck §§X, XI.

4. Claim 4

Kitawada discloses claim 4:



Ex. 1004, Figure 2; ¶[0020]; Ground 1, claim 12; Flasck §§X, XI.

5. Claim 5

Kitawada discloses and renders obvious a power source means because “the edge portion on the side with the data line drive circuit 60 includes constant power supplies VDDX, VSSX, VDDY, VSSY.” Ex. 1004, ¶[0020]. As a POSITA understands, it is obvious that there must be power source means to supply “constant power supplies VDDX, VSSX, VDDY, VSSY.” Moreover, the specification admits that "means for supplying the power source, etc., to the electro optical panel … are known." Ex. 1001, 1:51-62. Flasck, ¶¶242-243.

And Kitawada discloses and renders obvious signal generation means for supplying input signals. This inherently exists to supply "video signals VD1 to VD6." Ex. 1004, ¶[0019] ("The data line drive circuit 60 comprises an X-side shift register circuit, a sample hold circuit S/H equipped with TFTs that function as analog switches based on signals outputted from the X-side shift register circuit, and six video signal lines corresponding to each of the video signals VD1 to VD6 expanded to six phases. In this example, the data line drive circuit 60 is configured with the X-side shift register circuit in a four-phase configuration, and start signal DX, clock signals CLX1 to CLX4, and their inverted clock signals CLX1 bar to CLX4 bar are supplied to the X-side shift register circuit via terminals, and the data line drive circuit 60 is driven by these signals. Therefore, the sample hold circuit S/H causes each TFT to operate based on the signal outputted from the X-side shift register circuit, and enables video signals VD1 to VD6 supplied via the video signal line to be captured at a predetermined timing and supplied to the data lines 30 and each pixel 40. Meanwhile, start signal DY, clock signal CLY, and inverted clock signal CLY bar are supplied from outside via terminals to the scan line drive circuits 70, and the scan line drive circuits 70 are driven by these signals."); ¶[0020]. Alternatively, the voltage made available to (and stored on) each data line amounts to a grayscale analog signal; thus, the data line drive circuit (which "comprises an X-side shift register circuit, a sample hold circuit S/H equipped with TFTs that function as analog switches based on signals outputted from the X-side shift register circuit, and six video signal lines corresponding to each of the video signals VD1 to VD6," *id*., ¶ [0019]) is a signal generation means that is equivalent to the structure disclosed in the '146 patent and renders claim 5 obvious. Flasck ¶¶244-249, §XI.

6. Claim 6

As discussed in [10e], [10f], [10h], and claims 16 and 19-22 in Ground 1, it would have been obvious to modify Kitawada to utilize an external substrate containing an external data circuit for supplying image signals, with the external substrate comprising a flexible substrate connected to the LCD panel's plurality of input terminals through ACF. For similar reasons, it would have been obvious to use an external substrate including the "power source means" and "signal generation means" recited in claim 5, because there are a finite number of ways to include such means (*e.g*., implementing them on the LCD's panel's substrate or on an external substrate) and there were known technical benefits of using an external substrate for such components. As explained above in [10e], [10f], [10h], and claims 16 and 19-22 in Ground 1, it would have been obvious that such an external substrate would include a flexible substrate to connect to the LCD panel's substrate via connection

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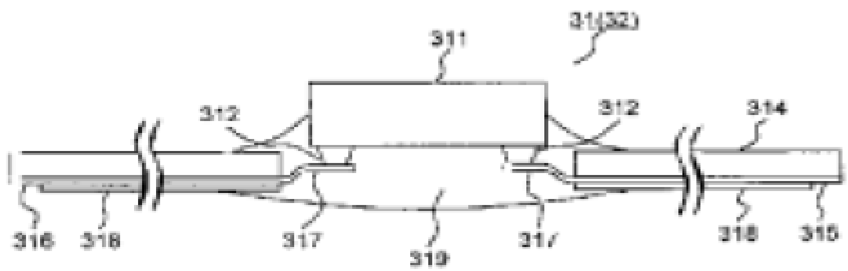
to Kitawada's power source terminals, clock signal input terminals, and image signal input terminals (Kitawada, Ex. 1004, Figure 2, ¶[0020]) through ACF.

And as discussed in Ground 1, Kawaguchi discloses a flexible substrate ("base substrate 314") and an external substrate ("mold 319") that are different than the LCD panel's first substrate:

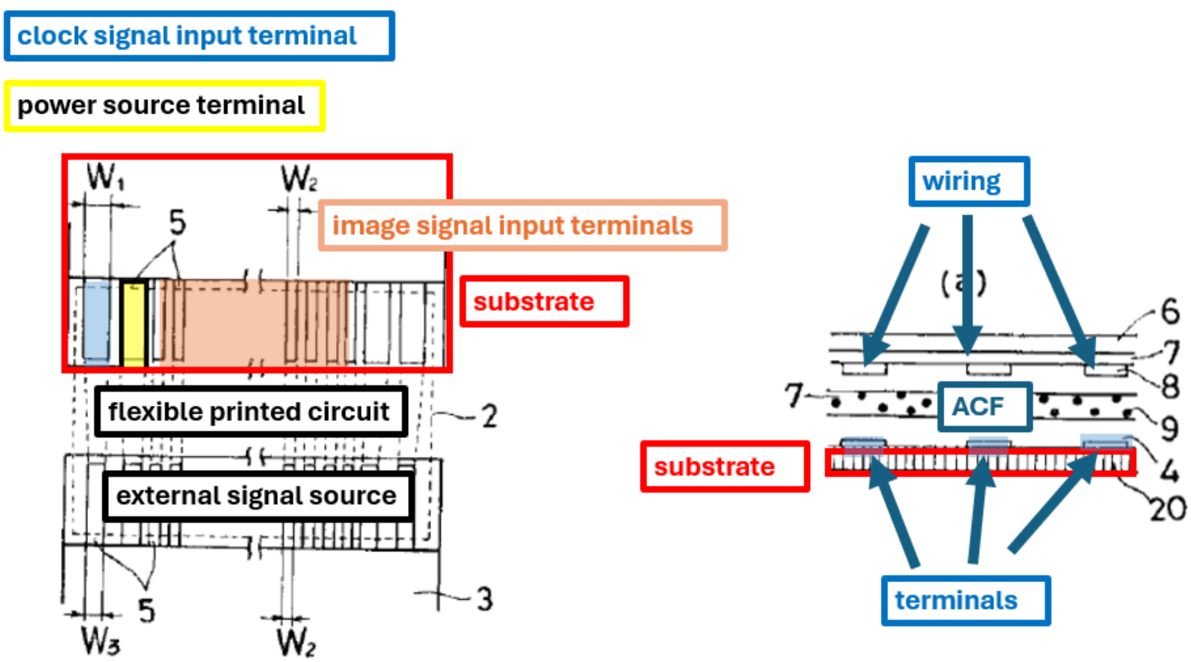
Figure 7



Ex. 1005, Figure 7; ¶[0051]. Kawaguchi's flexible mounting member is connected to Kawaguchi's LCD panel's substrate (through ACF) over the clock signal input terminal and image signal input terminals. Ex. 1005, Figure 2 (showing terminal groups 21 and 22, including 'x' terminals for image signals and 'y' terminals that could receive clock signals for the scanning line drive circuit); ¶¶[0042], [0055].

Using ACF in this manner was conventional, and the '146 patent admits that displays like those claimed were "known" (Ex. 1001, 1:17-62) and admits that "means for supplying the power source, etc. to the electro-optical panel, techniques which connect an input terminal formed on the electro-optical panel and a flexible substrate as a connection cable through an anisotropic conductive film are known." *Id*. at 1:51-62. These admissions underscore that it would have been obvious to connect Kitawada's clock-signal input terminals to a "flexible wiring substrate," (Ex. 1004, ¶[0029]) through ACF. Flasck §§X, XI.

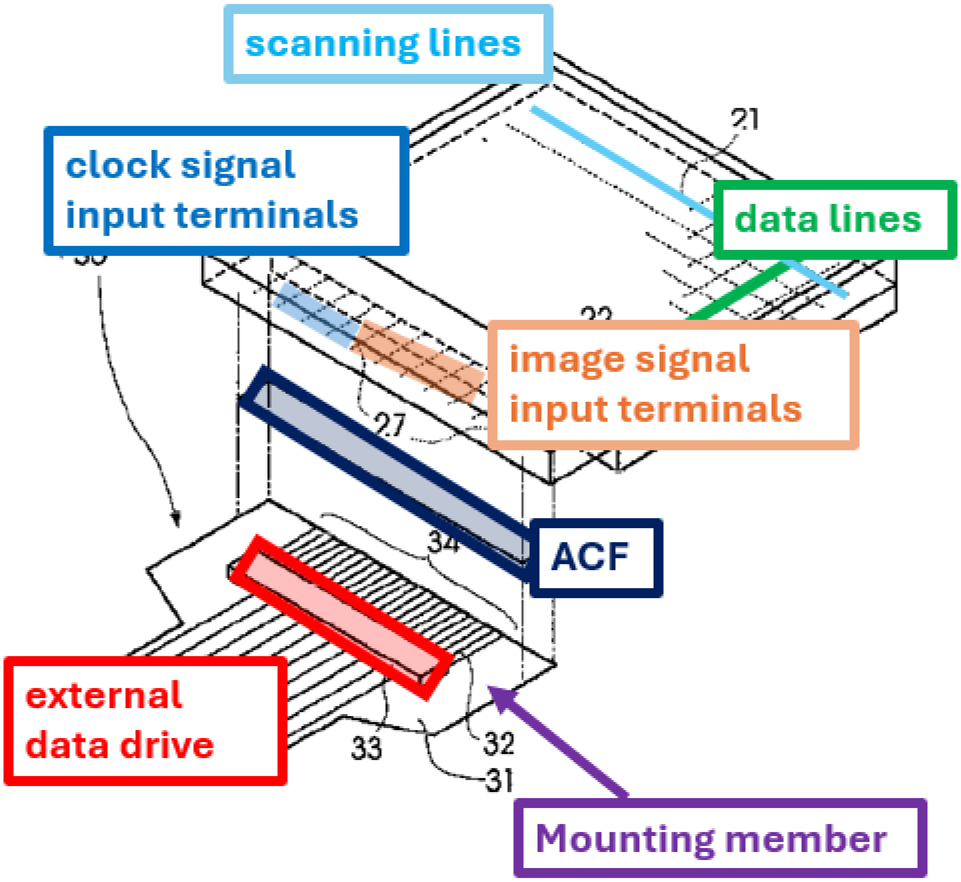
Similarly, Minami teaches using ACF to connect input terminals to a flexible printed circuit through ACF:

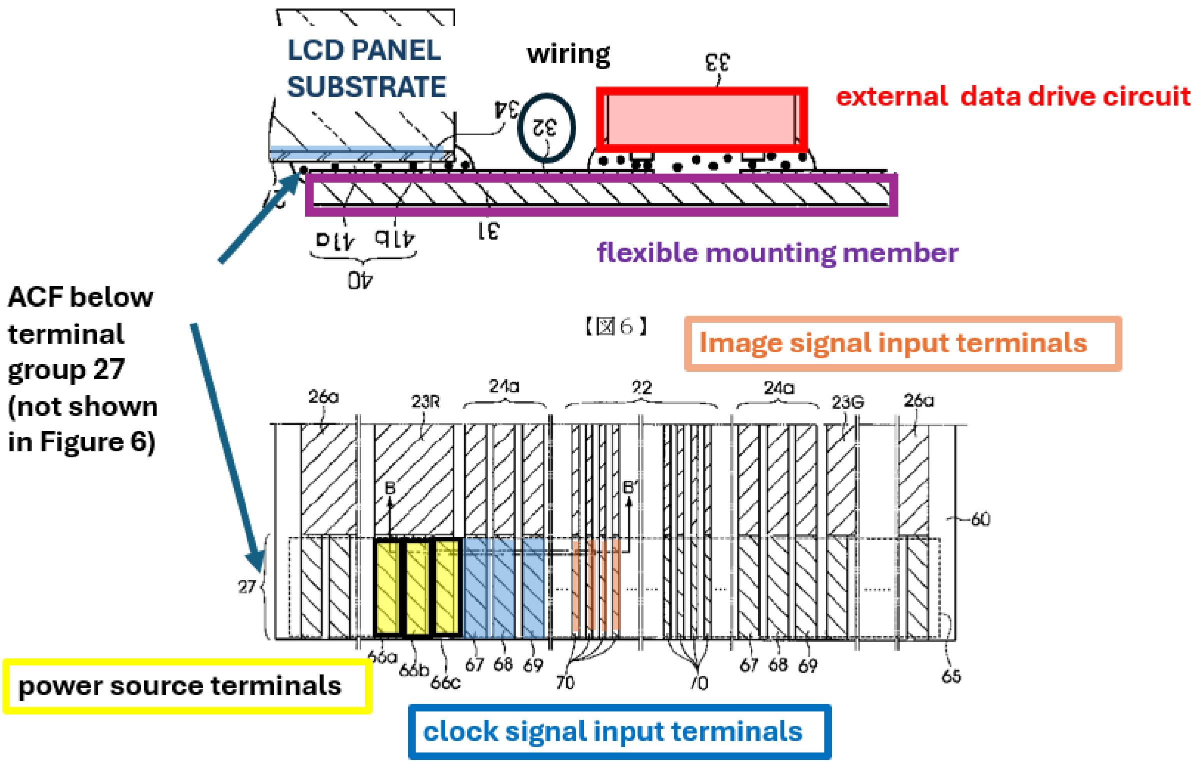


Ex. 1007, Figures 3 and 2a; Flasck, ¶¶250-254.

Showing that this was within POSITA's general knowledge, Nakanishi discloses a flexible substrate ("flexible base substrate 31") and an external substrate ("intermediate substrate 30") that are different than the LCD panel's first substrate. Ex. 1010, ¶[0018]. Nakanishi's flexible substrate is connected to Nakanishi's LCD panel's substrate (through ACF) over the clock signal input terminals, the image signal input terminals, and the power source terminals:

【図1】



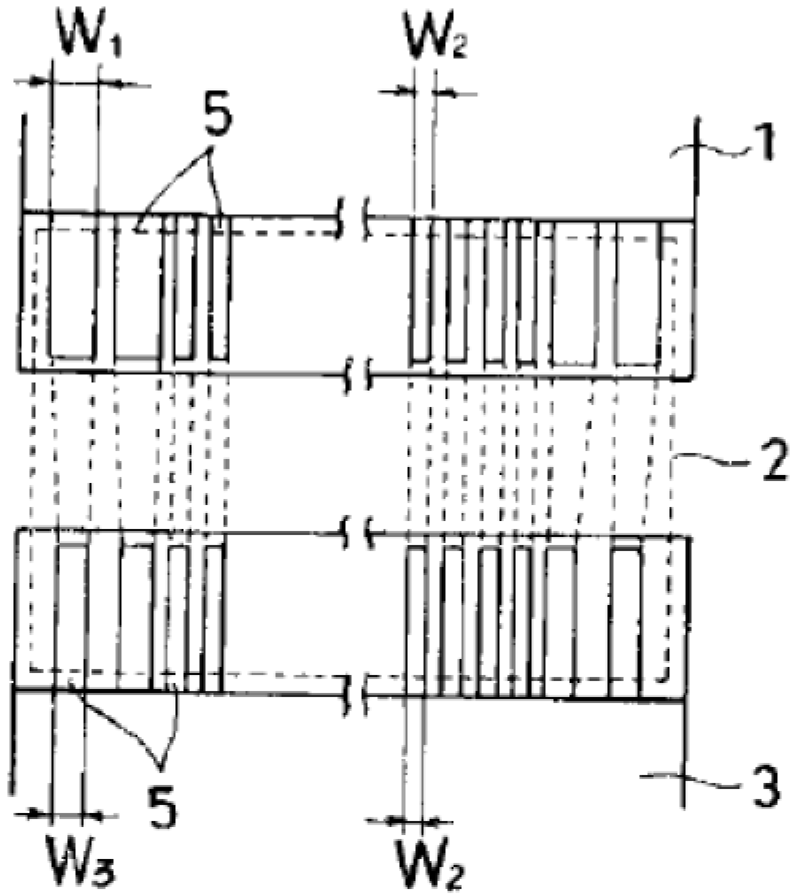


Ex. 1010, Figures 1, 2, 6; ¶¶[0019]-[0022].

7. Claim 7

It would have been obvious to modify Kitawada so that image signal wiring lines in the flexible substrate are formed corresponding to a reference pitch interval of the image signal input terminals. **Minami** discloses that terminals near the center of the substrate (corresponding to Kitawada's image signal input terminals) should have a narrow width ("W_2") and a pitch interval that corresponds to the pitch interval of the wirings in flexible printed circuit 2 and printed wiring board 3:

FIG. 3



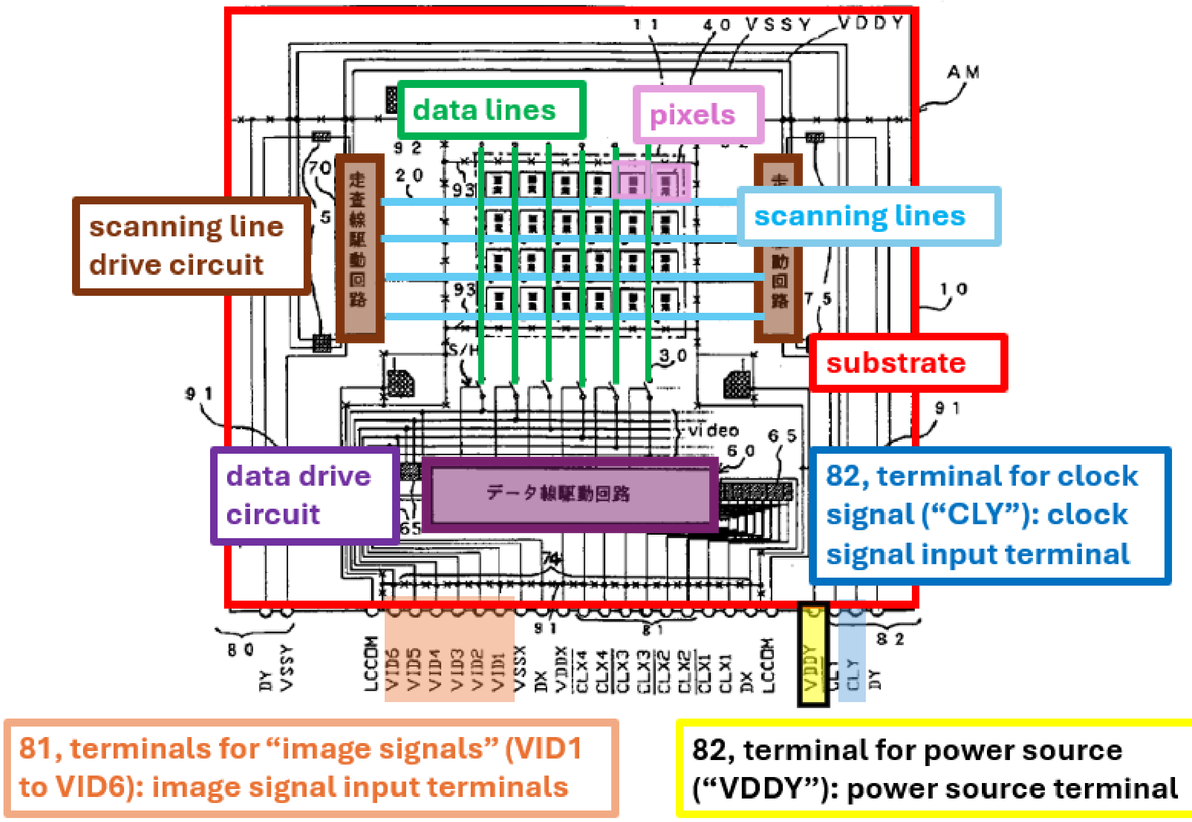
Ex. 1007, Figure 3. It would have been obvious to modify Kitawada to use the pitch interval of image signal input terminals as a "reference pitch" because, as Minami teaches, this matches the pitch interval of the fine pitch wiring. Flasck, ¶255, §XI.

8. Claim 8

Kitawada discloses using the claimed display in an electronic system. Ex. 1004, claim 7. Further, Kawaguchi discloses projectors and computers having LCD displays (Ex. 1005, Figures 11-12) while Matsumoto discloses televisions and other applications. Ex. 1008, §2.7; Flasck §XI.

9. Claim 9

Kitawada discloses claim 9:



Ex. 1004, Figure 2; ¶[0020]; Ground 1 [10b], [10g], claim 12; Flasck §XI.

X. CONCLUSION

Claims 1-23 are obvious. They recite old technology that was used in LCD displays for many decades, including a “substrate,” “pixels,” “data lines,” drive circuits to control the pixels, and so on. **Kitawada** by itself discloses this conventional technology. And it shows clock signal, image signal, and power source terminals formed in a line along one side of an LCD panel’s substrate, with the clock signal and power source terminals closer to the edge of the substrate than the image signal terminals—the arrangement that is the central focus of the ’146 patent.

While Kitawada may not expressly disclose larger area clock signal and power source terminals, the prior art supplies independent reasons for doing so. Flasck, §X. **Minami** and **Sano** ***independently*** teach use of clock signal input terminals having a “larger area” than image signal input terminals in an LCD display like Kitawada’s, so Grounds 1 and 2 rely on these references in the alternative. And **Minami** and **Kato** each ***independently*** teach use of power source input terminals have an area that is “not smaller” than the area of clock signal input terminals in an LCD display, and Ground 2 relies on these references in the alternative.

Dated: August 14, 2025

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CERTIFICATE OF WORD COUNT UNDER 37 CFR §42.24(D)

Under 37 C.F.R. §42.24(d), the undersigned certifies that the word count for this *Petition for Inter Partes Review* totals 13,418, excluding the parts exempted by 37 C.F.R. §42.24(a).

The word count was made using the built-in word count function in the Microsoft Word software used to prepare this document.

Dated: August 14, 2025

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The undersigned hereby certifies that true copies of this **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,636,146** and its supporting **Exhibits and Power of Attorney** have been served by FedEx delivery service on Patent Owner at the correspondence address for the attorney of record for the ’146 Patent shown in USPTO records:

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