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and SANDISK TECHNOLOGIES, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SANDISK CORPORATION, Plaintiff, v. IPVALUE MANAGEMENT, INC. and LONGITUDE FLASH MEMORY SOLUTIONS, LTD., Defendants.	Case No. 5:25-CV-02389-PCP **SANDISK CORPORATION AND SANDISK TECHNOLOGIES, INC.'S DISCLOSURE OF INVALIDITY CONTENTIONS PURSUANT TO PATENT LOCAL RULE 3-3** Date Filed: March 7, 2025 Trial Date:
AND RELATED COUNTERCLAIM.	

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Counterclaim-Defendants Sandisk Corporation and Sandisk Technologies (collectively, "Sandisk") hereby disclose these Invalidity Contentions, which include the claim charts and other materials attached hereto and cited herein, in accordance with Rule 3-3 of this District's Patent Local Rules and the Scheduling Order in this case[1].

These Invalidity Contentions were prepared in response to the claims asserted by Counterclaim-Plaintiffs IPValue Management, Inc. and Longitude Flash Memory Solutions, Ltd. (collectively, "IPValue") in IPValue's September 30, 2025 Infringement Contentions for U.S. Patent No. 8,633,537 ("the '537 patent"); U.S. Patent No. 9,929,240, ("the '240 patent"); U.S. Patent No. 11,456,365 ("the '365 patent"); and U.S. Patent No. 7,671,664 ("the '664 patent") (all four patents referred to collectively herein as "the Asserted Patents"). IPValue has not served disclosures under Patent Local Rule 3-1 for U.S. Patent No. 6,963,505 ("the '505 patent"), nor has the Court set a deadline for IPValue to make such disclosures under the Patent Local Rules. Therefore, these Invalidity Contentions do not address the '505 patent, as IPValue has not complied with Patent Local Rules 3-1 and 3-2 for that patent. Sandisk will prepare and serve Invalidity Contentions for the '505 patent and comply with Patent Local Rules 3-3 and 3-4 for the '505 patent, after IPValue complies with Patent Local Rules 3-1 and 3-2 for that patent and the Court sets a schedule for such events.

At present, and for purposes of these Invalidity Contentions, the Asserted Claims are:

- '537 patent: Claims 17, 18, and 19
- '240 patent: Claims 1, 3, 4, 5, 7, 9, 12, 14, 15, 16, 17, and 18
- '365 patent: Claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44 and 45
- '664 patent: Claims 1, 2, 3, 5, 15, 16, 18, and 19

Sandisk reserves the right to seek leave of Court to amend these Invalidity Contentions under Patent Local Rule 3-6 in view of claim-construction proceedings (as IPValue has not yet disclosed any proposed claim constructions) and the constructions issued by the Court, any Court-

[1] A password-protected FTP link containing Sandisk's invalidity claim charts has been provided to counsel for IPValue in the email accompanying this pleading.

approved amended or supplemental infringement contentions served by IPValue, further investigation and discovery (including third-party discovery into prior-art systems), and any positions taken by IPValue in this or related proceedings (including before the Patent Trial and Appeal Board in pending Inter Partes Review proceedings for the ’365 and ’240 patents), or to avoid unfair prejudice from IPValue’s failure to timely comply with its disclosure obligations under the Patent Local Rules, including IPValue’s deficient Infringement Contentions for the ’537, ’240, ’365, and ’664 patents, which fail to chart and set forth any infringement theory for the vast majority of accused products and technologies, thereby obscuring IPValue’s interpretation of the Asserted Claims and prejudicing Sandisk’s ability to prepare its defenses.

I. PRELIMINARY STATEMENT

As set forth below, all Asserted Claims are invalid under 35 U.S.C. §§ 101, 102, 103, and/or 112.

The identity of each item of prior art relied upon in these disclosures is listed below and in the attached claim charts. The references cited in the claim charts disclose the limitations of the Asserted Claims (explicitly and/or inherently) and may also be relied upon to show the state of the art in the relevant time frames. Sandisk reserves the right to rely on uncited (including cumulative) portions of the references, figures and charts within the references, other documents, and expert testimony to provide context (including, for example, what a person of ordinary skill in the art, or POSITA, would have known or understood at the time of the alleged invention regarding the technologies at issue) and/or to aid in understanding the cited portions of the references (including, for example, how certain technical terms within the cited portions would have been understood by a POSITA). Where Sandisk’s Invalidity Contentions cite to a particular figure in a reference, the citation should be understood to encompass the caption and description of the figure and any text relating to or discussing the figure. Conversely, where Sandisk’s Invalidity Contentions cite to particular text referring to or discussing a figure, the citation should be understood to include the figure as well.

The Asserted Claims must be interpreted the same when comparing them against the accused products and the prior art. *See Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d

1313, 1330 (Fed. Cir. 2003)[2] ("It is axiomatic that claims are construed the same way for both invalidity and infringement."). However, the claim construction process has not begun, and the Court has not yet issued any claim constructions. Therefore, these Invalidity Contentions are based in part on the claim scope and implied claim constructions (to the extent they can be gleaned and understood by Sandisk from IPValue's deficient disclosures) as reflected in IPValue's Complaint and its Infringement Contentions for the Asserted Claims, and are not necessarily based on Sandisk's understanding of or application of the proper claim constructions for the Asserted Claims. Indeed, IPValue's Infringement Contentions do not appear to apply proper claim constructions, and in some instances, ignore claim limitations completely.

By applying IPValue's apparent constructions and/or interpretations (to the extent Sandisk can determine them), Sandisk does not concede in any way that those constructions are correct, and instead expressly reserves the right to oppose those constructions and propose alternative constructions during claim construction. Therefore, these Invalidity Contentions are not, and nothing stated herein should be interpreted as an endorsement, acquiescence, or acceptance of any particular claim construction unless expressly stated. As stated above, Sandisk expressly reserves the right to amend these Invalidity Contentions after the Court has construed all relevant claim terms.

Sandisk incorporates by reference into these Invalidity Contentions all prior art cited during prosecution of the Asserted Patents (whether by the applicants or by the Examiner), which are identified in the file histories produced herewith for the Asserted Patents and also listed on the face of the Asserted Patents.[3] As noted above, Sandisk's ongoing investigation and discovery,

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[2] All internal citations have been omitted, and emphasis has been added unless otherwise stated.

[3] File Histories for the Asserted Patents can be found in the accompanying document production at the following bates: '664 patent (SD_IPV_00001983-2088); '537 patent (SD_IPV00002089-2469; SD_IPV_00003861-4241); '240 patent (SD_IPV_00002679-3379; SD_IPV_4331-4460; SD_IPV_00005047-5679; SD_IPV_00006349-8386; SD_IPV_00008455-8928; SD_IPV_00009955-10755); '365 patent (SD_IPV_00013936-14191; SD_IPV_00014305-14853; SD_IPV_00015946-17902; SD_IPV_00018053-18615; SD_IPV_00018850-19438)

Assignment Histories can be found in the accompanying document production at the following bates: '664 patent (SD_IPV_00000888-891); '240 patent (SD_IPV_00002676-2678); '537 patent (SD_IPV_00003380-3383).

including third-party discovery, may also uncover additional prior art, and Sandisk reserves the right to rely on such additional prior-art materials to further support these Invalidity Contentions.

II. PATENT L.R. 3-3(A): DISCLOSURE OF IDENTITY OF EACH ITEM OF PRIOR ART THAT ANTICIPATES OR RENDERS OBVIOUS EACH ASSERTED CLAIM

Sandisk identifies the following prior art now known to Sandisk to anticipate and/or render obvious one or more of the Asserted Claims of the Asserted Patents under at least 35 U.S.C. §§ 102(a), (b), (e), (g), and/or 103.

A. Prior Art Patents and Publications

The following patents and publications are prior art for the Asserted Claims under at least 35 U.S.C. §§ 102(a), (b), (e), and/or (g). Invalidity claim charts are attached as Exhibits 537-1 through 537-11; Exhibits 240-1 through 240-11; Exhibits 365-1 through 365-11; and Exhibits 664-1 through 664-13. For references that are not individually charted, Sandisk intends to rely on these references at least as background and as evidence of (1) the state of the art at the time of Counterclaim-Plaintiffs' alleged inventions, (2) the level of skill in the art at that time, and (3) the knowledge of a POSITA at that time. Sandisk also identifies as prior art all references cited on the face of the Asserted Patents, as well as cited or disclosed during prosecution.

Additionally, Sandisk identifies all prior art references disclosed and discussed in its Inter Partes Review ("IPR") petitions filed for the '240 patent (Case No. IPR2025-01283) and '365 patent (Case No. IPR2025-01281), and incorporates by reference into these Invalidity Contentions the entirety of those petitions and related exhibits, which have been produced in this litigation and served on IPValue. *See* '240 IPR Petition (SD_IPV_00013268-13370); '240 IPR Exs. (SD_IPV_00003861-13267); '365 IPR Petition (SD_IPV_00013371-13484); '365 IPR Exs. (SD_IPV_00013485-19713).[4]

Table #1

[4] Sandisk filed a *Sotera* stipulation in connection with the pending IPR petitions for the '240 and '365 patents. *See* ECF No. 69. Sandisk will abide by that stipulation, and nothing in these Invalidity Contentions is intended to modify the commitments set forth in that stipulation.

Patent Publications and Applications		
First Listed Inventor	**Patent or Publication**	**Filing Dates**[5]
Arakawa	U.S. Patent No. 5,883,501	4/4/1997
Assar	U.S. Patent No. 5,523,724	8/19/1994
Bazargan	U.S. Patent No. 6,300,839	8/22/2000
Cave	U.S. Patent No. 5,694,308	7/3/1995
Dohi	U.S. Patent No. 6,646,494 B2	11/16/2001
Doi	J.P. Patent Publication No. 2003-022686A	1/24/2003
Folmsbee	U.S. Patent No. 5,386,151	8/11/1993
Fujiwara	U.S. Patent Publication No. 2006/0065910 A1	9/16/2005
Fujioka	U.S. Patent No. 6,020,781	9/17/1997
Fujise	U.S. Patent No. 7,099,167 B2	11/21/2003
Ganguly	U.S. Patent Publication No. 2011/0281429 A1	7/22/2011
Hahn	U.S. Patent No. 7,215,181 B2	12/28/2004
Hiiragisawa	J.P. Patent Publication No. 09-128985A	10/31/1995
Hsu	U.S. Patent No. 6,278,317 B1	10/29/1999
Hwang	U.S. Patent Publication No. 2012/0061744 A1	9/9/2011
Ito	U.S. Patent No. 7,592,856 B2	11/18/2005
Jenne	U.S. Patent No. 8,710,578	3/27/2012
Kang	U.S. Patent No. 7,633,498 B2	11/12/2004

[5] Sandisk lists the filing date of the listed reference. Sandisk reserves the right to rely on an earlier applicable filing date, including the filing date for an earlier nonprovisional application, foreign application, or provisional application, as applicable.

Kawajiri	U.S. Patent 7,251,162 B2	4/27/2005
Kawasaki	U.S. Patent No. 5,587,683	12/6/1994
Kim	U.S. Patent No. 6,724,242 B2	2/20/2003
Koike	J.P. Patent Publication No. 2000-278937	3/23/1999
Kumamoto	J.P. Patent Publication No. 06-062562 A	8/4/1992
Lee	K.R. Patent Application 20030025514A	8/29/2011
Lee	K.R. Patent Application 10-2011-0119061 (“Lee 961”)	4/26/2010
Lee	U.S. Patent Publication No. 2012/0068255 (“Lee 255”)	9/16/2010
Levy	U.S. Patent Publication No. 2009/0179253 A1	6/13/2007
Maeda	J.P. Patent Application No. H10-312695A	5/9/1997
Maekawa	U.S. Patent Publication No. 2006/0267901 A1	5/18/2006
Mahajani	U.S. Patent Publication No. 2005/0062098 A1	9/23/2003
Masataka	J.P. Patent Publication No. 06-062562 U	2/3/1993
Mitsui	U.S. Patent No. 5,999,009	7/25/1997
Nakahara	U.S. Patent No. 6,492,862 B2	2/16/2001
Nicholson	U.S. Patent No. 6,859,091 B1	9/18/2003
Nishimura	J.P. Patent Publication No. 2007-199210	1/24/2006
Oswald	U.S. Patent Publication No. 2008/0084239 A1	9/10/2007
Pantelakis	U.S. Patent No. 5,532,915	3/23/1994

Raghavan	U.S. Patent No. 7,173,477 B1	10/29/2004
Ramkumar	U.S. Patent No. 9,102,522	3/29/2012
Schlueter	U.S. Patent No. 7,999,601 B2	4/1/2005
Shimura	J.P. Patent Publication No. 2005073437A	8/27/2003
Shuto	J.P. Patent Publication No. 2005-76159	3/17/2004
Song	U.S. Patent No. 5,818,766	3/5/1997
Soo	K.R. Patent Publication No. 20050038847A	10/23/2003
Stoops	U.S. Patent No. 7,068,087 B2	2/24/2004
Sugasawa	JP Patent Publication No. 20007236657A	2/15/1999
Sugasawa	U.S. Patent No. 6,249,445 B1	2/11/2000
Tasdighi	U.S. Patent No. 5,734,291	3/11/1996
Takahashi	U.S. Patent No. 6,879,537 B2	10/16/2002
Ubata	JP Patent Publication No. H6-149407A	11/12/1992
Uenishi	U.S. Patent Publication No. 2010/207192A	2/12/2010
Voo	U.S. Patent No. 6,320,796 B1	11/20/2000
Wang	U.S. Patent Publication No. 2009/0057752	8/28/2007
Yamawaki	U.S. Patent No. 5,159,543	12/20/1990
Yan	U.S. Patent Publication No. 2008/0135946 A1	12/11/2007
Yen	U.S. Patent Publication No. 2006/0197583 A1	6/10/2005
Yusada	U.S. Patent No. 8,674,430 B2	3/23/2012

Zheng	U.S. Patent No. 6,912,163 B2	9/9/2003
Kuo	U.S. Patent No. 6,768,366	6/17/2003
Non-Patent Publications		
Aochi	BiCS Flash as a Future 3D Non-Volatile Memory Technology for Ultra High Density Storage Devices	2009
Endoh	Novel Ultrahigh-Density Flash Memory With a Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell	2003
Fukuzumi	Optimal Integration and Characteristics of Vertical Array Devices for Ultra-High Density, Bit-Cost Scalable Flash Memory	2007
Ishiduki	Optimal Device Structure for Pipe=Shaped BiCS Flash Memory for Ultra High Density Storage Device with Excellent Performance and Reliability	2009
Jang	Vertical Cell Array Using TCAT (Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory	2009
Komori	Disturbless Flash Memory due to High Boost Efficiency on BiCS Structure and Optimal Memory Film Stack for Ultra High Density Storage Device	2009
Lue	A Highly Scalable 8-Layer 3D Vertical-Gate VG TFT NAND Flash Using Junction-Free Buried Channel BE-SONOS Device	2010
Maeda	Multi-Stacked 1G Cell Layer Pipe-Shaped BiCS Flash Memory	2009
Nitayama	Bit Cost Scalable (BiCS) Flash Technology for Future High Density Storage Devices	2009

Nitayama	Bit Cost Scalable BiCS Technology for Future Ultra High Density Storage Memories	2013
Pan	Charge Pump Circuit Design (McGraw-Hill Electronic Engineering, 1st Edition)	2006
Shin	A Novel NAND-type MONOS Memory using 63nm Process Technology for Multi-gigabit Flash EEPROMs	2005
Tanaka	Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash memory	2007
Toshiba Corp.	Toshiba Develops New NAND Flash Technology, Press Release	2007

Additionally, some of Sandisk's printed prior art references may share a common application or have a similar relationship (*e.g.*, as to publication or issuance) with other prior art, and therefore the related prior art contains substantially the same disclosure (*e.g.*, published U.S. patent applications corresponding to issued U.S. patents, or foreign applications). Any citation to or quotation from any such printed prior art references or patents should, therefore, be understood to encompass the parallel or equivalent citation to the same written disclosure in a related or corresponding application or patent, if any. For example, where a claim chart cites a published patent application that ultimately issued as a patent with substantially the same written description, Sandisk may rely upon the published patent application or the issued patent as prior art.

Sandisk also reserves the right to supplement or amend these disclosures as permitted by the Local Patent Rules, the Federal Rules of Civil Procedure, and/or any Order of this Court. Sandisk incorporates by reference (1) any and all prior art contained or identified in documents produced thus far by IPValue in this proceeding, (2) any and all additional materials regarding or bearing upon invalidity in IPValue's possession or control that have not been produced in this lawsuit to date, if any exist. Each disclosed item of prior art that is a product, system, or other implementation is contended to be a prior public use, on sale, or otherwise public availability of the claimed invention under 35 U.S.C. § 102. Sandisk further intends to rely on admissions of the named inventors concerning the prior art, including statements found in the Asserted Patents, their prosecution histories, related patents or patent applications, any deposition testimony, and the papers filed and any evidence submitted by IPValue in conjunction with this litigation.

Sandisk also incorporates by reference into these Invalidity Contentions, in full, each and every prior art reference cited in and on the face of the Asserted Patents, their prosecution histories, and any applicable post-grant proceedings.

Sandisk reserves the right to rely on the prior art listed above, as well as disclosures below related to the state of the art at the time of the purported inventions. In addition to the prior art listed above and disclosed herein, Sandisk reserves the right to rely on statements made by the Examiner at the U.S. Patent and Trademark Office discussing the prior art disclosed in the prosecution history of the Asserted Patent, and statements made by the applicants purporting to distinguish such prior art. Sandisk further reserves the right to rely on prior art, including references and evidence of prior public use, on sale, or otherwise public availability obtained in discovery from third parties, the inventors and the parties in this case. Further, Sandisk reserves the right to rely on systems, textbooks, and other references disclosed in fact and/or expert discovery to establish the state of the art and the knowledge of POSITAs at the time of the alleged invention of the Asserted Patents.

B. Prior Art Systems

Sandisk contends the following prior art systems that were in public use, on sale, or otherwise available to the public before the applicable priority date(s) anticipate and/or render obvious one or more Asserted Claims of the Asserted Patent under 35 U.S.C. § 102 and/or 35 U.S.C. § 103:

Table #2		
Prior-Art Systems Known, Used, Sold, or Offered for Sale		
Item	**Date**	**Person/Entity**

Cypress 65nm devices and other Cypress devices incorporating the technology claimed by the Polishchuk patents ("Cypress products" charted at Exs. 537-7, 240-7, and 365-7)	Prior to July 1, 2012	Cypress Semiconductor
12 V CMOS Voltage Converter (LTC1044A)	1993	Linear Technology
CMOS Monolithic Voltage Converter (MAX660)	1996	Maxim
Dual-Output Charge Pump with Shutdown (MAX864)	1996	Maxim
200mA Charge Pump Inverter or Doubler (SP6660)	2000	Sipex
High Frequency 200mA Charge Pump Inverter or Doubler (SP6661)	2004	Sipex
Charge Pump Regulator with Selectable 5.0V and 4.5V Output (SC603)	2004	Semtech
3-Channel DC-DC Converter (EL7583)	2005	Intersil
Bias Power Supply for TV and Monitor TFT LCD Panels (TPS65161)	2006	Texas Instruments
Charge Pump Voltage Converters (TJ7660)	2007	HTC

For prior art systems identified in these Invalidity Contentions as invalidating one or more of the Asserted Claims, where sufficient information was available and located after a diligent search at the time of this filing, Sandisk has included claim charts that identify and cite multiple pieces of evidence as reflecting the portions or features of those systems that Sandisk contends meet (*e.g.*, comprised, disclosed, taught, and/or practiced by) the corresponding limitations of the Asserted Claims, and as substantiating the features, functionality, and operation of the identified prior art systems, as well as their prior public use, on sale, and/or otherwise public availability.

However, in citing such evidence, Sandisk does not contend that each piece of cited evidence constitutes a printed publication, nor does Sandisk concede that a POSITA would have needed a motivation to combine such pieces of evidence. Instead, such material is cited as evidence to establish the features, functionality, and operation of the prior art systems, as well as their prior public use, on sale, and/or otherwise public availability. Notwithstanding the foregoing, Sandisk reserves the right to cite any or all of these evidentiary materials as background or as evidence of the skill and knowledge of a POSITA at the time of the alleged inventions in the Asserted Claims.

Despite Sandisk's diligent searching and investigation, information sufficient to chart many of the prior art systems has been difficult to find in publicly available resources. Sandisk's investigation into prior art systems remains ongoing and Sandisk reserves the right, pursuant to the Patent Local Rules, to identify and rely on systems that represent different versions or are otherwise related variations of the systems identified above based on information obtained through further searching and investigation, and through the service of third-party subpoenas for information that is not available or easily found in the public domain. Sandisk further reserves the right to seek leave to revise, amend, update, and/or supplement the information provided in these Invalidity Contentions (including the attached claim charts) for prior art systems, and reserves the right to submit additional claim charts, based on additional information and evidence obtained through discovery. Sandisk also reserves the right to rely on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed above. In addition to the prior art products, components, systems, and methods described above, Sandisk also reserves the right to rely on documents and publications relating to the prior art listed above as prior art publications.

III. PATENT L.R. 3-3(B): WHETHER EACH ITEM OF PRIOR ART ANTICIPATES OR RENDERS OBVIOUS EACH ASSERTED CLAIM

Subject to Sandisk's reservations of rights, Sandisk in the below subsections identifies each item of prior art that anticipates each of the Asserted Claims of the Asserted Patents under § 102 and/or renders it obvious under § 103. Sandisk also attaches limitation-by-limitation claim charts demonstrating where in each prior-art reference each limitation of the Asserted Claims of each of the Asserted Patents is found. These claim charts are based on Sandisk's current understanding of the terms and limitations of IPValue's Asserted Claims (including how IPValue is interpreting the Asserted Claims based on the Infringement Contentions), and Sandisk's current understanding (where discernible) of the claim constructions apparently underlying IPValue's Infringement Contentions. To the extent any limitation is deemed by IPValue, the Court, or the jury not to be fully disclosed, either expressly or inherently, by an item of prior art, Sandisk contends that the difference(s) would have been obvious to a POSITA and within the knowledge of one skilled in the art at the time of the alleged invention, so that the claimed invention would have been obvious both in light of the single reference alone and/or in light of a combination of references.

Much of the art identified in the attached exhibits/charts reflects common knowledge to POSITAs and the state of the relevant art at the time of the effective filing date of each of the Asserted Patents. Sandisk may rely on additional citations, references, expert testimony, and other material (such as demonstratives or illustrations) to provide context or to aid in understanding the cited portions of the references or cited features of the systems. Sandisk may also rely on expert testimony to explain relevant portions of references, relevant hardware or software products or systems, and other discovery regarding these subject matters. Additionally, Sandisk may rely on other portions of any prior art reference for purposes of explaining the background and general technical subject area of the reference.

Where an individual reference is cited in the attached exhibits/charts with respect to all limitations of an Asserted Claim, Sandisk contends that the reference anticipates the claim under one or more of 35 U.S.C. §§ 102(a), (b), (e), and/or (g) and also renders obvious the claim under 35 U.S.C. § 103, both by itself in view of the knowledge of a POSITA (including in view of admitted prior art disclosed in and on the face of the Asserted Patent and its corresponding prosecution history) and/or in combination with the other cited references to the extent the reference is not found to disclose one or more claim limitations. A single prior art reference, for example, can establish obviousness where the differences between the disclosures within the reference and the claimed invention would have been obvious to one of ordinary skill in the art.

For example, "[c]ombining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness." *Boston Scientific Scimed, Inc. v. Cordis Corp*., 554 F.3d 982, 991 (Fed. Cir. 2009). If IPValue contends that an embodiment within a particular item of prior art does not fully disclose all limitations of a claim, Sandisk reserves the right to rely, in rebuttal, on other embodiments in that prior art reference, or other information, to show single reference obviousness under 35 U.S.C. § 103. In addition, Sandisk reserves the right to argue with respect to any claim element that the prior art disclosure of that element is either express or inherent as understood by a POSITA.

Where an individual reference is cited in the attached exhibits/charts with respect to fewer than all limitations of an Asserted Claim, Sandisk contends that the reference renders obvious the claim under 35 U.S.C. § 103 by itself in view of the knowledge of a POSITA (including in view of admitted prior art disclosed in and on the face of the Asserted Patent and its corresponding prosecution history) and/or further in view of each other reference and combination of references that discloses the remaining claim limitation(s), as indicated in the claim charts submitted herewith. Each cited prior art reference may be combined with one or more other prior art references to render obvious, under § 103, the Asserted Claims in combination. The disclosures of these references may also be combined with information generally known to POSITAs at the time of the alleged inventions and understood and supplemented in view of the common sense of such persons, including any statements in the intrinsic records of the Asserted Patents and related applications.

As the Supreme Court held in *KSR Int'l Co. v. Teleflex, Inc.*, "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." 550 U.S. 398, 416 (2007). The Supreme Court further held that, "[w]hen a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *Id.* at 417. Moreover, the Supreme Court held that "in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *Id.* at 420. Indeed, the Supreme Court held that it is sufficient that a combination of elements was "obvious to try" holding that, "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense." *Id.* at 421. "In that instance the fact that a combination was obvious to try might show that it was obvious under § 103." *Id.*

The prior-art references relied upon herein for the ’664 patent are directed to the same or similar fields of endeavor. The same is true for the prior-art references relied upon herein for the three Polishchuk patents (the ’537, ’240, and ’365 patents), which are part of the same family of patents (the ’240 and ’365 patents purport to be continuations of the ’537 patent) and share a common specification, as well as the same named inventors. Accordingly, a POSITA would have recognized that the results of the combinations discussed herein for the ’664 patent were predictable and would have been clearly motivated to modify and combine any of the prior-art references identified below and in the attached claim charts for the ’664 patent to arrive at the claimed inventions of the ’664 patent’s Asserted Claims. The same is true for the three Polishchuk patents and all of the prior-art references identified below and in the attached claim charts for the ’537, ’240, and ’365 patents.

At least the following rationales support a finding of obviousness based on those combinations as well as those additional combinations set forth in detail below:

(A) Combining prior art elements according to known methods to yield predictable results;

(B) Simple substitution of one known element for another to obtain predictable results;

(C) Use of known technique to improve similar devices (methods, or products) in the same way;

(D) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(E) "Obvious to try"—choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

(F) Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art; and

(G) Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

Exemplary motivations to combine references for the Asserted Patents are discussed in greater detail below and may also be discussed in the exhibits and charts attached hereto. The fact that other motivations to combine are not discussed more specifically should not be interpreted as an admission or concession that they do not apply. To the contrary, the discussion above and throughout these Invalidity Contentions simply provides examples of the many motivations to combine that would have been felt by persons of ordinary skill in the art. Sandisk reserves the right to rely upon any references or assertions identified herein in connection with Sandisk's contention that each Asserted Claim is invalid under 35 U.S.C. § 103 and to rely upon expert testimony addressing these references and assertions. The fact that prior art is identified to anticipate the Asserted Claims under § 102 does not prevent Sandisk from also relying on the same reference as rendering the Asserted Claims invalid as obvious under § 103. *See In re Meyer*, 599 F.2d 1026, 1031 (C.C.P.A. 1979) (holding that "a rejection for obviousness under § 103 can be based on a reference which happens to anticipate the claimed subject matter"). If IPValue alleges, or a factfinder concludes, that any identified prior art item does not fully disclose a limitation, Sandisk contends the limitation is disclosed and identified in another prior art item, or is admitted prior art by the Asserted Patent, and therefore, all limitations of each Asserted Claim is invalid as anticipated and/or obvious in view of the prior art..

Sandisk also expressly incorporates by reference any statements and reasons set forth by the Examiner during prosecution of the Asserted Patents and related patent applications, as to why it would have been obvious to modify or combine references to achieve the limitations of the Asserted Claims. This includes, without limitation, (1) the Examiner's reasons set forth on Pages

2–6 in the Office Action Summary for Application No. 13/539,466, with a mailing date of September 28, 2012, for the ’537 patent and the combination(s) of the Levy *et al.* (U.S. Pub. No. 2009/0179253), Zheng *et al.* (U.S. Patent No. 6,912,163), Yan (U.S. Pub. No. 2008/0135946), Heurta *et al*. (W.O. 2008/129478, cited in Office Action as U.S. Pub. No. 2010/0117138), and Goebel *et al*. (U.S. Pub. No. 2003/0169629) prior-art references under § 103; and (2) the Examiner’s reasons set forth on Pages 8–16 in the Office Action Summary for Application No. 15/335,180, with a notification date of May 17, 2017, for the ’240 patent and the combination(s) of the Bhattacharyya (U.S. Pub. No. 2006/0284236), Kim *et al.* (U.S. Pub. No. 2008/0272424), Forbes (U.S. Pub. No. 2007/0233007, which corresponds to U.S. Patent No. 7,425,491), Hagemeyer *et al.* (U.S. Pub. No. 2006/0008959), Wang (U.S. Pub. No. 2006/0113586), and Lue *et al.* (U.S. Pub. No. 2007/0029625) prior-art references under § 103.

To the extent that any reference is found not to anticipate one or more asserted claims, various references described herein and/or the knowledge and skill of a POSITA at the time of the invention, in combination with any one of the other references, render the claim invalid as obvious under § 103. Sandisk’s contentions that the references in the below sections, in various combinations, render the Asserted Claims obvious under 35 U.S.C. § 103 are in no way an admission or suggestion that each reference does not independently anticipate or render obvious a particular claim under 35 U.S.C. § 102.

A. The ’537, ’240, and ’365 patents (the “Polishchuk patents”)

1. Priority

The three Polishchuk patents share a common specification and priority date. For purposes of these Invalidity Contentions and the Polishchuk patents, Sandisk has applied the priority date of July 1, 2012—the filing date of the application for the ’537 patent—as the relevant priority date. The application for the ’537 patent was a continuation-in-part of U.S. application No. 13/288,919, and introduced new matter claimed in the Polishchuk patents. Recognizing the new matter introduced in the application for the ’537 patent and claimed in the Polishchuk patents, IPValue’s Infringement Contentions and related disclosures under the Patent Local Rules likewise state that the Polishchuk patents are entitled to a July 1, 2012, priority date.

Further analysis of the priority date for the Polishchuk patents is provided in the IPR petitions filed for the ’240 and ’365 patents, which have been produced in this case and served on IPValue, and which are incorporated by reference in their entirety into these Invalidity Contentions. *See* ’240 IPR (Case No. IPR2025-01283) at 21–24 (priority date discussion); *see also* ’365 IPR (Case No. IPR2025-01281) at 20–22 (same).

2. Background on the State of the Art

Flash memory is a common type of non-volatile memory that was invented in the 1980s when Dr. Fujio Masuoka created the first NOR-based Flash memory while working at Toshiba in 1984. *See, e.g.*, https://computerhistory.org/events/flashback-story-flash-memory/; *see also* https://www.computerhistory.org/revolution/memory-storage/8/256; https://www.youtube.com/watch?v=jtj-ShlxOzQ (“Flashback - A Story of Flash Memory”). After Dr. Masuoka’s invention, several companies, including Intel and Sandisk (then called Sundisk when it was founded in 1988 until it was renamed in 1995), began developing, improving, and commercializing flash memory technology. By the early 1990s, Sandisk had already established itself as a key innovator in flash memory technology, and it remains an innovator today. *See* https://www.sandisk.com/company/newsroom/blogs/2025/an-enduring-legacy-the-sd-card-at-25.

Non-volatile memory is computer storage that retains data even when power to the memory device is turned off. The first semiconductor non-volatile memory was created in 1952 at MIT. *See* https://newsletter.semianalysis.com/p/the-history-and-timeline-of-flash (reproducing the history and timeline of flash memory from the 2022 Flash Memory Summit). Flash memory is a type of non-volatile memory. Specifically, flash memory is a type of EEPROM (Electrically Erasable Programmable Read-Only Memory) designed to have data be erased or written in large, fixed blocks or sectors, as opposed to byte-by-byte.

Early flash memory designs were based on “floating gate” technology. The devices used an electrically insulated gate that “floats” between two oxide layers such that any electron placed in the gate remains trapped there even after power is removed, which is what allows the technology to function as non-volatile memory. In the simplest example, the presence of sufficient electrons in the floating gate will cause the memory to be read at one state, *e.g.*, as a "1," while the absence of electrons in the floating gate will cause the memory to be read at a different state, *e.g.*, as a "0." The "1" or "0" represents the two binary states of a "bit," which is a fundamental unit of data. Computers that use binary storage systems rely on these two states to represent all data.

At a high level, electrons can be placed in the floating gate by various methods, including by "tunneling," where an electric field applied between the substrate and control gate causes electrons from the substrate to "tunnel" through the tunnel oxide layer and move into the floating gate. This is called a "program/write" operation. The electrons can be removed from the floating gate by applying an opposite electric field, which will cause the electrons trapped in the control gate to "tunnel" back to the substrate through the tunnel oxide layer. This is called a "clear/erase/wipe" operation.

Floating gates for non-volatile memory have been in use since at least 1961, when C.T. "Tom" Sah of Fairchild Semiconductor envisioned its use on the gate electrode of a MOS tetrode transistor. *See* https://newsletter.semianalysis.com/p/the-history-and-timeline-of-flash. Engineers at Bells Labs, Westinghouse, and Toshiba further developed and improved floating-gate and charge-trap techniques in the late 1960s and early 1970s. *See id.*; *see also* https://www.computerhistory.org/storageengine/reusable-semiconductor-rom-introduced (describing how "Dawon Kahng and Simon Sze of Bell Labs described in 1967 how the floating gate of an MOS semiconductor device could be used for the cell of a reprogrammable ROM"). Among the early innovators in floating-gate technology was Dr. Eli Harari, one of the founders of Sandisk, who invented the first practical floating gate EEPROM using thin SiO2 and Fowler-Nordheim tunneling for program and erase. *See* https://newsletter.semianalysis.com/p/the-history-and-timeline-of-flash; https://www.computerhistory.org/storageengine/reusable-semiconductor-rom-introduced (citing and discussing U.S. Patent No. 4,115,914 to Harari, entitled "Electrically Erasable Non-Volatile Semiconductor Memory").

By the early 2000s, flash memory devices were also fabricated using charge-trap "SONOS" (silicon–oxide–nitride–oxide–silicon) type transistors. SONOS-type flash memory is similar to floating gate memory except that the floating gate is replaced with a non-conductive silicon nitride layer (or similar layer) containing a large number of charge-trapping sites. By the early 2000s, how to design a SONOS-type flash memory was well known to a POSITA. For example, in a prior-art reference filed in 2003 that later matured into U.S. Patent No. 7,012,299, owned by Sandisk, the named inventors noted that their invention related to "an improved nonvolatile charge-storage memory cell related to a *traditional* SONOS device." Mahajani at [0021]. And the Polishchuk patents themselves acknowledge that the "processing" steps for "fabrication of a SONOS-type memory device" was already "known in the art" to a POSITA. *See, e.g.*, '537 patent at 12:14–16. This is further confirmed by the many "SONOS"-related prior art references cited on the face of the Polishchuk patents, including, without limitation, Yang *et al.*, "Reliability considerations in scaled SONOS nonvolatile memory devices, solid state Electronics", 43 (1999) 2025–2032; EP1487013A3 to Samsung ("SONOS memory device and method of manufacturing the same"), which has a priority date of June 10, 2003; and KR100594266B1 to Jeon Sang-hoon *et al*. ("Sonos type memory device"), which has a priority date of March 17, 2004.

Indeed, the use of a SONOS structure for memory devices generally has been discussed since at least the 1970s. *See* P.C.Y. Chen, "Threshold-alterable Si Gate MOS Devices," IEEE Transactions on Electron Devices, Vol. ED-24, No. 5, May 1977, New York (US), at 584–86 (discussing a method of making a threshold-alterable silicon gate memory device having a polysilicon-oxynitride-nitride-oxide-silicon (SONOS) structure which involved a step of steam oxidation of silicon nitride to form the oxynitride layer). And the development and improvement of SONOS technology continued in the decades thereafter. M. H. White, D. A. Adams and J. Bu, "On the go with SONOS," IEEE Circuits and Devices Magazine, vol. 16, no. 4, at 22–31, July 2000 (discussing advancements in scaling gate insulators for MOS transistors permit low-voltage, silicon-oxide-nitride-silicon (SONOS) nonvolatile semiconductor memories (NVSMs) for a wide range of applications).

Textbooks pre-dating July 2012 also discussed the use of SONOS (among other options) as one of many well-known charge trap NAND technologies. *See, e.g.*, Micheloni, Rino *et al.*, "Inside NAND Flash Memories," Springer Science & Business Media, Jul 27, 2010 (herein, "NAND Flash Memories Textbook"). For example, Page 121 of the NAND Flash Memories Textbook discusses "Stack options" in section 5.2.3 for "Planar charge trap NAND," and notes that "[i]n the last decade many CT NAND options have been proposed to continuously improve cell performance." *Id.* at 121. The NAND Flash Memories Textbook goes on to list "the most important CT options" in Table 5.1 on that same page (reproduced below), which included "SONOS," "SANOS," "MANOS," and "BE-MANOS," and further discusses that SONOS "is the simplest and first proposed stack" on Page 122. *Id.* at 121–22; Table 5.1.

Table 5.1. Summary of the most important acronyms used for CT memories

	SONOS	SANOS	MANOS	BE-MANOS
Gate	polySilicon	polySilicon	Metal	Metal
Blocking layer	silicon diOxide	Alumina	Alumina	Alumina
Storage layer	silicon Nitride	silicon Nitride	silicon Nitride	silicon Nitride
Tunnel layer	silicon diOxide	silicon diOxide	silicon diOxide	Band Engineered Oxide
Substrate	Silicon	Silicon	Silicon	Silicon

Therefore, long before the 2012 priority date of the Polishchuk patents, which are directed to charge-trap SONOS-type devices, use of SONOS or MANOS (with a metal, *e.g.*, high work function gate) structures for non-volatile memory design and SONOS-type flash memory devices were already viewed by companies and engineers in the memory field as a traditional/conventional non-volatile memory technology.[6] This is why the specification of the

[6] BE-MANOS, where "BE" refers to "Band-Engineered," was also well known before 2012. *See, e.g.*, Lai, Sheng-Chih, et al. "An Oxide-Buffered BE-MANOS Charge-Trapping Device and the Role of Al_2O_3." 2008 Joint Non-Volatile Semiconductor Memory Workshop and International Conference on Memory Technology and Design, Proceedings (NVSMW/ICMTD), 18–22 May 2008, Opio, France, IEEE, 2008, at 101-102.; Liao, Chien-Wei, et al. "Reliability Study of MANOS with and without a SiO_2 Buffer Layer and BE-MANOS Charge-Trapping NAND Flash Devices." 2009 International Symposium on VLSI Technology, Systems, and Applications (VLSI-TSA '09), at 27–29 Apr. 2009, Hsinchu, Taiwan. IEEE, 2009, at 152-153; Boutchich, M., D. S. Golubović, N. Akil, and M. van Duuren. "Evaluation of Layered Tunnel Barrier Charge Trapping Devices for Embedded Non-Volatile Memories." Microelectronic Engineering, vol. 87, no. 1, Jan. 2010, at 41-46; You, Hee-Wook, Jung-Woo Son, and Won-Ju Cho. "Engineering of Tunnel Barrier for Highly Integrated Nonvolatile Memory Applications." Applied Physics A, vol. 102, no. 4, Mar. 2011, at 921-926. Similarly, BE-SONOS was equally well known. *See, e.g.*, Lue, "A Highly Scalable 8-Layer 3D Vertical-Gate VG TFT NAND Flash Using Junction-Free Buried Channel BE-SONOS Device" (listed in Section II.A).

Polishchuk patents acknowledges that processes for the "fabrication of a SONOS-type memory device" was already "known in the art." *See, e.g.*, '537 patent at 12:14–16.

With the conventional SONOS structure well-established by the mid-2000s, the industry turned to engineering alternative configurations of the SONOS-type stack to optimize performance. A POSITA would have been very familiar prior to July 1, 2012, with a variation that added a second nitride layer to the conventional SONOS-type stack to create a SONNOS device. Of note, the Polishchuk patents describe problems with "conventional memory" that a POSITA would already have understood had been solved.

> One problem with conventional memory transistors and methods of forming the same is that the charge trapping layer typically has poor or decreasing data retention over time, limiting the useful transistor lifetime. Referring to FIG. 1A, if the charge trapping layer is silicon (Si) rich there is a large, initial window or difference between VTP, represented by graph or line 102, and the VTE, represented by line 104, but the window collapse very rapidly in retention mode to an end of life (EOL 106) of less than about 1.E+07 seconds.
>
> Referring to FIG. 1B, if on the other hand the charge trapping layer is if a high quality nitride layer, that is one having a low stoichiometric concentration of Si, the rate of collapse of the window or Vt slope in retention mode is reduced, but the initial program-erase window is also reduced. Moreover, the slope of Vt in retention mode is still appreciably steep and the leakage path is not sufficiently minimized to significantly improve data retention, thus EOL 106 is only moderately improved.

'537 patent, 1:57–2:7.

For example, it was well understood prior to July 2012 that making two charge trap layers of different compositions and trap densities, such as by making the lower layer of oxynitride (SiOxNy) and the top layer of nitride, could improve charge storage by preventing electron leakage from the top nitride layer. As one illustration of this point, U.S. Patent Application Publication No. 2003/0122204 ("Nomoto") from 2003, taught a SONNOS structure:

FIG.3H

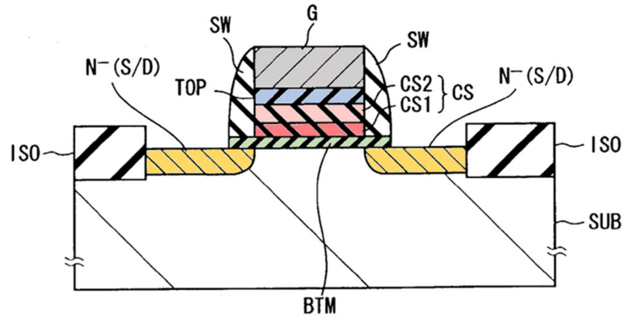


Fig. 3H shows a (i) silicon substrate ("SUB") with source and drain ("S/D"); (ii) a silicon dioxide (SiO_2) bottom dielectric film ("BTM"); (iii) a first nitride film ("CS1"); (iv) second nitride film ("CS2"); (v) silicon dioxide (SiO_2) top dielectric film ("TOP"); and (vi) doped polycrystalline silicon gate electrode ("G"). Nomoto at [0032]–[0038]. Nomoto teaches that the two nitride layers have different compositions (*id.*, [0035], [0044]–[0045]) so that the charge trap density of CS2 is higher than CS1 (*id.*, [0073]–[0088]). Nomoto teaches that the top nitride film (CS2) acts as the primary charge storage layer, while the lower nitride film (CS1) acts as a barrier that reduces leakage of charges from CS2. Nomoto at [0035]; *see also id.* at [0088] (explaining benefits of two nitride layers).

Many other references also taught a two-layer charge storage region long before July 1, 2012. *See, e.g.*, Fujiwara, Ganguly, Jenne, Lee 961, Mahajani, Ramkumar, Uenishi and Wang. Indeed, Mahajani notes that in 1996 Evtukh et al. proposed a multilayer charge storing region with silicon nitride presented with varying stoichiometry (*e.g.,* nitrogen-rich and silicon-rich layers). Mahajani at [0052] (citing "The Multilayer Silicon Nitride Films as a Media for Charge Storage in MNOS Structures," proceedings of the 1996 International Nonvolatile Memory Technology Conference).

It was also well-understood long before July 2012 to employ (i) an oxygen-lean nitride top layer primarily responsible for storing charges; and (ii) an oxygen-rich nitride bottom layer to prevent electron leakage from the oxygen-lean top layer, as described, for example by Nomoto. Numerous references disclose multi-layer charge trap regions, including those with an oxygen-rich layer adjacent to the tunneling layer and an oxygen-lean charge storage layer adjacent or near the blocking layer, and a POSITA would have been well aware prior to July 2012 that multilayer charge trap regions and those with oxygen-lean top layers and oxygen-rich bottom layers could potentially improve performance. *See, e.g.*, Fujiwara, Ganguly, Jenne, Lee 961, Mahajani, Ramkumar, Uenishi and Wang. For example, Mahajani discloses using a silicon oxynitride bottom layer (oxygen rich), with an upper layer of silicon-rich silicon nitride followed by another layer of silicon oxynitride. Mahajani at [0047]. The reference goes on to say that "Any SONOS-type device having a charge storage layer (formed between a blocking dielectric and a tunneling dielectric) comprising two or more dielectric films, wherein in the dielectric films are different materials, falls within the scope of the invention. 'Different materials' means having different chemical components." *Id*. at [0055].

Thus, a POSITA would have been well aware that multi-layer charge trap regions presented potential benefits, and that layers with different chemical components, such as an oxygen-rich SiON bottom layer and oxygen-lean SiN top layer could have been advantageous. *See also, e.g*., Uenishi at [0031] (noting that bottom charge trap layer 30n in Fig. 13 preferably "comprises silicon, nitrogen, and oxygen" while top charge trap layer 40t is stoichiometric SiN); Fujiwara at [0199] ("The memory transistor has a structure transition layer 12B1, for example, a SiON film, between the first oxidation film 12A serving as the bottom insulation film and the balk layer of the nitride film 12 (SiNx film) serving as the charge storage layer."); Ganguly at [0049] ("According to detailed embodiments of the device 10, the first trapping sub-layer 32 comprises a composition of at least one silicon nitride compound having a chemical formula of SixNy present in the range of about 50% to 100% on an atomic percentage basis and oxygen present in the range of about 0% to 50% on the same basis. The second trapping sub-layer 34 may comprise a silicon-rich silicon nitride compound containing more silicon on an atomic percentage basis than is present in stoichiometric silicon nitride."); Wang at [0030] ("the charge-trapping composite layer 104 can also have a structure that includes a stack with a silicon nitride layer on a silicon oxynitride layer"). Based on these disclosures and additional disclosures in the art cited in Sandisk's Invalidity Contentions, a POSITA would have known the potential advantages of an oxygen-rich charge trap layer near the tunneling layer and an oxygen-lean charge trap layer near the blocking layer. A POSITA would also have been aware that there were only a finite number of ways to approach designing a charge trap region, and that these were predictable solutions to the known problem of charge retention in SONOS structures, all of which had a reasonable expectation of success. *See, e.g., id.*, [0026].

Similarly, a POSITA would also have known well before July 1, 2012, that placing a thin anti-tunneling layer between two charge trap regions could potentially provide additional benefits by further reducing leakage of electrons. Indeed, a SONONOS-type structure, often described in addition to a SONNOS-type structure, was equally well-known in the prior art. *See, e.g.*, Lee 961; Mahajani. Further, it was well known to a POSITA before July 1, 2012 that there were a finite number of ways to approach designing a charge trap region, and these were predictable solutions to the known problem of charge retention in SONOS-type structures, which had a reasonable expectation of success, including adding a silicon oxide anti-tunneling barrier.

In sum, long before July 1, 2012, it was well known to a POSITA to create multi-layer charge trap regions, including those where the lower or first layer (closer to the tunneling layer) was oxygen rich and the top layer, where more electrons were to be trapped (closer to the blocking layer), was oxygen lean. It was also well known to a POSITA that this type of structure reduced electron leakage, ensuring that as the technology shrank, sufficient electrons would remain in the charge trap region and would not migrate away, which could cause errors.[7]

The nonvolatile memory described above can all be categorized as "planar" or "2-D" as the memory cells were all produced in a two-dimensional configuration. Since its founding in 1988, Sandisk has been a pioneer in innovating new approaches to increasing density in flash memory storage (density referring to the amount of data that can be stored within a given physical space of memory). Indeed, a few days after founding Sandisk, co-founder Eli Harari filed the company's first patent, entitled "Highly Compact EPROM and FLASH EEPROM Devices,"

[7] The BE-MANOS prior art references, discussed earlier in this section, provided similar teachings on adding, for example, a thin SiO_2 buffer in a CT stack to improve retention by reducing undesirable injection paths while preserving erase. Therefore, it would've been well known to a POSITA, or at least obvious to a POSITA, to insert an anti-tunneling oxide within the charge-trap region to suppress leakage/back-injection.

which disclosed Sandisk's first Multi-Level Cell (or MLC) flash memory concept. *See* https://futurememorystorage.com/assets/downloads/program/events-awards/lifetime-achievement-award/award-winner-2022.pdf (describing Dr. Harari's work at Sandisk and on MLC technology, including U.S. Patent No. 5,095,344).

However, it became clear to POSITAs in the early 2000s that traditional 2-D memory would hit a limit for miniaturization because the smaller memory cells became, the fewer electrons could be stored, and thus even small leakage of electrons could impact data stability. It was well known in the flash memory industry that at some point, 2-D memory would not be able to scale further, which would eventually limit flash memory's ability to compete in the marketplace with higher-density alternatives. As noted later by a prominent semiconductor industry blog, "everyone in the industry knew that there would come a point at which planar NAND could simply no longer be shrunk." *See, e.g.*, https://thememoryguy.com/why-do-we-need-3d-nand/.

The answer to the scaling "problem" came in 2007, with the invention of 3-D memory cells by Sandisk's longstanding (*i.e.*, over two decades) joint venture partner Toshiba (now Kioxia). *See* "Toshiba Develops New NAND Flash Technology", June 12, 2007 (https://www.global.toshiba/ww/news/corporate/2007/06/pr1201.html). The technology was called "BiCS" for Bit Cost Scaling. *See* Tanaka, H., et al., "Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory", June 14, 2007 (hereinafter, "Bit Cost Scalable Technology"). This new 3-D memory technology scaled the cost of memory without shrinking the length and the width of memory cells by essentially taking memory cells vertical in a so called "macaroni" structure. *See id.* ("In this paper, a novel SONOS flash memory using a newly devised Bit-Cost Scalable (BiCS) technology which realizes a multi-stacked array with a few constant number of critical lithography process steps, without area penalty and with continuous reduction of bit cost as shown as solid line in figure 2 is proposed"). While earlier alternative ideas for 3-D memory cells had been proposed, these concepts required extra lithography steps and control gates, adding to the cost. Indeed, Toshiba had been pursuing several alternative 3-D NAND technologies since at least 2003. *See* Endoh, T. et al., "Novel

Ultrahigh-Density Flash Memory With a Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell", (2003). Those early 3-D concepts, the research and development underlying them, and the learning from those efforts, evolved into the BiCS technology. Toshiba's invention of BiCS revolutionized flash memory, allowing much greater densities of memory in the same footprint, all at a low cost.

Conceptually, one variation of early BiCS technology took a 2-D NAND string, split it in half lengthwise, and turned it on its end to become a vertical string, essentially forming it into a U-shape. *See, e.g.,* https://thememoryguy.com/what-is-a-3d-nand/ (describing and illustrating, via animations, the BiCS 3-D NAND technology as essentially folding a 2-D NAND in half onto itself, forming what looks like a vertical sandwich).[8] Because this innovation takes a 2-D NAND layer structure and turns it on its side, the technical underpinnings of 2-D NAND, and decades of learnings, research, and innovations related to a 2-D planar memory structure, are equally applicable to 3-D NAND. Therefore, a POSITA would have readily understood that technology

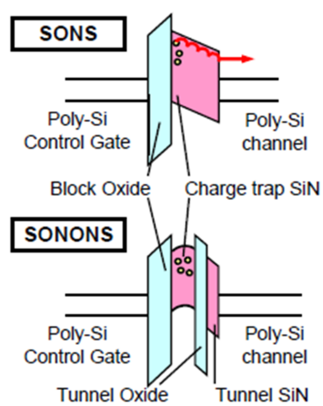


Fig.13 Schematic illustration of SONS and SONONS memory FET. Tunnel film in SONONS structure inhibits release of trapped charge in charge trap SiN and improves retention and disturbance characteristic.

[8] This early version of BiCS is sometimes called "U BiCS" (referring to the shape it creates) or "P BiCS", where the "P" means "Pipe" (referring to the channel connecting one half of the "U" to the other). Another early version of BiCS, sometimes called "I BiCS" or simply "BiCS," had an even simpler design. *See* Ishiduki, M.; Fukuzumi, Y.; Katsumata, R.; Kito, M.; Kido, M.; Tanaka, H.; Komori, Y.; Nagata, Y.; Fujiwara, T.; Maeda, T.; et al., "Optimal device structure for Pipe-shaped BiCS Flash memory for ultra high density storage device with excellent performance and reliability," In Proceedings of the 2009 IEEE International Conference on Electron Devices Meeting (IEDM), Baltimore, MD, USA, 7–9 December 2009; at 1–4 (describing P-BiCS and how it differs from the earlier non-U-shaped BiCS design). While the two early BiCS designs differed in certain respects (*e.g.*, the location of source and drain), the statements herein applied equally to both versions.

applicable and related to 2-D NAND, including the charge-trap technology used for 2-D memory structures, would also be readily applicable to 3-D NAND. Indeed, as early as 2009, Toshiba itself discussed using a multilayer SONONS structure in its BiCS charge trap, noting that the structure "improves retention and disturbance characteristics." Komori, Y. et al., "Disturbless Flash Memory due to High Boost Efficiency on BiCS Structure and Optimal Memory Film Stack for Ultra High Density Storage Device" (2009) ("Komori").

After the announcement of BiCS in 2007, Toshiba and Sandisk touted the new 3-D technology at well-known industry events (including trade shows) and in important industry papers that POSITAs would have been well aware of from 2007 to 2012. *See, e.g.*, Tanaka, H., et al., "Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory" (2007); Komori, Y. et al., "Disturbless Flash Memory due to High Boost Efficiency on BiCS Structure and Optimal Memory Film Stack for Ultra High Density Storage Device" (2008); Fukuzumi, Y., et al., "Optimal Integration and Characteristics of Vertical Array Devices for Ultra-High Density, Bit-Cost Scalable Flash Memory" (2007); Tanaka, H. et al., "Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory" (2007). Given that the data-storage density limits of 2-D NAND were already known to POSITAs in the early 2000s, a POSITA would have closely followed updates related to BiCS and 3-D NAND technology from 2007 to July 1, 2012. Indeed, the NAND Flash Memories Textbook, published in 2010, listed "BiCS" as one of the three 3-D NAND technologies that were already well-known at the time. *See* NAND Flash Memories Textbook at 126; Table 5.2 (reproduced below). Beyond BiCS, as shown in the table below, Samsung created the TCAT technology, a similar 3D NAND structure that incorporated a tungsten metal high work function gate. *See, e.g.*, Jang., J. et al., *Vertical Cell Array using TCAT (Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory*, VSLI Symposium (2009); Lee 255. Notably, as far back as 2009 the Jang paper highlighted the advantages of metal high work function gates in 3D NAND, noting their "faster erase speed, wider Vth margin, and better retention characteristics." Samsung and Sandisk have a longstanding cross-licensing agreement. *See* https://www.sec.gov/Archives/edgar/data/1000180/000119312509120383/dex991.htm.

Table 5.2. Summary of the most important characteristics of 3D vertical channel arrays

	BiCS [20]	VRAT [21]	TCAT [22]
Cell operation mode	Depletion	–	Enhancement
Gate all around	Yes	No	Yes
Gate/channel first	Gate first	Channel first	Channel first
Gate	p+ polysilicon	n+ polysilicon	Tungsten
Blocking/storage/tunnel	Oxide/nitride/oxide	Alumina/nitride/oxide	Oxide/nitride/oxide
Channel	n polysilicon	Polysilicon	p polysilicon

Toshiba's inventions related to 3-D BiCS memory revolutionized the industry, providing a path forward for more dense, cost-effective memory than could ever have been achieved before. And Sandisk engineers have worked hand-in-hand with Toshiba (now Kioxia) to continue developing and improving the original BiCS 3-D NAND technology first announced in 2007, as Sandisk and Toshiba jointly developed Flash memory technology through a joint venture for the past twenty years.

The Polishchuk patents–when compared to the earlier patents and applications within the same patent family–demonstrate the significance of Toshiba's invention regarding cost-effective 3-D flash memory. Prior to the July 1, 2012, continuation-in-part that became the '537 patent, the ***only*** disclosures in earlier applications within the same family of patents related to the rapidly aging 2-D flash memory structure and described only a two-layer charge trap layer. These more limited disclosures can be seen in, for example, U.S. Provisional Patent Application Ser. No. 60/940,160, filed May 25, 2007; U.S. Application Ser. No. 13/288,919, filed Nov. 3, 2011; and U.S. Application Ser. No. 12/152,518, filed on May 13, 2008, all of which are cited on the face of the Polishchuk patents as related applications.

Notably, the new matter introduced into the Polishchuk patents in the July 1, 2012, continuation-in-part added 3-D memory disclosures and specifically mentions "Bit-Cost Scalable or BiCS architecture" technology, even incorporating an image that appears almost identical to one from Toshiba's papers. *See, e.g.* '537 patent at 16:65–17:10; FIG. 8A. The new matter introduced to the Polishchuk patents on July 1, 2012, also includes the use of an "anti-tunneling layer," which as described below and in the attached claim charts, was not novel or inventive in

July 2012 either. In other words, it was not until July 1, 2012, nearly five years after the provisional patent application in the family was filed, that the Polishchuk patents first described 3-D flash memory, which Toshiba and Sandisk had already pioneered in the prior decade, and many other companies like Macronix, Samsung, and Micron were also already pursuing. In fact, the Polishchuk patents added disclosures related to not just the BiCS 3-D technology, but other already released 3-D memory technologies as well, including those pioneered by Macronix. Particularly relevant to these Invalidity Contentions, Macronix had already published a paper in 2010 showing a 3-D NAND structure with a multilayer ONONO structure. *See* Lue, H., et al., "A Highly Scalable 8-Layer 3D Vertical-Gate (VG) TFT NAND Flash Using Junction-Free Buried Channel BE-SONOS Device" (2010). That 2010 Macronix paper described and disclosed a structure similar to the one disclosed in the Polishchuk patents, as shown below. Notably, as shown below, this paper also described an ONONO stack, characterized as BE-SONOS.

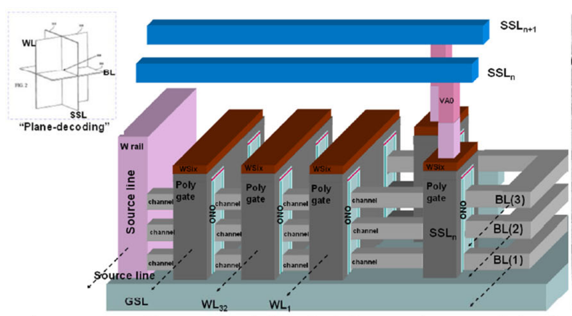


Fig. 1 3D array architectures of vertical-gate (VG) charge-trapping NAND Flash. Cell decoding is through the intercepts of WL, BL and SSL planes. The array layout resembles the conventional NAND, while the WL, BL are grouped into planes instead of lines. The array efficiency of the proposed structure is close to the conventional NAND. The poly-silicon channel is an n-type channel (buried-channel depletion mode) device so that n+ junction in between WL's is not necessary (junction-free NAND).

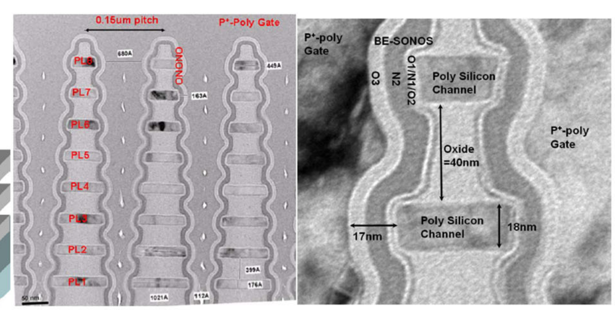
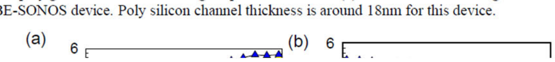
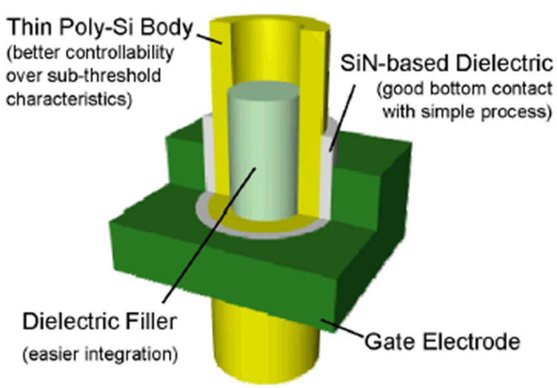
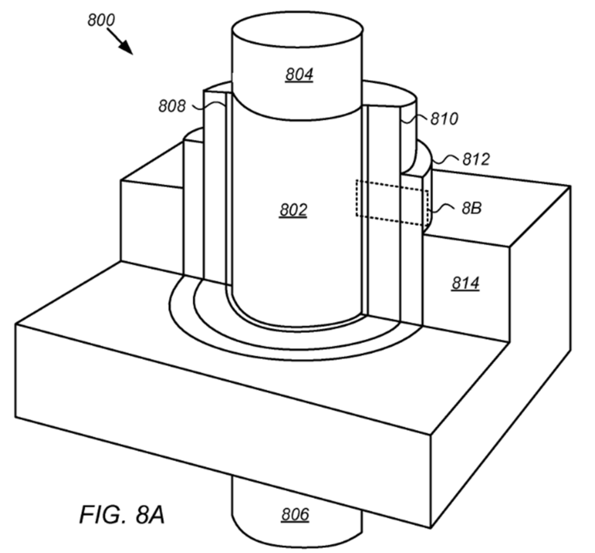


Fig. 2 (a) X-directional TEM cross-sectional view of the of 8-layer VG TFT BE-SONOS in a 75nm (half-pitch) technology. Gap filling of the multi-layer ONONO (BE-SONOS) and poly gate are excellent in a high aspect-ratio trench. (b) Each cell is a double-gate TFT BE-SONOS device. Poly silicon channel thickness is around 18nm for this device.



The Polishchuk patents, however, never credit Toshiba as the inventor of the Bit-Cost Scalable or BiCS architecture. As one example of how the Polishchuk patents appropriated Toshiba's 3-D Flash memory innovations, the Polishchuk patents simply describe "a Bit-Cost Scalable or BiCS architecture," '537 patent, 16:28–30, and explain that the "BiCS architecture reduces number [sic] of critical lithography steps compared to a simple stacking of layers, leading to a reduced cost per memory bit." *Id.*, 16:37–40. Of course, that is exactly what Toshiba described more than five years earlier when it invented this technology. *See, e.g.* Bit Cost Scalable Technology ("Bit density can be increased by adding more gate plates, while the number of the critical lithography steps remains constant because whole stack of control gates is punched with only one lithography step" and noting in Table 1 that BiCS lowers cost due to small number of lithography steps). Nowhere is Toshiba mentioned in this portion of the specification, or anywhere else in the specification, as the inventor of the BiCS 3-D NAND technology.

The Polishchuk patents also copy without attribution Toshiba's 2007 graphic demonstrating Toshiba's 3-D BiCS innovation, reproducing the graphic as FIG. 8A in the patents, shown in the side-by-side comparison below:

 Figure 10: Concept of 'Macaroni' Body Vertical FET.	 FIG. 8A
Fukuzimi, Y., et al., "Optimal Integration and Characteristics of Vertical Array Devices for Ultra-High Density, Bit-Cost Scalable Flash Memory", December 2007	Fig. 8A, Polishchuk patents, first included July 1, 2012.

While the Polishchuk patents do not mention Toshiba's contributions anywhere in their specifications, the use of the "BiCS" terminology (which is a registered trademark of Kioxia Corporation, U.S. Reg. No. 5718983) and the copied image (FIG. 8A) confirms that the inventors of the Polishchuk patents knew of, and copied, the revolutionary inventions made by Sandisk's joint venture partner Toshiba (now called Kioxia) into the applications that matured into the '537, '240, and '365 patents. The Polishchuk inventors saw Toshiba's 3-D NAND innovations and appropriated them into their earlier "inventions" without attribution.

In short, the Polishchuk patent inventors did not invent 3-D flash memory, which is the key technology that enables flash memory to compete in the modern marketplace. Instead, the Polishchuk patent inventors blatantly appropriated the inventions of Toshiba more than five years after Toshiba first announced its revolutionary technology and combined them with the already-known multi-layer charge trap layout.

As described above, the 3-D BiCS orientation (as well as other 3-D memory structures demonstrated by, for example, Macronix, Samsung, and Micron), would have been known to a POSITA since at least sometime in 2007, and well before the July 1, 2012 priority date, which is when the Toshiba/Kioxia/Sandisk 3-D Flash memory technology was integrated into the Polishchuk patents without attribution. Further, the oxygen-rich / -lean charge trap layers described by the Polishchuk patents were already known to a POSITA well before the July 1, 2012, priority date.[9]

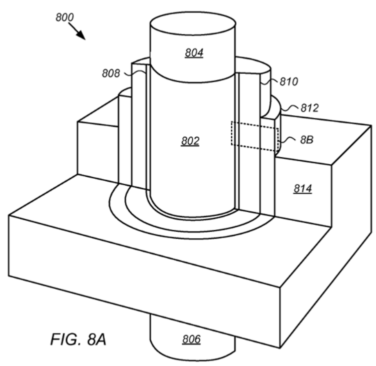
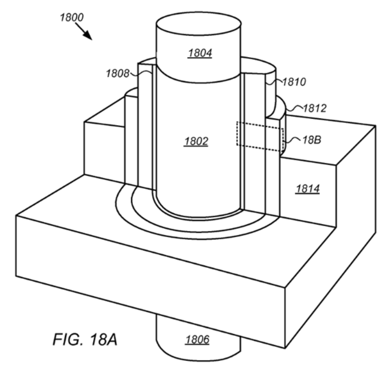
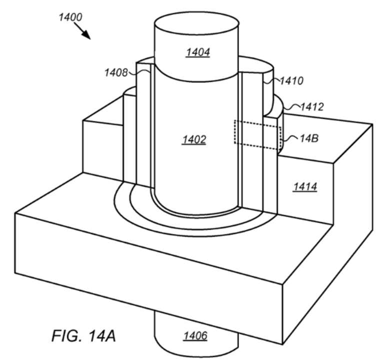
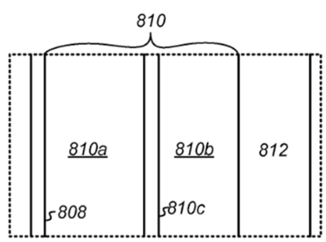
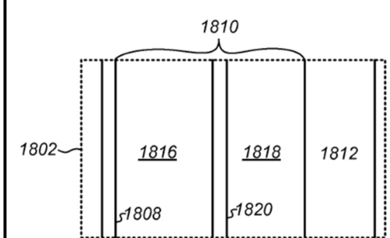
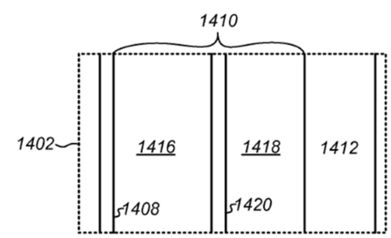
Additional claim elements like a high work function gate electrode, a high-K dielectric blocking layer, a high temperature oxide blocking layer, a MOS logic transistor with a high work function gate with similar materials that was employed on the substrate, and various aspects of the 3-D "macaroni" structure were already well known to a POSITA before July 1, 2012. Most of these claim elements were common parts of both 2-D and 3-D NAND at the time of the supposed invention of the Polishchuk patents, and the 3-D elements were already well known based on disclosures by Toshiba / Kioxia / Sandisk and other companies investigating 3-D NAND technology, like Sandisk, Macronix, Micron, and others. A POSITA would have understood that each of these limitations were simply one of a small number of common options that a POSITA would already have known could be advantageously employed when creating both 2-D and 3-D memory. For example, all NAND devices require additional logic, and thus a POSITA would find it obvious to include the claimed MOS logic gates, as well as the lower select gates created

[9] Moreover, as described below, the original assignee of the Polishchuk patents had also previously described the identical technology in other, earlier, patent applications with different inventors. Thus, even beyond the obvious combination of known methods and techniques to yield a result, the supposed inventions described in the Polishchuk patents had been previously disclosed in their entirety, rendering them invalid.

by the BiCS process, which IPValue asserts meets this claim limitation. Similarly, a POSITA would have known that a high-K blocking layer and high work function gate electrode were useful for retention, erase windows, and other benefits. For example, Samsung's TCAT 3-D NAND structure included both of these elements as early as 2009. *See, e.g.* Polishchuk patent claim charts, Ex. 1 ("Lee 255"). Features like high work function gate electrodes and high-K blocking layers were common alternatives that a POSITA would know could be advantageously used to improve retention and erasure, among other benefits. Similarly, various 3-D NAND features described in the Polishchuk patents were already well within a POSITA's understanding before July 1, 2012, given the disclosures of Samsung, Toshiba / Kioxia / Sandisk, and others. These features would be well-understood by a POSITA and could be employed without undue experimentation.

Finally, Cypress, the previous owner of the Polischuk patents, described the purported inventions of the Polishchuk patents in previous patents with at least one different inventor filed before July 1, 2012. For example, in U.S. Patent No. 8,710,578 ("Jenne"), filed March 27, 2012, and U.S. Patent No. 9,102,522 ("Ramkumar"), filed March 29, 2012, Cypress disclosed all material elements of the claims asserted against Sandisk. The inventors of Jenne are Frederik Jenne and Krishnaswamy Ramkumar, which includes only one of the three inventors of the Polishchuk patents and additionally includes Jenne. The inventors of Ramkumar are Ramkumar, Bo Jin, and Fredrick Jenne, which again includes only one of the three inventors of the Polishchuk patents, and additionally includes Jenne and Jin. Each of these patents were disclosed before the critical date of the Polishchuk patents, and therefore invalidating prior art. They disclose all elements of the Polishchuk patents, including the key multi-layer charge trap layer, a lower oxygen-rich charge trap layer coupled with an oxygen-lean upper charge trap layer, the same multi-layer charge trap region with an intermediate anti-tunneling layer made of an oxide, the 3-D "macaroni" channel originally described by Toshiba / Kioxia with its revolutionary BiCS products (including the annular shape of the channel), and described high work function gates, high-K / high temperature oxide (HTO) blocking layers, separate MOS logic device/transistor on the substrate using similar materials, and additional elements claimed by the Polishchuk patents.

See Polishchuk patent claim charts, Exs. 8, 10. The Jenne and Ramkumar patents also incorporate the same images as the Polishchuk patents, including images identical to Figs. 8a and 8b of the Polishchuk patents, as well as Figs. 9a–f and 10a–f.

Polishchuk Patents	Jenne (prior art)	Ramkumar (prior art)
 FIG. 8A	 FIG. 18A	 FIG. 14A
 FIG. 8B	 FIG. 18B	 FIG. 14B

3. Anticipation

Sandisk contends that each prior art reference listed below anticipates one or more claims of the Polishchuk patents under at least 35 U.S.C. §§ 102(a), (b), (e), and/or (g), as described further below.

Table #3
Anticipatory Reference for Polishchuk Patents
Jenne
Ramkumar
Lee 961

4. Obviousness

Sandisk contends that the additional prior art references identified below can be combined to render these claims invalid as obvious.

Sandisk provides the following legal background regarding obviousness combinations. No showing of a specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts, as each combination of art would have yielded expected results and at most would simply represent a known alternative to one of skill in the art. *See Apple Inc. v. LG Elecs. Co*., 839 F.3d 1034, 1058 (Fed. Cir. 2016); *Intercontinental Great Brands LLC v. Kellogg N. Am. Co.*, 869 F.3d 1336, 1344 (Fed. Cir. 2017); *KSR Int'l Co. v. Teleflex, Inc*., 127 S. Ct. 1727, 1739–40 (2007) (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, and instead applying an "expansive and flexible" approach). Indeed, the Supreme Court held that a POSITA is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR*, 127 S.Ct. at 1742. Nevertheless, in addition to the information contained in the section immediately above and elsewhere in these contentions, Sandisk hereby identifies motivations and reasons to combine.

One or more combinations of the prior art references identified below would have been obvious because these references would have been combined using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. *See Apple*, 839 F.3d at 1077; *Intercontinental Great Brands*, 869 F.3d at 1344. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. *See ACCO Brands Corp. v. Fellowes, Inc*., 813 F.3d 1361, 1367 (Fed. Cir. 2016); *Sanofi-Aventis Deutschland GmbH v. Glenmark Pharms. Inc*., USA, 748 F.3d 1354, 1360 (Fed. Cir. 2014);

Bayer Pharma AG v. Watson Labs., Inc., 874 F.3d 1316, 1329 (Fed. Cir. 2017); *KSR*, 127 S. Ct. at 1742. Further, the combinations of the prior art references identified above and in the claim charts would have been obvious because the combinations represent known potential options with a reasonable expectation of success. *See InTouch Techs., Inc. v. VGO Comms., Inc*., 751 F.3d 1327, 1347 (Fed. Cir. 2014).

Additional evidence that there would have been a motivation to combine the prior art references identified above includes the interrelated teachings of multiple prior art references; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the Asserted Claims of the Polishchuk patents; the existence of a known need or problem in the field of the endeavor at the time of the alleged inventions; and the background knowledge that would have been possessed by a POSITA. *See Arctic Cat Inc. v. Bombardier Recreational Prods. Inc*., 876 F.3d 1350, 1359 (Fed. Cir. 2017); *Intercontinental Great Brands*, 869 F.3d at 1344; *Unwired Planet, LLC v. Google Inc*., 841 F.3d 995, 1003 (Fed. Cir. 2016); *Norgren Inc. v. Int'l Trade Comm'n*, 699 F.3d 1317, 1322–23 (Fed. Cir. 2012).

The motivation to combine the teachings of the prior art references disclosed herein is also found in the references themselves and in: (1) the nature of the problem being solved; (2) the express, implied and inherent teachings of the prior art; (3) the knowledge of POSITAs; (4) the predictable results obtained in combining the different elements of the prior art; (5) the predictable results obtained in simple substitution of one known element for another; (6) the use of a known technique to improve similar devices, methods, or products in the same way; (7) the predictable results obtained in applying a known technique to a known device, method, or product ready for improvement; (8) the finite number of identified predictable solutions that had a reasonable expectation of success; and (9) known work in various technological fields that could be applied to the same or different technological fields based on design incentives or other market forces.

a. The '537 Patent

Sandisk contends that the Asserted Claims of the '537 Patent are invalid as anticipated under 35 U.S.C. § 102. Sandisk further contends that the Asserted Claims are invalid as obvious under 35 U.S.C. § 103. The individual exhibits show how the combinations render the ’537 patent invalid as obvious.

Table #4			
Prior Art Charted References and Combination Identification ’537 Patent			
Reference Name	**Reference**	**Claim Chart(s)**	**Exemplary Obviousness Combinations**
Lee 255	Number US 2012/0068255	Exhibit No. 537-1	In combination with one or more of at least the following: Fujiwara, Ganguly, Hwang, Cypress products, Lee 961, Mahajani, Uenishi, Wang
Fujiwara	US 2006/0065910 A1	Exhibit No. 537-2	In combination with at least Lee 255 and / or Lee 961 and / or Hwang.
Ganguly	US 2011/0281429 A1	Exhibit No. 537-3	In combination with at least Lee 255 and / or Lee 961 and / or Hwang.
Hwang	US 2012/0061744 A1	Exhibit No. 537-4	In combination with at least Lee 255 and / or Lee 961, and additionally in combination with Fujiwara, Ganguly, Cypress products, Lee 961, Mahajani, Uenishi, Wang.
Lee 961	KR 10-2011-0119061	Exhibit No. 537-5	In combination with one or more of at least the following: Fujiwara, Ganguly, Hwang, Cypress products, Lee 255, Mahajani, Uenishi, Wang

Mahajani	US 2005/0062098 A1	Exhibit No. 537-6	In combination with at least Lee 255 and / or Lee 961 and / or Hwang.
Cypress products	As embodied by US 8,222,688	Exhibit No. 537-7	In combination with at least Lee 255 and / or Lee 961 and / or Hwang.
Ramkumar	US 9102522	Exhibit No. 537-8	Anticipates
Uenishi	US 2010/207192A	Exhibit No. 537-9	In combination with at least Lee 255 and / or Lee 961 and / or Hwang.
Jenne	US 8710578	Exhibit No. 537-10	Anticipates
Wang	US 2009/0057752	Exhibit No. 537-11	In combination with at least Lee 255 and / or Lee 961 and / or Hwang.

i. Patent Prosecution

The ’537 patent was filed by Igor Polishchuk, Sagy Charel Levy, and Krishnaswamy Ramkumar as U.S. Patent Application No. 13/539,466 on July 1, 2012. The original application included application claims 1–20.

The Examiner allowed pending claims 11–20 without comment. The examiner rejected claims 1,3 and 4 as being unpatentable over Levy *et al.*, US 2009/0179253, in view of Zheng *et al.*, US 6,912,163 and in view of Yan, US2008/0135946.

Applicants responded by amending the claims, though the applicant did not amend original claim 18 (which became claim 17). The Examiner never analyzed or discussed 3-D NAND prior art related to claim 18, even though at the time the application was filed, a POSITA would have been well aware of numerous 3-D NAND applications, including Toshiba’s BiCS.

After the Notice of Allowance, Applicant submitted an Information Disclosure Statement that included 100 additional references. While the document states that the Examiner considered every reference unless lined through, the IDS was submitted ***after*** the Notice of Allowance and there is no indication that the Examiner specifically considered Fujiwara or any other reference submitted in the IDS, as these references were all submitted ***after*** the Examiner's notice of allowance.

In 2018, the Patent Owner requested a Certificate of Correction related to a purported error where the Patent Owner cited "Figs. 20A–F" and asked the Patent Office to correct that to "Figs. 18A–F." The Patent Office granted the request and issued the Certificate of Correction.

ii. Motivation to Combine

Sandisk further sets forth below exemplary combinations of references that Sandisk contends render the Asserted Claims invalid as obvious. This disclosure is based on Sandisk's present understanding of the Asserted Claims and the apparent constructions that Sandisk believes IPValue may be asserting based on its infringement contentions. Each of the below exemplary combinations should be understood to include and incorporate the background knowledge of a person of ordinary skill in the art, such as (but not limited to) the background information detailed in the above State of the Art section of this pleading. In addition, each of the below exemplary combinations should also be understood to encompass any subset (*i.e.*, less than all) of the references identified in the combination, whether or not the particular subset is specifically identified below.[10]

Sandisk also specifically incorporates by reference the IPR petitions filed for the '240 and '365 patents, which Sandisk has produced and served on IPValue with the accompanying document production (see '240 IPR Petition (SD_IPV_00013268-13370); '240 IPR Exs. (SD_IPV_00003861-13267); '365 IPR Petition (SD_IPV_00013371-13484); '365 IPR Exs. (SD_IPV_00013485-19713)), including the motivations to combine and expectations of success regarding those combinations for the various prior-art references discussed therein. *See* '240 IPR (Case No. IPR2025-01283); '365 IPR (Case No. IPR2025-01281). While Sandisk did not file an

[10] As a non-limiting example, a particular reference identified in a given combination may be necessary for that combination to render obvious some Asserted Claims but not others, in which case Counterclaim-Defendants may, depending on the Asserted Claim, assert invalidity due to obviousness based on the combination with and without that particular reference.

IPR petition for the ’537 patent, the Polishchuk patents share a common specification, and therefore, the motivations to combine and expectations of success discussed in the IPRs (which include the declarations filed in support thereof) apply equally to the ’537 patent and the combinations discussed herein.

(a) Primary References: Lee 255, Lee 961, Hwang

Lee 255, Lee 961, and Hwang each disclose and teach a 3-D non-volatile semiconductor memory device and methods of fabricating the same. One of ordinary skill in the art would have been motivated to combine Lee 255, Lee 961, and Hwang with each other and any other reference(s) in Table 4, as all references are analogous art to the ’537 patent because they teach improvements to non-volatile memory devices generally, and charge trap memory devices specifically. For example, one of ordinary skill in the art would have been motivated to combine Lee 255, Lee 961, and Hwang with at least the following references, and would have had a reasonable expectation of success in doing so:

(i) Lee 255 or Lee 961 or Hwang + any of Fujiwara, Ganguly, Cypress products, Lee 961, Mahajani, Uenishi, Wang.

A skilled artisan would have been motivated to combine any of the above references with Lee 255 and/or Lee 961 and/or Hwang and would have found it straightforward and obvious to do so, at least because it would amount to no more than combining prior art elements according to known methods to yield predictable results, simple substitution of one known element for another to obtain predictable results, using known technique to improve similar devices (methods, or products) in the same way, applying a known technique to a known device (method, or product) ready for improvement to yield predictable results, an “obvious to try” option—*i.e.*, choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success, and/or using known work in one field of endeavor that prompts variations of it for use in either the same field or a different one based on design incentives or other market forces.

For example, each of the above references are directed to the same field, which here is non-volatile semiconductor memory. As described above, a POSITA would know that any charge trap technology available regarding 2-D SONOS memory would be equally applicable to

3-D SONOS memory. Moreover, the references are all aimed at addressing the same or similar problem – ensuring charge trap retention. Thus, each reference presents at minimum an obvious to try variation of a finite number of predictable solutions, such as applying the charge trap layers from 2-D NAND in the 3-D NAND. A POSITA would also have been well aware of the move toward high work function gate electrodes, high-temperature dielectrics, and the need for logic devices that were made of similar materials.

As a specific example, and without limitation, a POSITA would have been motivated to combine Lee 255 and/or Lee 961 and/or Hwang with one or more of Fujiwara, Ganguly, Cypress products, Lee 961, Mahajani, Uenishi, Wang. Each of these references relates to SONOS charge trapping-type nonvolatile memory devices. A POSITA would have been motivated to modify the nitride charge trapping layer of Lee ’255 and Hwang to incorporate the multilayered charge trap layer configurations and oxygen-rich / -lean layers disclosed in these references. Further, a POSITA would have been motivated to modify the multilayer charge trapping layer of Lee 961 to incorporate the oxygen-rich / -lean layers disclosed in these references. Each of these references describes purported advantages for multiple charge trap layers and the oxygen-rich / -lean configuration of the charge trap layers.

For example, Fujiwara, Ganguly, Uenishi, Wang, Cypress products, and Mahajani describe advantages of incorporating multiple charge trap layers, including oxygen-rich layers by the tunneling layer and oxygen-lean layers by the blocking layer, in order to improve the film quality and promote charge retention. Specifically, these references teach that more charge will be stored deeper in the oxygen-lean region, helping prevent migration of electrons. It would have been obvious for a POSITA to consult the teachings of Fujiwara, Ganguly, Uenishi, Wang, Cypress products, and Mahajani in seeking to improve the memory transistor configuration of Lee 255 and/or Lee 961 and/or Hwang because they are also directed to improving the configuration of SONOS-type charge trapping memory transistors such as those taught in Lee 255, Lee 961 and Hwang. Thus, a POSITA would have been motivated to modify the nitride charge trapping layer of Lee 255 and Hwang to incorporate the two-level charge trap layers and oxygen-rich / -lean layers described in Fujiwara, Ganguly, Uenishi, Wang, Cypress products, and

Mahajani because it would, as described by the patentee, improve the charge storage capability of Lee 255 and Hwang. Further, a POSITA would have been motivated to modify the multi-layer charge trapping layer of Lee 961 to incorporate oxygen-rich / -lean layers described in Fujiwara, Ganguly, Uenishi, Wang, Cypress products, and Mahajani because it would purportedly improve the charge storage capability of Lee 961. A POSITA would have understood that the combination of these references with Lee 255 and/or Lee 961 and/or Hwang amounts to applying their teaching for their intended purposes of improving similar devices in the same ways. Further, the purported benefit of using an oxygen-rich bottom nitride layer and an oxygen-lean top nitride layer in a SONOS memory transistor would have been predictable to a POSITA prior to July 2012. As described in Section III.A.2, many other prior art references show that it was a routine design choice to use an oxygen-rich first nitride layer and an oxygen-lean second nitride layer to obtain improved charge retention characteristics. A POSITA would also expect success in applying these teachings because the underlying materials, equipment, and process knobs were mainstream.

Similarly, a POSITA would have been motivated to combine Lee 255 and/or Hwang with Lee 961 and / or Mahajani regarding creating an anti-tunneling layer in the multilayer charge trap region. Both describe advantages to using a thin SiO anti-tunneling layer to further assist in improving charge retention, and a POSITA would have been motivated to combine the references and would expect to find success as described above. It would simply be a routine design choice for a POSITA to employ a SONONOS configuration as compared to a SONNOS configuration, and a POSITA would have expected success in creating either. A POSITA would also have recognized the benefit of an anti-tunneling layer in additionally preventing charge migration.

(ii) Lee 255 and / or Lee 961 + Hwang + any of Fujiwara, Ganguly, Cypress products, Lee 961, Mahajani, Uenishi, Wang.

A skilled artisan would have been motivated to combine Hwang and any of the above references with Lee 255 and / or Lee 961 and would have found it straightforward and obvious to do so, at least because it would amount to no more than combining prior art elements according to known methods to yield predictable results, simple substitution of one known element for another to obtain predictable results, using known technique to improve similar devices (methods, or products) in the same way, applying a known technique to a known device (method, or product) ready for improvement to yield predictable results, an "obvious to try" option—*i.e.*, choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success, and/or using known work in one field of endeavor that prompts variations of it for use in either the same field or a different one based on design incentives or other market forces.

For example, each of the above references are directed to the same field, which here is non-volatile semiconductor memory. As described above, a POSITA would know that any charge trap technology available regarding 2-D SONOS memory would be equally applicable to 3-D SONOS memory. Moreover, the references are all aimed at addressing the same or similar problem – ensuring charge trap retention. Thus, each reference presents at minimum an obvious to try variation of a finite number of predictable solutions, such as applying the charge trap layers from 2-D NAND in the 3-D NAND. A POSITA would also have been well aware of the move toward high work function gate electrodes, high-temperature dielectrics, and the need for logic devices that were made of similar materials.

As a specific example, and without limitation, a POSITA would have been motivated to combine Lee 255 or Lee 961 with Hwang. Hwang relates to SONOS charge trapping-type nonvolatile memory devices. It also teaches three dimensional SONOS-style memory. A POSITA would have understood that the memory devices of Lee '255 and Lee 961 (and any of the charge trap memory devices in the above-cited prior art) would have been connected to MOS logic transistors in the peripheral regions of their respective devices to control their operation. Hwang expressly teaches such device electrical connections to MOS logic transistors in its peripheral circuit, along with a specific "step structure" approach, that it states provides simplified fabrication and improved reliability and integration. A POSITA also would have expected success in applying the teachings of Hwang to further modify the combination of Lee '255 or Lee 961 with the other art discussed below. Incorporating Hwang's explicit teaching into Lee '255 or Lee 961 would have been a routine design choice for a POSITA, providing improved clarity and reliability of the connection scheme without requiring new materials, new processes, or unconventional circuitry. Employing the electrical connection strategies and peripheral MOS transistor teachings of Hwang to the 3D device of Lee 255 or Lee 961 combined with the other references discussed below would therefore enable the combined device to function and provide the benefits taught by Hwang. A POSITA would have understood that this combination amounts to applying the teachings of Hwang for their intended purpose to improve similar devices in the same way.

Further, a POSITA would have been motivated to combine Lee 255 + Hwang or Lee 961 + Hwang with one or more of Fujiwara, Ganguly, Cypress products, Mahajani, Uenishi, Wang. Each of these references relates to SONOS charge trapping-type nonvolatile memory devices. A POSITA would have been motivated to modify the nitride charge trapping layer of Lee ’255 to incorporate the multilayered charge trap layer configurations disclosed in these references. Each of these references describes advantages for multiple charge trap layers.

For example, Fujiwara, Ganguly, Uenishi, Wang, Cypress products, and Mahajani describe advantages of incorporating multiple charge trap layers, including oxygen-rich layers by the tunneling layer and oxygen-lean layers by the blocking layer, in order to improve the film quality and promote charge retention. Specifically, these references teach that more charge will be stored deeper in the oxygen-lean region, helping prevent migration of electrons. It would have been obvious for a POSITA to consult the teachings of Fujiwara, Ganguly, Uenishi, Wang, Cypress products, and Mahajani in seeking to improve the memory transistor configuration of Lee 255 and Lee 961 because they are also directed to improving the configuration of SONOS-type charge trapping memory transistors such as those taught in Lee 255 and Lee 961. Thus, a POSITA would have been motivated to modify the nitride charge trapping layer of Lee 255 to incorporate the two-level charge trap layers described in Fujiwara, Ganguly, Uenishi, Wang, Cypress products, and Mahajani because it would improve the charge storage capability of Lee 255. Further, a POSITA would have been motivated to modify the multi-layer charge trapping layer of Lee 961 to incorporate oxygen-rich / -lean layers described in Fujiwara, Ganguly, Uenishi, Wang, Cypress products, and Mahajani because it would purportedly improve the charge storage capability of Lee 961. A POSITA would have understood that the combination of these references with Lee 255 or Lee 961 amounts to applying their teaching for their intended purposes of improving similar devices in the same ways. Further, the purported benefit of using an oxygen-rich bottom nitride layer and an oxygen-lean top nitride layer in a SONOS memory transistor would have been predictable to a POSITA prior to July 2012. As described in Section III.A.2, many other prior art references show that it was a routine design choice to use an oxygen-rich first nitride layer and an oxygen-lean second nitride layer to obtain improved charge retention characteristics in both SONNOS and SONONOS configurations. A POSITA would also expect success in applying these teachings because the underlying materials, equipment, and process knobs were mainstream.

Similarly, a POSITA would have been motivated to combine Lee 255 + Hwang with Lee 961 and / or Mahajani regarding creating an anti-tunneling layer in the multilayer charge trap region. Both describe advantages to using a thin SiO anti-tunneling layer to further assist in improving charge retention, and a POSITA would have been motivated to combine the references and would expect to find success as described above. It would simply be a routine design choice for a POSITA to employ a SONONOS configuration as compared to a SONNOS configuration, and a POSITA would have expected success in creating either. A POSITA would also have recognized the benefit of an anti-tunneling layer in additionally preventing charge migration.

Each of the listed combinations satisfy the elements of the asserted claims, and Sandisk reserves the right to supplement, amend, or refine its contentions, including its combinations and motivations to combine, in light of further discovery, expert analysis, developments in the record, or claim construction.

b. The ’240 Patent

Sandisk contends that the Asserted Claims of the ’240 Patent are invalid as anticipated under 35 U.S.C. § 102. Sandisk further contends that the Asserted Claims are invalid as obvious under 35 U.S.C. § 103. The individual exhibits show how the combinations render the ’240 patent invalid as obvious.

Sandisk further sets forth below exemplary combinations of references that Sandisk contends render the Asserted Claims invalid as obvious. This disclosure is based on Sandisk’s present understanding of the Asserted Claims and the apparent constructions that Sandisk believes IPValue may be asserting based on its infringement contentions. Each of the below exemplary combinations should be understood to include and incorporate the background knowledge of a person of ordinary skill in the art, such as (but not limited to) the background information detailed in the above State of the Art section of this pleading. In addition, each of the below exemplary combinations should also be understood to encompass any subset (*i.e.*, less than all) of the references identified in the combination, whether or not the particular subset is specifically identified below.[11]

Table #5			
Prior Art Charted References and Combination Identification ’240 Patent			
Reference Name	**Reference**	**Claim Chart(s)**	**Exemplary Obviousness Combinations**
Lee 255	Number US 2012/0068255	Exhibit No. 240-1	In combination with one or more of at least the following: Fujiwara, Ganguly, Hwang, Cypress products, Lee 961, Mahajani, Uenishi, Wang
Fujiwara	US 2006/0065910 A1	Exhibit No. 240-2	In combination with at least Lee 255 and / or Lee 961 and / or Hwang.
Ganguly	US 2011/0281429 A1	Exhibit No. 240-3	In combination with at least Lee 255 and / or Lee 961 and / or Hwang.
Hwang	US 2012/0061744	Exhibit No. 240-4	In combination with

[11] As a non-limiting example, a particular reference identified in a given combination may be necessary for that combination to render obvious some Asserted Claims but not others, in which case Defendants may, depending on the Asserted Claim, assert invalidity due to obviousness based on the combination with and without that particular reference.

	A1		at least Lee 255 and / or Lee 961, and additionally in combination with Fujiwara, Ganguly, Cypress products, Lee 961, Mahajani, Uenishi, Wang.
Lee 961	KR 10-2011-0119061	Exhibit No. 240-5	In combination with one or more of at least the following: Fujiwara, Ganguly, Hwang, Cypress products, Lee 255, Mahajani, Uenishi, Wang.
Mahajani	US 2005/0062098 A1	Exhibit No. 240-6	In combination with at least Lee 255 and / or Lee 961 and / or Hwang.
Cypress products	US 8222688	Exhibit No. 240-7	In combination with at least Lee 255 and / or Lee 961 and / or Hwang.
Ramkumar	US 9102522	Exhibit No. 240-8	Anticipates
Uenishi	US 2010/207192A	Exhibit No. 240-9	In combination with at least Lee 255 and / or Lee 961 and / or Hwang.
Jenne	US 8710578	Exhibit No. 240-10	Anticipates
Wang	US 2009/0057752	Exhibit No. 240-11	In combination with at least Lee 255 and / or Lee 961 and / or Hwang.

i. Patent Prosecution

The ’240 patent was filed by Igor Polishchuk, Sagy Charel Levy, and Krishnaswamy Ramkumar as U.S. Patent Application No. 15/335,180 on October 26, 2016. The original application included application claims 1–20, but Applicants subsequently filed a preliminary amendment replacing those claims with application claims 21–40.

Applicants submitted information disclosure statements during prosecution listing large numbers of prior art references (more than 500 references in total).

After the preliminary amendment, Applicants advanced three independent claims: 21, 33, and 38 (corresponding to issued claims 1, 12, and 16 after substantive amendment). Each independent claim, as filed, recites the basic features of a SONOS memory device, such as a channel, blocking dielectric layer, tunnel dielectric layer, and gate, along with a "multi-layer charge trapping layer compris[ing] a first dielectric layer disposed abutting a second dielectric layer, wherein the first dielectric layer includes oxygen-rich nitride, and the second dielectric layer includes oxygen-lean nitride." '240 patent at 21:13–17. Claims 33 and 38 additionally require that the gate is "high work function" and the presence in the memory device of a MOS logic device and claim 38 adds requirements that certain layers "abut" one another. Various dependent claims were also advanced, including some specifying that the channels were vertical and some specifying the presence of an anti-tunneling layer.

The Examiner rejected each of the independent claims, and many of the dependent claims, in view of several prior art references teaching SONOS memory devices with horizontal channels. Although SONOS devices with vertical channels were prior art to the '240 patent, the Examiner did not apply those references and found the dependent claims reciting vertical channels (25, 34, 36, and 39) to be allowable.

The Examiner rejected independent application claims 21, 33, and 38, based on various combinations of: (i) the (horizontal) multi-layer charge trapping region teachings of Kim '424, Wang '586, and Lue '625; (ii) the high work function gate electrode teachings of Kim '424, Lue '625, and Hagemeyer; and (ii) the MOS logic device teachings of Hagemeyer.

In response, Applicants did not dispute the unpatentability of the independent claims as filed. Rather, Applicants amended each of the independent claims. Regarding application claims 33 and 38, Applicants amended these claims to include the vertical channel limitations.

As for application claim 21, Applicants: (i) amended it to include the "anti-tunneling layer" originally recited in application claim 27; and (ii) argued for its patentability over Lue '625, which was the only reference applied by the Examiner against claim 27. But Applicants did not argue that Lue '625 does not teach an "anti-tunneling layer." Rather, Applicants argued that Lue '625 does not disclose the claimed "multi-layer charge storage layer" as a whole because Lue '625 explicitly teaches that dielectric layer 132—which would be analogous to the top oxygen-lean nitride for storing charges in the '240 patent—does not trap charges.

On October 4, 2017, the Examiner issued a Notice of Allowability for application claims 21–40. In the Statement of Reasons for Allowance for application claim 21 (issued claim 1), the Examiner stated that Kim '424, Wang '586, and Lue '625 "disclose[] all limitations of claim 21 except for . . . 'an anti-tunneling layer disposed between the first and second dielectric layers, wherein the anti-tunneling layer includes an oxide layer." For application claim 33 (issued claim 12), the Examiner stated that Hagemeyer and Wang '586 disclose everything except for that "the channel is vertical and oriented substantially perpendicular to a semiconductor material structure, and a tunnel dielectric layer, a multi-layer charge trapping layer, and a blocking dielectric layer are disposed between the gate structure and the channel." For application claim 38 (issued claim 16), the Examiner stated that Hagemeyer and Kim '424 disclose everything except for that "the channel is vertical and oriented substantially perpendicular to a semiconductor material structure; and a metal oxide semiconductor (MOS) logic device including a gate oxide layer, and a second high work function gate electrode disposed thereon."

ii. Motivation to Combine

Sandisk further sets forth below exemplary combinations of references that Sandisk contends render the Asserted Claims invalid as obvious. This disclosure is based on Sandisk's present understanding of the Asserted Claims and the apparent constructions that Sandisk believes IPValue may be asserting based on its infringement contentions. Each of the below exemplary combinations should be understood to include and incorporate the background knowledge of a person of ordinary skill in the art, such as (but not limited to) the background information detailed in the above State of the Art section of this pleading. In addition, each of the below exemplary combinations should also be understood to encompass any subset (*i.e.*, less than all) of the references identified in the combination, whether or not the particular subset is specifically identified below.[12]

Sandisk also specifically incorporates by reference the IPR petitions filed for the ’240 and ’365 patents, produced and served on IPValue herewith, including the motivations to combine and expectations of success regarding those combinations for the various prior-art references discussed therein. *See* ’240 IPR (Case No. IPR2025-01283); ’365 IPR (Case No. IPR2025-01281). The Polishchuk patents share a common specification, and therefore the motivations to combine and expectations of success discussed in both IPRs (which include the declarations filed in support thereof) apply to the ’240 patent and the combinations discussed herein.

(a) Primary References: Lee 255, Lee 961, Hwang

Lee 255, Lee 961, and Hwang each disclose and teach a 3-D non-volatile semiconductor memory device and methods of fabricating the same. One of ordinary skill in the art would have been motivated to combine Lee 255, Lee 961, and Hwang with each other and any other reference(s) in Table 5, as all references are analogous art to the ’240 patent because they teach improvements to non-volatile memory devices generally, and charge trap memory devices specifically. For example, one of ordinary skill in the art would have been motivated to combine Lee 255, Lee 961, and Hwang with at least the following references, and would have had a reasonable expectation of success in doing so:

(i) Lee 255 or Lee 961 or Hwang + any of Fujiwara, Ganguly, Cypress products, Lee 961, Mahajani, Uenishi, Wang.

A skilled artisan would have been motivated to combine any of the above references with Lee 255 and/or Lee 961 and/or Hwang and would have found it straightforward and obvious to do so, at least because it would amount to no more than combining prior art elements according to known methods to yield predictable results, simple substitution of one known element for another

[12] As a non-limiting example, a particular reference identified in a given combination may be necessary for that combination to render obvious some Asserted Claims but not others, in which case Counterclaim-Defendants may, depending on the Asserted Claim, assert invalidity due to obviousness based on the combination with and without that particular reference.

to obtain predictable results, using known technique to improve similar devices (methods, or products) in the same way, applying a known technique to a known device (method, or product) ready for improvement to yield predictable results, an "obvious to try" option—*i.e.*, choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success, and/or using known work in one field of endeavor that prompts variations of it for use in either the same field or a different one based on design incentives or other market forces.

For example, each of the above references are directed to the same field, which here is non-volatile semiconductor memory. As described above, a POSITA would know that any charge trap technology available regarding 2-D SONOS memory would be equally applicable to 3-D SONOS memory. Moreover, the references are all aimed at addressing the same or similar problem – ensuring charge trap retention. Thus, each reference presents at minimum an obvious to try variation of a finite number of predictable solutions, such as applying the charge trap layers from 2-D NAND in the 3-D NAND. A POSITA would also have been well aware of the move toward high work function gate electrodes, high-temperature dielectrics, and the need for logic devices that were made of similar materials.

As a specific example, and without limitation, a POSITA would have been motivated to combine Lee 255 and/or Lee 961 and/or Hwang with one or more of Fujiwara, Ganguly, Cypress products, Lee 961, Mahajani, Uenishi, Wang. Each of these references relates to SONOS charge trapping-type nonvolatile memory devices. A POSITA would have been motivated to modify the nitride charge trapping layer of Lee '255 and Hwang to incorporate the multilayered charge trap layer configurations and oxygen-rich / -lean layers disclosed in these references. Further, a POSITA would have been motivated to modify the multilayer charge trapping layer of Lee 961 to incorporate the oxygen-rich / -lean layers disclosed in these references. Each of these references describes purported advantages for multiple charge trap layers and the oxygen-rich / -lean configuration of the charge trap layers.

For example, Fujiwara, Ganguly, Uenishi, Wang, Cypress products, and Mahajani describe advantages of incorporating multiple charge trap layers, including oxygen-rich layers by the tunneling layer and oxygen-lean layers by the blocking layer, in order to improve the film quality and promote charge retention. Specifically, these references teach that more charge will be stored deeper in the oxygen-lean region, helping prevent migration of electrons. It would have been obvious for a POSITA to consult the teachings of Fujiwara, Ganguly, Uenishi, Wang, Cypress products, and Mahajani in seeking to improve the memory transistor configuration of Lee 255 and/or Lee 961 and/or Hwang because they are also directed to improving the configuration of SONOS-type charge trapping memory transistors such as those taught in Lee 255, Lee 961 and Hwang. Thus, a POSITA would have been motivated to modify the nitride charge trapping layer of Lee 255 and Hwang to incorporate the two-level charge trap layers and oxygen-rich / -lean layers described in Fujiwara, Ganguly, Uenishi, Wang, Cypress products, and Mahajani because it would, as described by the patentee, improve the charge storage capability of Lee 255 and Hwang. Further, a POSITA would have been motivated to modify the multi-layer charge trapping layer of Lee 961 to incorporate oxygen-rich / -lean layers described in Fujiwara, Ganguly, Uenishi, Wang, Cypress products, and Mahajani because it would purportedly improve the charge storage capability of Lee 961. A POSITA would have understood that the combination of these references with Lee 255 and/or Lee 961 and/or Hwang amounts to applying their teaching for their intended purposes of improving similar devices in the same ways. Further, the purported benefit of using an oxygen-rich bottom nitride layer and an oxygen-lean top nitride layer in a SONOS memory transistor would have been predictable to a POSITA prior to July 2012. As described in Section III.A.2, many other prior art references show that it was a routine design choice to use an oxygen-rich first nitride layer and an oxygen-lean second nitride layer to obtain improved charge retention characteristics. A POSITA would also expect success in applying these teachings because the underlying materials, equipment, and process knobs were mainstream.

Similarly, a POSITA would have been motivated to combine Lee 255 and/or Hwang with Lee 961 and / or Mahajani regarding creating an anti-tunneling layer in the multilayer charge trap region. Both describe advantages to using a thin SiO anti-tunneling layer to further assist in improving charge retention, and a POSITA would have been motivated to combine the references and would expect to find success as described above. It would simply be a routine design choice for a POSITA to employ a SONONOS configuration as compared to a SONNOS configuration, and a POSITA would have expected success in creating either. A POSITA would also have recognized the benefit of an anti-tunneling layer in additionally preventing charge migration.

(ii) Lee 255 and / or Lee 961 + Hwang + any of Fujiwara, Ganguly, Cypress products, Lee 961, Mahajani, Uenishi, Wang.

A skilled artisan would have been motivated to combine Hwang and any of the above references with Lee 255 and / or Lee 961 and would have found it straightforward and obvious to do so, at least because it would amount to no more than combining prior art elements according to known methods to yield predictable results, simple substitution of one known element for another to obtain predictable results, using known technique to improve similar devices (methods, or products) in the same way, applying a known technique to a known device (method, or product) ready for improvement to yield predictable results, an "obvious to try" option—*i.e.*, choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success, and/or using known work in one field of endeavor that prompts variations of it for use in either the same field or a different one based on design incentives or other market forces.

For example, each of the above references are directed to the same field, which here is non-volatile semiconductor memory. As described above, a POSITA would know that any charge trap technology available regarding 2-D SONOS memory would be equally applicable to 3-D SONOS memory. Moreover, the references are all aimed at addressing the same or similar problem – ensuring charge trap retention. Thus, each reference presents at minimum an obvious to try variation of a finite number of predictable solutions, such as applying the charge trap layers from 2-D NAND in the 3-D NAND. A POSITA would also have been well aware of the move toward high work function gate electrodes, high-temperature dielectrics, and the need for logic devices that were made of similar materials.

As a specific example, and without limitation, a POSITA would have been motivated to combine Lee 255 or Lee 961 with Hwang. Hwang relates to SONOS charge trapping-type nonvolatile memory devices. It also teaches three dimensional SONOS-style memory. A POSITA would have understood that the memory devices of Lee '255 and Lee 961 (and any of the charge trap memory devices in the above-cited prior art) would have been connected to MOS logic transistors in the peripheral regions of their respective devices to control their operation. Hwang expressly teaches such device electrical connections to MOS logic transistors in its peripheral circuit, along with a specific "step structure" approach, that it states provides simplified fabrication and improved reliability and integration. A POSITA also would have expected success in applying the teachings of Hwang to further modify the combination of Lee '255 or Lee 961 with the other art discussed below. Incorporating Hwang's explicit teaching into Lee '255 or Lee 961 would have been a routine design choice for a POSITA, providing improved clarity and reliability of the connection scheme without requiring new materials, new processes, or unconventional circuitry. Employing the electrical connection strategies and peripheral MOS transistor teachings of Hwang to the 3D device of Lee 255 or Lee 961 combined with the other references discussed below would therefore enable the combined device to function and provide the benefits taught by Hwang. A POSITA would have understood that this combination amounts to applying the teachings of Hwang for their intended purpose to improve similar devices in the same way.

Further, a POSITA would have been motivated to combine Lee 255 + Hwang or Lee 961 + Hwang with one or more of Fujiwara, Ganguly, Cypress products, Mahajani, Uenishi, Wang. Each of these references relates to SONOS charge trapping-type nonvolatile memory devices. A POSITA would have been motivated to modify the nitride charge trapping layer of Lee '255 to incorporate the multilayered charge trap layer configurations disclosed in these references. Each of these references describes advantages for multiple charge trap layers.

For example, Fujiwara, Ganguly, Uenishi, Wang, Cypress products, and Mahajani describe advantages of incorporating multiple charge trap layers, including oxygen-rich layers by the tunneling layer and oxygen-lean layers by the blocking layer, in order to improve the film quality and promote charge retention. Specifically, these references teach that more charge will be stored deeper in the oxygen-lean region, helping prevent migration of electrons. It would have been obvious for a POSITA to consult the teachings of Fujiwara, Ganguly, Uenishi, Wang, Cypress products, and Mahajani in seeking to improve the memory transistor configuration of

Lee 255 and Lee 961 because they are also directed to improving the configuration of SONOS-type charge trapping memory transistors such as those taught in Lee 255 and Lee 961. Thus, a POSITA would have been motivated to modify the nitride charge trapping layer of Lee 255 to incorporate the two-level charge trap layers described in Fujiwara, Ganguly, Uenishi, Wang, Cypress products, and Mahajani because it would improve the charge storage capability of Lee 255. Further, a POSITA would have been motivated to modify the multi-layer charge trapping layer of Lee 961 to incorporate oxygen-rich / -lean layers described in Fujiwara, Ganguly, Uenishi, Wang, Cypress products, and Mahajani because it would purportedly improve the charge storage capability of Lee 961. A POSITA would have understood that the combination of these references with Lee 255 or Lee 961 amounts to applying their teaching for their intended purposes of improving similar devices in the same ways. Further, the purported benefit of using an oxygen-rich bottom nitride layer and an oxygen-lean top nitride layer in a SONOS memory transistor would have been predictable to a POSITA prior to July 2012. As described in Section III.A.2, many other prior art references show that it was a routine design choice to use an oxygen-rich first nitride layer and an oxygen-lean second nitride layer to obtain improved charge retention characteristics in both SONNOS and SONONOS configurations. A POSITA would also expect success in applying these teachings because the underlying materials, equipment, and process knobs were mainstream.

Similarly, a POSITA would have been motivated to combine Lee 255 + Hwang with Lee 961 and / or Mahajani regarding creating an anti-tunneling layer in the multilayer charge trap region. Both describe advantages to using a thin SiO anti-tunneling layer to further assist in improving charge retention, and a POSITA would have been motivated to combine the references and would expect to find success as described above. It would simply be a routine design choice for a POSITA to employ a SONONOS configuration as compared to a SONNOS configuration, and a POSITA would have expected success in creating either. A POSITA would also have recognized the benefit of an anti-tunneling layer in additionally preventing charge migration.

Each of the listed combinations satisfy the elements of the asserted claims, and Sandisk reserves the right to supplement, amend, or refine its contentions, including its combinations and motivations to combine, in light of further discovery, expert analysis, developments in the record, or claim construction.

c. The ’365 Patent

Sandisk contends that the Asserted Claims of the ’365 Patent are invalid as anticipated under 35 U.S.C. § 102. Sandisk further contends that the Asserted Claims are invalid as obvious under 35 U.S.C. § 103.

Sandisk further sets forth below exemplary combinations of references that Sandisk contends render the Asserted Claims invalid as obvious. This disclosure is based on Sandisk’s present understanding of the Asserted Claims and the apparent constructions that Sandisk believes IPValue may be asserting based on its infringement contentions. Each of the below exemplary combinations should be understood to include and incorporate the background knowledge of a person of ordinary skill in the art, such as (but not limited to) the background information detailed in the above State of the Art section of this pleading. In addition, each of the below exemplary combinations should also be understood to encompass any subset (*i.e.*, less than all) of the references identified in the combination, whether or not the particular subset is specifically identified below.[13]

Table #6			
Prior Art Charted References and Combination Identification ’365 Patent			
Reference Name	**Reference**	**Claim Chart(s)**	**Exemplary Obviousness Combinations**
Lee 255	Number US 2012/0068255	Exhibit No. 365-1	In combination with one or more of at least the following: Fujiwara, Ganguly,

[13] As a non-limiting example, a particular reference identified in a given combination may be necessary for that combination to render obvious some Asserted Claims but not others, in which case Defendants may, depending on the Asserted Claim, assert invalidity due to obviousness based on the combination with and without that particular reference.

			Hwang, Cypress products, Lee 961, Mahajani, Uenishi, Wang
Fujiwara	US 2006/0065910 A1	Exhibit No. 365-2	In combination with at least Lee 255 and / or Lee 961 and / or Hwang.
Ganguly	US 2011/0281429 A1	Exhibit No. 365-3	In combination with at least Lee 255 and / or Lee 961 and / or Hwang.
Hwang	US 2012/0061744 A1	Exhibit No. 365-4	In combination with at least Lee 255 and / or Lee 961, and additionally in combination with Fujiwara, Ganguly, Cypress products, Lee 961, Mahajani, Uenishi, Wang.
Lee 961	KR 10-2011-0119061	Exhibit No. 365-5	Anticipates; Also renders obvious in combination with one or more of at least the following: Fujiwara, Ganguly, Hwang, Cypress products, Lee 255, Mahajani, Uenishi, Wang.
Mahajani	US 2005/0062098 A1	Exhibit No. 365-6	In combination with at least Lee 255 and / or Lee 961 and / or Hwang.
Cypress products	US 8222688	Exhibit No. 365-7	In combination with at least Lee 255 and / or Lee 961 and / or Hwang.
Ramkumar	US 9102522	Exhibit No. 365-8	Anticipates

Uenishi	US 2010/207192A	Exhibit No. 365-9	In combination with at least Lee 255 and / or Lee 961 and / or Hwang.
Jenne	US 8710578	Exhibit No. 365-10	Anticipates
Wang	US 2009/0057752	Exhibit No. 365-11	In combination with at least Lee 255 and / or Lee 961 and / or Hwang.

i. Patent Prosecution

Igor Polishchuk, Sagy Charel Levy, and Krishnaswamy Ramkumar (collectively, "the Applicants") filed the application for the '365 patent (U.S. Application No. 17/157,350) on January 25, 2021. The original application included only one claim. The Applicants submitted information disclosure statements during prosecution listing large numbers of prior art references (more than 300 references in total). Then, on November 1, 2021, Applicants filed a preliminary amendment replacing original claim 1 with new claims 2–46.

The Examiner allowed application claims 2–46 without rejection. The Examiner did not explicitly compare the limitations of claims 2–46 to any specific prior art reference. In the statement of reasons for allowance, the Examiner identified claim limitations that he believed were missing from the prior art, as discussed below.

Regarding application claim 2 (issued claim 1), the Examiner stated the prior art does not disclose "forming an opening extending through the stack of layers to a first doped diffusion region formed on the substrate; forming on sidewalls of the opening a blocking dielectric layer; forming on an inside sidewall of the blocking dielectric layer a multi-layer charge storing region; forming on an inside sidewall of the multi-layer charge storing region a tunnel dielectric layer; and forming on an inside sidewall of the tunnel dielectric layer a vertical channel having a semiconductor material extending from the first doped diffusion region through the opening to a top of the stack of layers."

Regarding application claim 24 (issued claim 23), the Examiner stated the prior art fails to disclose "forming on an inside sidewall of the tunnel dielectric layer an annular shaped vertical channel having a semiconductor material extending from the substrate through the opening towards a top of the stack of layer."

Regarding application claim 36 (issued claim 35), the Examiner stated the prior art fails to disclose "a semiconductor memory device, comprising a multi-layer charge storing region surrounding the tunnel dielectric layer, the multi-layer charge storing region formed in a substantially annular shape, a blocking dielectric layer surrounding the multi-layer charge storing region, the blocking dielectric layer formed in a substantially annular shape, and a gate electrode surrounding the blocking dielectric layer."

ii. Motivation to Combine

Sandisk further sets forth below exemplary combinations of references that Sandisk contends render the Asserted Claims invalid as obvious. This disclosure is based on Sandisk's present understanding of the Asserted Claims and the apparent constructions that Sandisk believes IPValue may be asserting based on its infringement contentions. Each of the below exemplary combinations should be understood to include and incorporate the background knowledge of a person of ordinary skill in the art, such as (but not limited to) the background information detailed in the above State of the Art section of this pleading. In addition, each of the below exemplary combinations should also be understood to encompass any subset (*i.e.*, less than all) of the references identified in the combination, whether or not the particular subset is specifically identified below.[14]

Sandisk also specifically incorporates by reference the IPR petitions filed for the '240 and '365 patents, produced and served on IPValue herewith, including the motivations to combine and expectations of success regarding those combinations for the various prior-art references discussed therein. *See* '240 IPR (Case No. IPR2025-01283); '365 IPR (Case No. IPR2025-

[14] As a non-limiting example, a particular reference identified in a given combination may be necessary for that combination to render obvious some Asserted Claims but not others, in which case Counterclaim-Defendants may, depending on the Asserted Claim, assert invalidity due to obviousness based on the combination with and without that particular reference.

01281). The Polishchuk patents share a common specification, and therefore the motivations to combine and expectations of success discussed in both IPRs (which include the declarations filed in support thereof) apply to the ’365 patent and the combinations discussed herein.

(a) Primary Reference: Lee 255, Lee 961, Hwang

Lee 255, Lee 961, and Hwang disclose and teach a 3-D non-volatile semiconductor memory device and methods of fabricating the same. One of ordinary skill in the art would have been motivated to combine Lee 255, Lee 961, and Hwang with each other and any other reference(s) in Table 6, as all references are analogous art to the ’365 patent because they teach improvements to non-volatile memory devices generally, and charge trap memory devices specifically. For example, one of ordinary skill in the art would have been motivated to combine Lee 255, Lee 961, and Hwang with at least the following references, and would have had a reasonable expectation of success in doing so:

(i) Lee 255 or Lee 961 or Hwang + any of Fujiwara, Ganguly, Cypress products, Lee 961, Mahajani, Uenishi, Wang.

A skilled artisan would have been motivated to combine any of the above references with Lee 255 and/or Lee 961 and/or Hwang and would have found it straightforward and obvious to do so, at least because it would amount to no more than combining prior art elements according to known methods to yield predictable results, simple substitution of one known element for another to obtain predictable results, using known technique to improve similar devices (methods, or products) in the same way, applying a known technique to a known device (method, or product) ready for improvement to yield predictable results, an “obvious to try” option—*i.e.*, choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success, and/or using known work in one field of endeavor that prompts variations of it for use in either the same field or a different one based on design incentives or other market forces.

For example, each of the above references are directed to the same field, which here is non-volatile semiconductor memory. As described above, a POSITA would know that any charge trap technology available regarding 2-D SONOS memory would be equally applicable to 3-D SONOS memory. Moreover, the references are all aimed at addressing the same or similar problem – ensuring charge trap retention. Thus, each reference presents at minimum an obvious to try variation of a finite number of predictable solutions, such as applying the charge trap layers from 2-D NAND in the 3-D NAND. A POSITA would also have been well aware of the move toward high work function gate electrodes, high-temperature dielectrics, and the need for logic devices that were made of similar materials.

As a specific example, and without limitation, a POSITA would have been motivated to combine Lee 255 and/or Lee 961 and/or Hwang with one or more of Fujiwara, Ganguly, Cypress products, Lee 961, Mahajani, Uenishi, Wang. Each of these references relates to SONOS charge trapping-type nonvolatile memory devices. A POSITA would have been motivated to modify the nitride charge trapping layer of Lee ’255 and Hwang to incorporate the multilayered charge trap layer configurations and oxygen-rich / -lean layers disclosed in these references. Further, a POSITA would have been motivated to modify the multilayer charge trapping layer of Lee 961 to incorporate the oxygen-rich / -lean layers disclosed in these references. Each of these references describes purported advantages for multiple charge trap layers and the oxygen-rich / -lean configuration of the charge trap layers.

For example, Fujiwara, Ganguly, Uenishi, Wang, Cypress products, and Mahajani describe advantages of incorporating multiple charge trap layers, including oxygen-rich layers by the tunneling layer and oxygen-lean layers by the blocking layer, in order to improve the film quality and promote charge retention. Specifically, these references teach that more charge will be stored deeper in the oxygen-lean region, helping prevent migration of electrons. It would have been obvious for a POSITA to consult the teachings of Fujiwara, Ganguly, Uenishi, Wang, Cypress products, and Mahajani in seeking to improve the memory transistor configuration of Lee 255 and/or Lee 961 and/or Hwang because they are also directed to improving the configuration of SONOS-type charge trapping memory transistors such as those taught in Lee 255, Lee 961 and Hwang. Thus, a POSITA would have been motivated to modify the nitride charge trapping layer of Lee 255 and Hwang to incorporate the two-level charge trap layers and oxygen-rich / -lean layers described in Fujiwara, Ganguly, Uenishi, Wang, Cypress products, and Mahajani because it would, as described by the patentee, improve the charge storage capability of

Lee 255 and Hwang. Further, a POSITA would have been motivated to modify the multi-layer charge trapping layer of Lee 961 to incorporate oxygen-rich / -lean layers described in Fujiwara, Ganguly, Uenishi, Wang, Cypress products, and Mahajani because it would purportedly improve the charge storage capability of Lee 961. A POSITA would have understood that the combination of these references with Lee 255 and/or Lee 961 and/or Hwang amounts to applying their teaching for their intended purposes of improving similar devices in the same ways. Further, the purported benefit of using an oxygen-rich bottom nitride layer and an oxygen-lean top nitride layer in a SONOS memory transistor would have been predictable to a POSITA prior to July 2012. As described in Section III.A.2, many other prior art references show that it was a routine design choice to use an oxygen-rich first nitride layer and an oxygen-lean second nitride layer to obtain improved charge retention characteristics. A POSITA would also expect success in applying these teachings because the underlying materials, equipment, and process knobs were mainstream.

Similarly, a POSITA would have been motivated to combine Lee 255 and/or Hwang with Lee 961 and / or Mahajani regarding creating an anti-tunneling layer in the multilayer charge trap region. Both describe advantages to using a thin SiO anti-tunneling layer to further assist in improving charge retention, and a POSITA would have been motivated to combine the references and would expect to find success as described above. It would simply be a routine design choice for a POSITA to employ a SONONOS configuration as compared to a SONNOS configuration, and a POSITA would have expected success in creating either. A POSITA would also have recognized the benefit of an anti-tunneling layer in additionally preventing charge migration.

Finally, a POSITA would also have been well aware of high work function gate electrodes, high-temperature and high k dielectrics and similar, and it would simply be a routine design choice for a POSITA to employ these and similar options in creating a semiconductor memory device.

Each of the listed combinations satisfy the elements of the asserted claims, and Sandisk reserves the right to supplement, amend, or refine its contentions, including its combinations and motivations to combine, in light of further discovery, expert analysis, developments in the record, or claim construction.

B. The ’664 Patent

1. Priority

For purposes of these Invalidity Contentions, Sandisk has applied the priority date of May 10, 2007—the filing date of the ’664 patent.

2. Patent Prosecution

The prosecution history of the ’664 patent confirms that the Examiner considered only a single prior art reference—Kuo (U.S. Patent No. 6,768,366)—and ultimately allowed the claims following an initial rejection solely because of an added limitation directed to switching between high- and low-frequency clock signals. Notably, as detailed below, the ’664 inventors, as well as the Examiner, apparently ignored a large corpus of relevant prior art that clearly discloses that exact limitation.

In relevant part, during the ’664 patent’s prosecution history claims 1–6 and 18 were initially rejected under 35 U.S.C. § 112 for indefiniteness because the Examiner found the claim language “a clock control circuit having a clock signal” to be unclear in describing the relationships among the clock control circuit, the clock switch signal, and the output of that circuit. The Examiner also determined that “dynamic load control circuit” lacked a clear antecedent basis. Office Action Summary (4/29/09) (SD_IPV_00001983 at 2019). Additionally, claims 1–6 and 16–20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kuo, which the Examiner found “teaches a charge pump control circuit, which includes: a clock control circuit” with a “dynamic load (MC1 and MC2 and the transistors connected to MC1-MC2 that have their gates controlled by the output of the inverter receiving CLKEN at the inverter input),” the “clock control circuit having a switch clock signal as an output;” a “clock switch signal control circuit … having an input coupled to the switch clock signal, the clock switch control circuit having a clock signal as an output … and a clock driver (the two NAND gates) having an input coupled to the clock signal … and an output of a differential clock signal (CLKI, CLK2).” *Id.* at SD_IPV_00001985. For claims 2 and 6, the Examiner explained that “Figure 6 [of Kuo] shows a dynamic load control circuit … having a start up signal (CLKEN) controlling the dynamic load, wherein the dynamic load control circuit is coupled to the switch clock signal (VU0)." *Id.* at SD_IPV_00001986. For claim 3, the Examiner found Kuo's Figure 6 disclosed "the dynamic load has a capacitor (MC1 or MC2) with a node coupled to a controllable switch (the transistors connected to MC1-MC2 that have their gates controlled by the output of the inverter receiving CLKEN at the inverter input)." *Id.* The Examiner further found that Kuo's Figure 6 showed "the clock switch control circuit (the two inverters connected to the NAND gates) has a low frequency clock input and a high frequency clock input (VU1 and VU2)." *Id.*

In response, the applicant canceled claim 1 and amended the remaining claims to specify that the "clock driver circuit" was configured "to switch a clock signal supplied to a charge pump circuit between one of a first clock signal and a second clock signal." Amendment and Response to 4/29/2009 Office Action (Dated 7/29/09) (SD_IPV_00001983 at 2013). The applicant argued that "Kuo increases a reference current to increase the charging time of capacitors, thereby increasing a frequency of the clock generator (Column 1, lines 39–47), but does not switch between one of a first clock signal and a second clock signal." *Id.* The Examiner, Long T. Nguyen, found this amendment sufficient, stating in the Reason for Allowance that Kuo:

> fails to disclose or suggest that the clock driver circuit is configured to switch a clock signal supplied to a charge pump circuit between one of a first clock signal and a second clock signal based on the switch control signal, wherein the first clock signal has a higher frequency than the second clock signal.

'664 Notice of Allowability (10/13/2009) (SD_IPV_00001983 at 2000-2001).

Additionally, the Examiner stated that Kuo:

> fails to disclose or suggest that the clock control circuit is configured to output a switch clock signal after a delay following enabling the charge pump control circuit, and the clock switch circuit switches a frequency of a clock signal supplied to a charge pump circuit in response to the switch clock signal.

'664 Notice of Allowability (10/13/2009) (SD_IPV_00001983 at 2001).

The Examiner's Reason for Allowance thus makes clear that patentability turned solely on the added limitation concerning frequency switching between two clock signals or based on a startup clock signal after enabling the charge pump. But the Examiner did not review or cite to any other prior-art references other than Kuo. Indeed, the prior-art references cited in Sandisk's Invalidity Contentions clearly disclose these so-called "novel" features, including clock selection or control circuits configured to switch a clock signal supplied to a charge pump between high and low frequency inputs as well as circuits configured to output switch clock signals after a delay following startup of the charge pump. Because these features were already well known in the art, the Asserted Claims of the '664 patent are invalid as anticipated or, at a minimum, obvious in view of the prior art, either alone or in combination with the other prior art references identified herein.

3. Background Knowledge of those Skilled in the Art

a. Charge Pumps

A charge pump is an electrical circuit designed to raise / "boost" (or lower) the voltage level. This is accomplished using a combination of common circuit elements such as switches / transistors, capacitors, and oscillators / clocks. Charge pumps have long been used in low-power electronics (such as flash memories) to boost voltages in different subparts of the circuitry, while minimizing overall power consumption.

The first charge pump (also known as a "voltage multiplier") was invented in 1919 by Swiss physicist Heinrich Greinacher. In 1930, Douglas Cockcroft and Ernest Walton used this basic circuit to generate high voltages for a particle accelerator, the first "atom smasher," which earned them the 1951 Nobel Prize in Physics. Consequently, a large class of charge pumps are referred to as "Cockcroft-Walton multipliers." Pan at [3].

Since the 1970s, charge pumps and their incorporation into integrated circuits (*i.e.*, computer chips) have been widely discussed and analyzed in the technical literature, including in hundreds of academic and scientific papers, patents, articles, textbooks, dissertations, and product data sheets/manuals. On-chip charge pumps became standard in the 1980s in flash memory technology, because erasing a flash memory cell requires a substantially higher voltage than programming or reading it. For this reason, every flash memory device incorporates integrated charge pump circuitry – this feature is mandatory. *See, e.g.*, G. Campardo, R. Micheloni, D. Novosel, *Circuits Used in Program and Erase Operations* 361, in VLSI-Design of Non-Volatile

Memories (Springer, Berlin, Heidelberg 2005).

b. Charge Pump Control Circuits and the Claimed Invention

Charge-pump control circuits were well known before the relevant priority date. The ’664 patent itself refers to a “conventional charge pump control circuit” that “generates a high frequency and low frequency oscillator and uses circuitry to control the clock switching.” ’664 at [1:31–34]. “During startup, the high frequency clock is used to generate the desired high output voltage, at which point the low frequency clock will take over the pump operation.” *Id*. at [1:34–36].

The ’664 patent specification identifies the “issue” with such conventional designs as the well-known trade-off between startup speed, voltage maintenance, and power consumption, stating: “in order to maintain the minimum positive pump voltage, the frequency of the low-frequency oscillator must be increased, which increases operating power consumption.” ’664 at [1:37–39]. The specification acknowledges that adding filter capacitance to “keep the charge longer” was already known but unsatisfactory because it “contribute[s] to a much longer startup time.” *Id*. at [1:40–42]. Thus, the ’664 patent’s stated goal was a system that provided fast startup with reduced steady-state power consumption. *Id.* at 1:44–46. The proposed “solution”—initially using a high-frequency clock to boost output, then switching to a low-frequency clock after startup—was conventional. The timing of that switch, governed by a control circuit outputting a “clock switch signal based on a dynamic load,” likewise reflects long-established practice.

None of this was new. By the time of the ’664 patent, the trade-off between fast startup and low steady-state power was a routine design problem. Designers knew that running a pump at high frequency enabled rapid voltage ramp-up but wasted power if maintained after startup. For instance, Yamawaki (a ***1991*** patent) sought “to provide an interface circuit … which has a reduced consumed electric power and which can speed up the start of the communication.” Yamawaki at [1:64–68]. Its solution matches the ’664’s approach: “a signal generation circuit generating ***a first signal having a first frequency, and a second signal having a second frequency lower than the first frequency,*** … and a selector … controlled by the comparator so as to supply the first signal … ***when powered on,*** and … the second signal … when an absolute value of the elevated output voltage reaches the reference voltage." Yamawaki at [Abstract]. Numerous pre-2007 references disclose the same concept. *See, e.g.*, Fujioka at 2:31–49 (reducing "time for a step-up voltage to reach a target value after power-on and sav[ing] power consumption in normal operation" via a step-up circuit with first and second clocks of different frequencies); Ubata at [0012] (reducing current consumption during standby with a booster circuit having an internal oscillator generating a higher-frequency second clock and a selection circuit choosing clocks "based on [a] control signal"); Maeda at [(57) Abstract, Claim 1] (aiming "to boost a charge pump circuit in a short time and reduce current consumption in a stable state" using first and second oscillation means and switching means triggered when the voltage reaches a set value).

Sandisk's own engineers Feng Pan and Tapan Samaddar described the same approach in the 2006 book they authored, entitled "Charge Pump Circuit Design,"[15] which explains that "multistep frequency control," where the pump first runs at high frequency to ramp up quickly and then switches to low frequency for regulation, was standard practice. Pan at [99–100]. Further, Toshiba (now Kioxia), Sandisk's joint-venture partner, likewise patented such methods. Shuto, for instance, teaches adjusting the current-driving capability of a boosting circuit "by switching a frequency of the clock signal according to the level of the supply voltage V_{cc}," using a lower frequency clock in the event of high supply voltage and a higher frequency clock in the event of low supply voltage (i.e., selecting a high frequency clock to raise supply voltage at the start of an operation). Shuto at [(57) Abstract]. Kawasaki, another Toshiba patent, describes a booster circuit with "a timing circuit (11) for outputting a select signal according to the dissipated current … [and] a drive signal select circuit (12) for selecting … any one of at least two drive signals CLK of different frequencies," to reduce current dissipation in the charge pump circuit.

[15] As described in the About the Authors section of the Pan textbook, at that time, Feng Pan was "doing circuit design at SanDisk Corporation," where he was "involved in defining the architecture and implementing charge pumps and related high-voltage circuits over several generations of NAND Flash memory products." Pan at [About the Authors]. Tapan Samaddar was a design engineer at SanDisk Corporation at the time, "where he [led] the company's high-voltage circuit designs." *Id.*

Kawasaki at [Abstract].

In short, Sandisk and Kioxia were pioneers in multi-frequency charge pump circuitry and clock control logic. Their publications, along with the numerous other prior art cited herein, provide the background knowledge of a person of ordinary skill in the art, and further anticipate or otherwise render obvious each and every element of the '664 patent's Asserted Claims, including high/low-frequency clock signal switching, startup-delay control, and dynamic-load-based switching. All such elements were well known long before 2007, indeed dating back to the early 1990s, as reflected in the priority dates of the references listed herein.

c. Multi-Frequency Clock Inputs and Frequency Switching Control Signals

Several of the Asserted Claims include limitations that involve switching between clocks with different frequencies—indeed, this limitation was the supposed "novelty" identified by the patent Examiner during prosecution. *See, e.g.*, '664 patent at [Claim 1, 5, 18, and 19]; *see also* '664 Notice of Allowability (10/13/2009) (SD_IPV_00001983 at 2000-2001).

Pan, the 2006 book authored by Sandisk engineers, teaches exactly that "novel" approach. Pan explains that "a ***standard practice*** is to allow the oscillator to operate at a high frequency and then use a series of dividers to step the frequency down to a required level." Pan at [100–101]. The book also illustrates this technique in Figure 5-3, entitled "Variable frequency clock generator" where two (or more) clock signals of different frequencies can be selected to operate the charge pump. *Id.* at [101].

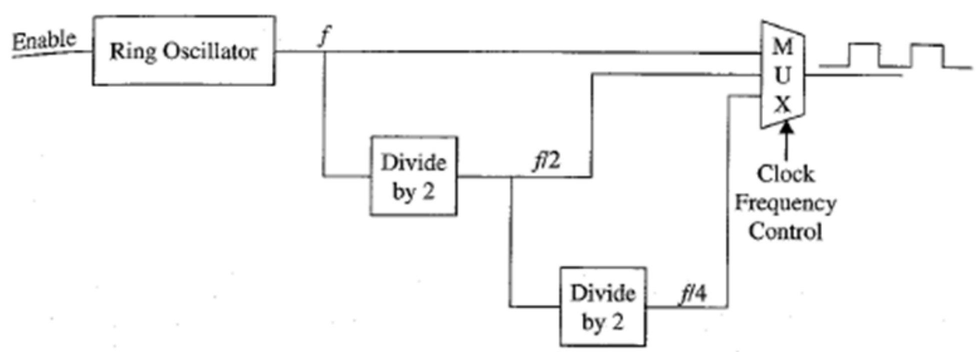


Figure 5-3 Variable frequency clock generator.

This 2006 book further explains that "once the output approaches its regulation level, … the clock frequency can be adjusted dynamically to scale down the power of the pump in regulation to match the magnitude of power consumed," and that "clock frequency can be adjusted accordingly to allow the pump to always deliver the power just consumed by the output." Pan at [136]. In other words, the clock frequency that this book teaches is load-dependent and dynamically adjustable. These disclosures show that, by 2006, the field of semiconductor engineering (and Sandisk in particular) was well-aware that dynamically adjusting the clock frequency (from high to low) was advantageous in charge pump design.

By 2007, two broad categories of implementation were commonly used in the art to support multi-frequency control: (1) systems with two distinct clock sources and a selector; or (2) systems with a single oscillator that generated multiple frequencies and selected which frequencies to output based on clock control signals. Both approaches were well known.[16]

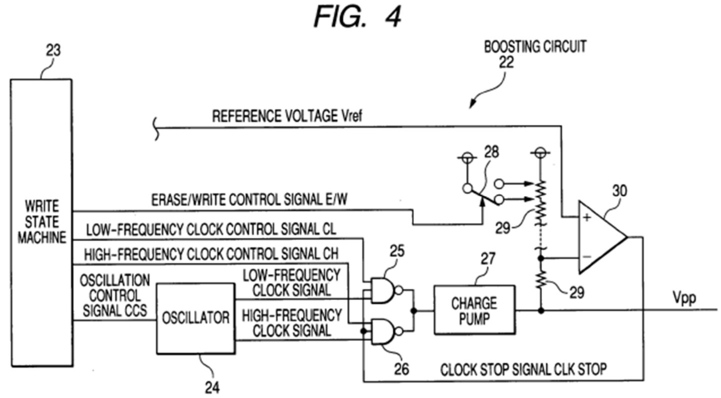
The first category, involving two clock sources, is exemplified at least by the following prior art references: Fujioka, Yamawaki, Ubata, Tasdighi, Kawasaki, and Koike. *See* Fujioka at [2:37–2:47] ("a clock generating circuit for providing a first clock with a first frequency when the control signal … and for providing a second clock with a second frequency when the control signal … the second frequency being lower than the first frequency; and a charging pump circuit driven by the first and second clocks."); Yamawaki [3:50–3:51] ("Specifically, the oscillation frequency of the oscillator circuit 21 is higher than that of the oscillator circuit 22."); Ubata at [0012] ("a first clock supplied to the charge pump; an internal oscillator configured to generate a second clock having a frequency higher than that of the first clock"); Tasdighi at [5:14–5:20] ("shown in FIG. 6, two oscillators, OSC1 and OSC2, are used, and the control signal on line 74

[16] IPValue does not make clear which embodiment it is claiming is allegedly practiced by Sandisk in its Infringement Contentions. Based on certain of IPValue's annotations to the figures in its '664 claim chart, it appears that IPValue may be claiming that Sandisk uses a single oscillator with variable frequencies, by suggesting, confusingly, that the '664 claim language involving high and low frequency clock "inputs" map onto the multi-frequency *outputs* of a clock frequency divider. *See, e.g.*, IPValue '664 Chart at p. 23. Sandisk reserves all rights to argue that such a configuration does not satisfy any claim limitations of the '664 patent, including the limitations that require a "clock switch control circuit" that "has a" or "receives" a high and/or low "frequency" clock "input." *See, e.g.*, Claims 5, 18, and 19.

controls a switch 76 which connects the charge pump 12 switching transistors to either the high frequency signals provided by OSC1 (for the normal operating mode) or the low frequency signals generated by OSC2 (for the low power consumption mode"); Kawasaki at [Figs. 7, 4:32–38, 6:13–25] ("high and low frequency clocks are inputted" to "drive signal select circuit 27); Koike at [0009] ["a plurality of clocks having different frequencies generated by another circuit … may be input to the selector").

The second category, using a single oscillator that generates multiple frequencies, was equally well known and understood. As mentioned above, Pan (2006) explains that "a standard practice is to allow the oscillator to operate at a high frequency and then use a series of dividers to step the frequency down to a required level." Pan at [100–101]. Pan further notes that this practice allows the clock frequency to be dynamically reduced as the output voltage approaches its regulated target — and emphasizes that such frequency scaling is a preferred design technique. Pan at [136]. Dozens of prior art references implement this multi-frequency approach. *See, e.g.*, Shuto at [Abstract], [Claims 1, 2], [Figs. 6, 9, 10]; Bazargan at [2:54–2:63], [Figs. 3, 7, 8]; Kawajiri at [Abstract], [Figs. 4, 5, 6, 7, 8, 9], [Claims 1, 2, 3, 6, 7], Maeda at [Abstract], [Figs. 1, 4], [15, 30, 32–35]; Koike at [Abstract], [Claims 1–5]; Maekawa at [Abstract], [Figs. 5, 6, 7, 10, 11, 12], [Claims 1, 2, 3, 6–8]; Cave at [Fig. 2]; and Arakawa at [7:9–7:20], [Figs. 4 and 6]. An exemplary illustration of this setup from Kawajiri, Figure 4, is provided below:

FIG. 4



Thus, the prior art makes clear that switching between high vs. low frequency clock signals to achieve energy-efficient startup and operational states, was conventional. By 2006, both of these techniques were broadly understood as standard design options in power-managed charge pumps.

d. Use of Startup Signals and Delays to Influence Clock Frequency Switching

In multi-frequency control systems, designers must decide how long to maintain the high-frequency clock during startup before transitioning to the low-frequency mode. A common and well-understood design solution was to use a combination of startup signaling and delay mechanisms to govern the duration of high-frequency operation.

The ’664 patent claims a “startup signal” or a “switch clock signal,” wherein the signal is used to initiate or switch the frequency of a clock signal supplied to a charge pump. These elements, in which the assertion of a startup or clock-switch signal controls the timing and/or frequency of the switch between a high-frequency and low-frequency clock input to dynamically adjust based on operational state, was a conventional, obvious solution that offered predictable behavior to ensure that the charge pump reached sufficient voltage before switching to a lower-frequency, power-efficient mode.

For example, both Shuto (a 2004 Toshiba patent) and Pan (the 2006 book devoted to charge pumps and authored by Sandisk engineers) teach the use of “an enable signal” that commands operation during startup and changes the frequency of the clock inputs accordingly. Shuto at [0034–0035]; Pan at [41-42, Fig. 3-1]. Another clearly anticipatory example is demonstrated in Fujioka, which describes a “step-up circuit” that “ includes a selection control circuit 50” for activating a “start/stop signal” STP/*STP, by “detecting an external power-supply voltage V_{cc},” and “a ring oscillator circuit 30 for generating and outputting a clock of a high frequency F_s when the start/stop signal STP is inactive” and a second “ring oscillator circuit 10 for generating a clock of a low frequency f_o, a selection circuit 40 for selecting the output of the oscillator 30 when the start/stop signal STP is inactive and for selecting the output of the oscillator 10 when the start/stop signal is active, and a charging pump circuit 20 driven by the clocks." Fujioka at [Abstract]. Fujioka further explains that "High frequency F_s is initially used to quickly bring an output voltage up to a desired operating level and low frequency f_o is used, in order to conserve power, to maintain the operating level once a predetermined level of the external power supply voltage V_{cc} has been reached in order to conserve power." *Id.*

Further examples include Arakawa, which similarly describes a "power on control circuit" and Cave, which teaches a "start-up clock circuit." Arakawa's "power on control circuit 64 outputs a control signal PON when the power is switched on . . . . In response to this signal, the pulse generator 62 generates a pump enable signal PENB held at high level at an interval TS and outputs it to the oscillator 10a . . . . In response to this, the booster circuit 30 operates continuously at the interval TS after the power is turned on, and the boosted voltage VOUT rises rapidly." Arakawa at [10:22–10:26]. Cave's "start-up clock circuit (12)" comprises "a ring oscillator (40)" "to generate a ting oscillator clock signal (63) which can be used to allow the charge pump (10) to begin operation before an external clock signal (44) is available." Cave at [Abstract]. Bazargan also describes a load control circuit (NOR gate 503A and associated components) that uses a startup/enable signal (OSCENB) to control the dynamic operation of the oscillator load. Bazargan at [5:67–6:7]. Yamawaki likewise teaches the use of a "communication start signal" such that "at the time of starting the data communication, namely, after the data communication is started until the elevated output voltage becomes stable, the clock having a high frequency is supplied to the DC/DC converter as the switching clock, and in a steady communication after the elevated output voltage has become stable, the clock having a low frequency is supplied to the DC/DC converter as the switching clock." Yamawaki at [2:16–2:30]. "Therefore, the output voltage quickly rises up at the time of starting the data communication, and the electric power consumption is low in the steady communication." *Id.*

Thus, there was nothing novel about using a startup signal to control or delay the timing of the switch between high and low frequency clock inputs after start-up based on varying operating conditions.

e. Clock Control and Clock Switch Circuits

The '664 patent divides the frequency switching functionality into two roles: (1) a "clock control circuit" that generates a "switch clock control signal" based on a "dynamic load" and (2) a "clock driver circuit"[17] that receives that signal and uses it to select and output the appropriate clock frequency. *See* '664 patent at [Claims 1, 15]. Functionally, these two roles were well-established and structurally implemented in familiar ways. In the '664 patent, the clock control circuit includes startup signal, gating, and logic that governs the transition between clocks. The clock driver circuit includes selection logic that chooses between two clock inputs and routes the selected signal to the pump control switches.

Each of these design choices—both structurally and functionally— had direct analogs in the prior art. It was well known to a POSITA as of the priority date of the '664 patent to use startup signals, delay circuits (including RC delays and counters), and logic blocks to generate a switch control signal. For example, two Toshiba patents and the Pan textbook describe control circuits that incorporate delays to govern the transition between clock frequencies based on changing operating conditions. *See* Shuto at [Claim 1] (describing a "voltage detection means" circuit that "detects a level of the supply voltage and outputs a detection signal to the clock signal generating means, wherein the frequency of the clock signal is switched according to the level of the supply voltage."); *see also* Kawasaki at [4:32–4:45] (describing a "timing circuit" that "outputs the select signal to the drive signal select circuit 12 in such a way that the high frequency clock can be outputted by the drive signal select circuit 12 as the drive signal CLK when the dissipated current $I._{disp}$ of the liquid crystal circuit 14 is large but the low frequency clock can be outputted by the drive signal select circuit 12 as the drive signal CLK when the dissipated current $I._{disp}$ of the liquid crystal circuit 14 is small"); Pan at [207] ("feedback control signals can be used to control the charge pump internal circuits to vary the power consumption").

Numerous other prior art references similarly teach control circuits that determine when to switch frequencies. *See, e.g.*, Fujioka [2:38–2:47] ("a selection control circuit for setting a control signal at one state in response to an external power-supply voltage being above a value which is lower than a normal voltage"); Ubata at [0028–35] (describing a "current mirror circuit"

[17] The Asserted Claims appear refer to this circuit with inconsistent terminology, sometimes referring to it instead as the "clock switch circuit" or "clock switch control circuit."

that monitors the VPM voltage level and generates a selection signal to control clock switching); Tasdighi at [6:40–6:52] (the "logic circuit 16" serves as the clock control circuit, outputting signals that control oscillator frequency switching); Koike at [0011] (providing for "a controller circuit that outputs, to the selector, a select signal instructing a boost clock to select in response to an output signal from the boost voltage detection circuit").

Likewise, the use of selectors and clock drivers, such as multiplexers, logic-gated inverters, or switch matrices to steer one of multiple clock signals to a destination was widespread. For instance, the "selection circuit 40" in Fujioka; the "selection circuit 126 "in Ubata; the "select circuit 114" in Maekawa; and the "drive signal select circuit 12" in Kawasaki all switch between different clock signals supplied to a charge pump based on a selection signal. *See* Fujioka at Abstract ["a selection circuit 40 for selecting the output of the oscillator 30 when the start/stop signal STP is inactive and for selecting the output of the oscillator 10 when the start/stop signal is active"); Ubata at [Claim 1] ("A semiconductor integrated circuit … [with] a selection circuit configured to select, based on the control signal, a clock to be input to the charge pump."); Maekawa at [0112] ("The select circuit 114 selects and outputs one of the first to nth frequency-divided clock signals CK 1 to CK n as the reference clock signal CK based on a select control signal SCO."); Kawasaki at [Abstract] ("a drive signal select circuit (12) for selecting and outputting any one of at least two drive signals CLK of different frequencies on the basis of the select signal outputted by the timing circuit").

Thus, the clock logic used in the '664 patent, *i.e.*, the clock control and driver circuits, and the way those components are organized, reflect known and standard design techniques already established in charge pump frequency management systems.

f. Dynamic Loads and Switch-Controlled Capacitors

Certain claims of the '664 patent require that the switch clock control signal or the duration of a delay before such a signal is output is to be "based on a dynamic load." *See* '664 patent at [Claim 1.A, 15.A–C]. The specification does not define this phrase nor sufficiently explain its scope (instead describing a single embodiment that is reflected in narrower, dependent claim 3). This lack of written description leaves all other claims ambiguous and subject to farreaching interpretations.

Based on IPValue's vague Infringement Contentions, Sandisk can only speculate that IPValue may be treating the phrase "based on a dynamic load" to encompass any varying load condition (*e.g*., voltage, current, or capacitance changes) that influences the timing or frequency of a clock signal to a charge pump. It is impossible to discern what IPValue believes the proper construction of this term to be, and Sandisk reserves all rights to argue that "based on a dynamic load" is indefinite and/or lacks adequate written description, particularly given that, under such a broad construction, virtually any circuit with load-dependent behavior would satisfy the claim language, leaving the claims either clearly anticipated or hopelessly indefinite. Sandisk further reserves the right to advocate for a narrower construction than what IPValue appears to be pursuing (which is unclear to begin with), including, for example, limiting the phrase to the single embodiment disclosed in the specification. For purposes of these invalidity contentions only, however, Sandisk has for now attempted to ascertain and apply the broad and unclear interpretation that appears to be advanced in IPValue's Infringement Contentions.

Under IPValue's apparent treatment of "based on a dynamic load," all prior art references listed herein for the '664 patent clearly teach this limitation because the timing or frequency of the clock signals are responsive to varying operating conditions. *See, e.g*., Fujioka at [Abstract] (oscillator frequency changes based on rising V_{cc}); Kawajiri at [Abstract] (transition from low- to high-frequency clock occurs after the pump output reaches a threshold voltage); Koike at [0029] (clock frequency is adjusted based on load current).

As for dependent Claim 3 of the '664 patent, that claim (and that claim only) specifies that the dynamic load has "a capacitor coupled to a node and a controllable switch," without further limiting its placement or function. This form of circuitry was routine in charge pump circuits by 2007. Designers frequently used capacitors, combined with switches or transistors, in the timing, oscillator, or charge pump stage to generate predictable delays and/or behavior. For instance, capacitors can be charged or discharged in a controlled manner to determine how long a signal remained in a particular state or how long a system would remain in a certain operating mode.

Indeed, the Examiner who considered the application for the '664 patent found that the "dynamic load" elements, including the embodiments containing a "dynamic load control circuit" and/or "a capacitor with a node coupled to a controllable switch," were already anticipated by Kuo (U.S. 6,768,366). *See* Office Action Summary (4/29/09) Office Action Summary (4/29/09) (SD_IPV_00001983 at 2020-21) (Examiner noting Kuo teaches "a clock control circuit" with a "dynamic load" and Kuo's Figure 6 discloses "a dynamic load control circuit … having a start up signal (CLKEN) controlling the dynamic load" and "the dynamic load has a capacitor (MCI or MC2) with a node coupled to a controllable switch"). And the '664 applicant did not even counter that argument in the response (instead distinguishing the '664 patent claims from Kuo by pointing to the language describing high and low frequency clock inputs). *See* Amendment and Response to 4/29/2009 Office Action (7/29/09) (SD_IPV_00001983 at 2013).

Several other references disclose the same conventional elements. For example, and without limitation, the Toshiba patent Shuto describes an R-C delay circuit that is switched in or out of the oscillator feedback path based on supply voltage detection. *See* Shuto at [0041, Figs. 3–4] (discussing switches SW1–SW3 and capacitor C1). Bazargan includes a literal "load control circuit" that switches capacitive loading on or off based on control input. *See* Bazargan at [6:10–50, Fig. 6]. Arakawa also employs a switched capacitor (C) and resistor (R) in its delay circuit (Fig. 7), which determines how long the oscillator runs during standby by generating a timed pulse. *See* Arakawa at [11:1–12:3] (describing Figure 7). Cave describes a start-up clock circuit 12 that includes a ring oscillator 40 with resistor–capacitor pairs (50/52 and 58/60). The capacitors are gated by switching logic (tri-state buffer 62 and transistor 53) and thus form RC time-constant networks controlling the oscillator frequency. This configuration implements a dynamic, switch-influenced timing element within the clock-generation path, analogous to the dynamic-load, switch-controlled capacitor arrangement described in the '664 patent. *See* Cave at [3:45–3:52] ("The frequency of the internal clock signal is controlled by two Resistor-Capacitor (RC) time constants."); *see also* Kawasaki at [1:10–2:3] (Kawasaki's booster circuit includes capacitors Ca and Cb that are alternately connected to supply and output nodes by controllable switches SW1 and SW2 driven by the oscillator signal CLK); Fujioka at [3:65-4:6] (describing switch-controlled capacitors).

The paper prior art thus makes clear that this concept — using a switched capacitor coupled to a node to influence, delay, extend, or generate signals or other conditions — was widely disclosed and implemented across oscillator and timing circuits, including in charge pumps.

g. Prior-Art Systems

Moreover, Sandisk's discovery efforts and investigations are ongoing with regards to commercial products for sale that practiced the '664 patent elements before the priority date of the patent. On information and belief, the use of multi-frequency clocks in charge pumps, as well as other '664 patent claim elements, was also practiced and embodied in numerous commercial products sold beginning in the early 1990s. These products were marketed by multiple companies that include "Texas Instruments", "Linear Technology Corporation", "Maxim Integrated Products", "Sipex Corporation", "Semtech Corporation", "Intersil", and "HTC". Some of these prior art systems that embody multi-frequency clocks in charge pumps, as well as other '664 patent claim elements, such as start-up signals and delays through analog timers, were described or taught in part by the following product / marketing data sheets:

- [1993, Linear Technology] 12V CMOS Voltage Converter (LTC1044A)
- [1996, Maxim] CMOS Monolithic Voltage Converter (MAX660)
- [1996, Maxim] Dual-Output Charge Pump with Shutdown (MAX864)
- [2000, Sipex] 200mA Charge Pump Inverter or Doubler (SP6660)
- [2004, Sipex] High Frequency 200mA Charge Pump Inverter or Doubler (SP6661)
- [2004, Semtech] Charge Pump Regulator with Selectable 5.0V and 4.5V Output (SC603)
- [2005, Intersil] 3-Channel DC-DC Converter (EL7583)
- [2006, Texas Instruments] Bias Power Supply for TV and Monitor TFT LCD Panels (TPS65161)
- [2007, HTC] Charge Pump Voltage Converters (TJ7660)

Sandisk's diligent search and investigation to date has uncovered public information sufficient to prepare an initial limitation-by-limitation chart for four of these prior art systems, Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661, at least based on Sandisk's understanding of what is described in their respective data sheets. Based on the disclosures in the respective data sheets, each of those four systems uses one or more analog capacitors to create startup timing delays that control when regulation or clock transitions occur.

For instance, it appears that the SemTech SC603 is a versatile charge pump designed for use in battery operated power supply applications. It uses two tiny ceramic bucket capacitors that cause analog delays at startup, and it uses an FSEL input for frequency selection, allowing a microprocessor to change the charge pump frequency from 650kHz to 262 kHz depending upon capacitor values, load current, and acceptable amount of output ripple. *See* SemTech SC603 Data Sheet (SD_IPV_00019935 at 19939). Similarly, the Sipex SP6661 is a high frequency charge pump that can be implemented as either a voltage inverter or doubler. The device includes a frequency control input that can be used to change the frequency of the device's oscillator from, for example, 70kHz to 170kHz when used with 22µF capacitors and from 500kHz to 1250 kHz when used with 3.3µF capacitors. *See* Sipex SP6661 Data Sheet (SD_IPV_00019714 at 19715-19716). Texas Instruments' TPS65161 uses external soft-start (SS) and delay (DLY1/DLY2) capacitors to create analog timing delays during startup, and it has enable pins (EN1/EN2) and an internal clock-select multiplexer that together adjust the clock frequency based on the output of a comparator. *See* TI TPS65161 Data Sheet (SD_IPV_00019754 at 19766-1976). Finally, Intersil EL7583 appears to employ a startup oscillator and soft-start capacitor that creates a delay defining when the system switches from high-frequency startup mode to normal operation. *See* Intersil EL7583 (SD_IPV_00019839 at 19847). These features show systems where startup-controlled capacitive loads govern timing and clock behavior, as described at least under IPValue's broad reading of the Asserted Claims of the '664 patent.

As for the other systems listed, Sandisk's diligent search and investigation to date has not yet uncovered public information sufficient to prepare a limitation-by-limitation chart for these prior art systems. Sandisk will continue its diligent investigation into these prior art systems, which may include subpoenaing third parties likely to have information about these systems for information once Sandisk's searching of public repositories is exhausted. If and when additional information from and about these third parties' products becomes available, including through third-party subpoenas (regardless of whether charted herein), Sandisk reserves the right to seek leave of Court, consistent with the Patent Local Rules, to supplement, amend, and/or modify these contentions with further disclosures and/or charts regarding these systems.

* * *

In summary, each element of the Asserted Claims in the ’664 patent — including high/low frequency clocking, switch control logic, startup-triggered delays, and dynamic loads and switch-controlled capacitors — was known, disclosed, and routinely implemented by 2006. The disclosures from Sandisk (Pan), Toshiba (Shuto/Kawasaki), and others not only anticipated but emphasized these techniques as standard practice. These teachings were widespread and would have been obvious to a POSITA at the time of the alleged invention.

A skilled artisan at the time of the ’664 patent would have possessed and been familiar with at least the above-referenced subject matter when evaluating the prior art references cited and discussed herein.

4. Anticipation

Sandisk contends that each prior art reference and system (collectively, “references”) listed below anticipates one or more claims of the ’664 patent under at least 35 U.S.C. §§ 102(a), (b), (e), and/or (g).

Table #7
Anticipatory Reference
Arakawa
Bazargan
Cave
Fujioka
Kawajiri
Kawasaki
Maekawa

Shuto
Tasdighi
Ubata
Yamawaki

5. Obviousness

Sandisk provides the following legal background regarding obviousness and combinations. No showing of a specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts, as each combination of art would have yielded expected results and at most would simply represent a known alternative to one of skill in the art. *See Apple*, 839 F.3d at 1058; *Intercontinental Great Brands*, 869 F.3d at 1344; *KSR*, 127 S. Ct. at 1739–40 (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, and instead applying an "expansive and flexible" approach). Indeed, the Supreme Court held that a POSITA is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR*, 127 S.Ct. at 1742. Nevertheless, in addition to the information contained in the section immediately above and elsewhere in these contentions, Sandisk hereby identifies motivations and reasons to combine.

One or more combinations of the prior art references identified above would have been obvious because these references would have been combined using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. *See Apple*, 839 F.3d at 1077; *Intercontinental Great Brands*, 869 F.3d at 1344. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. *See ACCO*, 813 F.3d at 1367; *Sanofi*, 748 F.3d at 1360; *Bayer Pharma AG*, 874 F.3d at 1329; *KSR*, 127 S. Ct. at

1742. Further, the combinations of the prior art references identified above and in the claim charts would have been obvious because the combinations represent known potential options with a reasonable expectation of success. *See InTouch*, 751 F.3d at 1347.

Additional evidence that there would have been a motivation to combine the prior art references identified above includes the interrelated teachings of multiple prior art references; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the Asserted Claims of the '664 patent; the existence of a known need or problem in the field of the endeavor at the time of the alleged inventions; and the background knowledge that would have been possessed by a POSITA. *See Arctic Cat*, 876 F.3d at 1359; *Intercontinental Great Brands*, 869 F.3d at 1344; *Unwired Planet*, 841 F.3d at 1003; *Norgren*, 699 F.3d at 1322–23.

The motivation to combine the teachings of the prior art references disclosed herein is also found in the references themselves and in: (1) the nature of the problem being solved; (2) the express, implied and inherent teachings of the prior art; (3) the knowledge of POSITAs; (4) the predictable results obtained in combining the different elements of the prior art; (5) the predictable results obtained in simple substitution of one known element for another; (6) the use of a known technique to improve similar devices, methods, or products in the same way; (7) the predictable results obtained in applying a known technique to a known device, method, or product ready for improvement; (8) the finite number of identified predictable solutions that had a reasonable expectation of success; and (9) known work in various technological fields that could be applied to the same or different technological fields based on design incentives or other market forces.

a. 35 U.S.C. § 103 Obviousness References

To the extent that the Asserted Claims are deemed not to be anticipated, Sandisk contends that the Asserted Claims are invalid as obvious under 35 U.S.C. § 103 in view of at least the prior art listed herein and set forth in the attached Exhibits. Table 8 below identifies charted prior art that renders several of the asserted claims invalid under 35 U.S.C. § 103, either alone or in combination with the other references.

Table #8			
Prior Art Charted References and Combination Identification ’664 Patent			
Reference Name	**Reference**	**Claim Chart(s)**	**Exemplary Obviousness Combinations**[18]
Ubata	JP H6-149407 A	Exhibit No. 664-1	Obviousness combinations with one or more of at least the following: Folmsbee, Maekawa, Fujioka, Bazargan, Kawajiri, Shuto, Pan, Kawasaki, Cave, Yamawaki, Tasdighi, Arakawa, Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661
Folmsbee	US 5,386,151	Exhibit No. 664-2	Obviousness combinations with one or more of at least the following: Ubata, Maekawa, Fujioka, Bazargan, Kawajiri, Shuto, Pan, Kawasaki, Cave, Yamawaki, Tasdighi, Arakawa, Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661
Maekawa	US 2006/0267901 A1	Exhibit No. 664-3	Obviousness combinations with one or more of at least the following: Folmsbee, Ubata, Fujioka,

[18] Exemplary combinations for specific claim elements for each reference are identified in the respective claim charts as warranted. Sandisk lists such exemplary combinations out of an abundance of caution in the event that a factfinder deems a combination as required. Listing such exemplary obviousness combinations should not be construed as an admission that any such reference requires a combination for any element of the ’664 patent. As Sandisk has argued above and in the relevant claim charts, several of the references anticipate or themselves render the claims of the ’664 patent obvious without a combination of any other reference.

			Bazargan, Kawajiri, Shuto, Pan, Kawasaki, Cave, Yamawaki, Tasdighi, Arakawa, Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661
Fujioka	US 6,020,781	Exhibit No. 664-4	Obviousness combinations with one or more of at least the following: Folmsbee, Maekawa, Ubata, Bazargan, Kawajiri, Shuto, Pan, Kawasaki, Cave, Yamawaki, Tasdighi, Arakawa, Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661
Bazargan	US 6,300,839	Exhibit No. 664-5	Obviousness combinations with one or more of at least the following: Folmsbee, Maekawa, Fujioka, Ubata, Kawajiri, Shuto, Pan, Kawasaki, Cave, Yamawaki, Tasdighi, Arakawa, Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661
Kawajiri	US 7,251,162 B2	Exhibit No. 664-6	Obviousness combinations with one or more of at least the following: Folmsbee, Maekawa, Fujioka, Bazargan, Ubata, Shuto, Pan, Kawasaki, Cave, Yamawaki, Tasdighi, Arakawa, Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661
Shuto	JP 2005-76159	Exhibit No.	Obviousness combinations

		664-7	with one or more of at least the following: Folmsbee, Maekawa, Fujioka, Bazargan, Kawajiri, Ubata, Pan, Kawasaki, Cave, Yamawaki, Tasdighi, Arakawa, Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661
Pan	Charge Pump Circuit Design (McGraw-Hill Electronic Engineering)	Exhibit No. 664-8	Obviousness combinations with one or more of at least the following: Folmsbee, Maekawa, Fujioka, Bazargan, Kawajiri, Shuto, Ubata, Kawasaki, Cave, Yamawaki, Tasdighi, Arakawa, Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661
Kawasaki	US 5,587,683	Exhibit No. 664-9	Obviousness combinations with one or more of at least the following: Folmsbee, Maekawa, Fujioka, Bazargan, Kawajiri, Shuto, Pan, Ubata, Cave, Yamawaki, Tasdighi, Arakawa, Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661
Cave	US 5,694,308	Exhibit No. 664-10	Obviousness combinations with one or more of at least the following: Folmsbee, Maekawa, Fujioka, Bazargan, Kawajiri, Shuto, Pan, Kawasaki, Ubata, Yamawaki, Tasdighi, Arakawa, Texas

			Instruments TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661
Yamawaki	US 5,159,543	Exhibit No. 664-11	Obviousness combinations with one or more of at least the following: Folmsbee, Maekawa, Fujioka, Bazargan, Kawajiri, Shuto, Pan, Kawasaki, Cave, Ubata, Tasdighi, Arakawa, Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661
Tasdighi	US 5,734,291	Exhibit No. 664-12	Obviousness combinations with one or more of at least the following: Folmsbee, Maekawa, Fujioka, Bazargan, Kawajiri, Shuto, Pan, Kawasaki, Cave, Yamawaki, Ubata, Arakawa, Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661
Arakawa	US 5,883,501	Exhibit No. 664-13	Obviousness combinations with one or more of at least the following: Folmsbee, Maekawa, Fujioka, Bazargan, Kawajiri, Shuto, Pan, Kawasaki, Cave, Yamawaki, Tasdighi, Ubata, Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661
Sipex SP6661	SD_IPV_00019714-19781 (Data Sheet)	Exhibit No. 664-14	Obviousness combinations with one or more of at least the following: Folmsbee, Maekawa,

			Fujioka, Bazargan, Kawajiri, Shuto, Pan, Kawasaki, Cave, Yamawaki, Tasdighi, Ubata, Texas Instruments TPS65161, Intersil EL7583, and Semtech SC603,
SemTech SC603	SD_IPV_00019936-19948 (Data Sheet)	Exhibit No. 664-15	Obviousness combinations with one or more of at least the following: Folmsbee, Maekawa, Fujioka, Bazargan, Kawajiri, Shuto, Pan, Kawasaki, Cave, Yamawaki, Tasdighi, Ubata, , Texas Instruments TPS65161, Intersil EL7583, and Sipex SP6661
Texas Instruments TPS65161	SD_IPV_00019754-19781(Data Sheet)	Exhibit No. 664-16	Obviousness combinations with one or more of at least the following: Folmsbee, Maekawa, Fujioka, Bazargan, Kawajiri, Shuto, Pan, Kawasaki, Cave, Yamawaki, Tasdighi, Ubata, Intersil EL7583, Semtech SC603, and Sipex SP6661
Intersil EL7583	SD_IPV_19839-19853 (Data Sheet)	Exhibit No. 664-17	Obviousness combinations with one or more of at least the following: Folmsbee, Maekawa, Fujioka, Bazargan, Kawajiri, Shuto, Pan, Kawasaki, Cave, Yamawaki, Tasdighi, Ubata, Texas Instruments TPS65161, Semtech SC603, and Sipex SP6661

b. Exemplary Combinations and Motivation to Combine

Sandisk further sets forth below exemplary combinations of references that Sandisk contends render the Asserted Claims invalid as obvious. This disclosure is based on Sandisk's present understanding of the Asserted Claims and the apparent constructions that Sandisk believes IPValue may be asserting based on its Infringement Contentions. Each of the below exemplary combinations should be understood to include and incorporate the background knowledge of a person of ordinary skill in the art, such as (but not limited to) the background information detailed in the above State of the Art section of this pleading. In addition, each of the below exemplary combinations should also be understood to encompass any subset (*i.e.*, less than all) of the references identified in the combination, whether or not that particular subset is explicitly identified below.[19]

i. Primary Reference: Fujioka

Fujioka discloses and teaches a charge pump circuit that includes a selection control circuit generating a startup signal (STP), which is supplied to a selection circuit that initially selects a high-frequency clock during startup and, as V_{cc} rises, switches to a low-frequency clock for normal continued operation. The STP signal is produced in response to the changing supply voltage—*i.e.*, a dynamic load condition. Fujioka also discloses switch-controlled capacitors that charge and discharge under the control of these clock signals. Accordingly, Fujioka anticipates or, at minimum, renders obvious every element of the Asserted Claims, including the startup-controlled clock selection, the dynamic-load-based switching behavior, and the presence of switch-controlled capacitors.

But, to the extent any individual element or claim is found not to be anticipated and/or obvious in light of this reference, a POSITA would have been motivated to combine Fujioka with any other reference(s) in Table 8. For example, one of ordinary skill in the art would have been motivated to combine Fujioka with at least the following references, and would have had a

[19] As a non-limiting example, a particular reference identified in a given combination may be necessary for that combination to render obvious some Asserted Claims but not others, in which case Defendants may, depending on the Asserted Claim, assert invalidity due to obviousness based on the combination with and without that particular reference.

reasonable expectation of success in doing so:

- Fujioka + Bazargan
- Fujioka + Bazargan + Pan
- Fujioka + Bazargan + Arakawa
- Fujioka + Maekawa
- Fujioka + Bazargan + Maekawa
- Fujioka + Arakawa
- Fujioka + Cave
- Fujioka + Cave + Ubata
- Fujioka + Shuto
- Fujioka + Kawasaki + Shuto
- Fujioka + Ubata
- Fujioka + Ubata + Bazargan
- Fujioka + Folmsbee
- Fujioka + Yamawaki
- Fujioka + Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and/or Sipex SP6661

A skilled artisan would have been motivated to combine any of the above references with Fujioka, and would have found it easy and obvious to do so, at least because it would amount to no more than combining prior art elements according to known methods to yield predictable results, simple substitution of one known element for another to obtain predictable results, using known technique to improve similar devices (methods, or products) in the same way, applying a known technique to a known device (method, or product) ready for improvement to yield predictable results, an "obvious to try" option—*i.e.*, choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success, and/or using known work in one field of endeavor that prompts variations of it for use in either the same field or a different one based on design incentives or other market forces.

For example, each of the above references are directed to the same field, which here is electronic voltage boosting circuits, such as charge pumps and booster circuits used to generate higher or regulated supply voltages in integrated circuits. Moreover, the references are all aimed at addressing the same or similar problem - balancing the tradeoffs in charge pump or booster circuits between startup time, power consumption, and voltage maintenance. Thus, each reference presents an obvious to try variation of a finite number of predictable solutions, such as varying clock frequency dynamically according to changing load conditions.

As a specific example, and without limitation, a POSITA would have been motivated to combine Fujioka's startup-controlled dual-oscillator system with Bazargan's switched-capacitor load control circuits in view of Pan's 2006 textbook guidance. All three address the same well-known design goal—achieving fast charge-pump startup while minimizing steady-state power consumption. Fujioka provides the startup-detection and control logic (STP signal selecting high-then low-frequency clocks). Bazargan teaches load-control circuits with switch-controlled capacitors that vary oscillator loading in response to output voltage and inherently introduce analog delays based on those voltage changes. A POSITA would recognize that coupling Bazargan's load-control circuits with Fujioka's STP-control path would allow the same analog delay effects to shape the timing of the startup transition—producing a smoother, dynamically tuned shift from high- to low-frequency operation. Pan confirms the motivation for this combination, explaining that running a charge pump at a higher frequency during startup and reducing the frequency after regulation is a standard and advantageous design practice. Integrating Bazargan's load-control delays into Fujioka's startup-based switching would therefore yield predictable improvements in startup control, timing, and power efficiency.

A POSITA would be similarly motivated to combine Fujioka's high–low frequency control logic with Arakawa's power-on circuit, Cave's startup timing circuit, Shuto's delay circuit, and Maekawa's clock-delay circuitry and voltage detection, because each addresses the same design goal—controlling oscillator operation during startup to achieve rapid voltage ramp-up, followed by stable steady-state performance. Arakawa provides a timed power-on enable signal, Cave supplies an RC-based startup timing network that governs oscillator load, Shuto teaches a voltage-dependent delay circuit that dynamically adjusts clock frequency, Maekawa adds a comparator-based voltage detection to control the precise moment of frequency switching after startup, and Folmsbee discloses a low-voltage MOS charge pump using p-well-driven capacitors whose wells are toggled by transistor switches responsive to clock signals. And each of the four system references—TI TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661—appear to use one or more analog capacitors to create startup timing delays that control when regulation or clock transitions occur. A POSITA would recognize that integrating Fujioka's frequency-selection logic with any of these well-known startup, delay, or load-based response mechanisms would yield predictable improvements in startup control and power efficiency using routine design techniques.

Each of the listed combinations satisfy the elements of the Asserted Claims, and Sandisk reserves the right to supplement, amend, or refine its contentions, including its combinations and motivations to combine, in light of further discovery, expert analysis, developments in the record, or claim construction.

ii. Primary Reference: Bazargan

Bazargan discloses and teaches a frequency-controlled system for positive voltage regulation in which a regulation circuit 301 (analogous to the '664 patent's clock-control circuit) monitors the pumped voltage and provides control signals to both the selection circuitry 701 and the ring oscillator 302 (analogous to the '664 patents clock driver circuit). The regulation circuit includes multiple differential amplifiers 305A-305C that each receive an internal voltage from a voltage divider 304 and a distinct reference voltage. Based on these comparisons, the regulation circuit outputs logic signals to the selection circuitry, which in turn selects the appropriate frequency of the ring oscillator. The ring oscillator drives the charge pump at a frequency determined by these control signals so that the oscillator and pump slow down or speed up in direct correlation with changes in the output voltage. Each oscillator stage includes load-control circuits 601 with pass gates and capacitors 605 that are switched in or out according to the differential-amplifier outputs, thereby varying the oscillator's capacitive load and frequency. Accordingly, Bazargan anticipates or, at minimum, renders obvious every element of the Asserted Claims, including the startup-controlled clock selection, the dynamic-load-based switching behavior, and the presence of switch-controlled capacitors.

But, to the extent any individual element or claim is found not to be anticipated and/or obvious in light of this reference, a POSITA would have been motivated to combine Bazargan with any other reference(s) in Table 8. For example, one of ordinary skill in the art would have been motivated to combine Bazargan with at least the following references, and would have had a reasonable expectation of success in doing so:[20]

- Bazargan + Kawasaki + Pan
- Bazargan + Cave
- Bazargan + Maekawa + Fujioka
- Bazargan + Kawajiri
- Bazargan + Ubata
- Bazargan + Arakawa
- Bazargan + Yamawaki
- Bazargan + Folmsbee
- Bazargan + Fujioka
- Bazargan + Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and/or Sipex SP6661

A skilled artisan would have been motivated to combine any of the above references with Bazargan and would have found it easy and obvious to do so, at least because it would amount to no more than combining prior art elements according to known methods to yield predictable results, simple substitution of one known element for another to obtain predictable results, using known technique to improve similar devices (methods, or products) in the same way, applying a known technique to a known device (method, or product) ready for improvement to yield predictable results, an "obvious to try" option—*i.e.*, choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success, and/or using known work in one

[20] To avoid unnecessary repetition, combinations previously identified and discussed in connection with an earlier primary reference are not restated again under later-discussed primary references. All such previously listed combinations are hereby incorporated by reference as if fully set forth in each corresponding section, including the rationale for motivation to combine.

field of endeavor that prompts variations of it for use in either the same field or a different one based on design incentives or other market forces.

For example, each of the above references are directed to the same field, which here is electronic voltage boosting circuits, such as charge pumps and booster circuits used to generate higher or regulated supply voltages in integrated circuits. Moreover, the references are all aimed at addressing the same or similar problem - balancing the tradeoffs in charge pump or booster circuits between startup time, power consumption, and voltage maintenance. Thus, each reference presents an obvious to try variation of a finite number of predictable solutions, such as varying clock frequency dynamically according to changing load conditions.

As a specific example, and without limitation, a POSITA would have been motivated to combine Bazargan with Kawasaki and Pan, because each teaches compatible aspects of dynamic frequency control in charge pump circuits. Bazargan teaches load-control circuits with switch-controlled capacitors that add or remove capacitive load on the oscillator stages that determine how quickly the oscillator responds to changes in output voltage. A POSITA would recognize that these same load-control circuits could be used in the startup-control path of Kawasaki's two-clock system, where their analog delay characteristics would naturally influence the timing of the startup signal and the transition between the high- and low-frequency clocks. Pan further motivates this design choice by explaining that running a pump at a higher frequency during startup and reducing the frequency as the output stabilizes is a well-known and desirable design practice. Integrating Bazargan's delayed, voltage-responsive load-control circuits into Kawasaki's clock-selection logic would yield predictable improvements in timing precision, startup smoothness, and power efficiency.

A POSITA would be similarly motivated to combine Bazargan with other references listed because integrating Bazargan's voltage-sensing and load-control circuits with the other references' startup or frequency-selection mechanisms, Folmsbee's low-voltage MOS charge pump, and/or the various systems' (TI TPS65161, Intersil EL7583, Semtech SC603, and/or Sipex SP6661) analog capacitors that create startup timing delays that are similar to the load control circuits Bazargan already implements, as doing so would produce predictable improvements in timing precision, startup stability, and overall efficiency.

Each of the listed combinations satisfy the elements of the asserted claims, and Sandisk reserves the right to supplement, amend, or refine its contentions, including its combinations and motivations to combine, in light of further discovery, expert analysis, developments in the record, or claim construction.

iii. Primary Reference: Kawasaki

Kawasaki discloses and teaches a "booster circuit device" in which a timing circuit outputs a select signal according to the dissipated current of a liquid crystal display drive circuit. The drive signal select circuit then selects and outputs one of at least two drive signals—a high-frequency clock when the dissipated current is large and a low-frequency clock when the dissipated current is small—based on the select signal from the timing circuit. Further embodiments include a comparator circuit (22), delay circuit (24), and adder circuit (25) that cooperate to control the drive signal select circuit (27) to adjust the clock frequency until the boosted voltage reaches a reference voltage. The delay circuit (24) introduces a resistor-capacitor (RC)-type analog delay to control the timing of the frequency-selection signal. Accordingly, Kawasaki anticipates or, at minimum, renders obvious every element of the asserted claims, including the startup-controlled clock selection, the dynamic-load-based switching behavior, and the presence of switch-controlled capacitors.

But, to the extent any individual element or claim is found not to be anticipated and/or obvious in light of this reference, one of ordinary skill in the art would have been motivated to combine Kawasaki with any other reference(s) in Table 8. For example, one of ordinary skill in the art would have been motivated to combine Kawasaki with at least the following references, and would have had a reasonable expectation of success in doing so:

- Kawasaki + Shuto
- Kawasaki + Shuto + Pan
- Kawasaki + Cave
- Kawasaki + Yamawaki
- Kawasaki + Yamawaki + Bazargan

- Kawasaki + Tashdighi + Shuto
- Kawasaki + Arakawa
- Kawasaki + Maekawa
- Kawasaki + Maekawa + Bazargan
- Kawasaki + Maekawa + Shuto
- Kawasaki + Folmsbee
- Kawasaki + + Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and/or Sipex SP6661

A skilled artisan would have been motivated to combine any of the above references with Kawasaki and would have found it easy and obvious to do so, at least because it would amount to no more than combining prior art elements according to known methods to yield predictable results, simple substitution of one known element for another to obtain predictable results, using known technique to improve similar devices (methods, or products) in the same way, applying a known technique to a known device (method, or product) ready for improvement to yield predictable results, an "obvious to try" option—*i.e.*, choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success, and/or using known work in one field of endeavor that prompts variations of it for use in either the same field or a different one based on design incentives or other market forces.

For example, each of the above references are directed to the same field, which here is electronic voltage boosting circuits, such as charge pumps and booster circuits used to generate higher or regulated supply voltages in integrated circuits. Moreover, the references are all aimed at addressing the same or similar problem - balancing the tradeoffs in charge pump or booster circuits between startup time, power consumption, and voltage maintenance. Thus, each reference presents an obvious to try variation of a finite number of predictable solutions, such as varying clock frequency dynamically according to changing load conditions.

As one specific example, and without limitation, a POSITA would have been motivated to combine Kawasaki, Shuto, and Pan because all three references originate from the same Toshiba–

Sandisk design lineage and address the same problem—precise, startup-based control of charge-pump frequency to achieve fast voltage ramp-up and low steady-state power consumption. Kawasaki provides the foundational two-clock frequency-selection architecture in which a timing circuit and drive-signal-select circuit control high- and low-frequency clocks based on load current and voltage. Shuto, a later Toshiba patent, refines this approach by incorporating a voltage-dependent RC delay circuit that adjusts oscillator timing and frequency dynamically as supply voltage changes. Pan, authored by Sandisk engineers working in the same joint-venture field, confirms that operating a charge pump at a higher frequency during startup and reducing frequency as the output stabilizes was a recognized and widely practiced design principle. A POSITA would have viewed these teachings as complementary developments within a continuous corporate research stream and would have combined them to achieve predictable improvements in startup timing, load-dependent control, and power efficiency using routine circuit-integration techniques.

A POSITA would be similarly motivated to combine Kawasaki with the other references listed because each contributes a complementary aspect of frequency and startup control that builds on Kawasaki's dual-clock, load-responsive system. Folmsbee provides the underlying charge-pump configuration, while Bazargan adds a voltage-sensing load-control circuit. In turn, Cave, Shuto, Maekawa, Arakawa, and the system references (such as TI TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661) each offer delay and timing circuits that refine startup operation and determine when the frequency transition occurs. Collectively, these teachings would predictably improve Kawasaki's startup timing, voltage regulation, and efficiency through known, compatible circuit-integration techniques.

Each of the listed combinations satisfy the elements of the asserted claims, and Sandisk reserves the right to supplement, amend, or refine its contentions, including its combinations and motivations to combine, in light of further discovery, expert analysis, developments in the record, or claim construction.

iv. Primary Reference: Arakawa

Arakawa discloses and teaches a power supply circuit with an operation control circuit to control the operation of an oscillator, a comparator, and a reference voltage generator by generating a pump enable signal. A power-on control circuit further outputs a signal (PON) to activate the booster circuit for a set interval, allowing rapid rise of the boosted voltage after powering on. Accordingly, Arakawa anticipates or, at minimum, renders obvious every element of the asserted claims, including the startup-controlled clock selection, the dynamic-load-based switching behavior, and the presence of switch-controlled capacitors.

But, to the extent any individual element or claim is found not to be anticipated and/or obvious in light of this reference, a POSITA would have been motivated to combine Arakawa with any other reference(s) in Table 8. For example, one of ordinary skill in the art would have been motivated to combine Arakawa with at least the following references, and would have had a reasonable expectation of success in doing so:

- Arakawa + Ubata
- Arakawa + Ubata + Folmsbee
- Arakawa + Cave
- Arakawa + Cave + Folmsbee
- Arakawa + Kawajiri + Fujioka
- Arakawa + Ubata + Shuto
- Arakawa + Tasdighi + Shuto
- Arakawa + Yamawaki + Shuto
- Arakawa + Maekawa + Ubata
- Arakawa + Yamawaki
- Arakawa + Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and/or Sipex SP6661

A skilled artisan would have been motivated to combine any of the above references with Arakawa and would have found it easy and obvious to do so, at least because it would amount to no more than combining prior art elements according to known methods to yield predictable results, simple substitution of one known element for another to obtain predictable results, using known technique to improve similar devices (methods, or products) in the same way, applying a known technique to a known device (method, or product) ready for improvement to yield predictable results, an "obvious to try" option—*i.e.*, choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success, and/or using known work in one field of endeavor that prompts variations of it for use in either the same field or a different one based on design incentives or other market forces.

For example, each of the above references are directed to the same field, which here is electronic voltage boosting circuits, such as charge pumps and booster circuits used to generate higher or regulated supply voltages in integrated circuits. Moreover, the references are all aimed at addressing the same or similar problem - balancing the tradeoffs in charge pump or booster circuits between startup time, power consumption, and voltage maintenance. Thus, each reference presents an obvious to try variation of a finite number of predictable solutions, such as varying clock frequency dynamically according to changing load conditions.

As a specific example, and without limitation, a POSITA would have been motivated to combine Arakawa and Ubata because each teaches complementary startup-control techniques for charge-pump and voltage-booster systems. Ubata provides the foundational architecture with a control-signal generation circuit that detects the operating state and selects between internal and external clock sources to enable or halt the oscillator during standby and startup. Arakawa adds a power-on control and enable-signal generator that employs a delay circuit formed by a resistor–capacitor (RC) network—*i.e.*, a switch-controlled capacitor—to create a timed analog pulse defining how long the oscillator and booster remain active at startup. A POSITA would have recognized that incorporating Arakawa's RC-based, switch-controlled capacitor delay into Ubata's clock-selection and startup logic would yield predictable benefits, including smoother startup timing, reduced power consumption, and faster transition to steady-state operation using routine techniques.

A POSITA would be similarly motivated to combine Arakawa with other references listed because each provides explicit clock-control or frequency-selection logic that complements Arakawa's power-on and RC-based startup circuitry. References such as Cave, Kawajiri, Fujioka, Tasdighi, and Yamawaki teach dual-oscillator or clock-selection mechanisms for switching between high- and low-frequency inputs based on startup or load conditions, while Shuto, Maekawa, and the system references (such as TI TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661) add voltage-detection and delay-control logic that governs when such switching occurs, and Folmsbee provides the underlying charge pump configuration. Integrating Arakawa's RC-based, switch-controlled capacitor delay circuit with these well-established frequency-selection systems would have yielded predictable improvements in startup timing, clock-transition control, and power efficiency using known techniques.

Each of the listed combinations satisfy the elements of the asserted claims, and Sandisk reserves the right to supplement, amend, or refine its contentions, including its combinations and motivations to combine, in light of further discovery, expert analysis, developments in the record, or claim construction.

v. Primary Reference: Cave

Cave discloses and teaches a self-starting low voltage charge pump control circuit comprising a start-up clock circuit that includes a ring oscillator formed by resistors, capacitors, and inverters that generate an internal clock signal having two resistor–capacitor (RC) time constants. This oscillator produces a startup clock that operates at a frequency determined by those RC time constants until an external clock becomes available. The clock signal multiplexer then switches control to the external clock once the output voltage reaches a predetermined threshold. Accordingly, Cave anticipates or, at minimum, renders obvious every element of the Asserted Claims, including the startup-controlled clock selection, the dynamic-load-based switching behavior, and the presence of switch-controlled capacitors.

But, to the extent that any individual element or claim is found not to be anticipated and/or obvious in light of this reference, a POSITA would have been motivated to combine Cave with any other reference(s) in Table 8. For example, one of ordinary skill in the art would have been motivated to combine Cave with at least the following references, and would have had a reasonable expectation of success in doing so:

- Cave + Ubata
- Cave + Ubata + Folmsbee

- Cave + Fujioka + Ubata
- Cave + Kawasaki + Folmsbee
- Cave + Kawasaki + Kawajiri
- Cave + Maekawa
- Cave + Maekawa + Yamawaki
- Cave + Yamawaki
- Cave + Yamawaki + Folmsbee
- Cave + Tasdighi
- Cave + Tasdighi + Folmsbee
- Cave + Shuto
- Cave + Shuto + Folmsbee
- Cave + Kawajiri
- Cave + Kawajiri + Fujioka
- Cave + Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and/or Sipex SP6661

A skilled artisan would have been motivated to combine any of the above references with Cave and would have found it easy and obvious to do so, at least because it would amount to no more than combining prior art elements according to known methods to yield predictable results, simple substitution of one known element for another to obtain predictable results, using known technique to improve similar devices (methods, or products) in the same way, applying a known technique to a known device (method, or product) ready for improvement to yield predictable results, an "obvious to try" option—*i.e.*, choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success, and/or using known work in one field of endeavor that prompts variations of it for use in either the same field or a different one based on design incentives or other market forces.

For example, each of the above references are directed to the same field, which here is electronic voltage boosting circuits, such as charge pumps and booster circuits used to generate higher or regulated supply voltages in integrated circuits. Moreover, the references are all aimed at addressing the same or similar problem - balancing the tradeoffs in charge pump or booster circuits between startup time, power consumption, and voltage maintenance. Thus, each reference presents an obvious to try variation of a finite number of predictable solutions, such as varying clock frequency dynamically according to changing load conditions.

As a specific example, and without limitation, a POSITA would have been motivated to combine Cave with Ubata because a POSITA would have seen Cave's internal-/external-clock ring-oscillator startup circuit as directly compatible with Ubata's two-clock selection scheme that likewise involves an internal oscillator and external clock source. Integrating the two would simply use Cave's RC-timed oscillator as the internal high-frequency clock in Ubata's selection logic. The analog timing characteristics from Cave's switched-capacitor network would refine Ubata's startup transition, providing smoother hand-off between the internal and external clocks.

A POSITA would be similarly motivated to combine Cave with other references listed at least because each provides complementary clock-control or startup mechanisms that align with Cave's internal/external clock and RC-based startup oscillator. References such as Fujioka, Ubata, Kawasaki, Yamawaki, Tasdighi, and Kawajiri supply explicit logic for switching between high- and low-frequency clocks; Maekawa, Shuto, and the system references (such as TI TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661) add voltage-detection or delay circuits that govern when that switching occurs; and Folmsbee reinforces standard charge-pump regulation using capacitor-based timing. Integrating these teachings with Cave's ring-oscillator and RC-timing structure would predictably enhance startup control, clock-transition precision, and overall voltage regulation.

Each of the listed combinations satisfy the elements of the Asserted Claims, and Sandisk reserves the right to supplement, amend, or refine its contentions, including its combinations and motivations to combine, in light of further discovery, expert analysis, developments in the record, or claim construction.

vi. Primary Reference: Ubata

Ubata discloses and teaches a semiconductor integrated circuit having a charge pump driven by either a first clock generated from an external clock or a second, higher-frequency clock generated by an internal oscillator. A selection circuit chooses which clock signal drives the pump based on a control signal from a control-signal generator. In one embodiment, a count-up timer (4) counts the oscillations of the internal clock and, after a predetermined number, outputs an end signal that causes the circuit to switch from the internal clock to the external clock. In another embodiment, Ubata replaces the count-up timer with a current-mirror circuit that monitors the level of the boosted voltage VPM; when VPM reaches VDD, the current-mirror output resets the selection signal and switches the pump input from the high-frequency internal clock to the lower-frequency external clock. Accordingly, Ubata anticipates or, at minimum, renders obvious every element of the Asserted Claims, including the startup-controlled clock selection, the dynamic-load-based switching behavior, and the presence of switch-controlled capacitors.

But, to the extent any individual element or claim is found not to be anticipated and/or obvious in light of this reference, a POSITA would have been motivated to combine Ubata with any other reference(s) in Table 8. For example, one of ordinary skill in the art would have been motivated to combine Ubata with at least the following references, and would have had a reasonable expectation of success in doing so:

- Ubata + Folmsbee
- Ubata + Kawasaki
- Ubata + Kawasaki + Bazargan
- Ubata + Shuto
- Ubata + Fujioka
- Ubata + Maekawa
- Ubata + Maekawa + Shuto
- Ubata + Maekawa + Bazargan
- Ubata + Yamawaki
- Ubata + Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and/or Sipex SP6661

A skilled artisan would have been motivated to combine any of the above references with Ubata and would have found it easy and obvious to do so, at least because it would amount to no more than combining prior art elements according to known methods to yield predictable results, simple substitution of one known element for another to obtain predictable results, using known technique to improve similar devices (methods, or products) in the same way, applying a known technique to a known device (method, or product) ready for improvement to yield predictable results, an "obvious to try" option—*i.e.*, choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success, and/or using known work in one field of endeavor that prompts variations of it for use in either the same field or a different one based on design incentives or other market forces.

For example, each of the above references are directed to the same field, which here is electronic voltage boosting circuits, such as charge pumps and booster circuits used to generate higher or regulated supply voltages in integrated circuits. Moreover, the references are all aimed at addressing the same or similar problem - balancing the tradeoffs in charge pump or booster circuits between startup time, power consumption, and voltage maintenance. Thus, each reference presents an obvious to try variation of a finite number of predictable solutions, such as varying clock frequency dynamically according to changing load conditions.

As a specific example, and without limitation, a POSITA would have been motivated to combine Ubata and Folmsbee because each discloses complementary aspects of charge-pump operation and control that together address the same goal of efficient, load-responsive voltage boosting. Ubata provides the startup and frequency-selection architecture, while Folmsbee supplies the underlying charge-pump structure employing switch-controlled capacitors that alternately charge and discharge under the control of clock phases to generate a boosted voltage. A POSITA would have recognized that integrating Folmsbee's switch-controlled capacitor network into Ubata's dual-clock, voltage-dependent control scheme would produce a predictable improvement in startup response, regulation accuracy, and power efficiency, fully within the skill of the art and consistent with standard charge-pump design practices.

A POSITA would be similarly motivated to combine Ubata with other references listed because each teaches compatible methods for controlling charge-pump frequency and operation during startup. Kawasaki, Shuto, Bazargan, and the system references (such as TI TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661) each provide dynamic, load-dependent frequency and voltage-regulation circuitry that could be driven by Ubata's dual-clock selection logic to achieve finer control of startup transitions.

Each of the listed combinations satisfy the elements of the Asserted Claims, and Sandisk reserves the right to supplement, amend, or refine its contentions, including its combinations and motivations to combine, in light of further discovery, expert analysis, developments in the record, or claim construction.

vii. Primary Reference: Maekawa

Maekawa discloses and teaches a reference clock signal generation circuit, an oscillation circuit, and a charge pump circuit driven by switch devices controlled by the generated reference clock signal. During a start period from the beginning of the charge-pump operation to completion of the wait time, the circuit outputs a clock signal having a first (higher) frequency; after that period, it outputs a second (lower) frequency during steady-state operation. The circuit further includes a counter, comparator, and switch circuit that cooperate to change the clock-selection control signal (SCO) after the wait time elapses or once the boosted output voltage reaches a predetermined level, thereby switching between clocks of different frequencies. The charge-pump circuit uses switched capacitors that alternately charge and discharge according to the clock phases. Accordingly, Maekawa anticipates or, at minimum, renders obvious every element of the Asserted Claims, including the startup-controlled clock selection, the dynamic-load-based switching behavior, and the presence of switch-controlled capacitors.

But, to the extent any individual element or claim is found not to be anticipated and/or obvious in light of this reference, a POSITA would have been motivated to combine Maekawa with any other reference(s) in Table 8. For example, one of ordinary skill in the art would have been motivated to combine Maekawa with at least the following references, and would have had a reasonable expectation of success in doing so:

- Maekawa + Shuto

- Maekawa + Bazargan
- Maekawa + Bazargan + Shuto
- Maekawa + Cave
- Maekawa + Cave + Tasdighi
- Maekawa + Cave + Yamawaki
- Maekawa + Yamawaki
- Maekawa + Kawajiri
- Maekawa + Kawajiri + Kawasaki
- Maekawa + Tasdighi
- Maekawa + Tasdighi + Shuto
- Maekawa + Yamawaki + Pan
- Maekawa + Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and/or Sipex SP6661

A skilled artisan would have been motivated to combine any of the above references with Maekawa and would have found it easy and obvious to do so, at least because it would amount to no more than combining prior art elements according to known methods to yield predictable results, simple substitution of one known element for another to obtain predictable results, using known technique to improve similar devices (methods, or products) in the same way, applying a known technique to a known device (method, or product) ready for improvement to yield predictable results, an "obvious to try" option—*i.e.*, choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success, and/or using known work in one field of endeavor that prompts variations of it for use in either the same field or a different one based on design incentives or other market forces.

For example, each of the above references are directed to the same field, which here is electronic voltage boosting circuits, such as charge pumps and booster circuits used to generate higher or regulated supply voltages in integrated circuits. Moreover, the references are all aimed at addressing the same or similar problem - balancing the tradeoffs in charge pump or booster circuits between startup time, power consumption, and voltage maintenance. Thus, each reference presents an obvious to try variation of a finite number of predictable solutions, such as varying clock frequency dynamically according to changing load conditions.

As a specific example, and without limitation, a POSITA would have been motivated to combine Maekawa and Shuto because each teaches complementary mechanisms for voltage-based and delay-controlled frequency switching in charge-pump power-supply circuits. A POSITA would have recognized that integrating Shuto's analog, voltage-responsive RC delay circuit with Maekawa's voltage-detection and frequency-selection architecture would yield predictable improvements. In addition, or alternatively, Bazargan's load-control circuit, which varies oscillator loading through switch-controlled capacitors, could be incorporated into Maekawa's design to provide an analog delay element that determines the precise timing of the clock event.

A POSITA would be similarly motivated to combine Maekawa with the other references listed because each contributes features that enhance or parallel Maekawa's dual-frequency, voltage-dependent clock-control system. References such as Cave, Yamawaki, Kawasaki, Kawajiri, and Tasdighi provide explicit dual-clock architecture and/or switching logic for selecting between high- and low-frequency clock inputs, while Cave and Shuto also include capacitors and RC networks within the oscillator path that establish startup timing. And the system references (such as TI TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661) offer delay and timing circuits that refine startup operation and determine when the frequency transition occurs. Integrating these complementary teachings with Maekawa's reference-clock generation circuit would predictably yield improved control over the timing and transition between multiple clock sources.

Each of the listed combinations satisfy the elements of the Asserted Claims, and Sandisk reserves the right to supplement, amend, or refine its contentions, including its combinations and motivations to combine, in light of further discovery, expert analysis, developments in the record, or claim construction.

viii. Primary Reference: Kawajiri

Kawajiri discloses and teaches a semiconductor integrated circuit device that includes a write state machine, an oscillator, low-frequency and high-frequency clock control signals (CL, CH, NAND circuits, a charge pump, and a comparator configured to generate a boosted voltage (V_{pp}) used in flash memory (and EEPROM). The comparator detects when V_{pp} reaches the threshold voltage and outputs a detection signal that triggers the change in clock frequency. In fact, the Kawajiri patent itself is very aptly entitled "Nonvolatile Memory with Multi-Frequency Charge Pump Control" and therefore this patent title itself discloses a "Multi-Frequency Charge Pump" in the context of "Nonvolatile Memory" (i.e. flash memory). Accordingly, Kawajiri anticipates or, at minimum, renders obvious every element of the Asserted Claims, including the startup-controlled clock selection, the dynamic-load-based switching behavior, and the presence of switch-controlled capacitors.

But, to the extent that any individual element or claim is found not to be anticipated and/or obvious in light of this reference, a POSITA would have been motivated to combine Kawajiri with any other reference(s) in Table 8. For example, one of ordinary skill in the art would have been motivated to combine Kawajiri with at least the following references, and would have had a reasonable expectation of success in doing so:

- Kawajiri + Bazargan
- Kawajiri + Bazargan + Cave
- Kawajiri + Cave
- Kawajiri + Kawasaki + Shuto
- Kawajiri + Tasdighi
- Kawajiri + Tasdighi + Shuto
- Kawajiri + Yamawaki
- Kawajiri +Yamawaki + Arakawa
- Kawajiri + Cave + Pan
- Kawajiri + Bazargan + Ubata
- Kawajiri + Bazargan + Fujioka

- Kawajiri + Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and/or Sipex SP6661

A POSITA would have been motivated to combine any of the above references with Kawajiri, and would have found it easy and obvious to do so, at least because it would amount to no more than combining prior art elements according to known methods to yield predictable results, simple substitution of one known element for another to obtain predictable results, using known technique to improve similar devices (methods, or products) in the same way, applying a known technique to a known device (method, or product) ready for improvement to yield predictable results, an "obvious to try" option—*i.e.*, choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success, and/or using known work in one field of endeavor that prompts variations of it for use in either the same field or a different one based on design incentives or other market forces.

For example, each of the above references are directed to the same field, which here is electronic voltage boosting circuits, such as charge pumps and booster circuits used to generate higher or regulated supply voltages in integrated circuits. Moreover, the references are all aimed at addressing the same or similar problem - balancing the tradeoffs in charge pump or booster circuits between startup time, power consumption, and voltage maintenance. Thus, each reference presents an obvious to try variation of a finite number of predictable solutions, such as varying clock frequency dynamically according to changing load conditions.

As a specific example, and without limitation, a POSITA would have been motivated to combine Kawajiri's dual-frequency control system with Bazargan's voltage-responsive load-control circuits and Cave's RC-timed startup oscillator because it would predictably improve frequency-transition timing, startup stability, and voltage regulation using known techniques.

A POSITA would be similarly motivated to combine Kawajiri with other references listed because each provides complementary features that refine or clarify Kawajiri's frequency-control system. References such as Kawasaki, Tasdighi, Ubata, and Fujioka, explicitly disclose two distinct clock sources and control logic, while Pan explains the need for switching and the tradeoffs of doing so at different times. References including Shuto, Cave, Bazargan, Arakawa, and the system references (such as TI TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661) contribute voltage-dependent or RC-based capacitive load circuits that introduce timing delays and/or dynamic-load adjustments directly in the oscillator or clock path. Integrating these mechanisms with Kawajiri's frequency-control framework would predictably enhance startup precision, transition timing, and power efficiency using routine techniques.

Each of the listed combinations satisfy the elements of the Asserted Claims, and Sandisk reserves the right to supplement, amend, or refine its contentions, including its combinations and motivations to combine, in light of further discovery, expert analysis, developments in the record, or claim construction.

ix. Primary Reference: Shuto

Shuto discloses and teaches a non-volatile semiconductor memory device having a boosting means driven by a clock signal, a clock signal generator that includes a ring oscillator, and a supply-voltage detector that outputs a detection signal (V_{out}) to control the oscillator. Each inverter in the ring oscillator includes a delay circuit (35a) with switch elements (SW1–SW3), a resistor (R1), and a capacitor (C1) forming an RC delay circuit (40) that is connected or disconnected based on Vout, thereby changing the oscillator's delay time and frequency according to the supply voltage. When Vcc is low, the clock frequency is switched to a higher frequency (f1), and when Vcc is high, it switches to a lower frequency (f2) to balance startup speed and power consumption. The boosting circuit uses capacitors (C2–C4) that alternately charge and discharge under the clock signals. Accordingly, Shuto anticipates or, at minimum, renders obvious every element of the Asserted Claims, including the startup-controlled clock selection, the dynamic-load-based switching behavior, and the presence of switch-controlled capacitors.

But, to the extent any individual element or claim is found not to be anticipated and/or obvious in light of this reference, a POSITA would have been motivated to combine Shuto with any other reference(s) in Table 8. For example, one of ordinary skill in the art would have been motivated to combine Shuto with at least the following references, and would have had a reasonable expectation of success in doing so:

- Shuto + Tasdighi
- Shuto + Yamawaki
- Shuto + Tasdighi + Yamawaki
- Shuto + Texas Instruments TPS65161, Intersil EL7583, Semtech SC603, and/or Sipex SP6661

A POSITA would have been motivated to combine any of the above references with Shuto and would have found it easy and obvious to do so, at least because it would amount to no more than combining prior art elements according to known methods to yield predictable results, simple substitution of one known element for another to obtain predictable results, using known technique to improve similar devices (methods, or products) in the same way, applying a known technique to a known device (method, or product) ready for improvement to yield predictable results, an "obvious to try" option—*i.e.*, choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success, and/or using known work in one field of endeavor that prompts variations of it for use in either the same field or a different one based on design incentives or other market forces.

For example, each of the above references are directed to the same field, which here is electronic voltage boosting circuits, such as charge pumps and booster circuits used to generate higher or regulated supply voltages in integrated circuits. Moreover, the references are all aimed at addressing the same or similar problem—balancing the tradeoffs in charge pump or booster circuits between startup time, power consumption, and voltage maintenance. Thus, each reference presents an obvious to try variation of a finite number of predictable solutions, such as varying clock frequency dynamically according to changing load conditions.

As a specific example, and without limitation, a POSITA would have been motivated to combine Shuto with Tasdighi and/or with Yamawaki because each teaches complementary techniques for controlling charge-pump frequency through startup-based clock switching. Tasdighi and Yamawaki disclose discrete selection between high- and low-frequency clocks depending on mode or voltage level, while Shuto introduces a voltage-dependent RC delay circuit that adjusts oscillator timing based on supply voltage. And the system references (such as TI TPS65161, Intersil EL7583, Semtech SC603, and Sipex SP6661) each offer delay and timing circuits that refine startup operation and determine when the frequency transition occurs. A POSITA would have recognized that integrating Shuto's (or any of the system's) RC delay networks into the control path of Tasdighi's or Yamawaki's clock-selection logic would allow the analog delay to determine or fine-tune the precise moment of switching between the discrete clock inputs. This predictable combination would yield smoother frequency transitions and more stable startup behavior.

A POSITA would be similarly motivated to combine Shuto with any and all of the other references previously listed for the reasons discussed above.

Each of the listed combinations satisfy the elements of the Asserted Claims, and Sandisk reserves the right to supplement, amend, or refine its contentions, including its combinations and motivations to combine, in light of further discovery, expert analysis, developments in the record, or claim construction.

IV. PATENT L.R. 3-3(C): CLAIM CHARTS IDENTIFYING WHERE THE LIMITATIONS OF THE ASSERTED CLAIMS ARE FOUND IN THE PRIOR ART.

Attached hereto and incorporated by reference are limitation-by-limitation claim charts demonstrating where specifically, in each anticipatory prior art item, each limitation of the Asserted Claims of the Asserted Patents is found.

These claim charts are largely based on Sandisk's understanding of the claim constructions applied by IPValue in its Infringement Contentions (to the extent such constructions can be ascertained from the Infringement Contentions), even though Sandisk does not necessarily agree with those constructions and reserves the right to dispute them. To the extent any limitation is deemed not to be met exactly by an item of prior art, Sandisk contends that the difference would have been obvious to a person of ordinary skill in the art and within the knowledge of one skilled in the art at the time of the alleged invention, so that the claimed invention would have been obvious both in light of that prior-art item alone and/or in combination with other prior art.

As a general matter, all portions (including text and any accompanying figures) of each prior art item are relied upon by Sandisk to support the disclosure of each patent claim limitation, as all portions of the prior art provide general support and context/background to the specifically cited. Supporting citations to specific portions of each prior art reference are nevertheless provided in the accompanying claim charts, but do not necessarily represent every location where a particular claim term may be found in the prior art item. Sandisk reserves the right to rely on additional, or different, portions of the prior art items other than those specifically cited in these claim charts.

The exhibit numbers of each claim chart submitted for each of the Asserted Patents and associated prior-art reference have been listed in **Tables #4–#8** above.

V. PATENT L.R. 3-3(D): INVALIDITY BASED ON OTHER GROUNDS

A. INVALIDITY UNDER 35 U.S.C. § 112

Subject to Sandisk's reservation of rights, Sandisk identifies the below grounds upon which Sandisk currently maintains that the Asserted Claims are invalid for lack of written description and/or enablement under 35 U.S.C. § 112 ¶ 1, and/or for failing to comply with the definiteness requirements of 35 U.S.C. § 112 ¶ 2 and ¶ 6. The disclosures below do not attempt to identify all recitations of a given term or phrase in each claim. Where Sandisk has identified an instance of a term or limitation in a particular claim that renders the claim invalid under section 112, Sandisk contends that ***every*** instance of the challenged term or limitation, or similar term or limitation, in the claim renders the claim invalid for the same reasons. Moreover, if that term or limitation appears in a different Asserted Claim, the same arguments apply to the appearance of that term or limitation in that different claim.

The following contentions are subject to revision and amendment as permitted by the Court under the Patent Local Rules and Federal Rule of Civil Procedure 26(e), and in light of further investigation and discovery regarding the defenses below, the Court's construction of the claims at issue, or the review and analysis of expert witnesses.

1. Lack of Enablement and Written Description

One or more Asserted Claims of the Asserted Patents are invalid under § 112 ¶ 1 for failing to particularly point out and distinctly claim the subject matter which the patentee regards as its alleged invention such that a POSITA would be reasonably apprised of the bounds of the Asserted Claims when read in light of the specification.

Section 112 ¶ 1 requires that the specification contain a written description of the invention. The test for whether a specification adequately describes an invention is "whether the disclosure of the application relied upon reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *Ariad Pharms., Inc. v. Eli Lilly and Co*., 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc); *Boston Scientific Corp. v. Johnson & Johnson*, 647 F.3d 1353, 1362 (Fed. Cir. 2011).

Section 112 ¶ 1 also requires that the patent specification enable "those skilled in the art how to make and use the full scope of the claimed invention without 'undue experimentation.'" *Genentech, Inc. v. Novo Nordisk A/S*, 108 F.3d 1361, 1365 (Fed. Cir. 1997) (quoting *In re Wright*, 999 F.2d 1557, 1561 (Fed. Cir. 1993)).

Sandisk identifies the following written description and enablement grounds with respect to the following Asserted Claims. The following does not purport to list every claim limitation to the foregoing disclosed grounds. Where a particular claim term or limitation is identified, Sandisk contends that the identified term or limitation, as well as the surrounding claim language in context as recited in the applicable claim, suffer from the identified Section 112 defect.

The Asserted Claims fail to meet the requirements of 35 U.S.C. § 112 ¶ 1 because the specifications of the Asserted Patent do not contain a written description of the alleged invention with respect to at least the following limitations or elements:

'537 patent, claim 18	"further comprising a metal oxide semiconductor (MOS) logic transistor on the substrate, wherein the MOS logic transistor comprises a gate oxide and a high work function gate electrode"
'240 patent, claims 12, 16	"a metal oxide semiconductor (MOS) logic device including a gate oxide layer and a second high work function gate electrode disposed thereon"
'240 patent, claims 14, 17	"wherein the MOS logic device is formed at least partially within a semiconductor material structure" / "wherein the MOS logic device is formed at least partially on the semiconductor material structure."

’664 patent, claims 1, 2, 3, 15, 16	“dynamic load”
’664 patent, claims 1 and 15	“based on a dynamic load”
’664 patent, claim 1	“clock driver circuit”
’664 patent, claim 15	“clock switch circuit”
’664 patent, claim 5	“clock switch control circuit”
’664 patent, claim 15	“a clock control circuit with a dynamic load”
’664 patent, claim 15	“the duration of the delay is based on the dynamic load”

The Asserted Claims fail to meet the requirements of 35 U.S.C. § 112 ¶ 1 because the specifications of the Asserted Patent do not enable a person skilled in the art to make and use the alleged invention with respect to at least the following limitations or elements:

’537 patent, claim 18	“further comprising a metal oxide semiconductor (MOS) logic transistor on the substrate, wherein the MOS logic transistor comprises a gate oxide and a high work function gate electrode”
’240 patent, claims 12, 16	“a metal oxide semiconductor (MOS) logic device including a gate oxide layer and a second high work function gate electrode disposed thereon”
’240 patent, claims 14, 17	“wherein the MOS logic device is formed at least partially within a semiconductor material structure” / “wherein the MOS logic device is formed at least partially on the semiconductor material structure.”
’240 patent, claim 1	“wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer and an anti-tunneling layer disposed between the first and second dielectric layers,”
’240 patent, claim 7	“The memory device of claim 1, wherein the blocking dielectric layer comprises high K high temperature oxide (HTO)”
’365 patent, claim 43	“The semiconductor memory device of claim 42, wherein the stack of layers includes a first dielectric layer, a gate layer and a second dielectric layer, wherein the gate layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by a sacrificial layer.”
’537 patent, claim 17	“the ONONO stack”

IPValue has not yet disclosed its proposed claim constructions to Sandisk for any of the Asserted Claims, and the deficient Infringement Contentions do not include any limitation-by-limitation analysis for the majority of accused products. Indeed, most of the accused products are not charted on a limitation-by-limitation basis in the claim charts for the Asserted Patents, making it impossible for Sandisk to glean how IPValue is interpreting the Asserted Claims and the meaning and scope of each limitation. Once IPValue discloses its proposed claim constructions, additional written description and enablement deficiencies may become known to Sandisk. For example, an exceptionally broad construction by IPValue may reveal new written description and enablement defects, as the full breadth of the Asserted Claims must satisfy 35 U.S.C. § 112 ¶ 1. Sandisk reserves all rights to seek leave to amend these Invalidity Contentions once IPValue's proposed constructions are disclosed, or in view of any other events that impact the scope of the Asserted Claims.

2. Indefiniteness

Claims are indefinite under 35 U.S.C. § 112 ¶ 2 when they "fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc*., 134 S. Ct. 2120, 2124 (2014).

Subject to the Court's written ruling on claim construction, and subject to changes in Counterclaim-Plaintiffs' positions in any further infringement contentions or its final infringement contentions, Sandisk reserves the right to allege at least one or more of these claim terms/phrases/limitations are indefinite because, read in light of the specifications and the prosecution histories, they fail to inform with reasonable certainty those skilled in the art about the scope of the invention, and are therefore invalid for indefiniteness under 35 U.S.C. § 112 ¶ 2. *See id.* at 901–02. For example, many of the claims or phrases below are terms of degree with no objective boundary, such as "oxygen-rich" and "oxygen-lean," and the specification fails to enable a POSITA to draw the line between "rich" and "lean," which invites *post-hoc* boundary setting by the IPValue in violation of *Nautilus.* The same defect applies to terms like "high work function gate electrode," among others. Other terms and phrases simply lack sufficient disclosure to enable a POSITA to tell whether a given structure meets the limitation, such as the "multi-layer charge storing" and "trapping" terms, which are claimed purely by function with insufficient guidance on a correlating structure or composition. A POSITA is therefore left to guess whether a particular structure meets this limitation (*e.g.*, what layers should be counted as part of the multi-layer structure, where the structure ends and begins, and whether all layers or only some layers must store or trap charge), which also violates *Nautilus*. Other terms, like "the ONONO stack," lack an antecedent basis, rendering the term indefinite.

An element in a claim "may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof." 35 U.S.C. § 112 ¶ 6. "Generic terms such as 'mechanism,' 'element,' 'device,' and other nonce words that reflect nothing more than verbal constructs may be used in a claim in a manner that is tantamount to using the word 'means' because they 'typically do not connote sufficiently definite structure' and therefore may invoke § 112, para. 6 [AIA § 112(f)]." *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1350 (Fed. Cir. 2015) (quotation omitted). If the specification fails to disclose adequate corresponding structure for a means-plus-function term, the term is indefinite. *Id*. at 1351–52.

Sandisk reserves the right to allege claims of the Asserted Patent are invalid because they include limitations and/or claim terms that fail to satisfy the definiteness requirement of 35 U.S.C. § 112 ¶ 2 and/or ¶ 6.

'537 patent, claim 17 '240 patent, claims 1, 12, 16 '365 patent, claims 6, 7, 8, 25, 26, 27, 34, 38, 39, 40	"oxygen-rich [nitride]" / "oxygen-lean [nitride]"
'537 patent, claim 17	"the ONONO stack"
'240 patent, claim 3	"first and second diffusion regions are disposed above a semiconductor material structure"
'240 patent, claim 4	"first and second diffusion regions are suspended above a semiconductor material structure"

’240 patent, claim 1	“wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer and an anti-tunneling layer disposed between the first and second dielectric layers”
’240 patent, claim 7	“The memory device of claim 1, wherein the blocking dielectric layer comprises high K high temperature oxide (HTO)”
’537 patent, claims 17, 19 ’240 patent, claims 1, 12, 13, 16, 18 ’365 patent, claims 1, 6, 21, 23, 25, 34, 35, 38	“multi-layer charge [storing region] / [trapping layer] / [trapping region]”
’365 patent, claims 4, 24	“wherein the second dielectric layer separates the sacrificial layer from an overlying memory transistor”
’365 patent, claim 13	“wherein the second dielectric layer separates the gate electrode from an overlying memory transistor”
’365 patent, claim 43	“The semiconductor memory device of claim 42, wherein the stack of layers includes a first dielectric layer, a gate layer and a second dielectric layer, wherein the gate layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by a sacrificial layer.”
’240 patent, claim 1	“wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer and an anti-tunneling layer disposed between the first and second dielectric layers,”
’240 patent, claim 7	“The memory device of claim 1, wherein the blocking dielectric layer comprises high K high temperature oxide (HTO)”
’365 patent, claim 43	“The semiconductor memory device of claim 42, wherein the stack of layers includes a first dielectric layer, a gate layer and a second dielectric layer, wherein the gate layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by a sacrificial layer.”
’664 patent, claim 1, 2, 3, 15, 16	“dynamic load”
’664 patent, claim 1	“a clock control circuit configured to output a switch clock control signal based on a dynamic load”

’664 patent, claim 15	“a clock control circuit with a dynamic load”
’664 patent, claim 15	“a clock control circuit with a dynamic load, wherein the clock control circuit is configured to output a switch clock signal after a delay following enabling the charge pump control circuit, wherein the duration of the delay is based on the dynamic load”
’664 patent, claim 5	“wherein the clock switch control circuit has a low frequency clock input and a high frequency clock input”
’664 patent, claim 2	“further including a dynamic load control circuit having a startup signal controlling the dynamic load”
’664 patent, claim 3	“wherein the dynamic load has a capacitor with a node coupled to a controllable switch”
’664 patent, claim 16	“further comprising a dynamic load control circuit having a startup signal that controls the dynamic load”
’664 patent, claim 1	“clock driver circuit”
’664 patent, claim 15	“clock switch circuit”
’664 patent, claim 5	“clock switch control circuit”

IPValue has not yet disclosed its proposed claim constructions to Sandisk for any of the Asserted Claims, and the deficient Infringement Contentions do not include any limitation-by-limitation analysis for the majority of accused products. Indeed, most of the accused products are not charted on a limitation-by-limitation basis in the claim charts for the Asserted Patents, making it impossible for Sandisk to glean how IPValue is interpreting the Asserted Claims and the meaning and scope of each limitation. Once IPValue discloses its proposed claim constructions, additional indefiniteness arguments may become known to Sandisk. For example, if IPValue proposes a construction that fails to inform, with reasonable certainty, those skilled in the art about the scope of the invention, Sandisk may argue that the claim term is indefinite. Sandisk reserves all rights to seek leave to amend these Invalidity Contentions once IPValue’s proposed constructions are disclosed, or in view of any other events that impact the scope of the Asserted Claims.

B. INVALIDITY UNDER 35 U.S.C § 101

Section 101 of the Patent Act has long had an important implicit exception, that "[l]aws of nature, natural phenomena, and abstract ideas are not patentable." *Alice Corp. Pty. Ltd. v. CLS Bank Int'l*, 573 U.S. 208, 216 (2014). In *Mayo Collaborative Servs. v. Prometheus Labs., Inc.* and *Alice Corp. Pty. Ltd. v. CLS Bank Int'l*, the Supreme Court established a two-step framework for applying this exception to § 101 patent eligibility. *Alice*, 208 U.S. at 217–18; *see also Mayo Collaborative Servs. v. Prometheus Labs., Inc.*, 566 U.S. 66, 71–79 (2012).

The first step is to "determine whether the claims at issue are directed to one of those patent-ineligible concepts"—laws of nature, natural phenomena, or abstract ideas. *Alice*, 208 U.S. at 217; *see Mayo*, 566 U.S. at 77–79. The Federal Circuit, applying the two-step framework for patent-eligibility under *Alice*, has explained that "[r]egardless of what statutory category . . . a claim's language is crafted to literally invoke," it is necessary to "look to the underlying invention for patent-eligibility purposes." *CyberSource Corp. v. Retail Decisions, Inc.*, 654 F.3d 1366, 1374 (Fed. Cir. 2011). In other words, the claims may be "[s]tripped of excess verbiage," *Intellectual Ventures I LLC v. Cap. One Fin. Corp.*, 850 F.3d 1332, 1339 (Fed. Cir. 2017), so that the claimed invention may be viewed in its "simplest form," *Dealertrack, Inc. v. Huber*, 674 F.3d 1315, 1333 (Fed. Cir. 2012). *See also Intellectual Ventures I LLC*, 850 F.3d at 1340 (concluding that claims were, "at their core," directed to abstract idea); *Affinity Labs of Texas, LLC v. DIRECTV, LLC*, 838 F.3d 1253, 1256 (Fed. Cir. 2016) ("Stripped of excess verbiage, claim 1 is directed to . . . ."); *Elec. Power Grp., LLC v. Alstom S.A.*, 830 F.3d 1350, 1353 (Fed. Cir. 2016) ("[W]e have described the first-stage inquiry as looking at the 'focus' of the claims, their '"character as a whole[.]"'"). "[W]ell-established, fundamental concepts fall within the category of abstract ideas." *Cyberfone Sys., LLC v. CNN Interactive Grp., Inc.*, 558 F. App'x 988, 991 (Fed. Cir. 2014).

If the claims are directed to a patent-ineligible concept, the second step of the patent-eligibility inquiry is to ask "what else is there in the claims"? *Alice*, 573 U.S. at 217; *Mayo*, 566 U.S. at 78. This second step is a search for an "inventive concept," that is, "an element or combination of elements that is 'sufficient to ensure that the patent in practice amounts to significantly more than a patent upon the ineligible concept itself.'" *Alice*, 573 U.S. at 217–18; *Mayo*, 566 U.S. at 71–73. "A claim that recites an abstract idea must include 'additional features' to ensure 'that the claim is more than a drafting effort designed to monopolize the abstract idea.'" *Alice*, 573 U.S. at 221; *see also Mayo*, 566 U.S. at 77. "'Simply appending conventional steps, specified at a high level of generality,' [is] not 'enough' to supply an 'inventive concept.'" *Alice*, 573 U.S. at 222; *see also Mayo*, 566 U.S. at 82. For example, "mere recitation of a generic computer cannot transform a patent-ineligible abstract idea into a patent-eligible invention," because "[g]iven the ubiquity of computers . . . wholly generic computer implementation is not generally the sort of 'additional feature' that provides any 'practical assurance that the process is more than a drafting effort designed to monopolize the abstract idea itself.'" *Alice*, 573 U.S. at 223–24. In other words, merely adding "purely functional and generic" components to a claim's recitation of a computer-implemented invention does not "transform an abstract idea into a patent eligible invention" because "[n]early every computer will include [components] capable of performing the basic . . . functions required by the . . . claims." *Alice*, 57 U.S. at 226. It is also not enough to "limit[] an abstract idea to one field of use," or add "token postsolution components," *Bilski v. Kappos*, 561 U.S. 593, 610–12 (2010), or "limit the use of the idea to a particular technological environment," *Alice*, 573 U.S. at 222.

The Asserted Claims of the '664 patent fail the Supreme Court's two-step test for patent-eligibility and are therefore patent-ineligible under Section 101.

<u>Step One</u>: The Asserted Claims are all directed to abstract ideas, and employ generic, functional, and results-oriented language that recites no specific technological solution for achieving their desired functional results or any improvement in the underlying system. Specifically, the Asserted Claims of the '664 patent are directed to the abstract idea of adjusting frequency to accommodate for varying operating conditions. The patent asserts that "[t]oday's mobile electronic products require low power consumption and fast startup times." '664 patent at 1:27–29. The '664 patent further explains that charge pumps, which are used to "provide boosted voltages above the power supply voltage in electronic circuits," need to provide "the desired boosted pump voltage quickly, and once stable consume as little power, or current, as possible."

See id. at 1:26–31. The patent notes that a "conventional charge pump" would use a "control circuit" that "generates a high frequency and low frequency oscillator and uses circuitry to control the clock switching. During startup, the high frequency clock is used to generate the desired high output voltage at which point, the low frequency clock will take over the pump operation." *See id.* at 1:31–37. The patent's purported solution to this problem is claiming a "charge pump control circuit" where a "dynamic capacitive load" that "incorporates a delay" is used to allow the high frequency clock to control the pump stage and "quickly charge the output to the desired boosted voltage." *See id.* at 1:54–57. The patent identifies no purported technological barrier to operating a charge pump in this manner—because none existed—nor does it describe any technological solution needed to overcome any such barrier. Instead, the patent claims—at most—the notion of adjusting frequency to accommodate for varying operating conditions, implemented using standard electronic components performing nothing more than their conventional functions. Indeed, the patent's specification repeatedly invokes conventional electronic components—such as transistors, NOR and NAND gates, capacitors, and oscillators—when describing the claimed charge pump control circuit. *See id.* at 2:43–4:35.

<u>Step Two</u>: The Asserted Claims of the '664 patent fail to recite any inventive concept sufficient to transform the abstract idea into a patent-eligible invention. The elements of the claims, whether viewed individually or as an ordered combination, were all well understood, routine, and conventional as of the applicable priority date. The Asserted Claims of the '664 patent generically recites "a clock control circuit," "a clock driver circuit," and "a clock switch circuit," but the patents do not claim to have invented or improved any of these components or features that make up these claimed circuits. To the contrary, these components were all well-understood, routine, and conventional, and are used in the Asserted Claims of the '664 patent only for their ordinary functions. *See Two-Way Media Ltd. v Comcast Cable Commc'ns LLC*, 874 F.3d 1329, 1339 (Fed. Cir. 2017) ("Nothing in the claims or their constructions . . . requires anything other than conventional computer . . . components operating according to their ordinary functions."). To the extent the specification sets forth any kind of implementation details, they do not remedy the generic, functional, results-oriented language of the claims. *See Alice*, 573 U.S. at

221 ("[W]e must examine the elements of the claim to determine whether it contains an 'inventive concept[.]'"); *RecogniCorp, LLC v. Nintendo Co.*, 855 F.3d 1322, 1327 (Fed. Cir. 2017) ("To save a patent at step two, an inventive concept must be evident in the claims."); *Synopsys, Inc. v. Mentor Graphics Corp.*, 839 F.3d 1138, 1149 (Fed. Cir. 2016) ("The § 101 inquiry must focus on the language of the Asserted Claims themselves.").

Sandisk reserves the right to supplement and/or modify these contentions regarding patent-ineligibility, including specifying additional and/or different representative claims, elaborating on the abstract idea to which the Asserted Claims of the '664 patent are directed, and further explaining how the claims include no more than well understood, routine, and conventional features that do not suffice as an inventive concept at *Alice* step two. Sandisk further reserves the right to submit and rely upon expert testimony in support of its contentions regarding patent ineligibility.

C. OTHER GROUNDS OF INVALIDITY UNDER §§ 102 and 103

Sandisk reserves the right to assert that the Asserted Claims are invalid under 35 U.S.C. §§ 102 and/or 103 in the event Sandisk obtains evidence (i) concerning prior art publications and systems through discovery, including that which is subject to any third-party subpoenas; (ii) concerning any on-sale or public use bars, or any products or devices offered for sale or sold that anticipate or render one or more of the Asserted Claims obvious; or (iii) that the named inventors of the patent-in-suit, did not first file (either alone or in conjunction with other parties) the subject matter claimed in the patent-in-suit.

Sandisk reserves the right to supplement these disclosures based on further investigation and discovery.

VI. DOCUMENT PRODUCTION ACCOMPANYING INVALIDITY CONTENTIONS

Documents required to be produced under the Patent Local Rules are being produced to IPValue in parallel with these Contentions under a separate letter (and certain files have been made available for inspection as described in the document production cover letter).

Sandisk reserves the right to produce and rely on additional documents relating to their products in view of, for example and without limitation, additional information revealed during discovery regarding IPValue's allegations and/or amendments to IPValue's Infringement Contentions.

VII. OTHER RESERVATIONS AND EXPLANATIONS

Nothing in these Invalidity Contentions constitutes an admission concerning the priority date, conception date, or date of reduction to practice of any of the Asserted Claims. If the Court finds that IPValue is entitled to a different priority date from the date(s) assumed herein, or IPValue attempts to argue for a different priority date notwithstanding its disclosures under the Patent Local Rules, Sandisk reserves the right to seek leave of Court to serve additional or modified invalidity contentions.

For prior art patents and prior art publications identified in these Invalidity Contentions, Sandisk reserves the right to rely on the public use, offer for sale, sale, and/or actual products embodying the methods and systems described therein uncovered during discovery. Sandisk also reserves the right to rely on any related patents and patent applications, foreign patent counterparts and foreign patent applications of U.S. patents identified in these Invalidity Contentions, and U.S. counterparts of foreign patents and foreign patent applications identified in these Invalidity Contentions.

The accompanying invalidity claim charts provide examples of prior art that discloses, either expressly or inherently, every limitation of certain claims and/or teachings, suggestions and motivations through which a POSITA at the time of the alleged invention would have considered the limitations obvious in view of the state of the art at the time, the differences between the claimed invention and the state of the art, and the foreseeability from a technical perspective and/or marketing and/or natural and expected evolution of the art. As stated throughout these Invalidity Contentions, Sandisk reserves the right to seek leave of Court, consistent with the Patent Local Rules, to revise the ultimate contentions concerning the invalidity of asserted the Asserted Claims, which may change depending upon discovery taken in the case, the Court's construction of the Asserted Claims, any findings as to the priority date of the Asserted Claims, and/or positions that IPValue or expert witness(es) may take concerning claim construction, infringement, and/or invalidity issues.

Sandisk may also rely on IPValue's or any named inventor admissions concerning the scope of prior art relevant to the Asserted Patent; the patent prosecution histories for the Asserted Patent; any deposition testimony of the named inventors on the Asserted Patent; and the papers filed and any evidence submitted by IPValue in connection with this litigation. For example, Sandisk reserves the right to assert that the Asserted Claims are invalid under 35 U.S.C. § 102(f) in the event that Sandisk obtains evidence that the named inventor did not invent (either alone or in conjunction with others) the subject matter claimed in the Asserted Patent. Should Sandisk obtain such evidence, it will provide the name(s) of the person(s) from whom and the circumstances under which the claimed invention or any part of it was derived.

Prior art not included in this disclosure, whether known or not known to Sandisk, may become relevant at a later time. In particular, Sandisk is currently unaware of the extent, if any, to which IPValue will contend that limitations of the Asserted Patent are not disclosed in the prior art identified by Sandisk. To the extent such an issue arises, Sandisk reserves the right, and will seek leave of Court if necessary, to identify other references that would render obvious the allegedly missing limitation(s) of the disclosed device or method.

Additionally, no third-party discovery has been taken, as discovery has just begun and Sandisk has been diligently investigating whether sufficient information about prior art can be found in the public record without burdening a third party through a subpoena. Sandisk reserves the right to seek leave of Court to present additional items of prior art under 35 U.S.C. §§ 102(a), (b), (e), and/or (g), and/or § 103, located during the course of forthcoming third-party discovery or further investigation, and to assert invalidity under 35 U.S.C. §§ 102(c), (d), or (f), to the extent that such discovery or investigation yields information forming the basis for such invalidity. For example, Sandisk anticipates that it will issue subpoenas to, and receive information from, third parties believed to have knowledge, documentation, and/or corroborating evidence concerning some of the potential prior art systems identified in these Invalidity Contentions. Potential third parties also include, without limitation, the authors, inventors, vendors, or assignees of the references listed in these disclosures.

Sandisk further reserves the right to seek leave of Court to modify or add contentions in the event that IPValue is permitted by the Court to serve amended Infringement Contentions and/or modify the patent claims asserted in this litigation.

Sandisk also contends that the Asserted Patents are invalid in view of public knowledge and uses and/or offers for sale or sales of products and services that are under 35 U.S.C. § 102(a) and/or 35 U.S.C. § 102(b) and/or prior inventions made in this country by other inventors who had not abandoned, suppressed, or concealed them under 35 U.S.C. § 102(g).

Dated: November 14, 2025

KEKER, VAN NEST & PETERS LLP

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