

EXHIBIT 41

Exhibit 41 – Claim Chart Showing TE Connectivity’s Infringement of U.S. Patent 11,012,252 (“’252 Patent”)

The following chart is based on information known to date. Credo reserves the right to amend and update this chart as additional information is obtained and analyzed. The exemplary claim mappings below rely on images and data from TE Connectivity and its suppliers’ public-facing materials. The following chart is representative of TE Connectivity’s infringement by its unlawful importation into the United States, sale for importation into the United States, and/or sale within the United States after importation of all the Accused TE Connectivity Products.

As outlined in the below claim chart, the Accused TE Connectivity Products infringe, either literally or under the doctrine of equivalents, at least Claims 1, 6, and 11 of the ’252 patent.

<u>’252 Patent</u>	<u>Accused TE Connectivity Products</u>
<u>Claim 1</u>	
[1pre] An active Ethernet cable that comprises:	The Accused TE Connectivity Products comprise an active Ethernet cable. See, e.g.:

'252 Patent

Accused TE Connectivity Products

Claim 1

OSFP Cable Assembly, 32 Positions, 3 m [9.84 ft], 56 Gb/s, Black Cable, Shielded, 26 AWG, OSFP Plug End A, OSFP Plug End B, VW-1, 16 Pairs



TE Internal #: 2336065-3

TE Internal Description: OSFP - OSFP, 3 METE R, 26AWG

Cable Assembly Type : OSFP

Number of Positions : 32

Cable Assembly Length : 3 m [9.84 ft]

Data Rate (Gb/s): 56

Cable Color : Black


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[Digital Datasheet](#)

Ex. 58, TE Connectivity OSFP Cable Assembly Website.

- 112G Product Support for SFP, SFP-DD, QSFP, QSFP-DD, OSFP, and OSFP-XD Interconnects
 - Direct Attached Copper Cables (DAC)
 - Active Copper Cables (ACC)
 - Active Electrical Cable (AEC)
 - Active Copper Cables (AOC)
 - I/O Connectors and Cages

Ex. 59, TE Connectivity 112G Portfolio External Cabling Solutions Datasheet.

'252 Patent	Accused TE Connectivity Products
Claim 1	
<p>[1a] electrical conductors connected between a first connector and a second connector,</p>	<p>The Accused TE Connectivity Products comprise electrical conductors connected between a first connector and a second connector.</p> <p>For example, the Accused TE Connectivity Products have first and second connectors at the end of the cables (e.g., the OSFP plugs shown below).</p> <p>See, e.g.:</p> <div data-bbox="709 561 1871 1224" style="border: 1px solid #ccc; padding: 10px; background-color: #f9f9f9;"> <p>OSFP Cable Assembly, 32 Positions, 3 m [9.84 ft], 56 Gb/s, Black Cable, Shielded, 26 AWG, OSFP Plug End A, OSFP Plug End B, VW-1, 16 Pairs</p>  <div style="float: right; padding-left: 10px;"> <p>TE Internal #: 2336065-3 TE Internal Description: OSFP - OSFP, 3 METE R, 26AWG</p> <p>Cable Assembly Type : OSFP Number of Positions : 32 Cable Assembly Length : 3 m [9.84 ft] Data Rate (Gb/s): 56 Cable Color : Black</p> <p>Add to List Similar Products </p> <p>Digital Datasheet</p> </div> </div> <p>Ex. 58, <i>TE Connectivity OSFP Cable Assembly Website</i>.</p> <p>The electrical conductors are round jacketed twin-axial wire.</p> <p>See, e.g.:</p>

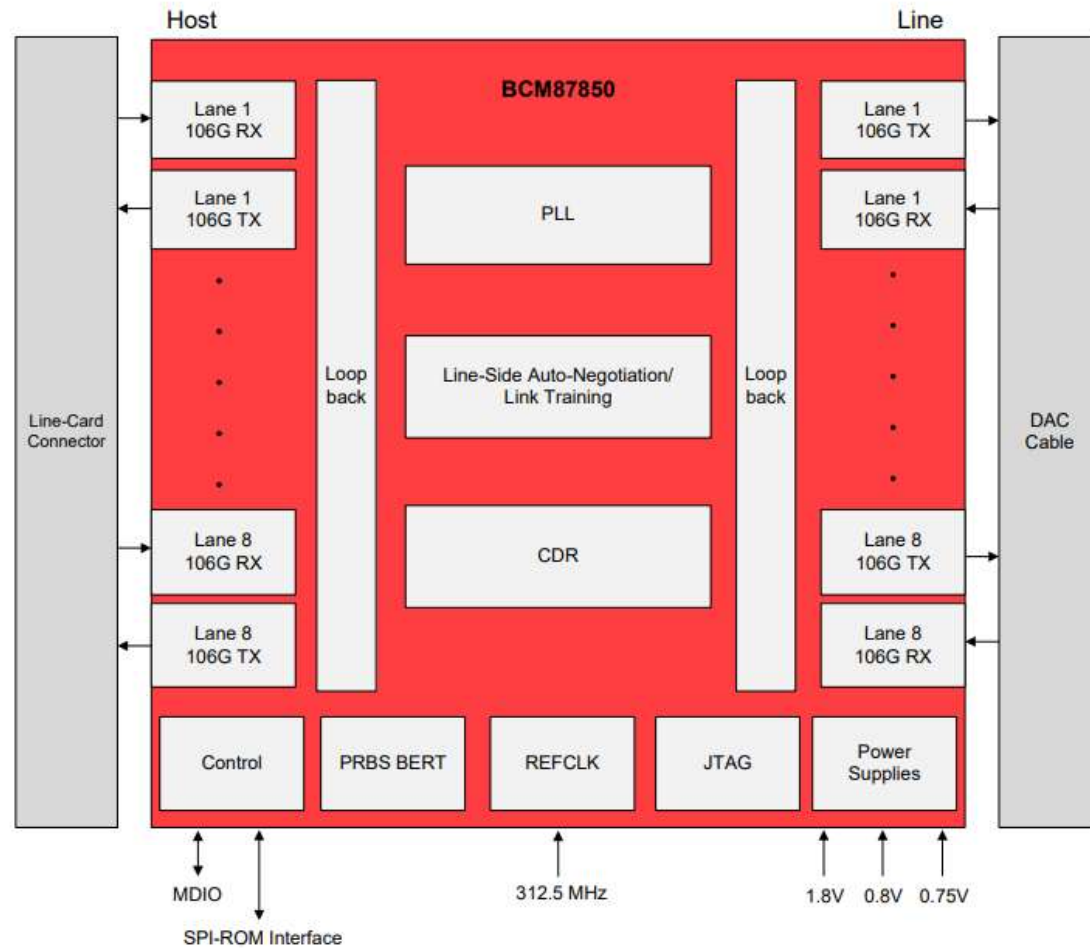
<u>'252 Patent</u>	Accused TE Connectivity Products
<u>Claim 1</u>	
	<p>Product Type Cable Assembly Category: High Speed Features Cable Assembly Type: OSFP Cable Style: Round Jacketed Twinax Cable Assembly (End A): OSFP Plug Cable Assembly (End B): OSFP Plug</p> <p><i>Ex. 58, TE Connectivity OSFP Cable Assembly Website.</i></p>
<p>[1b] each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable,</p>	<p>The first and second connectors in the Accused TE Connectivity Products are adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable.</p> <p>For example, the connectors in the Accused TE Connectivity Products include DSPs manufactured by Broadcom and others. These DSPs are retimers that receive inbound Ethernet data streams from a host and convey them to the cable and conversely receive outbound Ethernet data streams from the cable and provide them to the host.</p>

'252 Patent	Accused TE Connectivity Products
<u>Claim 1</u>	<p>TE's live and static displays will demonstrate how TE is paving the way to meet the technology demands for next-generation products and architectures. TE will showcase its innovative solutions in the following booths:</p> <ul style="list-style-type: none">• TE Connectivity – Booth #6035• Broadcom – Booth #6425• Ethernet Alliance – Booth #5417• Intel – Booth #2901• MACOM – Booth #3927• Marvell – Booth #4326• Optical Internetworking Forum (OIF) – Booth #5101• SEMTECH – Booth #5417• Spirent – Booth #5304

<u>'252 Patent</u>	Accused TE Connectivity Products
<u>Claim 1</u>	<p>TE's featured live demos will include:</p> <p>800G QSFP-DD active optical cables (AOC) The 800G quad small form-factor pluggable double density (QSFP-DD) AOC live demo showcases TE's 800 Gbps optical data link using an IEEE 802.3df 800GBASE-SR8 AOC in QSFP-DD form factor running live 8x112G traffic end-to-end. The AOC uses low-cost multimode optics and low power electronics, resulting in a per end power consumption below 14W. Initial beta product sampling is available now.</p> <p>800G active cable technologies The 800G active copper cable (ACC) and active electrical cable (AEC) demonstrate the latest in TE's bulk cable and termination technology. A retimer or redriver embedded in the module extends the reach of copper cables while consuming less power than equivalent optical cables. AEC/ACC technology also enables fine wire gauges for short links to ease routing challenges in dense next-gen racks. This live demo shows eight lanes of 112G PAM-4 data running through TE's AEC/ACC with a host trace and connector on each side.</p> <p>TE's innovative solutions will also be displayed across its partner booths. Broadcom (booth #6425) will showcase TE's 800G AEC technology. Intel (booth #2901) will demonstrate TE's 1.6Tb 224 Gbps OSFP connector and DAC technology. MACOM (booth #3927) will display TE's 800G ACC technology. Marvell's exhibit (booth #4326) will include TE's 800G AEC technology. SEMTECH (booth #5417) will feature TE's 800G ACC technology. And Spirent (booth #5304) will highlight TE's 800G DAC technology in their demonstration.</p> <p><i>Ex. 60, TE Connectivity OFC 2023 Press Release.</i></p> <p>Active electrical cables powered by Marvell Alaska A PAM4 DSPs are sampling now from Amphenol, Molex and TE Connectivity.</p>

Claim 1

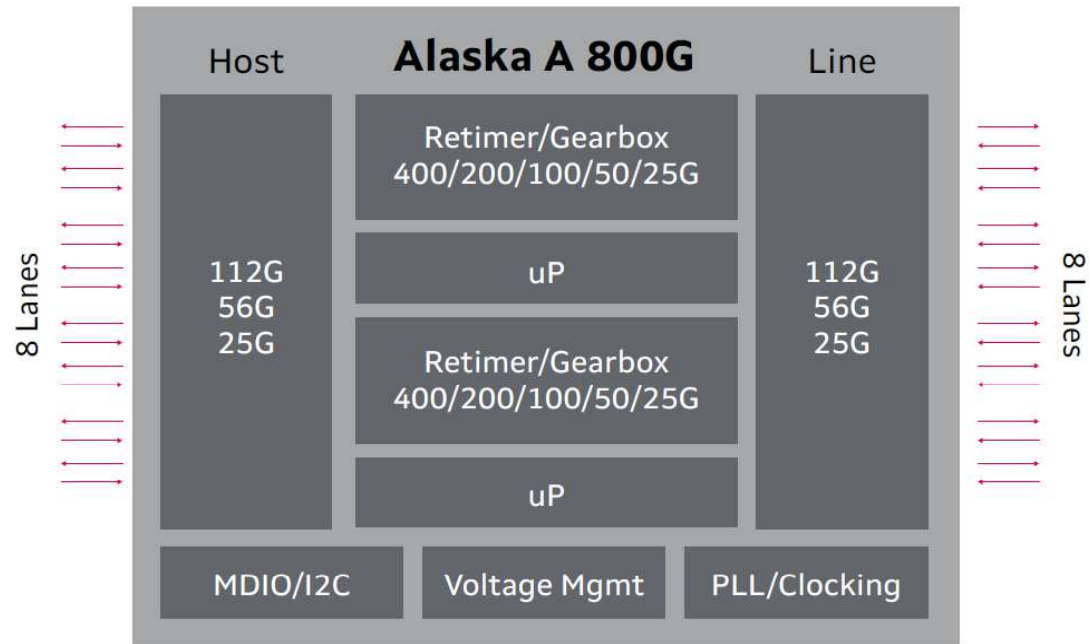
Ex. 23, *Marvell Announces Availability Of Active Electrical Cables Powered By Its Industry-Leading PAM4 DSP Technology Article, Oct. 20, 2022.*



Ex. 50, *Broadcom BCM87850 Product Brief.*

<u>'252 Patent</u>	Accused TE Connectivity Products
<u>Claim 1</u>	<p data-bbox="716 358 905 391">Overview</p> <p data-bbox="716 415 1793 591">The Broadcom® BCM87850 is a single-chip, eight-lane, ultra-low power, ultra-low latency PHY that integrates retimer and equalizer to support active cable applications. The BCM87850 is capable of equalizing 22 dB of loss on both the client-side and line-side interfaces. Each lane is capable of multiple data rates, including 106.25 Gb/s.</p> <p data-bbox="716 626 1713 727">The on-chip clock synthesis is performed by a low-cost 312.5-MHz reference clock through high-frequency, low jitter phase-locked loops (PLLs).</p> <p data-bbox="716 764 1793 865">The BCM87850 is fabricated in low-power 7-nm CMOS technology and is available in a 12 mm × 12 mm, 0.5-mm pitch, 485-ball BGA, RoHS-compliant package.</p> <p data-bbox="705 889 1434 922"><i>Ex. 50, Broadcom BCM87850 Product Brief (annotated).</i></p>

Claim 1



Ex. 51, *Marvell Alaska Product Brief*.

[1c] each of the first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream,

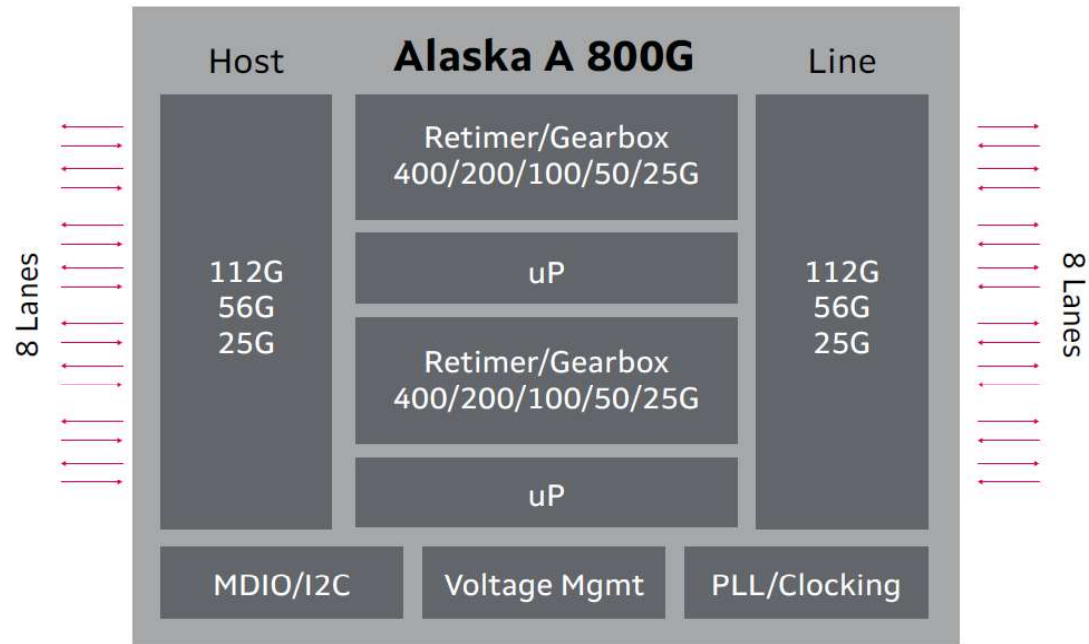
Each of the first and second connectors in the Accused TE Connectivity Products includes a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream.

For example, the Accused TE Connectivity Products include a transceiver in the DSP chip on each end of the cable. The transceiver in each DSP performs clock and data recovery via “retiming” on the electrical input signal to extract and re-modulate the inbound data stream

'252 Patent	Accused TE Connectivity Products
<u>Claim 1</u>	<p>for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream.</p> <p>See, e.g.:</p> <p>Overview</p> <p>The Broadcom® BCM87850 is a single-chip, eight-lane, ultra-low power, ultra-low latency PHY that integrates retimer and equalizer to support active cable applications. The BCM87850 is capable of equalizing 22 dB of loss on both the client-side and line-side interfaces. Each lane is capable of multiple data rates, including 106.25 Gb/s.</p> <p>The on-chip clock synthesis is performed by a low-cost 312.5-MHz reference clock through high-frequency, low jitter phase-locked loops (PLLs).</p> <p>The BCM87850 is fabricated in low-power 7-nm CMOS technology and is available in a 12 mm × 12 mm, 0.5-mm pitch, 485-ball BGA, RoHS-compliant package.</p> <p>Ex. 50, <i>Broadcom BCM87850 Product Brief</i> (annotated).</p>

'252 Patent	Accused TE Connectivity Products
Claim 1	
	<p data-bbox="709 277 894 315">Overview</p> <p data-bbox="709 347 1524 553">The Marvell Alaska A MV-CHA180C0C 800G is a PAM4 DSP retimer for 800G Active Electrical Cable (AEC) application, optimized for Switch to Switch and Switch to Server connectivity inside next generation cloud data center, high-performance computing and AI systems.</p> <p data-bbox="709 597 1583 803">Alaska A 800G is a retimer device which utilizes a 112G Gbps PAM4 DSP SERDES. There are 8-host and 8-line ports with each receiver port being able to recover 112Gbps PAM-4 signals and transmit to partnered TX. It can provide up to 800G (8 x 112G) full duplex mission mode traffic.</p>

Claim 1



Ex. 51, *Marvell Alaska Product Brief (annotated)*.

[1d] the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and remodulate the transit data stream as the outbound data stream from the cable, and

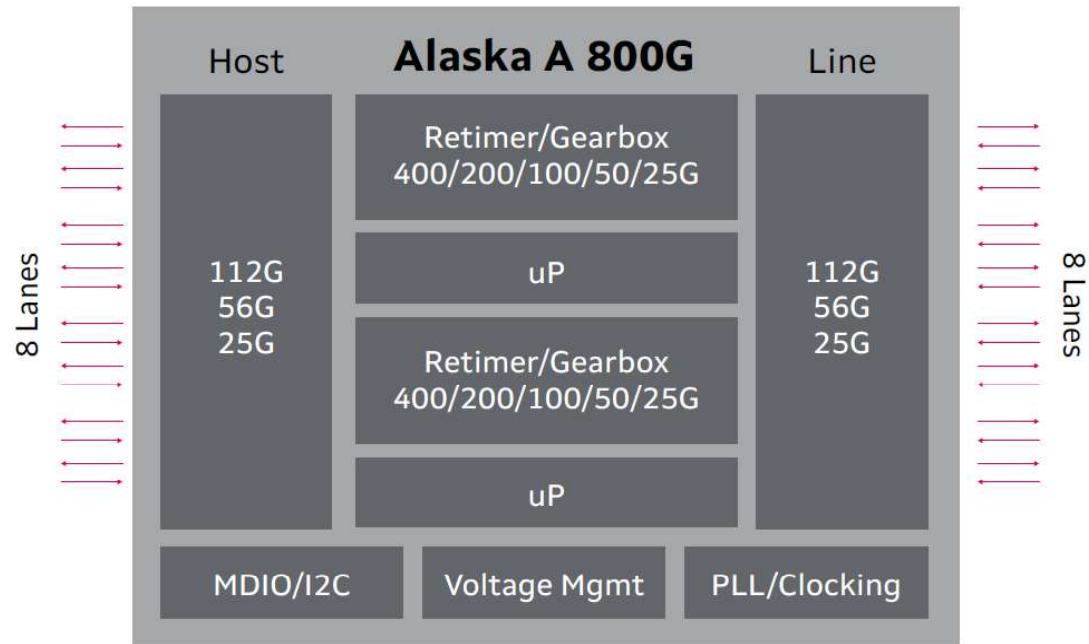
The respective transceiver for each of the first and second connectors in the Accused TE Connectivity Products performs clock and data recovery on the respective electrical transit signal to extract and remodulate the transit data stream as the outbound data stream from the cable.

For example, the transceiver in each DSP performs clock and data recovery via “retiming” on the electrical input signal to extract and re-modulate the transit data stream as the outbound data stream from the cable.

'252 Patent	Accused TE Connectivity Products
<u>Claim 1</u>	<p>See, e.g.:</p> <p>Overview</p> <p>The Broadcom® BCM87850 is a single-chip, eight-lane, ultra-low power, ultra-low latency PHY that integrates retimer and equalizer to support active cable applications. The BCM87850 is capable of equalizing 22 dB of loss on both the client-side and line-side interfaces. Each lane is capable of multiple data rates, including 106.25 Gb/s.</p> <p>The on-chip clock synthesis is performed by a low-cost 312.5-MHz reference clock through high-frequency, low jitter phase-locked loops (PLLs).</p> <p>The BCM87850 is fabricated in low-power 7-nm CMOS technology and is available in a 12 mm × 12 mm, 0.5-mm pitch, 485-ball BGA, RoHS-compliant package.</p> <p>Ex. 50, <i>Broadcom BCM87850 Product Brief</i> (emphasis added).</p>

'252 Patent	Accused TE Connectivity Products
Claim 1	
	<p data-bbox="709 277 894 315">Overview</p> <p data-bbox="709 347 1524 553">The Marvell Alaska A MV-CHA180C0C 800G is a PAM4 DSP retimer for 800G Active Electrical Cable (AEC) application, optimized for Switch to Switch and Switch to Server connectivity inside next generation cloud data center, high-performance computing and AI systems.</p> <p data-bbox="709 597 1583 803">Alaska A 800G is a retimer device which utilizes a 112G Gbps PAM4 DSP SERDES. There are 8-host and 8-line ports with each receiver port being able to recover 112Gbps PAM-4 signals and transmit to partnered TX. It can provide up to 800G (8 x 112G) full duplex mission mode traffic.</p>

Claim 1



Ex. 51, *Marvell Alaska Product Brief (annotated)*.

[1e] the respective transceivers each employing fixed, cable-independent equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal.

The respective transceivers in the Accused TE Connectivity Products employ fixed, cable-independent equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal.

For example, the DSPs at each end of the cable employ fixed, cable-independent equalization parameters for the remodulation of the transit data stream as the outbound stream and the clock and data recovery performed on the input signal. These parameters

'252 Patent	Accused TE Connectivity Products
Claim 1	<p>(i.e., transmit and receive filter coefficient values) are fixed and cable-independent per the IEEE 802.3ck standard (which are independent of communications through the cable).</p> <p>See, e.g.:</p> <p>120G.3.4 Module input characteristics</p> <p>The module input shall meet the specifications given in Table 120G-9. Channel equalization is provided by an adaptive equalizer in the module.</p> <p>Ex. 52, <i>IEEE 802.3ck Specification</i> at 7275 (annotated).</p> <p>The Accused TE Products comply with the OSFP standard.¹</p>

¹ The Accused TE Connectivity Products that use a QSFP form factor likewise comply with the IEEE 802.3ck standard and the the Common Management Interface Specification (CMIS) standard. See Ex. 77, QSFP-DD Specification at 34; Ex. 78, *QSFP112 Specification* at 10.

Claim 1

OSFP Cable Assembly, 32 Positions, 3 m [9.84 ft], 56 Gb/s, Black Cable, Shielded, 26 AWG, OSFP Plug End A, OSFP Plug End B, VW-1, 16 Pairs



TE Internal #: 2336065-3

TE Internal Description: OSFP - OSFP, 3 METE R, 26AWG

Cable Assembly Type : OSFP

Number of Positions : 32

Cable Assembly Length : 3 m [9.84 ft]

Data Rate (Gb/s): 56

Cable Color : Black

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[Digital Datasheet](#)

Ex. 58, *TE Connectivity OSFP Cable Assembly Website*.

As explained in the OSFP specification, the high-speed signals of the Accused TE Products meet the requirements of the IEEE 802.3ck standard.

The high-speed signals follow the electrical specifications of IEEE802.3bs, IEEE802.3cd, IEEE 802.3ck and CEI-56G-VSR-PAM4 as defined in OIF-CEI-05.2 for 400GAUI-8 mode and IEEE802.3bj, IEEE802.3bm for CAUI-4 mode.

Ex. 54, *OSFP Specification* at 147.

The 802.3ck standard defines the chip-to-module connection, including requiring that the transmitters use a pre-equalized set of filters as part of selecting a short or long channel.

'252 Patent	Accused TE Connectivity Products
Claim 1	<p data-bbox="722 289 1129 318">120G.3.2.1 Module output modes</p> <p data-bbox="722 354 1822 470">The module output shall support two modes: short and long. The means of controlling the module output mode is implementation dependent. For each output mode, the module shall meet the requirements for eye height (min) and VEC (max) in Table 120G-3 for both near-end and far-end measurements (see 120G.3.2.2.1).</p> <p data-bbox="701 503 1417 535">Ex. 52, <i>IEEE 802.3ck Specification</i> at 7275 (annotated).</p> <p data-bbox="701 576 1822 609">The OSFP standard also requires compliance of the control plane to the CMIS standard.</p> <p data-bbox="722 657 1123 690">The OSFP specification defines:</p> <ul data-bbox="766 706 1843 1063" style="list-style-type: none"> • The OSFP module mechanical form factor, including the latching mechanism; • The host cage together with the mating connector; • The electrical interface, including pin-out, data, control, and power and ground signals; • The mechanical interface, including the package outline, front panel, and printed circuit board (PCB) layout requirements; • Thermal requirements and limitations, including heat sink design and airflow; • Electrostatic discharge (ESD) requirements; • The module management interface as contained in the Common Management Interface Specification (CMIS). <p data-bbox="701 1096 1281 1128">Ex. 54, <i>OSFP Specification</i> at 15(annotated).</p> <p data-bbox="701 1169 1885 1307">The CMIS standard controls the equalization of the port transceiver, including employing fixed, cable-independent equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal.</p>

Claim 1

6.2.5.1 Tx Input Equalization Control

The controls for Tx input equalization can be grouped by equalization type, as shown in Table 6-5.

Table 6-5 Tx Input Eq control relationship to AdaptiveInputEqEnableTx

Equalization Type	Control	AdaptiveInputEqEnableTx
Adaptive	AdaptiveInputEqFreezeTx	1
	AdaptiveInputEqStoreTx	
	AdaptiveInputEqRecallTx	
Non-Adaptive	FixedInputEqTargetTx	0

The controls relevant for **adaptive** Tx input equalization are described in section 6.2.5.4.

The controls relevant for **non-adaptive** Tx input equalization, when Tx input equalization settings are pre-determined or host provisioned, are described below.

The module ignores control field values that are not relevant for the current AdaptiveInputEqEnableTx setting.

Host Controlled Equalization

Tx input equalization values in dB are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

SCS<k>::**FixedInputEqTargetTx**<i> is a four-bit control field for lane <i> and encoded as shown in Table 6-6. This field allows the host to specify a fixed (non-adaptive) Tx input equalization target and is ignored by the module if AdaptiveInputEqEnableTx<i> is set for that lane.

The module advertises support of non-adaptive Tx input equalization control as described in Table 8-48.

The module advertises the maximum supported Tx input equalization values as described in Table 8-44.

Table 6-6 Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000b	No Equalization
1	0001b	1 dB
2	0010b	2 dB
3 - 8	0011b ... 1000b	3 dB ... 8 dB
9	1001b	9 dB
10	1010b	10 dB
11	1011b	11 dB
12	1100b	12 dB
13-15		Custom

Claim 1

6.2.5.2 Rx Output Equalization Control

Rx output equalization is defined at an appropriate test point defined by the relevant standard.

SCS<k>::**OutputEqPreCursorTargetRx**<i> and SCS<k>::**OutputEqPostCursorTargetRx**<i> are four-bit control fields for lane <i> and encoded as shown in Table 6-7.

The module advertises support of Rx output equalization control as described in Table 8-48.

The module advertises the maximum supported Rx output equalization values as described in Table 8-44.

Modules that require only output emphasis utilize the SCS<k>::**OutputEqPostCursorTargetRx**<i> fields and set the SCS<k>::**OutputEqPreCursorTargetRx**<i> fields to zero.

Table 6-7 Rx Output Equalization Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000b	0dB (No Equalization)	0dB (No Equalization)
1	0001b	1 dB	0.5 dB
2	0010b	2 dB	1.0 dB
3	0011b	3 dB	1.5 dB
4	0100b	4 dB	2.0 dB
5	0101b	5 dB	2.5 dB
6	0110b	6 dB	3.0 dB
7	0111b	7 dB	3.5 dB
8-10	1000b-1010b	Reserved	Reserved
11-15	1011b-1111b	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to

$$\text{Pre EQ (dB)} = -20 \cdot \log_{10} \left(\frac{1 - C_{-1}}{C_{-1} + C_0 + C_1} \right) \quad (\text{Eq. 6-1})$$

The post-cursor equalizer settings in dB approximates to

$$\text{Post EQ (dB)} = -20 \cdot \log_{10} \left(\frac{1 - C_1}{C_{-1} + C_0 + C_1} \right) \quad (\text{Eq. 6-2})$$

Equalizer coefficients C_n are pre-cursor for $n < 0$ and post-cursor when $n > 0$.

Ex. 55, *CMIS Specification* at 60–61.

The website for the exemplary TE Connectivity products notes that they support the 802.3ck standard:

'252 Patent	Accused TE Connectivity Products
Claim 1	
	<p>TE Connectivity's (TE) next generation octal small form-factor pluggable 224G DAC/AEC/ACC portfolio offers industry standard operations at 1600 Gbps complying with IEEE 802.3df and IEEE 802.3ck. The OSFP specification is designed to support high density applications, up to 32 1.6T ports per 1RU and TE offers a wide variety of configurations to support a range of power levels and cooling solutions. TE's OSFP-224G product line is well suited for artificial intelligence (AI) and machine learning (ML) architectures.</p> <p style="text-align: center;">OSFP 1.6T AEC (Active Electrical Cable)</p> <ol style="list-style-type: none"> 1. Industry Standard - Up to 1600 Gbps aggregate throughput, compliant to IEEE 802.3ck. 2. Low Power – Lower power compared to optics; targeting <20W per module. 3. Active cables optimized for heat dissipation and system airflow. <p>Ex. 61, <i>TE Connectivity OSFP Connectors and Cable Assemblies Website</i> (annotated).</p>

'252 Patent	Accused TE Connectivity Products
Claim 6	
[6pre] A communication method that comprises, in a network cable having conductor pairs electrically connecting a first connector to a second connector	<p>TE Connectivity performs a communication method that comprises, in a network cable having conductor pairs electrically connecting a first connector to a second connector.</p> <p><i>See [1pre] above.</i></p>
[6a] receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device;	<p>The Accused TE Connectivity Products receive with the first connector a first electrical input signal conveying a first inbound data stream from a first host device</p> <p><i>See [1b] above.</i></p>
[6b] performing clock and data recovery on the first electrical input signal with a first transceiver in the	<p>The Accused TE Connectivity Products perform clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream.</p>

'252 Patent	Accused TE Connectivity Products
Claim 6	
first connector to extract the first inbound data stream;	<i>See [1c], [1d] above.</i>
[6c] re-modulating the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs;	The Accused TE Connectivity Products re-modulate the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs <i>See [1c], [1d] above.</i>
[6d] receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device;	The Accused TE Connectivity Products receive with the second connector a second electrical input signal conveying a second inbound data stream from a second host device <i>See [1b] above.</i>
[6e] performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream;	The Accused TE Connectivity Products perform clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream. <i>See [1c], [1d] above.</i>
[6f] re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs;	The Accused TE Connectivity Products re-modulate the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs <i>See [1c], [1d] above.</i>
[6g] performing clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream;	The Accused TE Connectivity Products perform clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream. <i>See [1c], [1d] above.</i>
[6h] re-modulating the first transit data stream as a second outbound data stream conveyed by a second	The Accused TE Connectivity Products re-modulate the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device.

'252 Patent	Accused TE Connectivity Products
Claim 6	
electrical output signal to the second host device;	<i>See</i> [1c], [1d] above.
[6i] performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream; and	The Accused TE Connectivity Products perform clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream. <i>See</i> [1c], [1d] above.
[6j] re-modulating the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device,	The Accused TE Connectivity Products re-modulate the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device <i>See</i> [1c], [1d] above.
[6k] wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters.	The Accused TE Connectivity Products perform wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters. <i>See</i> [1e] above.

'252 Patent	Accused TE Connectivity Products
<u>Claim 11</u>	
[11pre] A cable manufacturing method that comprises:	<p>The Accused TE Connectivity Products are produced using a cable manufacturing method.</p> <p><i>See</i> [1pre] above.</p>
[11a] connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver;	<p>The Accused TE Connectivity Products are produced using a cable manufacturing method, including connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver.</p> <p><i>See</i> [1a], [1b] above.</p>
[11b] packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device; and	<p>The Accused TE Connectivity Products are produced using a cable manufacturing method, including packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device.</p> <p><i>See</i> [1b] above.</p>
[11c] packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the	<p>The Accused TE Connectivity Products are produced using a cable manufacturing method, including packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device.</p> <p><i>See</i> [1b] above.</p>

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<u>Claim 11</u>	
network interface port of the second host device,	
<p>[11d] the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical transit signals to extract and re-modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals.</p>	<p>The Accused TE Connectivity Products are produced using a cable manufacturing method, wherein the first and second transceivers of the Accused TE Connectivity Products are configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical transit signals to extract and re-modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals</p> <p><i>See [1c], [1d], [1e] above.</i></p>