


EXHIBIT 66

Exhibit 66 – Domestic Industry Claim Chart for U.S. Patent No. 11,012,252 (“’252 Patent”)

The following chart is based on information known to date. Credo reserves the right to amend and update this chart as additional information is obtained and analyzed. The exemplary claim mappings below rely on images and data from Credo’s 800G OSFP PAM4 to 800G OSFP PAM4 Plug & Play Active Electrical Cable. The following chart is representative of all the Domestic Industry Products.

As outlined in the below claim chart, the Domestic Industry Products practice, either literally or under the doctrine of equivalents, at least Claim 1 of the ’252 patent.

’252 Patent	Domestic Industry Products
Claim 1	
<p>[1pre] An active Ethernet cable that comprises:</p>	<p>The Domestic Industry Products comprise an active Ethernet cable.</p> <p>See, e.g.:</p> <div data-bbox="553 1184 1117 1409" data-label="Image"> </div> <p>Ex. 62, <i>Credo 800G OSFP AEC Product Specification</i> at 1.</p>

'252 Patent	Domestic Industry Products								
Claim 1									
<p>[1a] electrical conductors connected between a first connector and a second connector,</p>	<p>The Domestic Industry Products comprise electrical conductors connected between a first connector and a second connector.</p> <p>For example, the Domestic Industry Products comprise a set of 32-pair, 32AWG copper conductors connected between two connector plugs (e.g., the OSFP plugs shown below).</p> <p>Mechanicals</p> <table border="1" data-bbox="578 877 1341 940"> <thead> <tr> <th>Parameter</th> <th>Cable Type</th> <th>Typical</th> <th>Length</th> </tr> </thead> <tbody> <tr> <td>Diameter</td> <td>16P 32AWG</td> <td>6.8mm</td> <td>0.5-2.5m</td> </tr> </tbody> </table>  <p>Ex. 62, <i>Credo 800G OSFP AEC Product Specification</i> at 2.</p>	Parameter	Cable Type	Typical	Length	Diameter	16P 32AWG	6.8mm	0.5-2.5m
Parameter	Cable Type	Typical	Length						
Diameter	16P 32AWG	6.8mm	0.5-2.5m						

'252 Patent	Domestic Industry Products																						
Claim 1																							
<p>[1b] each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable,</p>	<p>The first and second connectors in the Domestic Industry Products are adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable.</p> <p>For example, the Domestic Industry Products include digital signal processors (“DSPs”) at each end of the cable. Each DSP is a retimer that exchanges inbound and outbound multi-lane data streams (i.e., 16 TX and 16 RX) with a first host interface port (i.e., an OSFP-XD port) via a connector plug (i.e., an OSFP-XD 120-pin edge connector) at one end of the cable.</p> <p>See, e.g.:</p> <table border="1" data-bbox="553 1016 1445 1436"> <thead> <tr> <th>Parameter</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>Module Form Factor</td> <td>OSFP</td> </tr> <tr> <td>Number of Data Lanes</td> <td>8 TX and 8 RX per module (PAM4)</td> </tr> <tr> <td>Maximum Aggregate Data Rate</td> <td>800Gbps</td> </tr> <tr> <td>Nominal Data Rate per Lane</td> <td>106.25Gbps (PAM4)</td> </tr> <tr> <td>Electrical Interface and Pin-out</td> <td>60-pin edge connector</td> </tr> <tr> <td>Pin Description</td> <td>Per OSFP Hardware Specification</td> </tr> <tr> <td>Management Interface</td> <td>I²C, serial, timing per Common Management Interface Specification for 8X/16X Pluggable Transceivers v 4.0</td> </tr> <tr> <td>Length of Copper AEC</td> <td>0.5m - 2.5m in 0.5m increments</td> </tr> <tr> <td>BER (Pre-FEC)*</td> <td>Typ. <10⁻⁸</td> </tr> <tr> <td>BER (Post-FEC)*</td> <td><10⁻¹⁵</td> </tr> </tbody> </table> <p>* Tested with QPRBS31 pattern</p> <p>Ex. 62, <i>Credo 800G OSFP AEC Product Specification</i> at 2 (annotated).</p>	Parameter	Value	Module Form Factor	OSFP	Number of Data Lanes	8 TX and 8 RX per module (PAM4)	Maximum Aggregate Data Rate	800Gbps	Nominal Data Rate per Lane	106.25Gbps (PAM4)	Electrical Interface and Pin-out	60-pin edge connector	Pin Description	Per OSFP Hardware Specification	Management Interface	I ² C, serial, timing per Common Management Interface Specification for 8X/16X Pluggable Transceivers v 4.0	Length of Copper AEC	0.5m - 2.5m in 0.5m increments	BER (Pre-FEC)*	Typ. <10 ⁻⁸	BER (Post-FEC)*	<10 ⁻¹⁵
Parameter	Value																						
Module Form Factor	OSFP																						
Number of Data Lanes	8 TX and 8 RX per module (PAM4)																						
Maximum Aggregate Data Rate	800Gbps																						
Nominal Data Rate per Lane	106.25Gbps (PAM4)																						
Electrical Interface and Pin-out	60-pin edge connector																						
Pin Description	Per OSFP Hardware Specification																						
Management Interface	I ² C, serial, timing per Common Management Interface Specification for 8X/16X Pluggable Transceivers v 4.0																						
Length of Copper AEC	0.5m - 2.5m in 0.5m increments																						
BER (Pre-FEC)*	Typ. <10 ⁻⁸																						
BER (Post-FEC)*	<10 ⁻¹⁵																						

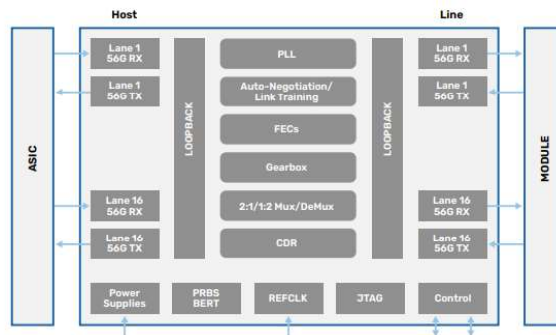
'252 Patent	Domestic Industry Products
Claim 1	
<p>[1c] each of the first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream,</p>	<p>Each of the first and second connectors in the Domestic Industry Products includes a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream.</p> <p>For example, each of the DSPs in the Domestic Industry Products performs retiming that involves clock and data recovery on the electrical input signal and extracts and remodulates the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream.</p>

'252 Patent

Domestic Industry Products

Claim 1

- Multi-channel bidirectional retimers for 10 - 56Gbps
- Superior random jitter performance
- Up to 35dB insertion loss
- CEI-56G-VSR/MR/LR-PAM4 compliant
- CEI-28G-LR and CEI-28G-VSR/SR/MR compliant
- TX equalization with programmable main, pre, and post-cursor
- Fully adaptive and programmable RX equalization with CTLE,FFE, and DFE
- Auto negotiation between the link partners on both sides of the retimer (IEEE 802.3 clause 73)
- KR back-channel training (IEEE 802.3 clause 72,92,93,136)
- Input/output polarity switch control
- Register control via I²C or standard MDIO interface
- Built in diagnostic features including PRBS generator and checker, PRBS FEC Analyzer, internal eye monitor and analog test point



Ex. 53, CRT55321 Product Brief at 2 (annotated).

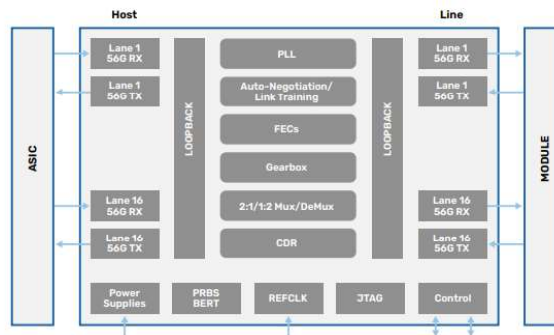
'252 Patent	Domestic Industry Products
Claim 1	
<p>[1d] the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and remodulate the transit data stream as the outbound data stream from the cable, and</p>	<p>The respective transceiver for each of the first and second connectors in the Domestic Industry Products performs clock and data recovery on the respective electrical transit signal to extract and remodulate the transit data stream as the outbound data stream from the cable.</p> <p>For example, each of the DSPs in the Domestic Industry Products performs retiming that involves performing clock and data recovery on electrical signals to extract and remodulate the transit data stream as the outbound data stream from the cable.</p>

'252 Patent

Domestic Industry Products

Claim 1

- Multi-channel bidirectional retimers for 10 - 56Gbps
- Superior random jitter performance
- Up to 35dB insertion loss
- CEI-56G-VSR/MR/LR-PAM4 compliant
- CEI-28G-LR and CEI-28G-VSR/SR/MR compliant
- TX equalization with programmable main, pre, and post-cursor
- Fully adaptive and programmable RX equalization with CTLE,FFE, and DFE
- Auto negotiation between the link partners on both sides of the retimer (IEEE 802.3 clause 73)
- KR back-channel training (IEEE 802.3 clause 72,92,93,136)
- Input/output polarity switch control
- Register control via I²C or standard MDIO interface
- Built in diagnostic features including PRBS generator and checker, PRBS FEC Analyzer, internal eye monitor and analog test point



Ex. 53, CRT55321 Product Brief at 2 (annotated).

'252 Patent	Domestic Industry Products
Claim 1	
<p>[1e] the respective transceivers each employing fixed, cable-independent equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal.</p>	<p>The respective transceivers in the Domestic Industry Products employ fixed, cable-independent equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal.</p> <p>For example, the DSPs at each end of the cable employ fixed, cable-independent equalization parameters for the remodulation of the transit data stream as the outbound stream and the clock and data recovery performed on the input signal. These parameters (i.e., transmit and receive filter coefficient values) are fixed and cable-independent per the IEEE 802.3ck standard (which are independent of communications through the cable).</p> <p>For example, the exemplary Domestic Industry Products comply with the OSFP standard.</p> <p>Supported Standards and Interfaces</p> <hr style="width: 50px; margin-left: 0;"/> <ul style="list-style-type: none"> • Common Management Interface Specification (CMIS) v4.0 • OSFP MSA v3.0 <p>Ex. 62, <i>Credo 800G OSFP AEC Product Specification</i> at 1.</p> <p>As explained in the OSFP specification, the high-speed signals of the Domestic Industry Products meet the requirements of the IEEE 802.3ck standard.</p>

'252 Patent	Domestic Industry Products
Claim 1	
	<p>The high-speed signals follow the electrical specifications of IEEE802.3bs, IEEE802.3cd, IEEE 802.3ck and CEI-56G-VSR-PAM4 as defined in OIF-CEI-05.2 for 400GAUI-8 mode and IEEE802.3bj, IEEE802.3bm for CAUI-4 mode.</p> <p>Ex. 54, <i>OSFP Specification</i> at 147.</p> <p>The 802.3ck standard defines the chip-to-module connection, including requiring that the transmitters use a pre-equalized set of filters as part of selecting a short or long channel.</p> <p>120G.3.2.1 Module output modes</p> <p>The module output shall support two modes: short and long. The means of controlling the module output mode is implementation dependent. For each output mode, the module shall meet the requirements for eye height (min) and VEC (max) in Table 120G-3 for both near-end and far-end measurements (see 120G.3.2.2.1).</p> <p>Ex. 52, <i>IEEE 802.3ck Specification</i> at 7275 (annotated).</p> <p>The Domestic Industry Products also comply with the Common Management Interface Specification (CMIS) standard.</p> <p>Supported Standards and Interfaces</p> <hr/> <ul style="list-style-type: none"> • Common Management Interface Specification (CMIS) v4.0 • OSFP MSA v3.0

'252 Patent	Domestic Industry Products											
Claim 1												
	<p>Ex. 62, <i>Credo 800G OSFP AEC Product Specification</i> at 1.</p> <p>The CMIS standard controls the equalization of the port transceiver, including employing fixed, cable-independent equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal.</p> <p>6.2.5.1 Tx Input Equalization Control</p> <p>The controls for Tx input equalization can be grouped by equalization type, as shown in Table 6-5.</p> <p>Table 6-5 Tx Input Eq control relationship to AdaptiveInputEqEnableTx</p> <table border="1" data-bbox="594 926 1411 1041"> <thead> <tr> <th>Equalization Type</th> <th>Control</th> <th>AdaptiveInputEqEnableTx</th> </tr> </thead> <tbody> <tr> <td rowspan="3">Adaptive</td> <td>AdaptiveInputEqFreezeTx</td> <td rowspan="3">1</td> </tr> <tr> <td>AdaptiveInputEqStoreTx</td> </tr> <tr> <td>AdaptiveInputEqRecallTx</td> </tr> <tr> <td>Non-Adaptive</td> <td>FixedInputEqTargetTx</td> <td>0</td> </tr> </tbody> </table> <p>The controls relevant for adaptive Tx input equalization are described in section 6.2.5.4.</p> <p>The controls relevant for non-adaptive Tx input equalization, when Tx input equalization settings are pre-determined or host provisioned, are described below.</p> <p>The module ignores control field values that are not relevant for the current AdaptiveInputEqEnableTx setting.</p>	Equalization Type	Control	AdaptiveInputEqEnableTx	Adaptive	AdaptiveInputEqFreezeTx	1	AdaptiveInputEqStoreTx	AdaptiveInputEqRecallTx	Non-Adaptive	FixedInputEqTargetTx	0
Equalization Type	Control	AdaptiveInputEqEnableTx										
Adaptive	AdaptiveInputEqFreezeTx	1										
	AdaptiveInputEqStoreTx											
	AdaptiveInputEqRecallTx											
Non-Adaptive	FixedInputEqTargetTx	0										

'252 Patent	Domestic Industry Products																														
Claim 1																															
	<p>Host Controlled Equalization</p> <p>Tx input equalization values in dB are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.</p> <p>SCS<k>::FixedInputEqTargetTx<i> is a four-bit control field for lane <i> and encoded as shown in Table 6-6. This field allows the host to specify a fixed (non-adaptive) Tx input equalization target and is ignored by the module if AdaptiveInputEqEnableTx<i> is set for that lane.</p> <p>The module advertises support of non-adaptive Tx input equalization control as described in Table 8-48.</p> <p>The module advertises the maximum supported Tx input equalization values as described in Table 8-44.</p> <p style="text-align: center;">Table 6-6 Fixed Tx Input Equalization Codes</p> <table border="1" data-bbox="735 894 1250 1121"> <thead> <tr> <th>Code Value</th> <th>Bit pattern</th> <th>Input Equalization</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0000b</td> <td>No Equalization</td> </tr> <tr> <td>1</td> <td>0001b</td> <td>1 dB</td> </tr> <tr> <td>2</td> <td>0010b</td> <td>2 dB</td> </tr> <tr> <td>3 - 8</td> <td>0011b ... 1000b</td> <td>3 dB ... 8 dB</td> </tr> <tr> <td>9</td> <td>1001b</td> <td>9 dB</td> </tr> <tr> <td>10</td> <td>1010b</td> <td>10 dB</td> </tr> <tr> <td>11</td> <td>1011b</td> <td>11 dB</td> </tr> <tr> <td>12</td> <td>1100b</td> <td>12 dB</td> </tr> <tr> <td>13-15</td> <td></td> <td>Custom</td> </tr> </tbody> </table>	Code Value	Bit pattern	Input Equalization	0	0000b	No Equalization	1	0001b	1 dB	2	0010b	2 dB	3 - 8	0011b ... 1000b	3 dB ... 8 dB	9	1001b	9 dB	10	1010b	10 dB	11	1011b	11 dB	12	1100b	12 dB	13-15		Custom
Code Value	Bit pattern	Input Equalization																													
0	0000b	No Equalization																													
1	0001b	1 dB																													
2	0010b	2 dB																													
3 - 8	0011b ... 1000b	3 dB ... 8 dB																													
9	1001b	9 dB																													
10	1010b	10 dB																													
11	1011b	11 dB																													
12	1100b	12 dB																													
13-15		Custom																													

Claim 1

6.2.5.2 Rx Output Equalization Control

Rx output equalization is defined at an appropriate test point defined by the relevant standard.

SCS<k>::**OutputEqPreCursorTargetRx**<i> and SCS<k>::**OutputEqPostCursorTargetRx**<i> are four-bit control fields for lane <i> and encoded as shown in Table 6-7.

The module advertises support of Rx output equalization control as described in Table 8-48.

The module advertises the maximum supported Rx output equalization values as described in Table 8-44.

Modules that require only output emphasis utilize the SCS<k>::**OutputEqPostCursorTargetRx**<i> fields and set the SCS<k>::**OutputEqPreCursorTargetRx**<i> fields to zero.

Table 6-7 Rx Output Equalization Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000b	0dB (No Equalization)	0dB (No Equalization)
1	0001b	1 dB	0.5 dB
2	0010b	2 dB	1.0 dB
3	0011b	3 dB	1.5 dB
4	0100b	4 dB	2.0 dB
5	0101b	5 dB	2.5 dB
6	0110b	6 dB	3.0 dB
7	0111b	7 dB	3.5 dB
8-10	1000b-1010b	Reserved	Reserved
11-15	1011b-1111b	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
 Pre EQ (dB) = $-20 \cdot \log_{10}(1 - C_{-1} / (C_{-1} + C_0 + C_1))$ (Eq. 6-1)
 The post-cursor equalizer settings in dB approximates to
 Post EQ (dB) = $-20 \cdot \log_{10}(1 - C_1 / (C_{-1} + C_0 + C_1))$ (Eq. 6-2)
 Equalizer coefficients C_n are pre-cursor for $n < 0$ and post-cursor when $n > 0$.

Ex. 55, *CMIS Specification* at 60–61.

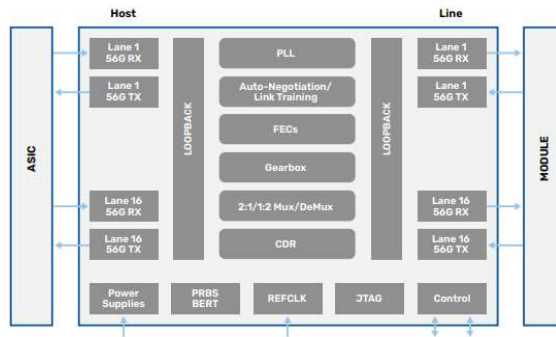
See also, e.g.:

'252 Patent

Domestic Industry Products

Claim 1

- Multi-channel bidirectional retimers for 10 - 56Gbps
- Superior random jitter performance
- Up to 35dB insertion loss
- CEI-56G-VSR/MR/LR-PAM4 compliant
- CEI-28G-LR and CEI-28G-VSR/SR/MR compliant
- TX equalization with programmable main, pre, and post-cursor
- Fully adaptive and programmable RX equalization with CTLE,FFE, and DFE
- Auto negotiation between the link partners on both sides of the retimer (IEEE 802.3 clause 73)
- KR back-channel training (IEEE 802.3 clause 72.92,93,136)
- Input/output polarity switch control
- Register control via I²C or standard MDIO interface
- Built in diagnostic features including PRBS generator and checker, PRBS FEC Analyzer, internal eye monitor and analog test point



Ex. 53, CRT55321 Product Brief at 2 (annotated).