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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
61/084,616	07/29/2008		105			

CONFIRMATION NO. 3183

Jeffrey Raymond Eastlack
301 E. 4TH ST #314
Austin, TX 78701

FILING RECEIPT

OC000000031424050

Date Mailed: 08/13/2008

Receipt is acknowledged of this provisional patent application. It will not be examined for patentability and will become abandoned not later than twelve months after its filing date. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Jeffrey Raymond Eastlack, Austin, TX;

Power of Attorney: None

If Required, Foreign Filing License Granted: 08/06/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 61/084,616**

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****
Title

Vampire Proof Device Controlled Battery Charger System

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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Doc Code: **TR.PROV**
Document Description: Provisional Cover Sheet (SB16)

PTO/SB/16 (04-07)
Approved for use through 06/30/2010 OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Provisional Application for Patent Cover Sheet

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c)

Inventor(s)

Inventor 1 — Remove

Given Name	Middle Name	Family Name	City	State	Country i
Jeffrey	Raymond	Eastlack	Austin	TX	US

All Inventors Must Be Listed – Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. — Add

Title of Invention	Vampire Proof Device Controlled Battery Charger System
Attorney Docket Number (if applicable)	

Correspondence Address

Direct all correspondence to (select one):

○ The address corresponding to Customer Number	◉ Firm or Individual Name
Firm or Individual Name 1	Jeffrey Raymond Eastlack
Firm or Individual Name 2	

Mailing Address of Applicant:

Address 1	301 E. 4TH ST #314		
Address 2			
City	Austin	State/Province	TX
Postal Code	78701	Country i	US
Phone	512-784-4307		

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

◉ No.

○ Yes, the name of the U.S. Government agency and the Government contract number are:

Doc Code: **TR.PROV**
Document Description: Provisional Cover Sheet (SB16)

PTO/SB/16 (04-07)
Approved for use through 06/30/2010 OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Entity Status

Applicant claims small entity status under 37 CFR 1.27

(•) Yes, applicant qualifies for small entity status under 37 CFR 1.27

( ) No

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Signature

Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Jeffrey R. Eastlack/			Date (YYYY-MM-DD)	Jul 4, 2008
First Name	Jeffrey	Last Name	Eastlack	Registration Number (If appropriate)	

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Vampire Proof Device Controlled Battery Charger System

Inventor – J. R. Eastlack, Vampire Labs

Abstract— **Vampire energy loss occurs when an electronic or mechanical machine consumes energy while not being utilized for any useful purpose. Vampire energy losses in consumer electronic devices are under intense scrutiny for needlessly wasting an estimated 12% of the electric power production in the United States. The current invention proposes a method to eliminate vampire energy loss in battery chargers by employing the use of a digital control circuit coupled with intelligent software algorithms to eliminate this power loss.**

Index Terms— **"Zero No Load Loss" (ZNLL), Vampire Energy Loss, Vampire Proof, Standby Power**

I. Background

Field of Invention

THIS invention relates to power efficient battery chargers and technology that eliminates vampire energy loss using the circuit resources of the target device for application specific shutdown intelligence of the DC power source.

The basic DC power supply or battery charger plugs into an AC source via a wall receptacle and employs the use of a step-down transformer **104**, signal rectification circuitry **106**, and voltage regulation circuitry **108**. The transformer consists of two conductively independent coils that are mutually coupled by magnetic flux when current flows in one of them. The AC current flowing in the primary coil produces a changing magnetic field within the transformer core and there by induces an electric current in the secondary coil as described by Faraday's Law.

From transformer theory "no-load loss" is when energy loss occurs even when the secondary coil is left open or not attached to a load. According to academic literature the cause of no-load loss is attributed to eddy currents and magnetic hysteresis within the transformer core. In addition to no-load loss from the transformer, DC power supplies also incur dynamic and static power loss within the rectification and regulation circuitry. All of these combined losses within the DC power supply attribute to a significant portion of "vampire energy loss" which exists in many electronic product domains. In addition to no-load loss, it was noted during characterization experiments of charging batteries that the chargers incurred loading from the target device even after the target device battery had been charged as shown in section **706**. This power usage from the target device after the battery is charged is defined as parasitic loading within this document. The term "parasitic" is used by Electrical Engineers to illustrate that a particular quantity is undesired in the context of a circuit or a specific application domain. Techniques have been in place to reduce no-load loss within transformers and parasitic loading of electronic devices; however the only way to completely stop no-load loss and parasitic loading of existing devices is to take the DC power supply and the target device off of the power grid.

There are existing solutions for reducing vampire power loss but they are markedly different from the proposed invention.

The first of these inventions is the USB Ecostrip. In the design of this USB connected power strip, the power bus of a standard USB compliant port of a host device is used to provide the power to the switching mechanisms of the power strip. If the USB host is turned off then the power strip has no power for other devices on the power strip. In another power strip design called the Smart Power Strip, one master outlet on the strip controls six other slave outlets. When the power usage of the master outlet decreases, it automatically turns off the slave outlets.

Next is an invention titled "Vampire Proof Analog Controlled Mobile Device Battery Charger" (US patent application number 61078365) proposed by the same inventor of this invention but involves analog control circuits for application specific shutdown intelligence of the charger. The problem with this invention is that it is not ideal for all use cases of battery operated devices. The user must initiate the charging session by pressing the push button switch, and then the control circuit disconnects the charger from the power grid once the battery has charged. Each session must be initiated by the pushbutton switch and if the battery is drained by standby mode or actual use of the device then the push button must be pressed again.

These inventions differ from the proposed invention as they lack application specific shutdown intelligence for all use cases. Both power strips monitor the power usage of a master device and make the assumption that a slave device adheres to the same use case as the master device. There are many possible cases where slave devices require power during times that a master device does not. These conditions may limit the functionality of both the USB Ecostrip and the Smart Power Strip for many peripheral devices which could result in vampire energy loss. The "Vampire Proof Analog Controlled

Mobile Device Battery Charger" eliminates vampire energy loss but is not capable of maintaining a charged battery once the charge session has completed which may be necessary for some devices and use cases.

Therefore, there is a need for a battery charger which eliminates the vampire energy loss and capable of maintaining a charged battery even after the completion of the charge session.

II. Summary

The "Vampire Proof Target Device Controlled Battery Charger System" employs support hardware and the built-in battery monitoring capabilities of the target device to make a decision on when to disconnect itself and the charger from the electric power grid. Control algorithms will be used to monitor the digitized status of the battery and digitally control the "on current" to the opto-coupled relay to allow AC power to the charger components. This allows CPU control of the battery charger which allows use case flexibility for many CPU controlled mobile devices which are commonly used while plugged in such as laptop computers and other mobile devices which are illustrated in **FIG. 5**. It also allows the employment of non-linear charging regiments to increase the health and life of the battery.

The "Vampire Proof Target Device Controlled Battery Charger System" eliminates all components of vampire energy loss in this particular application domain which includes the "no load loss" of the step down transformer **104**, static and dynamic power consumption of the signal rectification **106** and regulation **108** circuitry within the device battery charger **112**, and the post charge parasitic loading of the connected mobile device **110**. The Target Controlled Vampire Proof ZNLL mobile device battery charger circuitry has been designed to be integrated into future charger designs and require hardware and software support from the target device.

III. Description Of The Drawings

FIG. 1 shows the basic components of a typical battery charger without vampire proof capabilities.

FIG. 2 shows an application block diagram that illustrates the integration of the target controlled relay circuit with future charger designs and the necessary circuit support from future mobile devices.

FIG. 3 outlines the basic block components of the target controlled charger system with arrows representing the flow of the operational signals between the target device and the charger. The blocks on the left illustrate hardware on the charger and blocks on the right depict hardware on the target device.

FIG. 4 shows the design schematic of the necessary hardware from the target and the charger's relay circuitry. The diagram also illustrates connection ports which map to signals in the block diagram shown **FIG. 2**.

FIG. 5 illustrates an image of how the charger hardware of the vampire proof target controlled charger system could be realized with the push button switch and the required six terminal connection port.

FIG. 6 illustrates how the invention concept could be expanded to other products. The examples include various types of battery operated portable devices that require frequent battery charging and could be capable of monitoring the charge level of the battery.

FIG. 7 shows a usage flow chart that illustrates temporal operation between the user initiated charging session, and the target devices control algorithm.

IV. Detailed Description

The Vampire Proof target controlled mobile device battery charger system requires hardware and software support from the target device. The majority of battery operated mobile devices today employ the use of battery monitor **316** for a variety of reasons. This proposed invention will expand the need for such capabilities as they will be employed by the control algorithm of this charger system.

The charger system uses a voltage signal that is referred to as the "source signal" **302** by the target device, a feedback loop that is referred to as the "source feedback" **304** of the source signal **302** from the charger back to a "feedback sense" input buffer **306** of the target device. This feedback can only occur when the target device is connected to the charger and thus serves as a detection mechanism for the control algorithm described in **FIG. 7**. A logic state change on the feedback sense input buffer **306** will trigger an interrupt by the interrupt controller **308** to initiate an interrupt service routine (ISR) by the CPU **310**. Based on the strength of the battery reported by the battery monitor **316,** the control algorithm as described in **FIG. 7** will make the decision to provide the "on current" to the AC relay circuit **314** on the charger **216** via the output buffer **312**.

The voltage source signal **302** is simply connected by node **424** to the IO supply **408** of the system on a chip (SoC). A ground connected decoupling capacitor **426** is placed in parallel to the IO supply **408** in order to reduce noise. The source signal **302** maps to signal **206** and is connected to signal **208** via the source feedback circuit **304** which electrically shorts the two signals **206** and **208** together as described by connection **412**. The feedback loop serves as the detection mechanism for the feedback sense input buffer **306** on the target device. Modern SoC's employ widespread use of General Purpose Input Output (GPIO) hardware for a large

variety of applications and are used in this invention for the output buffer **312** and feedback sense input **306**. In **FIG. 4** the output buffer **312** is the last stage of the MOSFET inverter chain found on SoC IO signals and is composed of pFET **418** and nFET **420**. Feedback sense input buffer **306** is conversely the first stage of the input inverter chain and is composed of pFET **414** and nFET **416**. The logical equivalent of the input voltage present at signal **208** will be mapped to an internal register address that can be accessed by the CPU **310** of the SoC. When the voltage state of signal **208** is changed by the user connecting or disconnecting the charger from the device, the interrupt controller **308** will trigger an ISR for the CPU **310** to service. A high valued pull down resistor **422** is used to keep the input port from "floating" while not connected to the charger. When the control algorithm decides that the battery needs charging the CPU will write a logic 1 to the register address that maps to the GPIO output buffer **312** which is the last stage of the inverter chain with an output value that is the inverted value of signal **406**. The GPIO port employed as output buffer **312** must be capable of providing the necessary on current to the AC relay circuit **314** composed of an opto-coupled relay **402** and a current limiting resistor **404**.

FIG. 7 is a flow chart that describes the user operations to initiate a charge session in which the user must plug in the charger and connect the device as described in step **704**. In the case where the device battery is completely discharged the user must hold down the push button switch **502** until the device boots up and the control algorithm is able to source the "on current" to the AC relay circuit **314**. At step **710,** the target device **110** will be able to source the "on current" to the relay circuit. The CPU **310** will then check the status of the GPIO input port employed as the feedback sense input buffer **306** by polling the internal register address that maps to that particular GPIO signal. If the feedback signal is not present then the target device is not connected to the charger and the CPU will exit the ISR, if the feedback signal is present then the CPU will write a logic '1' to the GPIO output port that is being employed as the output buffer **312**, which will source the "on current" to the AC relay circuit **314** thus turning on the charger circuit to charge the battery. The CPU will then monitor the digitized charge strength status of the battery via the battery monitoring circuitry **316** while keeping the "on current" to the AC relay circuit **314** as described in step **714**. At step **716** a check of historical information on the same charge session is performed to determine if the charge strength is increasing over time. If the battery strength is not increasing over time the control algorithm determines that the charger not connected to the wall receptacle and the CPU will then disables the "on current" to the relay circuit **314** to preserve battery strength. Other methods to determine if the charger is connected to the device without the charger connected to the AC source from the wall receptacle could include the uses of another GPIO port configured as an input. This input port could be connected to the level shifted voltage of the charger's supply voltage. This input could be then incorporated into the control algorithm as a flag to signal the connection status of the charger to the wall receptacle.

When the battery is charged the CPU will write a logic '0' to the output buffer **312** which stops the "on current" to the relay circuit **314** which electrically disconnects the charger from the wall receptacle thus eliminating vampire energy loss as described in step **720**. If the user decides to keep the device connected to the charger as in step **722** the feedback signal will be present and the control algorithm will then monitor the strength of the battery until the standby mode of the device drains the battery past a predefined threshold described in step **724** in which case the CPU will allow "on current" to the AC relay circuit **314**.

In **FIG. 4** it is important to clarify that the output buffer **312** and feedback sense input buffer **306** represent the GPIO ports on a modern SoC. Signals **406** and **410** map to register addresses that are assigned by the particular SoC's memory map. It is also important to note that many different implementation methods from the proposed invention are possible. For example instead of using the CPU resources of the mobile devices SoC, the control algorithm could be realized using state machines coupled with the required support circuitry. This digitized control algorithm could also be realized using a hardware description language (HDL) and incorporated directly into a power management integrated circuit (IC) or even a standalone IC with assumed direct access to the battery monitor **316** of the target device **110**.

V. DRAWINGS

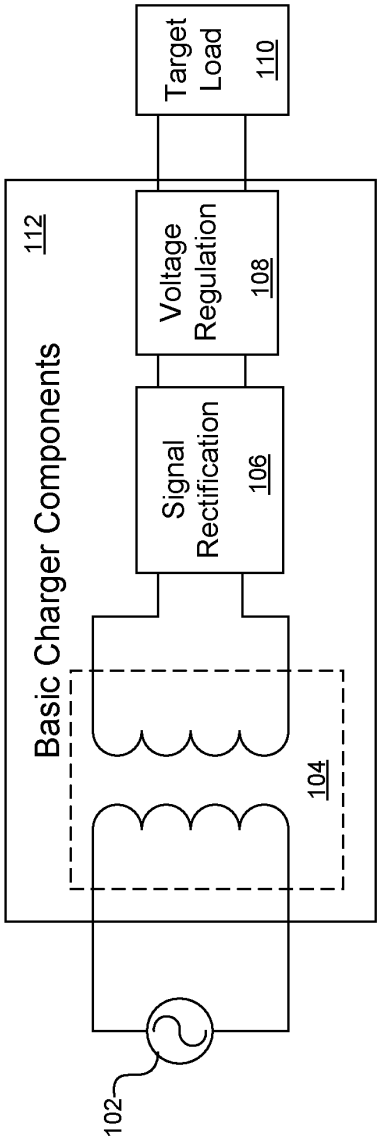

FIG. 1

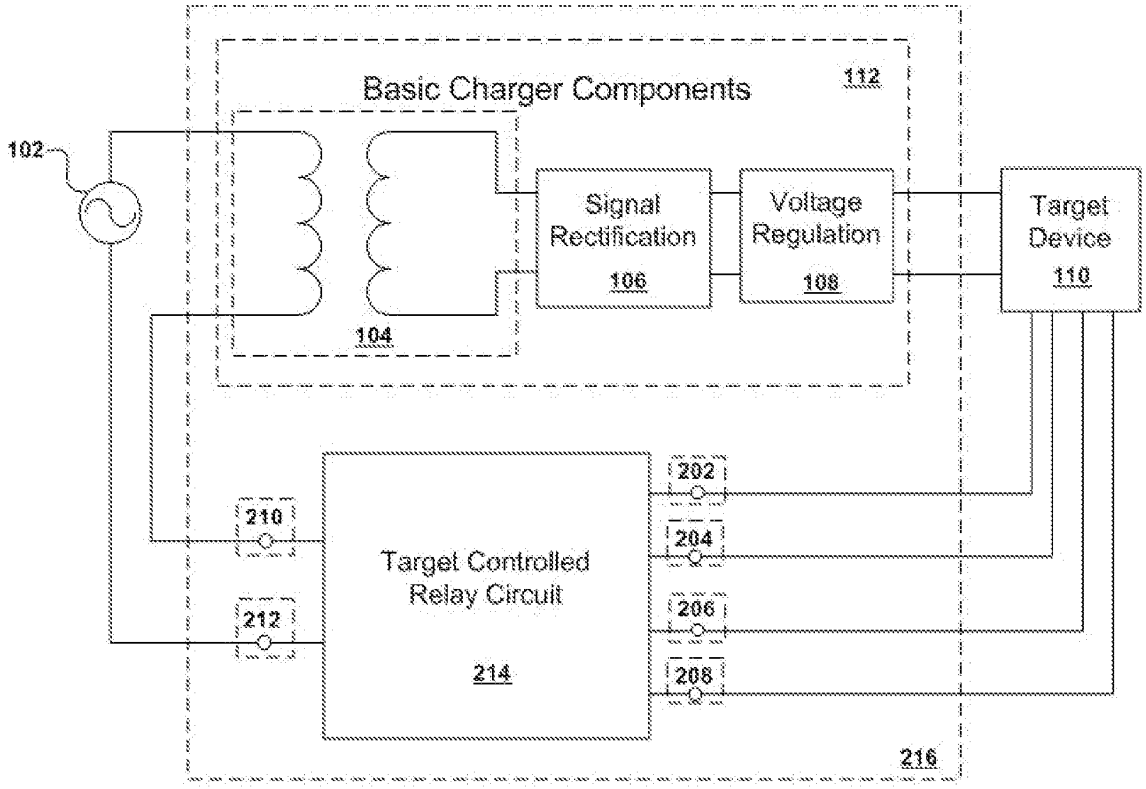
Basic Charger Components
112
102
Signal Rectification
106
Voltage Regulation
108
Target Device
110
104
210
212
Target Controlled Relay Circuit
214
202
204
206
208
216

FIG. 2

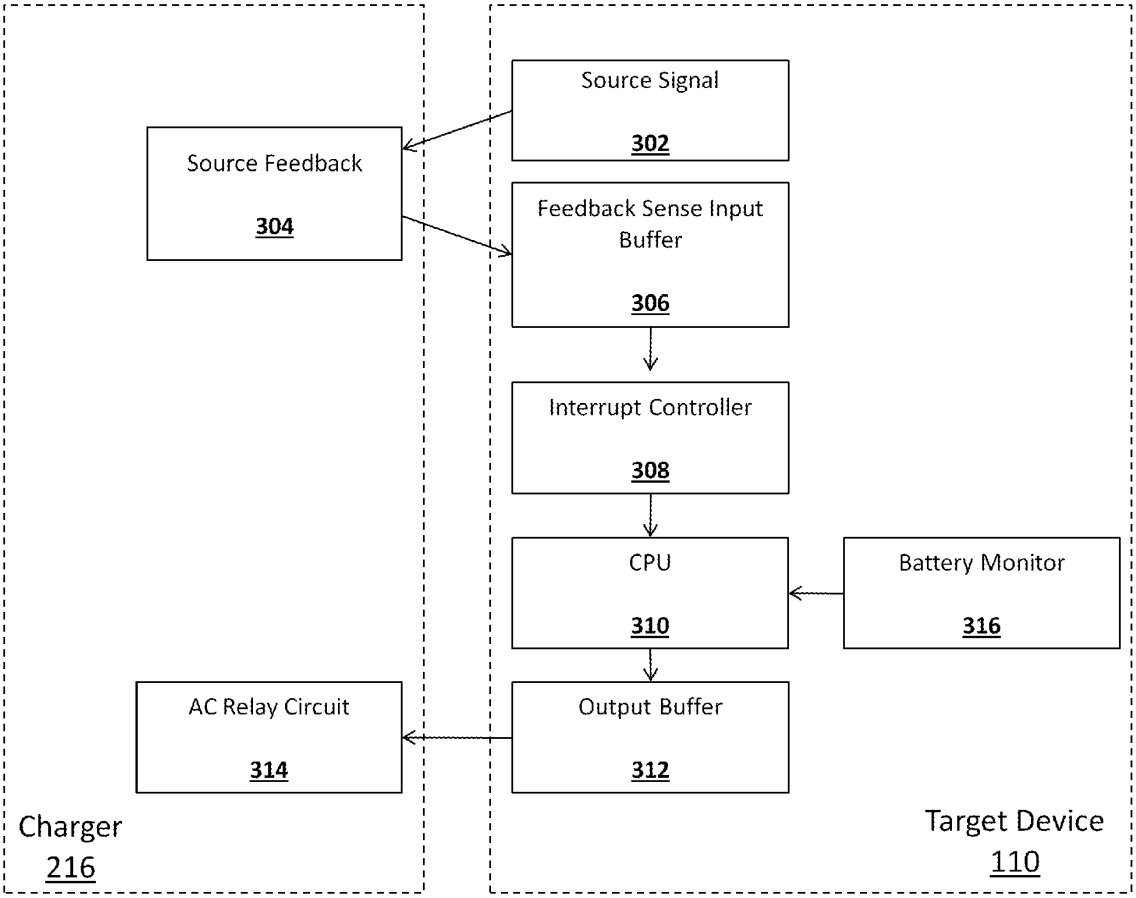
Source Signal
302
Source Feedback
304
Feedback Sense Input Buffer
306
Interrupt Controller
308
CPU
310
Battery Monitor
316
AC Relay Circuit
314
Output Buffer
312
Charger
216
Target Device
110

FIG. 3

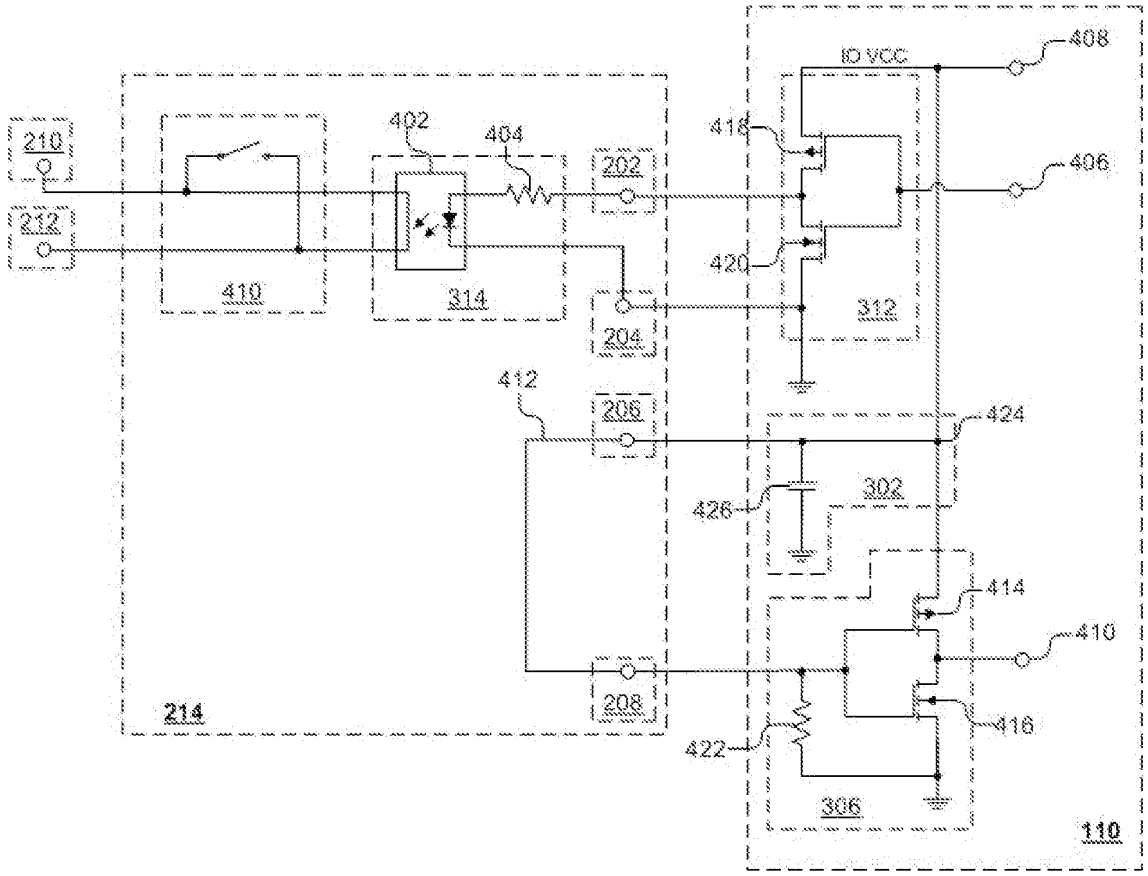
ID VCC
408
406
416
420
312
210
212
410
402
404
314
202
204
412
206
424
302
426
414
410
208
214
416
422
306
110

FIG. 4

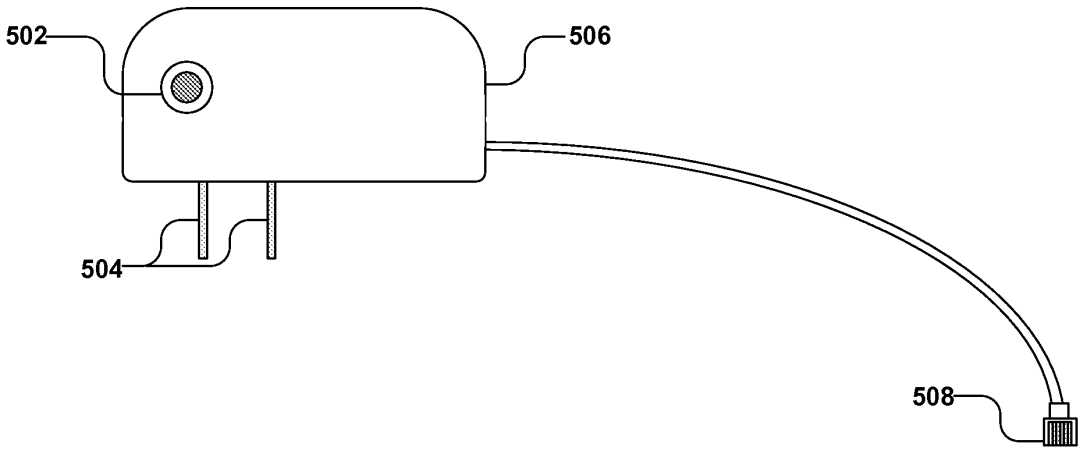
502
506
504
508

FIG. 5

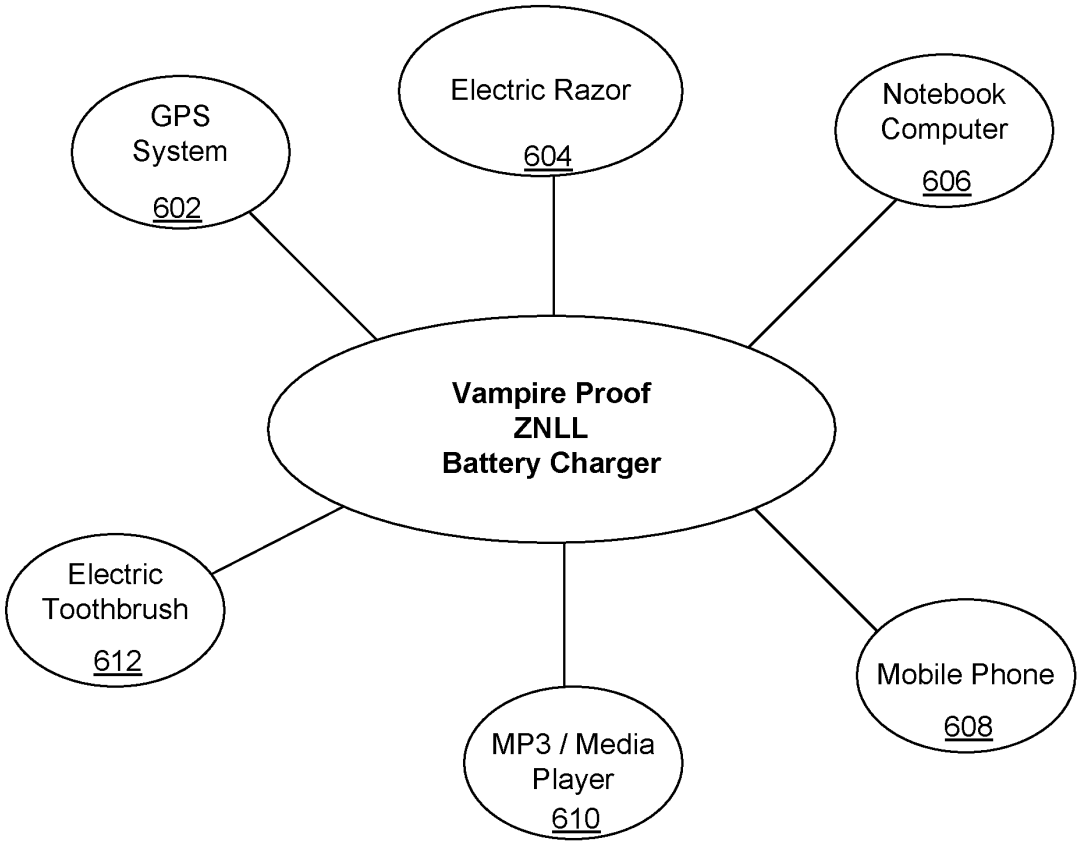
GPS System
602
Electric Razor
604
Notebook Computer
606
Vampire Proof
ZNLL
Battery Charger
Electric Toothbrush
612
MP3 / Media Player
610
Mobile Phone
608

FIG. 6

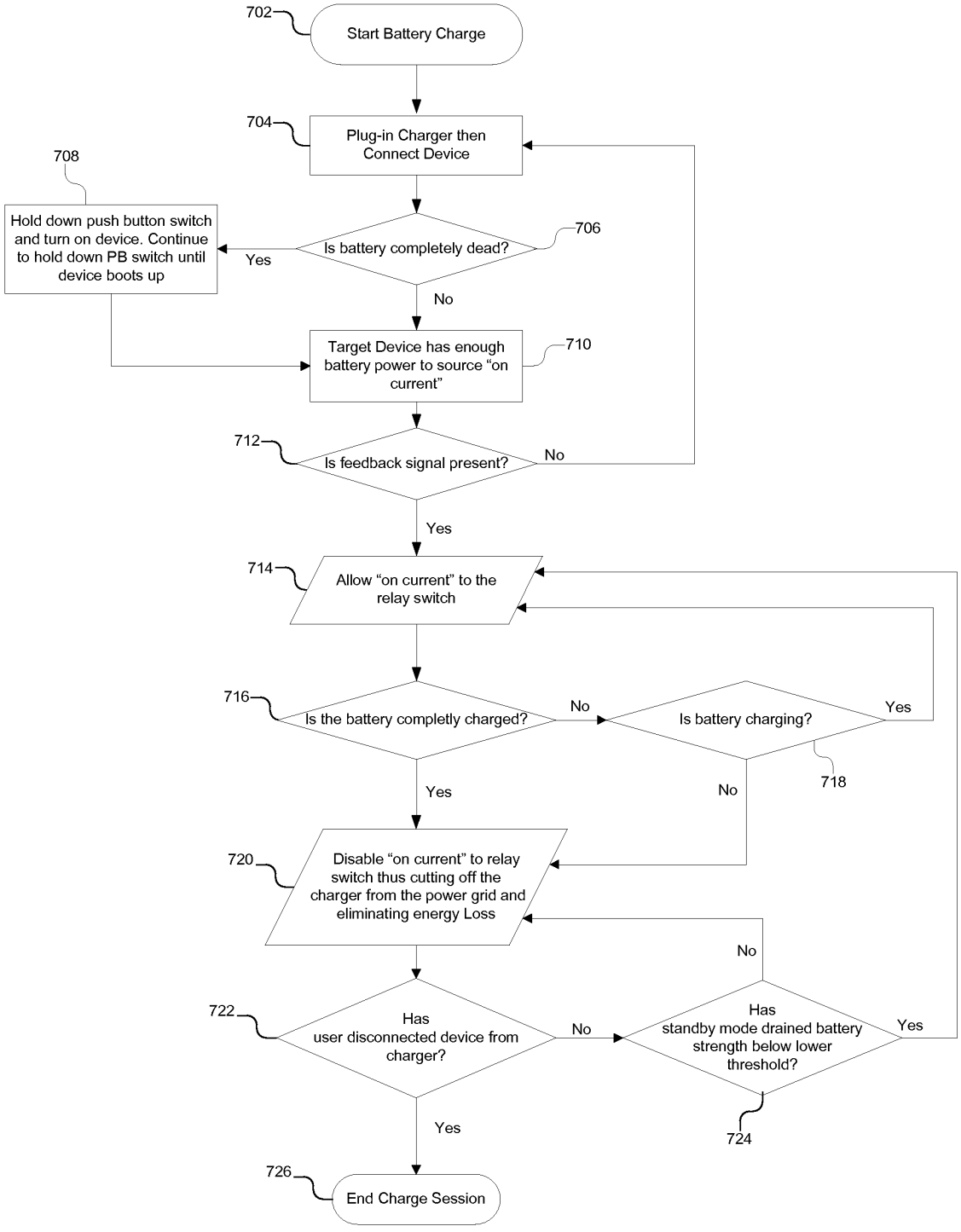
702
Start Battery Charge
704
Plug-in Charger then Connect Device
708
Hold down push button switch and turn on device. Continue to hold down PB switch until device boots up
Is battery completely dead?
706
Yes
No
Target Device has enough battery power to source "on current"
710
712
Is feedback signal present?
No
Yes
714
Allow "on current" to the relay switch
716
Is the battery completly charged?
No
Is battery charging?
Yes
718
Yes
No
720
Disable "on current" to relay switch thus cutting off the charger from the power grid and eliminating energy Loss
No
722
Has user disconnected device from charger?
No
Has standby mode drained battery strength below lower threshold?
Yes
724
Yes
726
End Charge Session

FIG. 7

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	Vampire Proof Device Controlled Battery Charger System
First Named Inventor/Applicant Name:	Jeffrey Raymond Eastlack
Filer:	Jeffrey Eastlack
Attorney Docket Number:	

Filed as Small Entity

Provisional Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Provisional Application filing fee	2005	1	105	105
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**105**

Electronic Acknowledgement Receipt	
EFS ID:	3698099
Application Number:	61084616
International Application Number:	
Confirmation Number:	3183
Title of Invention:	Vampire Proof Device Controlled Battery Charger System
First Named Inventor/Applicant Name:	Jeffrey Raymond Eastlack
Correspondence Address:	Jeffrey Eastlack - 301 E. 4TH ST #314 Austin TX 78701 US 512-784-4307 jeff@vampirelabs.com
Filer:	Jeffrey Eastlack
Filer Authorized By:	
Attorney Docket Number:	
Receipt Date:	29-JUL-2008
Filing Date:	
Time Stamp:	23:32:27
Application Type:	Provisional

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$105

RAM confirmation Number	4704
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Provisional Cover Sheet (SB16)	Eastlack_002_ProvisionalPatentApplicationCover.pdf	1523023 75ec5126d9611504b1225370bada50f79305c900	no	3
Warnings:					
Information:					
2	Specification	VampireProofDeviceControlledBatteryChargerSystem.pdf	319380 1a7dbae63f09f31a41d050b7ee0f5113fc260609	no	9
Warnings:					
Information:					
3	Fee Worksheet (PTO-06)	fee-info.pdf	8103 1b576d5146fc5d38f1ba862cd13ca8abc11b9fccf	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1850506		

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