Mike Shuo-Wei Chen

3737 Watt Way, PHE 622, Los Angeles, CA 90089
Email: shuowei@gmail.com (Alt: swchen@usc.edu)
Phone: 510-517-0052

Curriculum Vitae

EDUCATION

University of California, Berkeley 2002 – 2006
- PhD in Electrical Engineering and Computer Science
- Dissertation: "High-Speed, Low-Power A/D Converter for a Low-Cost UWB Sub-sampling Radio"
- Advisor: Robert W. Brodersen

University of California, Berkeley 2000 – 2002
- Master of Science in Electrical Engineering and Computer Science
- Thesis: "Ultra Wideband Baseband Design and Implementation"

National Taiwan University 1994 – 1998
- Bachelor of Science in Electrical Engineering
- Top 1 student for upper division

ACADEMIC EXPRIENCE

- Full Professor, Department of Electrical Engineering, University of Southern California, 2021 – Present.
- Associate Professor, Department of Electrical Engineering, University of Southern California, 2017 – 2021.
- Colleen and Roberto Padovani Early Career Chair, USC, 2014 – 2021
- Assistant Professor, Department of Electrical Engineering, University of Southern California, 2011 – 2017.
- Graduate Student Researcher, Berkeley Wireless Research Center, Berkeley, CA, 2001 – 2006.

WORK EXPRIENCE

- Analog Senior Technical Staff, Atheros Communications, Santa Clara, CA, 2006–2010.
  -Designed RF, analog mixed-signal circuits for various wireless products

CONSULTING EXPERIENCE

- Legal Consulting
  (2019-2022): Xilinx-ADI litigation

Legal consultant, working with counsels to prepare/review legal documents, non-infringement arguments, deposition, source codes, PTAB, etc.
(2023-Present): Aptiv-Microchip
Legal expert, working with counsel on IPR expert declaration, source code review for litigation, etc.
(2023-2024): ARM-Qualcomm litigation
Legal expert, working on source code review, expert report, and deposition, testifying expert during trial
(2025-Present): Renasas-Monterey Research
Legal expert, IPR

- Technical Consulting:
  Qualcomm, Samsung, BAE system, Tetramem → Provide technical advices on various electronic projects for the client.

HONORS and AWARDS

- IEEE Fellow 2024
- ISSCC 2022 Jack Kilby Award (co-recipient)
- RFIC 2022 Best Student Paper Award – First Place (co-recipient)
- IEEE Solid-State Circuit Society (SSCS) Distinguished Lecturer 2021-2023.
- Qualcomm Faculty Award, 2019.
- DARPA Young Faculty Award (YFA), 2014.
- NSF Faculty Early Career Development (CAREER) Award, 2014.
- Analog Devices Outstanding Student Award, 2006
- UC Regents Fellowship, UC Berkeley, 2000
- Lin's Foundation Award for Top 1 engineering college student over the academic year, 1996-1997
- Presidential Awards, National Taiwan University, 1996-1998
- Member of National Mathematics Team of Taiwan, awarded with Honourable Mention in Asian Pacific Mathematics Olympiad, 1994.

AREA OF INTEREST

I worked on various Analog Mixed-Signal, VLSI, SoC and RF circuit architectures/techniques, covering a wide range of topics/areas in academia and industry, including

- Data Converters (e.g. ADC and DAC)
- RF/mm-Wave Wireless Communications (e.g. WiFi, 5G/6G, Bluetooth, GPS, etc.)
- I/O, Wireline Communications (e.g. SerDes, CDR, Clock generation)
- Computing (e.g. AI/ML accelerators, neuromorphic processor)
- Design Methodology (AI-ML assisted CAD).
- Digital VLSI, SOC, RTL
- Analog Mixed-Signal Circuit
- Power management circuit

PUBLICATIONS

Conferences

1. S. Mahapatra, M. Ayesh, C. Yang, M. Palaria, S. Su, A. Zhang, **M. S.-W. Che**n, "A 24GHz Direct Digital Transmitter Using Multiphase Subharmonic Switching PA Achieving 3.2Gbps Data Rate and -30.8dB EVM in 65nm CMOS", IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2025.
2. C. Yang, S. Su, M. Ayesh, S. Mahapatra, M. Hamada, V. Chenna, H. Hashemi, **M. S.-W. Chen**, "A Blocker Tolerant Receiver with VCO-based Non-Uniform Multi-Level Time-Approximation Filter With -36dB EVM in 28nm CMOS", IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2025. (to be presented)
3. J. Liu, A. Shabra, S. Ho, G. Manganaro, **M. S.-W. Chen**, "A 16GS/s 10b Time-domain ADC using Pipelined-SAR TDC with Delay Variability Compensation and Background Calibration Achieving 153.8dB FoM in 4nm CMOS" in *IEEE Symposium on VLSI Technology and Circuits (VLSI Technol. Circuits)*, June 2024.
4. Q. Zhang*, S. Su*, B. R. Biswas, S. Gupta, **M. S.-W. Chen**, "Synthesizable 10-bit Stochastic TDC Using Common-Mode Time Dithering and Passive Approximate Adder With 0.012mm2 Active Area in 12nm FinFET," in *IEEE Symposium on VLSI Technology and Circuits (VLSI Technol. Circuits)*, June 2024. (* equal contribution)
5. Q. Zhang*, S. Su*, Z. Liu*, H.-C. Cheng, Z. Qiu, M. Palaria, J. Ye, D. Meng, B. Chen, S. Hossain, W. Wu, **M. S.-W. Chen**, "A Stochastic Analog SAT Solver in 65nm CMOS Achieving 6.6µs Average Solution Time with 100% Solvability for Hard 3-SAT Problems," in *IEEE Symposium on VLSI Technology and Circuits (VLSI Technol. Circuits)*, June 2024. (* equal contribution)
6. M. Ayesh, S. Mahapatra, C. Yang and **M. S.-W. Chen**, "A 0.072-mm2 18-21GHz Non-Uniform Sub-Sampling Receiver with a Non-Uniform Discrete-Time FIR Filter Achieving 42dB Blocker Rejection in 28nm CMOS", *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2024.
7. M. Palaria, S. Su, H.-C. Cheng, R. Rasul, Q. Zhang, S. Mahapatra, C.-F. Law, S. Hossain, R. Bena, W. Wu, Q. Nguyen, M. S.-W. Chen, "Analog Kalman Filter with Integration and Digitization via a Shared Thyristor-Based VCO for Sensor Fusion in 65 nm CMOS", in *IEEE European Solid-State Circuits Conference (ESSCIRC)*, Sep. 2023.
8. H.-C. Cheng, S. Su, M. Palaria, Q. Zhang, C. Yang, S. Hossain, R. Bena, B. Chen, Z. Liu, J. Liu, R. Rasul, Q. Nguyen, W. Wu, **M. S.-W. Chen**, "A Memristor-Based Analog Accelerator for Solving Quadratic Programming problems," in IEEE Custom Integrated Circuits Conference (CICC), April 2023.
9. S. Su*, Q. Zhang*, and **M. S.-W. Chen**, "A 2GS/s 8.5-Bit Time-Based ADC Using a Segmented Stochastic Flash TDC," in 2023 IEEE Custom Integrated Circuits Conference (CICC), Apr. 2023 (* equal contribution)
10. Q. Zhang, H.-C. Cheng, S. Su, and **M. S.-W. Chen**, "A Fractional-N Digital MDLL with Injection Error Scrambling and Background Third-Order DTC Delay

Equalizer Achieving –67dBc Fractional Spur," in IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2023.

11. Q. Zhang*, S. Su*, and **M. S.-W. Chen**, "A Cost-Efficient Fully Synthesizable Stochastic Time-to-Digital Converter Design Based on Integral Nonlinearity Scrambling," in 2022 59th ACM/EDAC/IEEE Design Automation Conference (DAC), July 2022. (*contributed equally to this work)
12. C. Yang, S. Su and **Mike Chen**, "A Millimeter-Wave Mixer-First Receiver with Non-Uniform Time-Approximation Filter Achieving >45-dB Blocker Rejection," in IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2022. (Best Student Paper Award – First Place)
13. S. Su, and **M. S.-W. Chen**, "High-Speed Digital-to-Analog Converter Design Towards High Dynamic Range," (invited paper) *IEEE Custom Integrated Circuits Conference (CICC), Apr. 2022.*
14. J. Liu, M. Hassanpourghadi, and **M. S.-W. Chen**, "A 10GS/s 8b 25fJ/c-s 2850um2 Two-Step Time-domain ADC Using Delay-Tracking Pipelined-SAR TDC with 500fs Time Step in 14nm CMOS Technology", *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2022.
15. S. Su, Q. Zhang, M. Hassanpourghadi, J. Liu, R.A. Rasul, and **M. S.-W. Chen**, "Analog/Mixed-Signal Circuit Synthesis Enabled by the Advancements of Circuit Architectures and Machine Learning Algorithms," (invited paper) *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2022.
16. S. Su, Q. Zhang, J. Liu, M. Hassanpourghadi, R.A. Rasul, and **M. S.-W. Chen**, "TAFA: Design Automation of Analog Mixed-Signal FIR Filters Using Time Approximation Architecture," *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2022.
17. J. Liu, S. Su, M. Madhusudan, M. Hassanpourghadi, S. Saunders, Q. Zhang, R. Rasul, Y. Li, J. Hu, A. Kumar, S. S. Sapatnekar, R. Harjani, A. Levi, S. Gupta and **M. S.-W. Chen**, "From Specification to Silicon: Towards Analog/Mixed-Signal Design Automation using Surrogate NN Models with Transfer Learning", *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2021.
18. M. Hassanpourghadi, S. Su, R.A. Rasul, J. Liu, Q. Zhang, and **M. S.-W. Chen**, "Circuit Connectivity Inspired Neural Network for Analog Mixed-Signal Functional Modeling," *58th ACM/EDAC/IEEE Design Automation Conference (DAC)*, Dec. 2021.(to appear)
19. R.A. Rasul, and **M. S.-W. Chen**, "A 128×128 SRAM Macro with Embedded Matrix-Vector Multiplication Exploiting Passive Gain via MOS Capacitor for Machine Learning Application," *IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2021.
20. A. Zhang, M. Ayesh, S. Mahapatra, and **M. S.-W. Chen**, "A 24-28 GHz Concurrent Harmonic and Subharmonic Tuning Class E/F2,2/3 Subharmonic Switching Power Amplifier Achieving Peak/PBO Efficiency Enhancement," *IEEE Custom Integrated Circuits Conference (CICC), Apr. 2021*.
21. Q. Zhang, S. Su, C.-R. Ho, and **M. S.-W. Chen**, "A Fractional-N Digital MDLL with Background Two-Point DTC Calibration Achieving -60dBc Fractional Spur," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2021.
22. A. Zhang, C. Yang, M. Ayesh, and **M. S.-W. Chen**, "A 5-6 GHz Current-Mode Subharmonic Switching Digital Power Amplifier for Enhancing Power Back-off

Efficiency," *IEEE International Solid-State Circuits Conference (ISSCC),* Feb. 2021.

23. Q. Zhang, S. Su, J. Liu and **M. S.-W. Chen**, "CEPA: CNN-based Early Performance Assertion Scheme for Analog and Mixed-Signal Circuit Simulation," in *2020 IEEE/ACM International Conference on Computer-Aided Design (ICCAD),* November 2020.
24. J. Liu, M. Hassanpourghadi, Q. Zhang, S. Su and **M.S.-W. Chen**, "Transfer Learning with Bayesian Optimization-Aided Sampling for Efficient AMS Circuit Modeling," in *2020 IEEE/ACM International Conference on Computer-Aided Design (ICCAD),* November 2020.
25. C. Yang, M. Ayesh, A Zhang, T.F. Wu, **M. S.-W. Chen**, "A 29-mW 26.88-GHz Non-Uniform Sub-Sampling Receiver Front-End Enabling Spectral Alias Spreading, " *IEEE Radio Frequency Integrated Circuits Symposium (RFIC),* June, 2020.
26. S. Su and **M. S.-W. Chen**, "A SAW-Less Direct-Digital RF Modulator with Tri-Level Time-Approximation Filter and Reconfigurable Dual-Band Delta-Sigma Modulation," *IEEE International Solid-State Circuits Conference (ISSCC),* Feb. 2020.
27. T.-F. Wu and **M. S.-W. Chen**, "A 40MHz-BW 76.2dB/78.0dB SNDR/DR noise-shaping nonuniform sampling ADC with single phase-domain level crossing and embedded nonuniform digital signal processor in 28nm CMOS," *IEEE International Solid-State Circuits Conference (ISSCC),* Feb. 2020.
28. S. Su and **M. S-W Chen** , "A 1–5GHz Direct-Digital RF Modulator with an Embedded Time-Approximation Filter Achieving -43dB EVM at 1024 QAM," *IEEE Symposia on VLSI Technology and Circuits (VLSIC),* June 2019.
29. J.W. Nam, **M.S-W Chen**, "A 12.8-Gbaud ADC-based NRZ/PAM4 Receiver with Embedded Tunable IIR Equalization Filter Achieving 2.43-pJ/b in 65nm CMOS," *IEEE Custom Integrated Circuits Conference (CICC),* April 2019.
30. M. Hassanpourghadi, **M.S-W Chen**, "A 2-way 7.3-bit 10 GS/s Time-based Folding ADC with Passive Pulse-Shrinking Cells," *IEEE Custom Integrated Circuits Conference (CICC),* April 2019.
31. A. Zhang and **M. S-W Chen**, "A Watt-Level Phase-Interleaved Multi-Subharmonic Switching Digital Power Amplifier Achieving 31.4% Average Drain Efficiency," *IEEE International Solid-State Circuits Conference (ISSCC),* Feb. 2019.
32. A. Zhang, **M. S-W Chen**, "A Sub-Harmonic Switching Digital Power Amplifier with Hybrid Class-G Operation for Enhancing Power Back-off Efficiency," *IEEE Symposia on VLSI Technology and Circuits (VLSIC),* 2018.
33. T.F. Wu, **M. S-W Chen**, "A 200MHz-BW 0.13mm2 62dB-DR VCO-Based Non-Uniform Sampling ADC with Phase-Domain Level Crossing in 65nm CMOS," *IEEE Custom Integrated Circuits Conference (CICC),* 2018.
34. S. Su and **M. S-W Chen**, "A 16-bit 12GS/s Single/Dual-Rate DAC with Successive Bandpass Delta-Sigma Modulator Achieving <-67dBc IM3 within DC to 6GHz Tunable Passbands," *IEEE International Solid-State Circuits Conference (ISSCC),* Feb. 2018.

35. C.R. Ho, **M. S-W Chen**, "A digital frequency synthesizer with dither-assisted pulling mitigation for simultaneous DCO and reference path coupling," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2018.
36. C.R. Ho, **M. S-W Chen**, "A fractional-N digital PLL with background dither noise cancellation loop achieving <-62.5dBc worst-case near-carrier fractional spur in 65nm CMOS," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2018.
37. R. Rasul, P. Teimouri, and **M. S-W Chen**, "A Time Multiplexed Network Architecture for Large-Scale Neuromorphic Computing," IEEE MWSCAS, August 2017.
38. C.R. Ho, **M. S-W Chen**, "Interference-Induced DCO Spur Mitigation for Digital Phase Locked Loop in 65-nm CMOS," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, Sep. 2016.
39. J.W. Nam, M. Hassanpourghadi, A. Zhang, **M.S-W Chen**, "A 12-bit 1.6 GS/s Interleaved SAR ADC with Dual Reference Shifting and Interpolation Achieving 17.8 fJ/conv-step in 65nm CMOS," *IEEE Symposia on VLSI Technology and Circuits (VLSIC)*, June 2016.
40. C.R. Ho, **M. S-W Chen**, "A Digital PLL with Feedforward Multi-Tone Spur Cancelation Loop Achieving <-73dBc Fractional Spur and <-110dBc Reference Spur in 65nm CMOS," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2016.
41. S. Su, **M. S-W. Chen**, "A 12b 2GS/s Dual-Rate Hybrid DAC with Pulsed Timing-Error Pre-Distortion and In-Band Noise Cancellation Achieving >74dBc SFDR up to 1GHz in 65nm CMOS," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2016.
42. T.F. Wu, C.R. Ho, **M. S.-W. Chen**, "A Flash-Based Non-Uniform Sampling ADC Enabling Digital Anti-Aliasing Filter in 65nm CMOS," *IEEE Custom Integrated Circuits Conference (CICC)*, Sep 2015.
43. S. Su, T. Tsai, P. Sharma, **M. S.-W. Chen**, "A 12-bit Hybrid DAC with 8GS/s Unrolled Pipeline Delta-Sigma Modulator achieving >75dB SFDR over 500MHz in 65nm CMOS," *IEEE Symposia on VLSI Technology and Circuits (VLSIC)*, June 2014.
44. C.R. Ho, **M. S.-W. Chen**, "A Fractional-N DPLL with Adaptive Spur Cancellation and Calibration-Free Injection-Locked TDC in 65nm CMOS," to be presented at *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June, 2014.
45. J.W. Nam, D. Chiong, and **M. S.W. Chen**, "A 95-MS/s 11-bit 1.36-mW Asynchronous SAR ADC with Embedded Passive Gain in 65nm CMOS," *IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2013
46. P.K. Sharma, and **M. S.W. Chen**, "A 6b 800MS/s 3.62mW Nyquist AC-coupled VCO Based ADC in 65nm CMOS ," *IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2013
47. **M. S.W. Chen**, "Trend of High-Speed SAR ADC towards RF Sampling," *10th International Conference on Sampling Theory & Applications (SampTA)* (Invited), July. 2013.
48. D. Hand, and **M. S.W. Chen**, "A Non-Uniform Sampling ADC Architecture with Embedded Alias-Free Asynchronous Filter," Global Telecommunications Conference (GLOBECOM), Dec. 2012.

49. **M. S.W. Chen**, "Overhead Minimization Techniques for Digital Phase-Locked Loop Frequency Synthesizer, " IEEE MWSCAS (Invited Session), Aug. 2012.
50. **M.S.W. Chen**, D. Su, S. Mehta, "A Calibration-Free 800MHz Fractional-N Digital PLL with Embedded TDC," *IEEE International Solid-State Circuits Conference (ISSCC),*Feb. 2010.
51. Nathawad, L.; Zargari, M.; Samavati, H.; Mehta, S.; Kheirkhahi, A.; Chen, P.; Gong, K.; Vakili-Amini, B.; Hwang, J.; **Chen, M.S.W.**; Terrovitis, M.; Kaczynski, B.; Limotyrakis, S.; Mack, M.; Gan, H.; Lee, M.; Abdollahi-Alibeik, S.; Baytekin, B.; Onodera, K.; Mendis, S.; Chang, A.; Jen, S.; Su, D.; Wooley, B., "A Dual-Band CMOS MIMO Radio SoC for IEEE 802.11n Wireless LAN," *IEEE International Solid-State Circuits Conference (ISSCC),*Feb. 2008.
52. A. Fort, **M. S.-W. Chen**, R.W. Brodersen, C. Desset, P. Wambacq, L. Van Biesen, "Impact of Sampling Jitter on Mostly-Digital Architectures for UWB Bio-Medical Applications," *IEEE International Conference on Communications (ICC),* June 2007.
53. A. Fort, **M. S.-W. Chen**, C. Desset, P. Wambacq, L. Van Biesen, "Clock offset tracking for subsampling UWB architectures in a body area network," *IEEE International Conference on Ultra-Wideband (ICUWB),* Sep. 2007.
54. **M. S.-W. Chen** and R. W. Brodersen, "Digital Complex Signal Processing Techniques for Impulse Radio," *Global Telecommunications Conference (GLOBECOM),* Nov. 2006.
55. **M. S.-W. Chen** and R. W. Brodersen, "Implementation Considerations for a Sub-sampling Impulse Radio," *IEEE International Conference on Ultra-Wideband (ICUWB),* Sep. 2006.
56. **M. S.-W. Chen** and R. W. Brodersen, "A 6b 600MS/s 5.3mW Asynchronous ADC in 0.13μm CMOS," *IEEE International Solid-State Circuits Conference (ISSCC),* Feb. 2006.
57. D. Cabric, **M. S.-W. Chen**, D. Sobel, J. Yang, and R. Brodersen, "Future Wireless Systems: UWB, 60 GHz, and Cognitive Radios," (Invited paper) at *Custom Integrated Circuits Conference (CICC),* Sep. 2005
58. **M. S.-W. Chen**, R. W. Brodersen, "The Impact of a Wideband Channel on UWB System Design," *Military Communication Conference (MILCOM),* Nov. 2004.
59. **M. S.-W. Chen**, R. W. Brodersen, "A Subsampling UWB Radio Architecture by Analytic Signaling," *International Conference on Acoustics, Speech, and Signal Processing (ICASSP),* May 2004.
60. I. O'Donnell, **M. S.-W. Chen**, S. Wang, R. W. Brodersen, "An Integrated, Low-Power, Ultra-Wideband Transceiver Architecture for Low-Rate, Indoor Wireless Systems," *IEEE CAS Workshop on Wireless Communications and Networking,* Sep. 2002.

Journals

1. S. Su, Q. Zhang, B. R. Biswas, S. K. Gupta, **M. S.-W. Chen**, "Stochastic TDC Using Common-Mode Time Dithering and Passive Approximate Adders," *IEEE J. Solid-State Circuits,* April 2025.

2. M. Ayesh, S. Mahapatra, C. Yang and **M. S.-W. Chen**, "A Blocker-Tolerant Non-Uniform Sub-Sampling Receiver With a Non-Uniform Discrete-Time FIR Filter", *IEEE J. Solid-State Circuits*, 2024.
3. W. Song, M. Rao, Y. Li, C. Li, Y. Zhuo, F. Cai, M. Wu, W. Yin, Z. Li, Q. Wei, S. Lee, H. Zhu, L. Gong, M. Barnell, Q. Wu, P. Beerel, **M. S.-W. Chen**, N. Ge, M. Hu, Q. Xia, J. Yang, "Programming memristor arrays with arbitrarily high precision for analog computing," Science, 2024.
4. Q. Zhang, H.-C. Cheng, S. Su**,** and **M. S.-W. Chen**, "Fractional-N Digital MDLL with Injection-Error Scrambling and Calibration," *IEEE J. Solid-State Circuits*, 2023.
5. C. Yang, S. Su, and **M. S.-W. Chen**, "Millimeter-Wave Receiver with Non-Uniform Time-Approximation Filter," IEEE J. Solid-State Circuits, 2023 (in press).
6. J. Liu, M. Hassanpourghadi, and **M. S.-W. Chen**, "A 10-GS/s 8-bit 2850-μm2 Two-Step Time-Domain ADC With Speed and Efficiency Enhanced by the Delay-Tracking Pipelined-SAR TDC," IEEE J. Solid-State Circuits, 2022.
7. S. Su and **M. S.-W. Chen**, "SAW-Less Direct RF Transmitter with Multi-Mode Noise Shaping and Tri-Level Time-Approximation Filter," IEEE J. Solid-State Circuits, Mar. 2022.
8. Q. Zhang, S. Su, C.-R. Ho, and **M. S.-W. Chen**, "A Fractional-N Digital MDLL With Background Two-Point DTC Calibration," (Invited) *IEEE J. Solid-State Circuits* (JSSC), Jan. 2022.
9. M. Hassanpourghadi, R. A. Rasul, and **M. S. W. Chen**, "A Module-Linking Graph Assisted Hybrid Optimization Framework for Custom Analog and Mixed-Signal Circuit Parameter Synthesis" ACM Transactions on Design Automation of Electronic Systems, June 2021.
10. X. Yan, J. Ma, T. Wu, A. Zhang, J. -B. Wu, M. Chin, Z. Zhang, M. Dubey, W. Wu, **M. S.-W. Chen**, J. Guo, H. Wang "Reconfigurable Stochastic Neurons Based on Tin Oxide/MoS2 Hetero-memristors for Simulated Annealing and the Boltzmann Machine" Nature Communications, 12, Article number: 5710 (2021)
11. S. Su, **M. S.-W. Chen**, "A Time-approximation Filter for Direct RF Transmitter," *IEEE J. Solid-State Circuits* (JSSC) 2021.
12. J.W. Nam, **M. S.-W. Chen**, "A 12.8-Gbaud ADC-based Wireline Receiver with Embedded IIR Equalizer," (Invited) *IEEE J. Solid-State Circuits* (JSSC), Mar. 2020.
13. A. Zhang, **M. S-W. Chen**, "A Watt-Level Phase-Interleaved Multi-Subharmonic Switching Digital Power Amplifier," (Invited) *IEEE J. Solid-State Circuits* (JSSC) Nov., 2019.
14. A. Zhang, **M. S-W. Chen**, "A Subharmonic Switching Digital Power Amplifier for Power Back-Off Efficiency Enhancement," (Invited) *IEEE J. Solid-State Circuits* (JSSC) Feb., 2019.
15. T.F. Wu, **M. S.-W. Chen**, "A VCO-Based Nonuniform Sampling ADC with Phase-Domain Level Crossing," (Invited) *IEEE J. Solid-State Circuits* (JSSC) Mar., 2019.
16. S. Su, **M. S.-W. Chen**, "A 16-bit 12GS/s Single/Dual-Rate DAC with a Successive Bandpass Delta-Sigma Modulator Achieving <-67dBc IM3 within DC to 6GHz Tunable Passbands," (Invited) *IEEE J. Solid-State Circuits* (JSSC) Dec., 2018.

17. T.F. Wu, **M. S-W. Chen**, "A Subranging-Based Nonuniform Sampling ADC With Sampling Event Filtering," *IEEE Solid-State Circuits Letters* (SSC-L) April, 2018.
18. J.W. Nam, M. Hassanpourghadi, A. Zhang, **M.S-W Chen**, "A 12-bit 1.6/3.2/6.4 GS/s 4 b/cycle Time-interleaved SAR ADC with Dual Reference Shifting and Interpolation," *IEEE J. Solid-State Circuits* (JSSC), June, 2018.
19. T.F. Wu, C.R. Ho, **M. S.-W. Chen**, "A Flash-Based Non-Uniform Sampling ADC With Hybrid Quantization Enabling Digital Anti-Aliasing Filter," *IEEE J. Solid-State Circuits* (JSSC) Sep., 2017.
20. M. Hassanpourghadi, P.K. Sharma, and **M. S.-W. Chen**, "A 6-bit Nyquist AC-coupled VCO Based ADC at 800MS/s," IEEE Transactions on Circuits and Systems (TCAS-I) 2017.
21. C.R. Ho, **M. S.-W. Chen**, "A Digital PLL with Feedforward Multi-Tone Spur Cancelation Loop Achieving <-73dBc Fractional Spur and <-110dBc Reference Spur in 65nm CMOS," (Invited) accepted for *IEEE J. Solid-State Circuits* (JSSC) Dec., 2016.
22. S. Su, **M. S.-W. Chen**, "A 12b 2GS/s Dual-Rate Hybrid DAC with Pulsed Timing-Error Pre-Distortion and In-Band Noise Cancellation Achieving >74dBc SFDR up to 1GHz in 65nm CMOS," (Invited) accepted for *IEEE J. Solid-State Circuits* (JSSC) Dec., 2016.
23. J.W. Nam, **M. S.-W. Chen**, "An Embedded Passive Gain Technique for Asynchronous SAR ADC Achieving >10 ENOB, 1.36 mW at 95MS/s in 65nm CMOS," accepted by IEEE Transactions on Circuits and Systems (TCAS-I) 2016
24. T.F. Wu, S. Dey, **M. S.-W. Chen**, "A Non-Uniform Sampling ADC Architecture with Reconfigurable Digital Anti-aliasing Filter," accepted by IEEE Transactions on Circuits and Systems (TCAS-I) 2016
25. C.R. Ho, **M. S.-W. Chen**, "A Fractional-N DPLL with Calibration-free Multi-phase Injection-locked TDC and Adaptive Single-tone Spur Cancellation Scheme," accepted by IEEE Transactions on Circuits and Systems (TCAS-I) 2016
26. S. Su, T. Tsai, P. Sharma, **M. S.W. Chen**, "A 12-bit 1GS/s Dual-Rate Hybrid DAC with an 8GS/s Unrolled Pipeline Delta-Sigma Modulator Achieving >75dB SFDR over the Nyquist Band," (Invited) *IEEE J. Solid-State Circuits*, April, 2015.
27. Y. Cao, J. Velamala, K. Sutaria, **M. S.W. Chen**, J. Ahlbin, I. Esqueda, M. Bajura, M. Fritze, "Cross-Layer Modeling and Simulation of Circuit Reliability", *IEEE Transactions on CAD of Integrated Circuits and Systems*, Jan. 2014.
28. **M.S.W. Chen**, D. Su, S. Mehta, "A Calibration-Free 800MHz Fractional-N Digital PLL with Embedded TDC," (Invited) *IEEE Journal of Solid-State Circuits*, Dec. 2010.
29. Zargari, M.; Nathawad, L.Y.; Samavati, H.; Mehta, S.S.; Kheirkhahi, A.; Chen, P.; Gong, K.; Vakili-Amini, B.; Hwang, J.A.; **Chen, S.-W.M.**; Terrovitis, M.; Kaczynski, B.J.; Limotyrakis, S.; Mack, M.P.; Gan, H.; MeeLan Lee; Chang, R.T.; Dogan, H.; Abdollahi-Alibeik, S.; Baytekin, B.; Onodera, K.; Mendis, S.; Chang, A.; Rajavi, Y.; Jen, S.H.-M.; Su, D.K.; Wooley, B.A., "A Dual-Band CMOS MIMO Radio SoC for IEEE 802.11n Wireless LAN," *IEEE J. Solid-State Circuits*, Dec. 2008.

30. **M.S.W. Chen**, R. W. Brodersen, "A Subsampling Radio Architecture for Ultrawideband Communications," *IEEE Transactions on Signal Processing*, Oct. 2007.
31. **M.S.W. Chen**, R. W. Brodersen, "A 6-bit 600-MS/s 5.3-mW Asynchronous ADC in 0.13-um CMOS," *IEEE J. Solid-State Circuits*, Dec. 2006.
32. **M.S.W. Chen**, R. W. Brodersen, "A Subsampling UWB Impulse Radio Architecture Utilizing Analytic Signaling," (Invited Paper) *IEICE Trans. on Electronics*, June 2005.
33. D. Cabric, **M. S.-W. Chen**, D. Sobel, S. Wang, J. Yang, and R. W. Brodersen, "Novel Radio Architectures for UWB, 60GHz, and Cognitive Wireless Systems," *EURASIP J. on Wireless Commnucations and Networking*, 2006.

Magazine

1. **M. S.-W. Chen**, "Trend and New Opportunities in Digital PLL Design", (Invited) IEEE Solid State Circuit Magazine, 2020 winter issue.
2. C.R. Ho, **M. S-W. Chen**, "Clock Generation in the future with Digital Signal Processing Technique for Mitigating Spur and Interference," IEEE Microwave Magazine 2019.
3. Sankaran, S.G.; Zargari, M.; Nathawad, L.Y.; Samavati, H.; Mehta, S.S.; Kheirkhahi, A.; Chen, P.; Ke Gong; Vakili-Amini, B.; Hwang, J.; **Chen, S.-W.M.;** Terrovitis, M.; Kaczynski, B.J.; Limotyrakis, S.; Mack, M.P.; Gan, H.; Lee, M.; Chang, R.T.; Dogan, H.; Abdollahi-Alibeik, S.; Baytekin, B.; Onodera, K.; Mendis, S.; Chang, A.; Rajavi, Y.; Jen, S.H.-M.; Su, D.K.; Wooley, B., "Design and implementation of a CMOS 802.11n soc –[integrated circuits for communications]," *Communications Magazine*, April 2009.
4. D. Cabric, I. O'Donnell, **M. S.-W. Chen**, and R.W. Brodersen, "Spectrum Sharing Radios," (Invited) *IEEE Circuits and Systems Magazine*, 2006.

Book Chapter

1. C.R. Ho, **M. S.-W. Chen**, "Fractional-N spur reduction techniques for DPLL," *Phase-Locked Frequency Generation and Clocking: Architectures and Circuits for Modern Wireless and Wireline Systems*, IET 2019 (under preparation).
2. **M. S.-W. Chen**, "Challenges and Emerging Trend of DSP Enabled Frequency Synthesizer," Digitally-Assisted Analog *and Analog-Assisted Digital IC Design.* Chapter4, 2015, Cambridge University Press.
3. **M. S.-W. Chen**, "Energy-Efficient ADC Topology Enabled with Asynchronous Techniques," *Circuits for Nanoscale: Communications, Imaging, and Sensing.* Chapter14, Sep. 2008.

Patent

1. **M.S.W. Chen**, C.R. Ho, "Adaptive spur cancellation techniques and multi-phase injection locked TDC for digital phase locked loop circuit," US patent #9941891, 2018.

2. **M. S.W. Chen**, "Non-uniform Sampling Analog to Digital Converter (ADC) Architecture with Digital Reconfigurable Anti-Aliasing Filter," filed for provisional patent application, No. 61/911,261, Dec., 2013.
3. **M. S.W. Chen**, D. Su, "Fractional and Integer PLL Architectures," US patent #8289086, 2012.

INVITED TALKS/TUTORIALS/WORKSHOPS

1. ITRI, Taiwan, "New Opportunities in Mixed-Signal ICs", June, 2011.
2. UMC, Taiwan, "New Opportunities in Mixed-Signal ICs", June, 2011.
3. HRL Laboratories, LLC: "Enhancing A-to-D Conversion Efficiency". July 2nd, 2012
4. "Analog-to-Digital Interface: A Time Approach" 2013 CMOS Emerging Technologies Research Symposium, Whistler, July 2013.
5. "Path towards High-Speed High-Resolution Data Converters with Diminishing Cost", Sep. 2013, Broadcom.
6. "Analog-Digital Interface Research, really?" Sep. 2013, Qualcomm-Atheros.
7. "Re-shape Future Mixed-Signal IC Design" Oct. 2013. Qualcomm.
8. "Path towards High-Speed High-Resolution Data Converters with Diminishing Cost", Nov. 2013, UT Dallas.
9. "Path towards High-Speed High-Resolution Data Converters with Diminishing Cost", Nov. 2013, Texas Instrument.
10. "Power efficient ADC Topologies towards RF Sampling" 2014 RFIC Tutorial.
11. "Path Towards Direct RF Synthesis: A Hybrid Digital-to-Analog Converter Architecture" 2014 IEEE MWSCAS Conference, Distinguished Speaker Series.
12. "Asynchronous SAR ADC: Past, Present and Beyond" 2014 IEEE MWSCAS Conference Tutorial
13. "Exploring Limits of Mixed-Signal ICs" Sep. 2014, MaxLinear Corp.
14. "Rethinking Analog-Digital Interface Circuit Architectures" Oct. 2014, IC Seminar, Columbia University, NY.
15. "Rethinking Analog-Digital Interface Circuit Architectures" Mar. 2015, IC Seminar, UC Berkeley, CA.
16. "Rethinking Analog-Digital Interface Circuit Architectures" Dec. 2015, IC Seminar, National Taiwan University(NTU)/IEEE Chapter, Taipei, Taiwan.
17. "Rethinking Analog-Digital Interface Circuit Architectures" Feb. 2016, IC Seminar, UT Austin, Texas.
18. "Asynchronous SAR ADC: Past, Present and Beyond", Feb. 2016, EE department Colloquium, UT Austin/IEEE Chapter.
19. "Rethinking Analog-Digital Interface Circuit Architectures" Feb. 2016, IC Seminar, University of Michigan, Ann Arbor.
20. "Rethinking Analog-Digital Boundary from Circuit to System Level towards Reconfigurability of Everything" Mar. 2016, SystemX Seminar, Stanford
21. "Rethinking Analog-Digital Interface Circuit Architectures" April. 2016, EE department Colloquium. Carnegie Mellon University (CMU).
22. "Rethinking Analog-Digital Interface Circuit Architectures" April. 2016, IC Seminar, University of California, Los Angeles (UCLA).
23. "IC Research overview," TSMC, 2017

24. "IC Research overview," Intel Lab, 2017
25. "IC Research overview," InPhi, 2017
26. "Advancing Low-Power High-Speed Analog-to-Digital Converters: An Asynchronous Design Approach", VLSI DAT tutorial, 2017
27. "Generic spur cancellation for digital PLL," Qualcomm 2017
28. "Evolutions of SAR ADC: from High Resolution to High Speed Regime," IEEE CICC 2018 tutorial.
29. "Emerging Opportunities in Analog Mixed-Signal Circuit Design Automation," ACM/IEEE ICCAD 2018 workshop.
30. "Analog-to-Digital Converter Architecture Opportunities in Emerging Wireless Systems," RFIC 2018 workshop
31. "How can hardware designers reclaim the spotlight?" moderator/co-organizer of ISSCC 2019 evening panel.
32. "Fundamentals of Analog-to-digital conversion," 2-day tutorial in Shanghai, China 2019.
33. "Digital Fractional-N Phase Locked Loop Design," tutorial, ISSCC Feb 2020
34. "Digital Fractional-N Phase Locked Loop Design," ISSCCedu Feb 2020
35. "Low Spur PLL architectures," MEAD tutorial in EPFL, 2021 (to appear)
36. "Low Spur PLL architectures and techniques, " IEEE CICC 2020
37. "New Opportunities in Nonuniform Sampling," IEEE SSCS Webinar Oct 2020.
38. "High-Performance Digital-to-Analog Converter Design: A Path towards Digital Transmitter," ISESD Keynote June 2021
39. "ADC Evolution via Architectural Rethinking: from Asynchronous SAR to Non-uniform Sampling ADC," IEEE SSCS Tainan Chapter, Oct 2021
40. "High-Performance Digital-to-Analog Converter Design: A Path towards Digital Transmitter," IEEE SSCS Atlanta Chapter, Nov. 2021
41. "Asynchronous SAR ADC: Past, Present and Beyond," IEEE Southern Alberta Chapter, Nov. 2021
42. "Non-Uniform Sampling Data Converters: A Journey to Uncharted Circuits and Systems" IEEE VLSI-DAT April 2022
43. "Asynchronous SAR ADC: Past, Present and Beyond," IEEE Swiss Chapter, May 2022
44. "New Opportunities in Nonuniform Sampling," IEEE Penang Chapter, July 2022
45. "Trend in Digital PLL Design and New Opportunities in Spur Cancellation," IEEE Southern Alberta Chapter, Sep. 2022
46. "High-Performance Digital-to-Analog Converter Design: A Path towards Digital Transmitter," IEEE Egypt Chapter Nov. 2022
47. "New Opportunities in Nonuniform Sampling," IEEE Taipei Chapter, Dec. 2022
48. "Trend in Digital PLL Design and New Opportunities in Spur Cancellation," IEEE Tainan Chapter, Dec. 2022

PROFESSIONAL SERVICES

Review Panel:

1. IEEE SSCS James D. Meindl Innovators Award
2. NSF Panelist

3. Samsung Research

Journal article review:

1. IEEE Journal of Solid-State Circuits
2. IEEE Solid-State Circuits Letters (SSC-L)
3. IEEE Transactions on Signal Processing
4. IEEE Transactions on Communications
5. IEEE Transactions on Circuits and Systems I
6. IEEE Transactions on Circuits and Systems II
7. IEEE Transactions on Vehicular Technology
8. IEEE Communications Letters
9. Journal of VLSI Signal Processing Systems

USC Department Services:

1. Munishian Series Committee
2. EFC
3. EE Festival reviewer

Conference TPC:

IEEE European Conference on Solid-State Circuits (ESSCIRC) (2022- present)
IEEE International Solid State Circuits Conference (ISSCC) (2018 - present)
IEEE Symposium on VLSI Circuits (VLSIC) (2017 - 2020)
IEEE Custom Integrated Circuits Conference (CICC) (2015 - 2019)
IEEE GlobalSIP (2014)

Organized/Participated Panel/Forum/Workshops for SSCS:

1. Forum: “Emerging Design Techniques for Data Converters” served as organizer at CICC 2017
2. Panel: “What can/should Circuit Designers do to Ride on the Wave of Machine Learning?” served as co-organizer and moderator at CICC 2018
3. Panel: “How can hardware designers reclaim the spotlight?” served as co-organizer and moderator at ISSCC 2019
4. Panel: “Favorite circuit design and testing mistakes of starting engineers?” served as co-organizer at ISSCC 2021
5. VLSI Symposia Mentoring Event June 2021
6. Panel: “How to choose career path, academia, industry, startups?” served as panelist at CICC 2022 (to appear)
7. Panel: “Open Source Systems, Circuits, and Design: Is It the Future?” served as panelist at CICC 2022 (to appear)

Associate Editor:

SSC-L, TCAS-II

Society Membership:

Senior Member of IEEE