

Advanced Metallization Conference 2002 (AMC 2002)

Proceedings of the Conference held October 1–3, 2002, in San Diego, California, U.S.A., and October 29–30, 2002, University of Tokyo, Tokyo, Japan. This Conference is MRS affiliated and sponsored by Continuing Education in Engineering, University Extension, University of California at Berkeley, California, U.S.A.

EDITORS:

Bradley M. Melnick

Motorola, Inc.
Austin, Texas, U.S.A.

Timothy S. Cale

Rensselaer Polytechnic Institute
Troy, New York, U.S.A.

Shigeaki Zaima

Nagoya University
Nagoya, Japan

Tomohiro Ohta

Tokyo Electron Ltd.
Tokyo, Japan



Materials Research Society
Warrendale, Pennsylvania

ALBERTSONS LIBRARY
BOISE STATE UNIVERSITY

TSMC-1037
TSMC Ltd.
IPR2025-01211

Single article reprints from this publication are available through
University Microfilms Inc., 300 North Zeeb Road, Ann Arbor, Michigan 48106

CODEN: MRSPDH

Copyright 2003 by Materials Research Society.
All rights reserved.

This book has been registered with Copyright Clearance Center, Inc. For further information, please
contact the Copyright Clearance Center, Salem, Massachusetts.

Published by:

Materials Research Society
506 Keystone Drive
Warrendale, PA 15086
Telephone (724) 779-3003
Fax (724) 779-8313
Web site: <http://www.mrs.org/>

Manufactured in the United States of America

ALBERTSONS LIBRARY
MIDLAND

Geometrical Aspects of Stress-Induced Voiding in Copper Interconnects

A. von Glasow¹, A.H. Fischer¹, M. Hierlemann², S. Penka¹ and F. Ungar¹

¹ Reliability Methodology, ² Simulation, Infineon Technologies, Munich, Germany
alex.glasow@infineon.com

Abstract

The influence of various geometrical aspects and different layout configurations on the stressvoiding (SV) behavior of copper interconnect systems was studied. Via-line structures with large design features such as metal plates or meshes turned out to be highly susceptible to stress-induced voiding. Based on comprehensive plate size investigations, the stressvoiding rate depends primarily on the available active diffusion volume of the respective structure i.e. the volume which acts as reservoir of vacancies that might contribute to the voiding process inside (or next to) the via. As a general trend, large plates show smaller failure times i.e. they are more susceptible to stress-induced voiding compared to small plates. Since the change of the active volume over time depends on the specific plate layout, different SV behaviors were observed for plates with different length/width ratios. Hereby, simulated resistance drifts are in good agreement with experimental data.

Slight changes in structural features such as via-diameter or via-to-line misalignment were found to cause significant changes in the SV failure times. Based on FEA simulations the via-misalignment effect is attributed to changes in the stress gradients i.e. the driving force.

The stressvoiding rate turned out not only to be influenced by geometrical aspects of the large reservoir features, but also on those test structure parts which are not affected by stress-induced voids. Stress simulations suggest differences in the stress gradients and hence the driving force of the SV mechanism as root cause of this phenomenon.

Introduction

Stress-induced voiding is a serious wear-out mechanism in copper metallizations, limiting the lifetime of integrated circuits [1]. Since copper was introduced as a metallization option only recently, most publications discuss the stressvoiding phenomenon with respect to fundamental material properties or process-related aspects [2, 3, 4]. This work will focus on the influence of geometrical features and design aspects of interconnect systems on their SV behavior. It will be shown how sensitive the voiding kinetics depend on geometrical features such as line width, line length, overlap and via diameter. Here, special layout configurations turned out to be more critical than others. This implies that not only an optimized process is necessary to suppress the stressvoiding risk but also to implement as much as possible built-in reliability in an integrated interconnect network by means of smart SV-design rules.

Experimental

Stressvoiding studies were carried out on copper metal lines from a 0.18 μ m technology connected by dual damascene vias and tungsten plugs, respectively. The

interconnects are surrounded by SiO₂ dielectric using a TaN/Ta liner system and a SiN cap layer. The growth of stress-induced voids was monitored by the resistance shift during high temperature storage (HTS) on wafer level at 275 °C.

Test structure design

On copper interconnects with dual damascene vias stressvoids can be found at different locations: 1) next to the via in the metal level underneath and 2) inside the via (Fig.1). The location depends on the test structures layout. In our studies the structures are designed in a way that only one metal level ("voiding level") is affected by stressvoids, whereas the other ("connecting level") remains intact. Generally, the voiding level is characterized by a large active metal line volume [5]. In metallizations where copper interconnects are connected by W-plugs to an aluminum level, stressvoids are detected exclusively in the copper level underneath the plug. The aluminum level is thereby not affected by stress voiding.

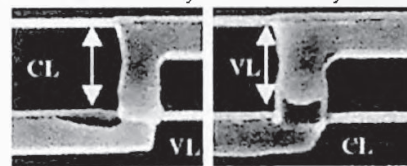


Fig.1 Two different failure modes for stress-induced voiding can be observed dependent on the test structure design. Left: voiding next to the via in the copper metal line below. Right: voiding inside the dual damascene via. (VL = voiding level, CL = connecting level)

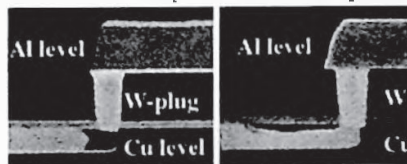
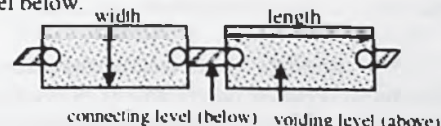


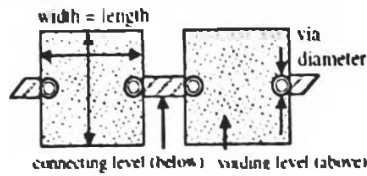
Fig.2 On test structures with a copper/tungsten-plug/aluminum-stack, stressvoids are exclusively found in the copper line; either underneath the W-plug (left) or next to it (right). The Al-line remains unaffected.

The influence of geometrical aspects on the stress voiding behavior is investigated by using a set of various test structures. Numerous geometries are realized by varying the length and width of the connecting level or the voiding level, respectively. In addition, the effect of geometrical features such as line extensions or slitted plates ("meshes") on the voiding kinetics was studied. Five different types of test structures were used:

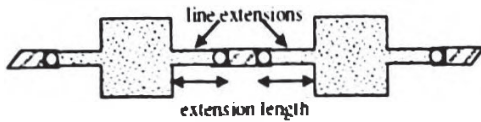
1) "rectangular plates (single or chain)": single element or chain of 28 rectangular plates in different widths and lengths connected over a single via by narrow links in the metal level below.



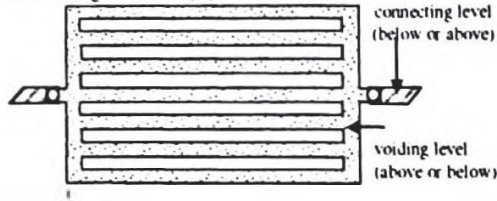
2) "square-shaped plate chain": chain of 50 square plates of different sizes in the upper metal level linked with $0.5 \times 3.3 \mu\text{m}^2$ segments by single vias.



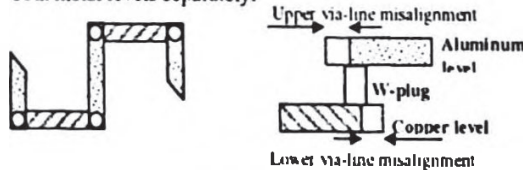
3) "square plate chains with line extensions": same as type 2) but with plates having short narrow "nose-like" extension out to the via. The plate size is $7 \times 7 \mu\text{m}^2$.



4) "mesh-type chain": chain of 34 meshes connected over single vias by $4 \mu\text{m}$ long links of different width (narrow link $w=0.28 \mu\text{m}$; wide link $w=2.5 \mu\text{m}$). Each mesh consists of parallel lines of $0.28 \mu\text{m}$ width and space covering an area of $3 \times 100 \mu\text{m}^2$. It simulates a high fan-out from a single contact [6].



5) "short via chains": chain of 10000 W-plugs linked by $0.28 \times 1.5 \mu\text{m}^2$ lines in the aluminum and copper level. The via-to-line overlap can be varied from -0.06 to $+0.2 \mu\text{m}$ in both metal levels separately.



Failure criterion

In general, a certain amount of relative resistance increase is used in the reliability community to define the electromigration or stressmigration failure time of a single metal line configuration. This value reflects a maximum tolerable shift of resistance under which the product functionality can still be guaranteed. However, since most of the test structures compared in this study have different geometries, their initial resistances are different as well. Hence the use of a relative resistance criterion has the disadvantage that a larger void volume is required in via-line structure with long lines compared to those with shorter lines. In this case only the use of an absolute resistance increase as a failure criterion does allow a quantitative comparison of the voiding kinetics.

Results - Single rectangular plates

The use of different failure criteria is discussed by data gathered on rectangular plates terminated with a single via

on both ends. The length of the plates was varied from 30 to $400 \mu\text{m}$ at a constant width of $0.28 \mu\text{m}$. Since the initial resistance is increasing with the line length, the failure times are increasing as well when using a relative failure criterion of 5% resistance increase (Fig.3).

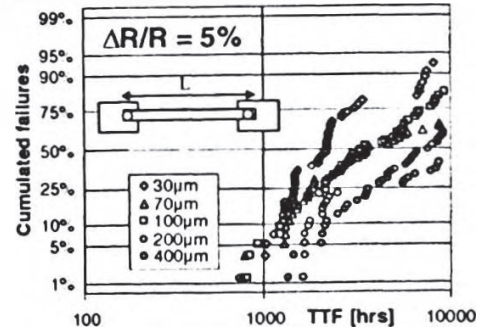


Fig. 3 SV failure times obtained during HTS at 275°C on $0.28 \mu\text{m}$ wide rectangular plates with different length (L) using a relative resistance increase of 5% as failure criterion. The failure times are increasing steadily with increasing line length.

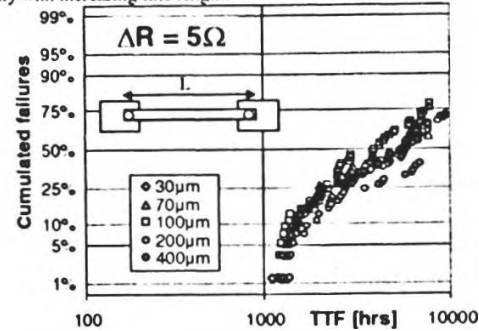


Fig. 4 SV failure times obtained during HTS at 275°C on $0.28 \mu\text{m}$ wide rectangular plates with different length (L) using the same SV data as in Fig.3 but now with an absolute resistance increase of 5Ω as failure criterion.

The difference between the individual distributions becomes smaller (compared to Fig.3) when calculating the failure times using an absolute failure criterion of 5Ω resistance increase (Fig.4). The medium time to failure (MTF) shows a distinct minimum for plate lengths $L=100 \mu\text{m}$ (Fig.5).

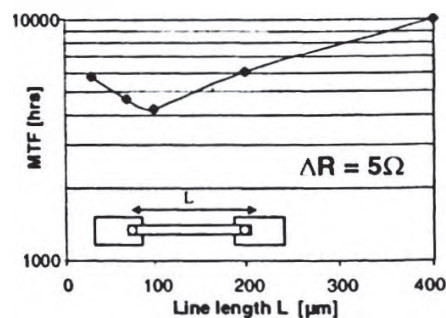


Fig. 5 Medium time to failure (MTF) derived for a 5Ω absolute failure criterion from distributions in Fig.4. A distinct minimum of MTF is obtained for plate lengths $L=100 \mu\text{m}$ during HTS at 275°C .

The failure times obtained for $L=30 \mu\text{m}$ are about 50% and for $L=400 \mu\text{m}$ about 150% larger.

Since the void volume is assumed to be directly related to the absolute resistance increase, the voiding rate on rectangular plates is obviously dependent on the plate length with a maximum for $L=100\mu\text{m}$.

Results - Rectangular plate chains

A pronounced plate size effect was observed on chains of rectangular plates having widths (w) between 0.28 and $10\mu\text{m}$ and a maximum length (L) of $1500\mu\text{m}$. Both, plate width as well as plate length turned out to influence the medium stressvoiding failure time

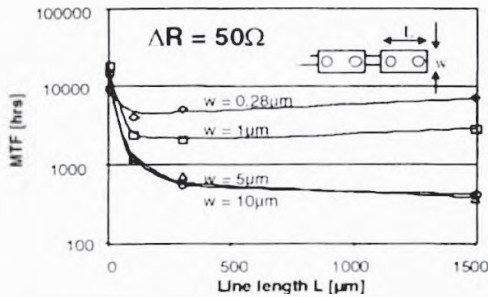


Fig. 6 MTF obtained on chains with rectangular plates of different width (w) as a function of plate length (L) using an absolute failure criterion $\Delta R=50\Omega$. The length dependence of narrow plates ($w=0.28$ and $1.00\mu\text{m}$) is characterized by a minimum at 100 and $300\mu\text{m}$, respectively.

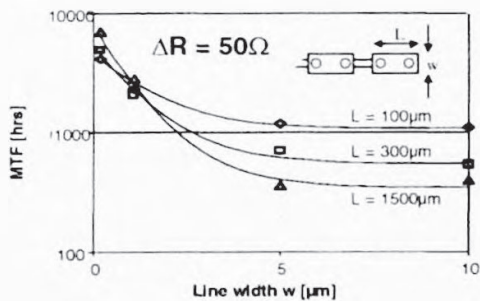


Fig. 7 MTF obtained on chains with rectangular plates of different length (L) as a function of width (w) using an absolute failure criterion $\Delta R=50\Omega$. The decrease of MTF is saturating for large plate widths.

As a general trend, large plates show smaller MTFs i.e. they are more susceptible to stress-induced voiding compared to small plates. For example, on $1500\mu\text{m}$ long plates with $1\mu\text{m}$ width about $10\times$ longer life times are obtained compared to those with $10\mu\text{m}$ width (Fig.6). Thereby, the length dependence of narrow plates was observed to be different from wide plates (Fig.6). Narrow plates ($w<5\mu\text{m}$) show a more or less pronounced minimum of MTF, whereas wider plates are characterized by a steady decrease of MTF with plate length up to $L=1500\mu\text{m}$. For $w=0.28\mu\text{m}$ a minimum MTF is obtained at $L=100\mu\text{m}$. This behavior is similar to the corresponding test structure with the single plate (Fig.5). For $w=1\mu\text{m}$ this minimum shifts to $L=300\mu\text{m}$ suggesting the existence of a critical length/width ratio. In contrast, the width dependence is characterized by a decrease of MTF with increasing w with a saturation for large plate widths (Fig.7).

Results - Square-shaped plate chains

In addition to the plate size effect a strong influence of the via-diameter was observed on chains of square-shaped plates. Since the overall resistance of such chains is independent on the plate size, failure times can be compared also by using a relative 5% failure criterion. The failure rate after 2000hrs HTS at 275°C was found to be increasing for both increasing plate size and decreasing via-diameter, respectively (Fig.8). For nominal via sizes SV failures are obtained only on large $20\times 20\mu\text{m}^2$ plates. The failure frequencies are increasing significantly as the connecting vias become smaller and smaller. For via-diameters 50nm smaller than the nominal size, a high amount of failures is obtained on all plate sizes. For 10×10 and $20\times 20\mu\text{m}^2$ plate size all specimens of the sample failed and even on the smallest plates ($4\times 4\mu\text{m}^2$) almost half of the samples failed.

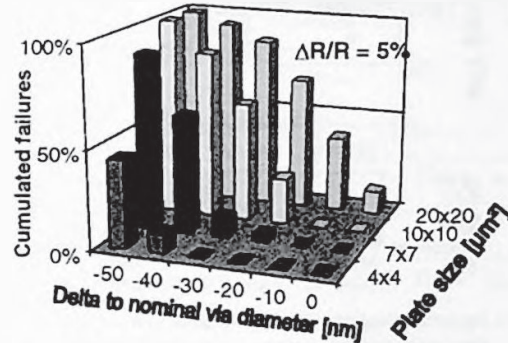


Fig.8 SV failures obtained after 2000hrs HTS at 275°C on a sample of square-shaped plate chains with varying plate size and via-diameter. The failure frequency is increasing with increasing plate size and decreasing via-diameter, respectively ("delta to nominal via diameter" corresponds to vias which are up to 50nm smaller than the nominal via).

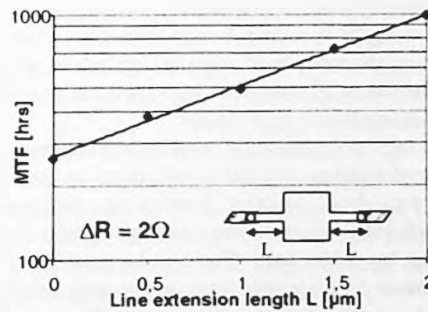


Fig.9 Influence of narrow "nose-like" line extensions on the SV behavior of square shaped plates. The MTF is increasing exponentially with the line extension up to $L=2\mu\text{m}$.

How sensitive the SV behaves with respect to small changes in the plate design is demonstrated on square-shaped plate structures with "nose-like" extensions. The MTFs obtained on those modified plates were found to increase exponentially with the length of the line extension within the investigated range $L=0\dots 2\mu\text{m}$. Although the SV mechanism cannot be suppressed by using this design feature, it can be applied to reduce the voiding rate inside the via (i.e. increased lifetime) and hence to improve built-in reliability.

Results – Mesh-type chains

Mesh-type test structures were investigated in different configurations: 1) mesh in metal M_x level below via V_x (x=1, 2) where voiding occurs in the mesh level next to the via; 2) mesh in level M_{x+1} above via V_x where the stressvoids develop inside the dual damascene via (Fig.10). In addition the meshes are available with two different link widths: w=0.28μm ("narrow") and w=2.5μm ("wide"), respectively. Since the geometrical features of the meshes are identical, the resistance of all test structures is nearly the same (variations of link width is negligible) and hence a relative failure criterion of ΔR/R=5% was used to compare the different medium times to failure.

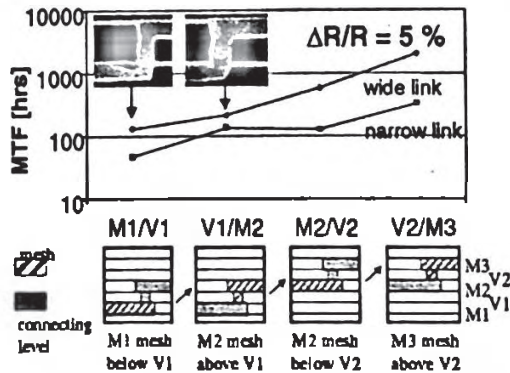


Fig.10 Stressmigration behavior of mesh type test structures at 275°C. The voiding occurs exclusively in the mesh level. MTFs determined for a 5% failure criterion depend on the mesh level as well as on the connecting level. Larger MTFs are obtained for wide connecting links.

Fig.10 indicates that the MTF is not only affected by the metal level of the mesh but also by the level of the connecting link: 1) keeping the via level constant, mesh below results in smaller failure times than mesh above; 2) keeping the mesh level constant, via below yields smaller failure times; 3) structures with identical layouts are less SV susceptible in upper levels.

Although the connecting level is not affected by stress-induced voiding, the link width plays an important role for the stress voiding kinetics in the mesh level. Significantly larger failure times are obtained on meshes linked by wide lines (Fig.10). In analogy to the line extension on plate structures, wider links can be used in an interconnect layout to reduce the SV risk of mesh-like configurations and gain as much built-in reliability as possible.

Results – Via misalignment

The influence of the via-to-line misalignment on the stressvoiding behavior was investigated on short via chains, where the copper segments are connected to the aluminum level by W-plugs. Via-line misalignments in a range between -0.06 and +0.20μm were investigated separately for both levels.

For this metal stack architecture the voiding occurs always inside the copper level underneath or next to the W-plug (Fig.2).

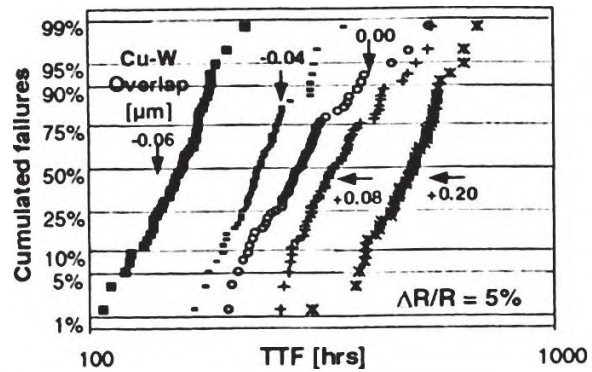


Fig.11 Failure distributions obtained at 275°C on short via chains as a function of the Cu-to-W-via overlap using an 5% relative failure criterion. The failure times become smaller with smaller overlap between copper line and W-plug.

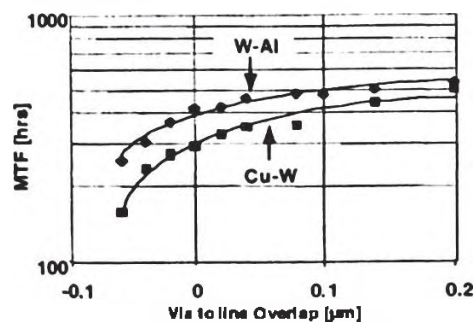


Fig.12 MTFs obtained at 275°C on short via chains as a function of the Cu-W and Al-W overlap, respectively. Increasing overlaps with respect to both copper or aluminum metal line yield longer failure times

Failure time distributions obtained on via-chains with varying overlap between W-plug and copper level are summarized in Fig.11. As can be seen, the distributions have similar shape factors but failure times become steadily smaller with smaller overlap. The MTF is reduced by about 2x when decreasing the overlap from 0.00 to -0.06μm. On the other hand, the failure time is increased by less than 25% when enlarging the overlap from 0.00 to +0.06 (Fig.12). Although no stressvoids are observed in the aluminum level, the variation of the overlap between W-plug and Al-metal line is influencing the voiding kinetics in the copper level underneath. Again, the negative Al-W overlap implies a significant drop in the MTF, whereas a large positive overlap leads to a slight increase of the failure time (Fig.12).

From these results, it can be concluded that sufficient large (positive) overlaps must be implemented in a design to assure the highest possible level of built-in reliability and to compensate possible process-related via-to-line misalignments.

Discussion

The stress voiding mechanism in via-line interconnect systems is of complex nature. It is primarily enabled and enhanced by following items:

- 1) Large number of free vacancies contributing to the voiding process. Their amount depends on the available copper volume and the copper microstructure which is

strongly process dependent. They can be present already after the deposition process, but also be generated during lifetime (or test) by mechanisms such as recrystallization or recovery of crystal defects.

2) Easy diffusion pathways enabling the migration of free vacancies. These pathways are controlled by the interface properties and the copper microstructure. The particular microstructural properties are influenced by the process and the materials used as liner or capping layers.

3) High stress gradients imply an increase of the driving force for vacancy movement towards the via. Since the stress gradients induced in a via-line system are influenced by the thermal mismatch between the used dielectric materials, interface layers and copper lines they can change with the temperature. Beside this, the stress gradients depend on geometrical aspects of the connected metal lines including the via-size.

4) Large number of void nucleation sites. Especially pre-existing voids in the copper, defects in the liner (missing liner, liner roughness) or triple points of interfaces may serve as sites of preferred void nucleation and can enhance the voiding process.

The variation of one of these 4 items can cause the change of the SV behavior of a considered structure. The results gathered on numerous test structures suggest that from a layout perspective the SV mechanism is primary controlled by metal line volume in the voiding level which defines the vacancy reservoir and the stress gradient which is dependent on specific layout configurations.

The plate size effect can qualitatively be explained by estimating the active volume over time. The active diffusion volume is a coexistence region of three volumes [5]: 1) diffusion volume defined by the characteristic diffusion path length ($x_D(t,T) = \sqrt{Dt}$, where $D(T)$ is the diffusivity) of free vacancies. For a given time interval and temperature only those vacancies have the potential to contribute to the voiding that are in a distance smaller x_D from the voiding location. 2) Metal line volume containing free vacancies. 3) Region of stress gradients in the interconnect that force vacancies towards the voiding location.

The behavior of the stress gradient region (3) was simulated by Finite Element Analysis (FEA) considering all important material features of the metal stack, the dielectric encapsulation and interface layers. As can be seen in Fig.13, the hydrostatic stress in the via is almost independent of the geometry (i.e. width) of the upper metal line. Furthermore, the stress in the bulk of the line above the via is not changing significantly with the line width. Only the stress profile within the SiN-cap layer is slightly changing, indicating that the hydrostatic stress decreases with increasing line width. The variation of the hydrostatic stress with the line width can therefore not explain the pronounced effect of plate sizes on the SV behavior observed in the studies of this work.

Assuming that the vacancies are homogeneously distributed within the interconnect volume, the change of the active volume is dominated by the change of the diffusion volume of the respective test structure.

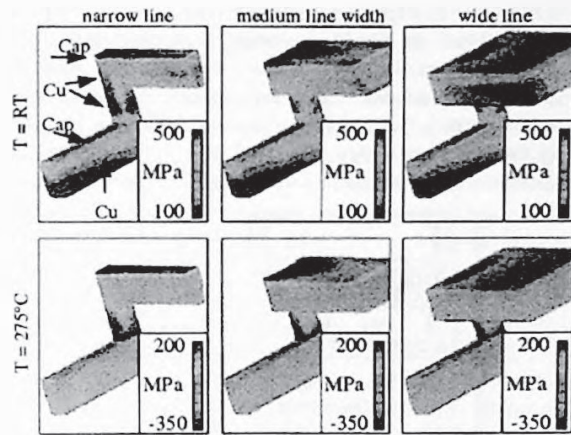


Fig.13 Simulation of the hydrostatic stress in via-line structures for 3 different top line widths for room temperature (upper pictures) and 275°C (bottom), respectively.

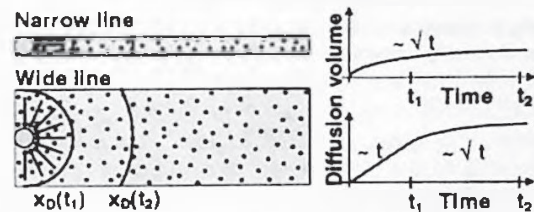


Fig.14 Diffusion area as a function of time calculated for narrow and wide lines, respectively.

The vacancies present in the bulk copper are captured by the stress field around the via-to-line transition and driven towards the voiding location inside or next to the via (Fig.1). The number of vacancies which might contribute to the voiding process is then defined by the interconnect volume in a distance $x \leq x_D$ from the via. Thereby, narrow lines behave different in comparison to wide metal plates. While in narrow lines only vacancies beside the via can move to the via, in wide lines significantly more vacancies from all directions are available around the via. Hence, the one dimensional vacancy transport in narrow lines should result in a \sqrt{t} -dependence of the resulting diffusion volume around the via, while two dimensional vacancy transport in wide lines from a circular catchment area yield to linear time dependence (Fig.14).

However, once the diffusion length has reached half of the line width and hence all vacancies around the via have been pulled towards the via, only the more distant vacancies can be responsible for a further replenishment. Therefore the vacancy transport also for wide lines then will then change to a \sqrt{t} -dependence. Consequently, wide lines can provide more vacancies per time to a via, leading to earlier failure times. For line widths larger than x_D , the amount of captured vacancies within a time t gets independent of the line width, resulting in a saturation of the medium time to failure (Fig.7).

In general, SV failure times are defined by a certain amount of resistance increase. Since voiding occurs inside or next to the dual damascene via, the resistance increase

is not linearly dependent with the void size. This behavior is simulated in Fig.15 assuming a square-shaped void growing from the via edge towards the top line. The simulation considers "liner redundancy" i.e. even if the void occupies the whole via the via resistance is limited by the liner resistivity. Therefore, the increase of the via resistance becomes more pronounced for thinner liners.

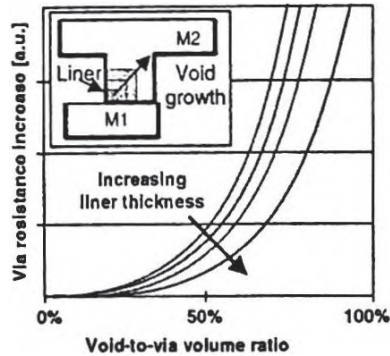


Fig.15 Change of the via resistance calculated as a function of the void size assuming a square-shaped void growing from via edge towards the top line. The resistance increase becomes more pronounced as the liner becomes thinner.

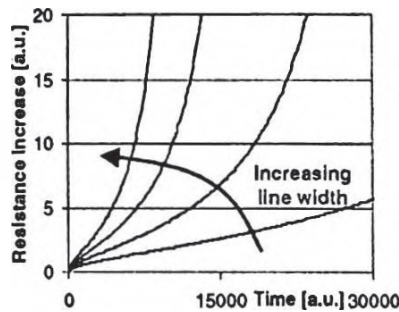


Fig.16 Resistance drift calculated for a via-line structure dependent on the line width of the connected metal plate. The calculation is based on a combination of the available diffusion volume (Fig. 14) and the resulting via-resistance increase (Fig. 15).

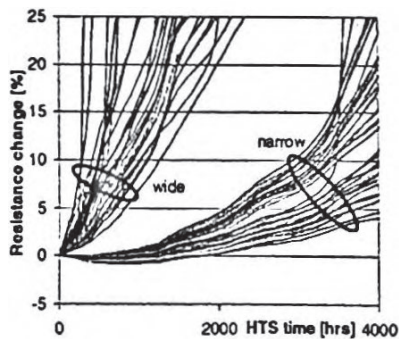


Fig.17 Resistance drift typically measured on plate structures with small ($w=0.28\mu\text{m}$) and large line widths ($w=10\mu\text{m}$), respectively.

A combination of the diffusion volume dependence (Fig.14) and the via-resistance dependence (Fig.15) results in a possible $R(t)$ diagram (Fig.16) that remarkably resembles the experimentally determined plot (Fig.17):

for narrow plates the rise of the resistance is observed much later compared to wide lines.

The hypothesis, that the available vacancy volume is mainly responsible for the SV behavior is further supported by the results gathered on square shaped plate structures (Fig.8) where the failure rate was found to increase with the plate size. The effect of the nose-like line extension changes the SV-behavior (Fig.9). While the plates still serve as large vacancy reservoir, the line extension is a bottle neck for the vacancy movement. The longer the line extension, the more the diffusion volume is dominated by the behavior of the narrow line. Hence, the efficiency of the plate as the vacancy reservoir is suppressed.

Some discrepancy between SV failure time and the available vacancy reservoir was observed in the line length dependence for narrow lines (Fig.5), where MTFs reach a minimum at about $100\mu\text{m}$ ($w=0.28\mu\text{m}$). The reason of this behavior is a possible change in the driving force with the line length.

The influence of the via-size on the SV behavior is of complex nature. The observed increase of the failure frequency with decreasing via diameter (Fig.8) can obviously be related to three different aspects: 1) The smaller the via diameter the less void volume and hence time is needed to reach the failure criterion: this situation is simulated in Fig.18 (in analogy to Fig.15); 2) with decreasing via diameter it is more difficult to deposit a continuous defect-free via liner, resulting in a higher resistive shunt layer once a void has formed. With this, a higher resistance increase is obtained for a given void volume (Fig.15); 3) the smaller the via diameter the smaller is the area of contact between via and bottom line. Thus, the stress level and hence the driving force for vacancy movement will be increasing in smaller vias.

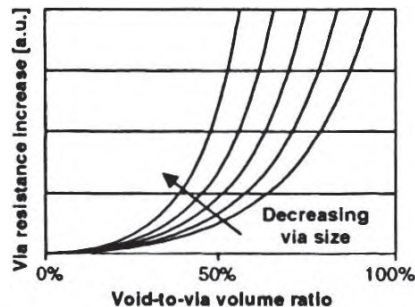


Fig.18 Via resistance calculated for different via diameters. For the same void volume, a larger resistance increase is obtained for smaller vias. The calculation is based on the same assumptions as in Fig.15.

In the case of the via-to-line misalignment, the driving force is a key factor influencing the SV behavior, rather than the diffusion volume of the connected metal lines. Simulations of the linear stress components for via-line structures with and without misalignment reveal, that regions of high σ_{xx} stress gradients are obtained in the upper part of the metal line next to the via, whereas σ_{yy} gradients are located directly under the via (Fig.19). In both regions stress-induced voids can be found after HTS

test. They can be attributed to different failure modes with individual activation energies [4].

The effect of misalignment on the stress voiding behavior can be explained by the increase of both stress gradients with increasing misalignment (Fig. 19). Consequently, higher driving forces are obtained at a large negative via-to-line overlap leading to a reduction of SV failure times on those structures (Fig. 11).

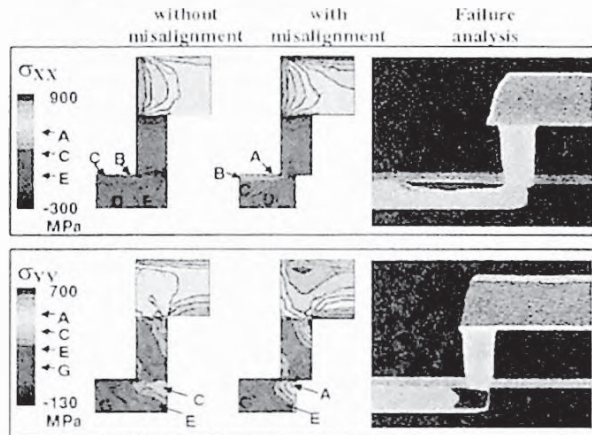


Fig. 19 FEA simulations of the linear σ_{xx} (top) and σ_{yy} (bottom) stress components for via-line structures without and with misalignment of the line below the via respectively. Regions of high σ_{xx} stress gradients are obtained in the upper part of the metal line next to the via. σ_{yy} gradients directly under the via. In both regions stress-induced voids can be found after HTS test corresponding to two different SV failure modes.

Beside the reservoir geometry which primarily influences the SV behavior, also design features of the connecting level (which is not affected by stress-induced voiding) were found to play an important role. In the case of the via-misalignment in a lower metal level, the FEA shows that the stress even in the metal level above the via is changed. In analogy, the effect of a via-misalignment in the Al-level on the SV behavior in the copper level of short via chains can be explained (Fig. 12).

Similar to the via-misalignment, the width of the connecting line is changing the SV behavior of the mesh-type via-chains - arrow lines in the connecting level are assumed to induce a larger driving force in the voiding level resulting in lower failure times (Fig. 10).

The influence of the metal level on the voiding kinetics in mesh-type test structures (Fig. 10) is possibly the result of the wafer curvature, that may induce higher stress gradients to the lower levels. Since this effect is assumed to yield only small differences, another aspect may explain the observed behavior. Considering that the lower metallization levels have been subjected to several high temperature anneal steps up to 400 °C during e.g. the dielectric and cap-layer deposition of all following levels, a SV incubation time may already have partially elapsed. Hence, the time to first resistance increase becomes smaller with every metal level that has been processed above the respective layer.

Conclusion

High temperature storage studies on numerous samples of test structures with varying designs revealed a strong influence of geometrical aspects on the SV behavior. Thereby, the geometries of both the voiding level and that of the connecting level have an effect on the voiding kinetics. Therefore, they have to be distinguished from a methodology's point of view. A large voiding rate is obtained on structures with large design features such as plates or meshes. The larger the diffusion volume the more vacancies can contribute to the voiding process. The voiding rate saturates, if the plate or mesh size is larger than the characteristic diffusion length of vacancies from the via. Although the connecting level is not affected by stress voids, it is influencing the driving force of the SV mechanism and hence the failure time in the voiding level. In this context wider connecting links were found to yield larger failure times most probably due to a relief of the driving force. Furthermore, via-line misalignments were found to reduce SV failure times significantly. On the one hand, the consideration of these aspects in the design and layout of interconnect networks can reduce SV-susceptibility in complex products and thus improve their built-in reliability. On the other hand, these results imply that each new interconnect generation must thoroughly be investigated with multiple sets of different test structures in a wide geometrical range in order to find (and test!) the worst case configuration with respect to their reliability.

Acknowledgement

The authors would like to acknowledge the work of the Infineon Reliability Methodology Stress Center, the failure analysis department as well as Andy Cowley and Mark Honkisz who gave important inputs to this work.

References

- [1]: A.von Glasow et al., "Electromigration and Stressvoiding Investigations on Dual Damascene Copper Interconnects", AMC 2001
- [2]: D.Gan et al., "Effects of dielectric material and line width on thermal stresses of Cu line structures", IITC 2002
- [3]: K.Musaka et al., "Thermal Stress and Reliability Characterization of Barriers for Cu interconnects", IITC 2001
- [4]: A.v.Glasow et al., "New Approaches for the assessment of stress-induced voiding in Cu Interconnects", IITC 2002
- [5]: E.T.Ogawa et al., "Stress-Induced Voiding under vias connected to wide Cu metal leads", IRPS 2002
- [6]: D.Edelstein et al., "Full Cu Wiring in a sub-0.25µm CMOS ULSI technology", IEDM 1997