

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING CO. LTD.,

Petitioner

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,

Patent Owner

Case IPR2025-01211

Patent 7,439,623

**PATENT OWNER'S REPLY BRIEF IN SUPPORT OF DISCRETIONARY
DENIAL PURSUANT TO THE BOARD'S MARCH 26, 2025
INTERIM PROCESSES FOR PTAB WORKLOAD MANAGEMENT
[PUBLIC REDACTED VERSION]**

Mail Stop "PATENT BOARD"

Patent Trial and Appeal Board

U.S. Patent and Trademark Office

P.O. Box 1450

Alexandria, VA 22313-1450

TSMC’s opposition (“Opp’n”) does not dispute that its five IPR petitions seek to invoke the Board’s limited resources to adjudicate 89 claims, most of which are ***both*** expired ***and*** not asserted in any lawsuit. Nor does TSMC dispute that the trial court can resolve all pertinent validity disputes in a ***single*** proceeding without requiring the Board to undertake ***five*** laborious IPR proceedings. And TSMC admits that the scheduled trial date precedes the projected FWD date by months, Opp’n at 18, meaning that the district court will likely do so well before the Board. Instead, TSMC advances four flawed arguments, none of which merits institution.

I. TSMC’s Examiner Error Arguments Are Flawed

The Petition does not assert examiner error. *See* Petition (no reference to “error” or similar). This is because none of the references of record merited an examiner rejection. Now, however, TSMC shifts course, asserting that two such references—namely, Kunikiyo and Nasu—invalidate the claims. Opp’n at 4-9. TSMC’s disbelief in its own theory is reflected by the Petition’s (1) reliance on Nasu only for dependent claim limitations in claims 29-30; and (2) failure to rely on Kunikiyo at all. Petition at 1-2. And, because the Petition’s invalidity theories differ fundamentally from TSMC’s examiner error invalidity theory, even assuming incorrectly that the examiner erred, institution would not reevaluate TSMC’s examiner error theory or correct the alleged error.

In any event, Kunikiyo and Nasu fail to disclose, *inter alia*, the claimed

structure wherein “the second interconnect” forms “a dual damascene structure” with “the via” and “the dummy via,” as recited in claim 1 of the ’623 patent. EX1001 at 31:4-7. The Petition explains that, in the “[d]ual damascene” method, “patterns of trenches and underlying via holes [in an insulating film] are filled with conductive metal(s),” *id.* at 3, and shows an exemplary damascene “T” shaped conductor formed in an insulating film wherein the trench is the horizontal top of the “T” and the via is the vertical portion of the “T,” Petition at 4 (Figure 2-5); *see also* EX1033 ¶ [0007] (explaining that in “a dual damascene process,” “metal is buried or embedded in a trench defined by a via hole formed between multi-layer wirings and a trench for the upper wiring” in “the interlayer insulating film”). TSMC’s annotated version of Figure 2B of the ’623 patent shows that same type of “T” structure—namely, the green horizontal interconnect trench and vertical vias *all formed in the purple insulating film*. Opp’n at 7. But TSMC’s annotated version of Kunikiyo Figure 12 does not show the green interconnect 28A located in a trench within purple insulating film 23. *Id.* And the same is true for TSMC’s annotated version of Nasu Figure 5, which does not show green conductor B located in a trench within insulating film 6. *Id.* at 8.

Cognizant that these figures cannot invalidate, TSMC resorts to misstating Kunikiyo’s written description. While TSMC misleadingly suggests that Kunikiyo only teaches the damascene method for forming interconnects, Opp’n at 4,

Kunikiyo teaches different methods. EX1007 at 1:36-58 (discussing the “etching method” and the “damascene method”). *None of the text relating to Kunikiyo Figure 12 suggests that the damascene method was used or that interconnect 28A is located within a trench in insulating film 23.* See *id.* at 20:5-42. And, hidden in a footnote, TSMC concedes that Nasu does not teach the claimed dual damascene structure at all; TSMC simply wants to infer that structure based on Nasu’s reference to copper interconnects. Opp’n at 7 n.5. The examiner did not err.

TSMC then pivots to asserting error because the examiner did not locate two of the Petition’s references, Watanabe and Hasunuma. *Id.* at 9-12. The fact that an examiner did not locate a particular reference is not examiner error. TSMC’s theory is a thinly disguised merits argument. AICP has explained that it is not addressing the Petition’s merits at this stage, partly because TSMC is using the IPR process “as a tactical stalking horse to learn AICP’s rebuttals to its validity challenges prior to the due date for its expert reports in the Lawsuit.” Paper 10 at 18. Further, while AICP prepared and filed preliminary responses exposing some of the numerous flaws in six of TSMC’s earlier IPR petitions, doing so created significant expense and duplication even though the Director ultimately granted discretionary denial. *Id.* at 18-19 (referencing IPR2025-00682, Paper 17 and IPR2025-00828, Paper 17). If proceedings are instituted here, AICP intends to develop rebuttals to the Petition’s grounds and vigorously defend the ’623 patent’s validity.

II. TSMC’s “Settled Expectations” Arguments Are Flawed

The ’623 patent issued over seventeen years ago and is now expired. The Director has already (1) held that other similarly situated AICP patents create strong settled expectations for AICP; and (2) rejected the very same arguments TSMC now makes. *See* Paper 10 at 19-20. AICP’s settled expectation arguments are even stronger here because [REDACTED]

[REDACTED]. *Intel Corp. v. Proxense LLC*, IPR2025-00327, Paper-12, 2-3 (June 26, 2025). Moreover, the licenses doubtless are in TSMC’s technology space because, as TSMC concedes, the four patents are focused on a single technology: namely, “semiconductor design and manufacture.” Opp’n at 20.

III. TSMC’s Arguments Relating to the Other *Fintiv* Factors Are Flawed

While TSMC’s *Fintiv* arguments are flawed, two merit special attention. First, although TSMC admits the trial date precedes the projected FWD due date by months, Opp’n at 18, TSMC nevertheless says *Fintiv* Factor 2 is “at least neutral,” *id.* TSMC is incorrect. *See* Paper 10 at 11-12. And TSMC’s trial statistics have little weight because a firm trial date exists and no evidence suggests that trial will be delayed. TSMC’s example of a trial that was delayed by just three weeks (*i.e.*, from October 3rd to 27th), Opp’n at 19, highlights why, even if trial was delayed, it

would likely not invert the order of the trial and FWD dates.

Second, TSMC does ***not*** dispute that discovery available only in the district court could eliminate some of the IPR petitions' grounds. *See* Paper 10 at 17-18. While TSMC labels such evidence "speculat[ive]," Opp'n at 21, it does ***not*** dispute that: (1) regardless of institution, AICP must continue litigating validity in court to obtain the evidence; and (2) if AICP does so successfully, thereby defeating some invalidity theories in court, inconsistent decisions between tribunals could occur.

IV. TSMC's Arguments Relating to National Security Are Flawed

TSMC's feigned fears over national security are meritless. First, TSMC's alleged fear that its products will be enjoined because boilerplate language in AICP's complaint "seeks an injunction," Opp'n at 2, is nonsense. TSMC admits the '623 patent is expired, *id.* at 15, and black letter law establishes that "the district court cannot enjoin [an accused infringer] from infringing an expired patent." *Lans v. Digital Equip. Corp.*, 252 F.3d 1320, 1328 (Fed. Cir. 2001).

Second, even if a theoretical risk of an injunction existed, AICP has already waived injunctive remedies with respect to the '623 patent. *See* Paper 10 at 18-19.

Third, the Director has already explained the two requirements for TSMC to advance its national security argument. *See* Paper 10 at 18. But TSMC refuses to "specifically identify the affected military products." Opp'n at 22-23. And it also refuses to explain how the '623 patent allegedly relates to national security.

Dated: November 5, 2025

Respectfully submitted,

By: /Russell A. Chorush /
Russell A. Chorush (Reg. No. 55,869)
Attorney for Patent Owner
Advanced Integrated Circuit Process, LLC

CERTIFICATE OF SERVICE

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), a copy of the foregoing **Patent Owner’s Reply Brief in Support of Discretionary Denial Pursuant to The Board’s March 26, 2025 Interim Processes for PTAB Workload Management [Public Redacted Version]**, was served to the following counsel of record for Petitioner addressed as follows:

Lead Counsel for Petitioner	Back-up Counsel for Petitioner
Michael Houston Reg. No. 58,486 FOLEY & LARDNER LLP 321 North Clark Street, Suite 3000 Chicago, Illinois 60654 312-832-4500 mhouston@foley.com	Pavan Agarwal Reg. No. 40,888 FOLEY & LARDNER LLP 3000 K Street N.W., Suite 600 Washington, DC 20008 202-672-5300 pagarwal@foley.com Nicholas Lagerwall Reg. No. 63,272 FOLEY & LARDNER LLP 150 East Gilman Street, Suite 5000 Madison, Wisconsin 53703 608-257-5035 nlagerwall@foley.com

Dated: November 5, 2025

By: / Russell A. Chorush /
Russell A. Chorush (Reg. No. 55,869)
Attorney for Patent Owner
Advanced Integrated Circuit Process, LLC