35% Drive Current Improvement from Recessed-SiGe Drain Extensions on 37 nm Gate Length PMOS

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Abstract

Results from the best reported PMOS transistor at a 37 nm gate length (Lg) built on a process with a recessed SiGe epitaxial layer are discussed. The process details include successful integration of SiGe at the drain extension (DE) location. A highly compressive SiGe layer, in close proximity to the channel, results in large hole mobility improvements. HRTEM based lattice parameter extractions confirm the compressive strain in the channel. *In situ* doped B in SiGe can be activated to a higher degree than implanted B in bulk Si resulting in further improvements from the lower DE resistance. Both changes combine to give an unprecedented 35% PMOS performance improvement. Process and device simulations that predict the observed parametric behavior quantitatively isolate the improvements to be ~ 28% from stress and 7% from DE resistance improvement.

Introduction

Epitaxial SiGe, grown in recessed Si, has been used to compressively strain the PMOS channel and increase the hole mobility [1]. In those experiments, SiGe layer was grown in recessed Source/Drain (SD) regions (Figure 1a) where a relatively thick spacer separates the SiGe region from the channel. ANSYS based stress simulations (Figure 1b) illustrate the advantage of incorporating the SiGe layer at the DE location (Figure 1c). A 30 nm thick recessed SiGe at the SD location results in a 250 MPa stress in the middle of the channel; however, the same SiGe layer when present at the DE location stresses the channel to ~900 MPa. The reference stress state arising from the STI and the spacer layers is shown in the same figure to be negligible. A process to build the device shown schematically in Figure 1c was developed to take advantage of the higher channel compressive stress from SiGe incorporation at the DE location. The entire SiGe layer was contained in the DE region. Detailed modeling helped engineer identical DE and channel dopant profiles with and without the *in situ* doped SiGe layer.

Process

A novel, complex and selective, recess etch process was used to etch the silicon while maintaining the lateral integrity of the gate with a thin offset spacer. The *in situ* doped SiGe epitaxial film was deposited selectively in the recess. The details of the integration sequence used are shown as the process flow in Figure 2. The additional thermal budget from SiGe deposition is less of a concern when integrated at DE compared to the SD location. Reference and recessed SiGe devices were built on a standard state of the art CMOS flow [2] that included plasma nitrided gate oxide and nickel silicide processes. A TEM image in Figure 3 shows, for the first time, a cross-section of a 37nm gate PMOS with SiGe integrated at the DE location. An etch that maintains the structural integrity and a uniform selective epitaxial film are apparent from the cross-section. A HRTEM lattice image and the relevant diffractograms are shown in Figure 4. A compressive stress gradient that decays from the SiGe/channel interface toward the center of the device and a tensile stress on Si right below the SiGe are observed.

Device Results

Figure 5 shows the drive current (Ion) to off current (Ioff) comparison at -1.2V operating voltage (Vdd). A 35% drive current improvement is apparent from this plot. Data from multiple locations on the wafers illustrate the manufacturability and robustness of the processes developed. Ioff as a function of gate length (Figure 6) shows that the 37 nm gate length device can support a 40 nA/µm Ioff. Performance of the reference and SiGe device in Figure 7a indicates that electrostatics based subthreshold behavior of the two devices are identical. However, the wide separation on the Ion vs Vtsat (Figure 7b) plot indicates that there is a significant decrease in the net (channel + DE) resistance in the SiGe device.

Discussion

Calibrated simulations are used to quantitatively isolate the relative contributions from channel resistance and DE resistance and predict the performance at a 50 nm Lg. Process and device simulations were exercised at multiple gate lengths to obtain the Lg dependence of Ion at 40 nA Ioff. The simulations match the observed trend in the data as shown in Figure 8. HRTEM analysis (Figure 4) and stress simulations (Figure 1) show stress profiles that decay monotonically from the edge of SiGe layer toward the channel; therefore, longer gate length channels experience a lower magnitude of stress from the SiGe layer. Stress profiles were input into a device simulator where mobility dependence on stress is captured. Lowering of DE resistance with SiGe was also modeled. Linear current (Idlin) as a function of gate length data in Figure 9 shows that at long gate lengths the recessed-SiGe device does not show any improvement. At target Lg, the Idlin improves by ~70%, consistent with the previously reported [1] ratio 2:1 Idlin:Ion improvement. Simulations with the stress profile gradients accurately predict gate length dependent linear current improvements; while, simulations of devices with a constant uniform stress over-predict the drive current at long gate lengths. Stress enhanced channel mobility increase results in 28% drive current improvement in these simulations. The intercept of the simulated fit to the data on the resistance (calculated as Vd/Id linear) vs L plot (Figure 10) shows a 25% DE resistance decrease that translates to 7% drive current improvement.

Conclusions

A novel and manufacturable process that integrates a SiGe epitaxial film at the DE location is demonstrated for the first time. The resulting PMOS transistor at 37 nm gate length is parametrically the best reported (Table 1) device to date. Compressive stress induced in the channel by the SiGe layer at the DE location, is shown to be the major source of the observed 35% performance gain.

References

[1] T. Ghani et. al. IEDM Digest 2003 p. 978.
[2] B. Hornung et al. VLSI Symp. Proceedings 2003 p. 85.

 0-7803-8289-7/04/$20.00 © 2004 IEEE

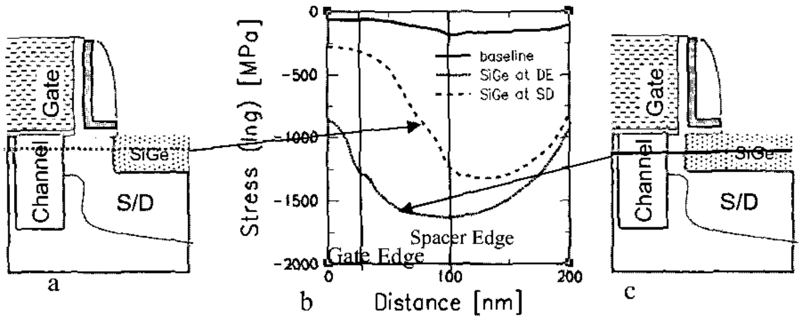

Fig. 1. Schematic illustration of 30 nm $Si_{0.8}Ge_{0.2}$ incorporation at a) SD and c) DE locations and the resulting stress profiles (b)

- Gate etch
- Thin offset spacer dep-etch
- Recess and SiGe deposition
- SW spacer definition
- Source/Drain implant
- Source/Drain Anneal

Fig. 2. Process flow used to incorporate the SiGe with in the drain extension region

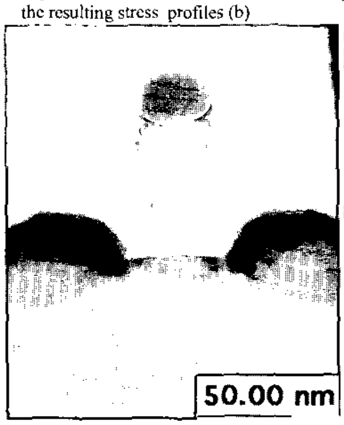

Fig. 3. TEM cross-section of 37 nm gate with SiGe layer in the DE region

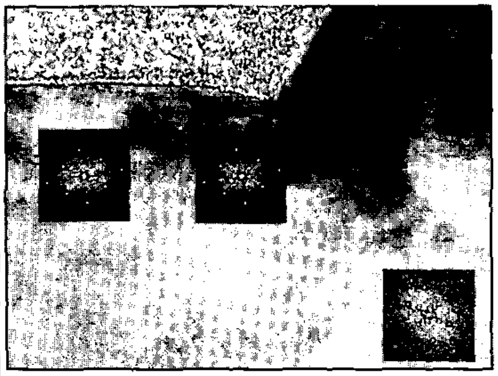

Fig. 4. HREM image with diffractograms taken from the indicated areas shown as insets. Lattice spacing measurements show ~0.7% peak compressive strain on silicon channel under the gate

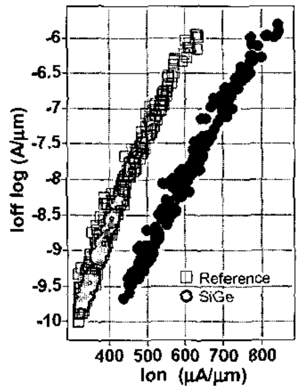

Fig. 5. Ion/Ioff measured at Vdd=-1.2V plot showing the improvement with SiGe layer

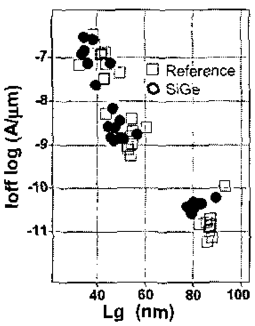

Fig. 6. Ioff vs L gate showing 30-50 nA/μm leakage at 37 nm Lg

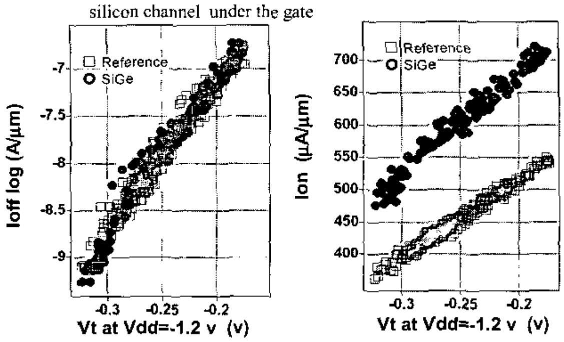

Fig. 7. Ioff and Ion variation as function of Vt at Vdd illustrating the lower resistance of the recessed-SiGe device for the same sub threshold behavior

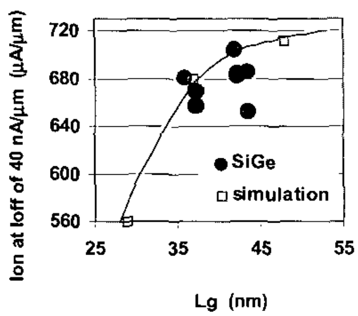

Fig. 8. Data and simulation showing the Lg dependence of Ion at a given Ioff for the SiGe device. At 50nm Lg, Ion=710 μA/μm

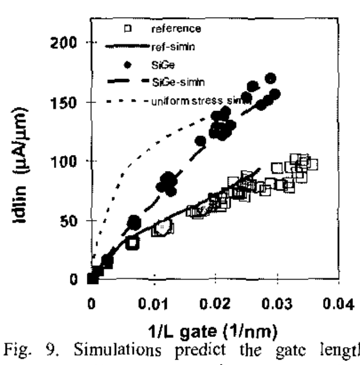

Fig. 9. Simulations predict the gate length dependent linear current improvement. The uniform stress simulation merges with the SiGe data at short gate lengths

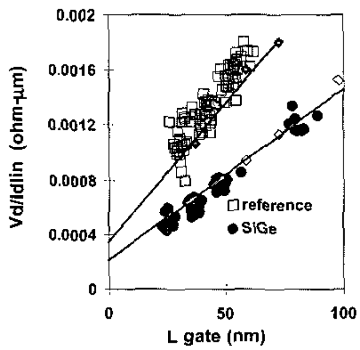

Fig. 10. DE resistance improvement shown in the resistance vs gate length plot. Simulated lines extended to 0 Lg show the lower DE resistance observed with SiGe

	Reference	SiGe	PMOS[1]
Ion μA/μm	500	660	700
Idlin μA/μm	95	160	
Ioff nA/μm	40	40	40
Vt (Vd=0.5 v)	-0.44	-0.40	-0.37
Gate length (nm)	40	40	50
Cgd (fF/μm)	0.27	0.28	
Projected Ion at Lg = 50 nm & Ioff = 40 nA/μm	540	710	700

Table 1. Comparison of the parametric data of the SiGe device at Vdd=-1.2 V showing the 70% linear and 35 % saturation current improvements