Low Standby Power CMOS with HfO_2 Gate Oxide for 100-nm Generation

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Abstract

We have fabricated 55-nm poly-Si gated n- and p-MOSFETs with HfO_2 gate dielectric of 3-nm physical thickness deposited by atomic layer deposition (ALD). Conventional CMOS process was used with high-temperature S/D anneal of $\geq 1000^0$ C, cobalt-silicide and pocket implant. The devices showed very promising characteristics for low standby power applications due to drastic reduction of gate leakage current.

Introduction

According to the International Technology Roadmap for Semiconductors (ITRS), high-k dielectrics are predicted to be required for low power – low leakage current applications in 100-nm CMOS technology node. Recently, there has been much interest in hafnium dioxide due to its thermodynamic stability with poly-Si gate, high dielectric constant, and high band gap [1]. Several research groups reported on successful fabrication of short channel MOSFETs with thin HfO_2 gate dielectric [2-5]. To our knowledge, the shortest devices with HfO_2 fabricated using the conventional process are 80-nm CMOS devices announced in [3]. However, low temperature anneal was used in [3], while in the conventional CMOS flow anneals of $\geq 1000^0$C are required. In this work, we used 3-nm (by TEM) HfO_2 gate dielectric and achieved 55-nm gate length CMOS devices with low off-state current values and high inversion capacitance values.

Fabrication Process

The process flow is shown in Fig. 1. The fabrication process includes dual doped poly-Si gates, high temperature anneal of $\geq 1000^o$C, cobalt silicide, extension and pocket implants. The HfO_2 film was deposited by ALD. In Fig. 2 we show cross-section TEM photograph of ultra-thin (<3 nm) HfO_2 demonstrating very good film uniformity. Very thin (less than 0.5 nm) silicon oxide interfacial layer is visible at the silicon substrate – HfO_2 interface. After HfO_2 deposition samples were annealed and then 150-nm poly-Si film was deposited by LPCVD. Poly-Si was patterned by EB and etched by RIE. Poly-Si gates down to sub-50 nm lengths were achieved. The HfO_2 film remained on silicon substrate after RIE and subsequent HF treatment. Therefore, extension and pocket implants energies and/or doses were increased to account for the effect of this film. After extension and pocket implants, LTO sidewall was formed and then, source, drain and gate were implanted. In Fig. 3 cross-section SEM photograph of 50-nm gate length HfO_2 transistor with cobalt silicide in source, drain and gate areas is shown. Metal contacts for our devices were formed in a standard metallization process.

Measurement Results

In Fig.4 and Fig.5 we show capacitance characteristics for n- and p-MOSFETs, correspondently. The electrical oxide thickness of the HfO_2 film is approximately 1.4 nm, as estimated from accumulation capacitance. Good suppression of gate depletion with high-temperature anneal is demonstrated. Fig. 6 shows that higher temperature anneal is beneficial for HfO_2 devices. In Fig. 7 we show that more than 3 orders of magnitude reduction in gate leakage current is achieved using HfO_2 as compared to reference SiO_2 gate dielectric. In Fig. 8 we compare for the same channel dose subthreshold characteristics for long-channel (L_{GATE}=300 nm) MOSFETS with HfO_2 and SiO_2 gate dielectrics. Threshold voltage for all channel lengths is determined in this work at constant drain current of 100-nA/µm. Devices with HfO_2 exhibit 10000x lower off-state current than SiO_2 samples. For SiO_2 devices in Fig. 8 the off-state current is high because of high gate leakage current and therefore the off-state current cannot be suppressed by increasing the threshold voltage. Devices with HfO_2 show the off-state current lower than 1pA/µm and meet the ITRS off-state current requirements for low standby power applications. In Fig. 9 we show threshold voltage roll-off for n-MOSFET with HfO_2 gate dielectric. The short-channel effect is suppressed down to 50-nm gate length. The threshold voltage shift related to HfO_2 film can be compensated by reducing the channel doping. In Fig. 10 we demonstrate that the subthreshold factor roll-up is suppressed down to 50-nm gate length for higher channel doping, and to 55-nm gate length for lower channel doping. In Fig. 11 we show the threshold voltage roll-off for p-MOSFET. Well-behaved transistor characteristics are obtained down sub-50nm gate length. The dependence of threshold voltage on channel dose is very weak for p-MOSFET. In Fig. 12 the subthreshold factor roll-up for p-MOSFET is shown. The subthreshold factor for long-channel p-MOSFET is 100 mV/dec (80 mV/dec for reference SiO_2 device). The degradation is explained by boron penetration through HfO_2 confirmed by SIMS. Therefore, suppression of boron penetration is the main concern for improving HfO_2 p-MOSFET characteristics. In Fig. 13 we demonstrate well-behaved drain current–gate voltage characteristics for 55-nm MOSFETs. Off-state current of 25 pA/µm is achieved. The increase of off-state current as compared to long-channel devices of Fig. 8 is explained by threshold voltage decrease and subthreshold factor increase due to the short-channel effect. In Fig. 14 we show well behaved drain current – drain voltage characteristics as function of gate voltage. In Table 1 we summarize results for devices with 3-nm HfO_2 gate dielectric at supply voltage of 1.2 V. Improved I_{ON}-I_{OFF} ratio is predicted with improving mobility (60% of SiO_2 mobility in this work) and suppressing boron penetration.

Conclusion

55-nm CMOS with 3-nm HfO_2 gate dielectric was fabricated using conventional process flow with high-temperature anneal of $\geq 1000^0$C and cobalt silicide. Gate current reduction of more than 3 orders of magnitude was achieved and low off-state current devices were obtained demonstrating very promising characteristics of HfO_2 for low standby current applications.

References

1. E.P.Gusev et al., IEDM Tech. Dig., 2001.
2. Y.Kim et al., IEDM Tech. Dig., 2001.
3. C.Hobbs et al., IEDM Tech. Dig., 2001.
4. D.Barlage et al., IEDM Tech. Dig., 2001.
5. J.M.Hergenrother et al., IEDM Tech. Dig., 2001.

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- Device Isolation
- Well and Channel Implants
- HF-dip+SC2 wet clean
- ALD Deposition of 3-nm HfO_2
- Post-Deposition Anneal
- Poly-Si Deposition and Etch
- Extension and Pocket Implants
- LTO Spacer Deposition and Etch
- Source-Drain Implant
- RTA (800°C~1025°C)
- Cobalt-Silicide Formation
- Standard Metallization Process

Fig.1 Fabrication process flow

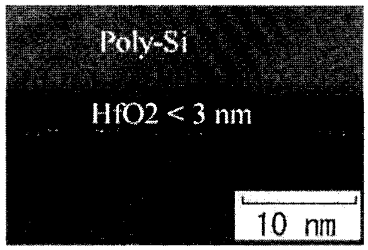

Fig.2 HR-TEM micrograph showing details of the gate stack

Fig. 3 SEM micrograph of 50-nm Poly-Si/HfO_2 MOSFET with Co-silicide

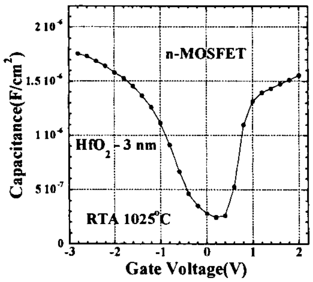

Fig.4 Capacitance – voltage characteristics for n-MOSFET with 3-nm HfO_2 oxide

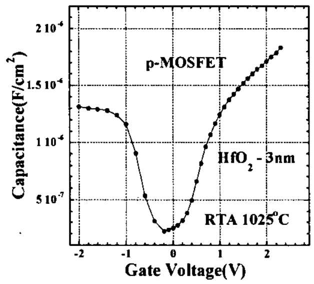

Fig.5 Capacitance-voltage characteristics for p-MOSFET with 3-nm HfO_2 oxide

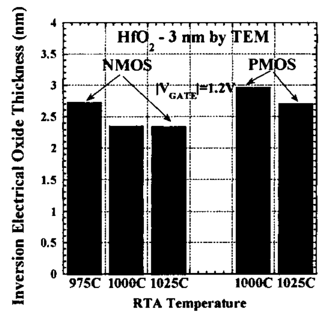

Fig.6 Dependence of inversion oxide thickness on RTA temperature

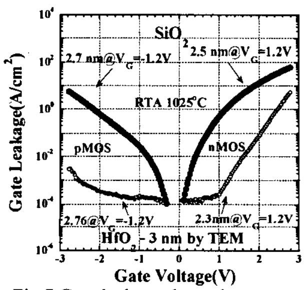

Fig.7 Gate leakage dependence on gate voltage for n- and p-MOSFET in inversion

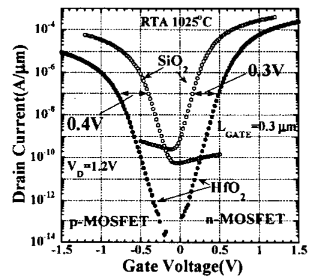

Fig.8 Threshold voltage shift for long-channel n- and p-MOSFETs with 3-nm HfO_2

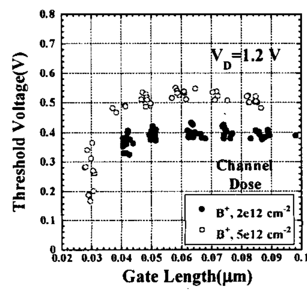

Fig.9 Threshold voltage roll-off for n-MOSFET with 3-nm HfO_2

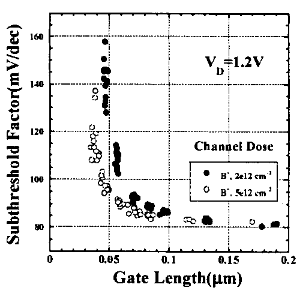

Fig.10 Subthreshold factor roll-up for n-MOSFET with 3-nm HfO_2

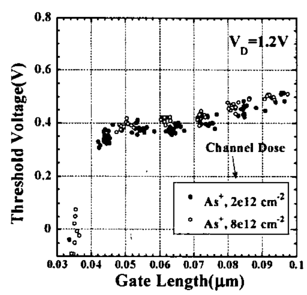

Fig.11 Threshold voltage roll-off for p-MOSFET with 3-nm HfO_2

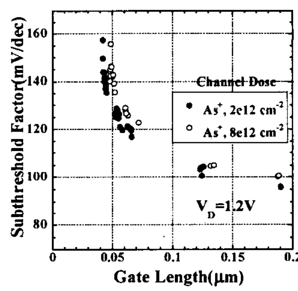

Fig.12 Subthreshold factor roll-up for p-MOSFET with 3-nm HfO_2

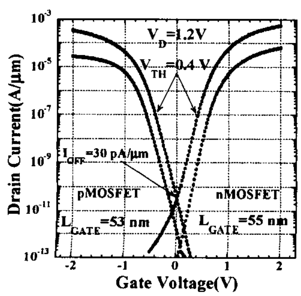

Fig.13 Drain current – gate voltage characteristics for n- and p-MOSFETs with 3-nm HfO_2

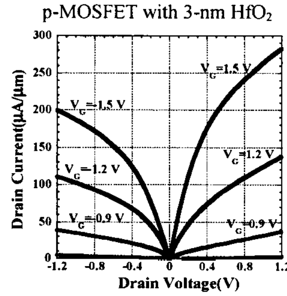

Fig. 14 Drain current – drain voltage characteristics for n- and p-MOSFETs with 3-nm HfO_2

	nMOSFET	pMOSFET
Gate Length (nm)	55	55
HfO_2 Physical Thickness (nm)	3	3
Gate Leakage (A/cm²)	0.2m	0.5m
T_{OX} in Inversion (nm)	2.3	2.9
Off-State Current (pA/μm)	25	25
Saturation Current (μA/μm)	140	110

Table 1 Summary of device results for supply voltage of 1.2V