

Stress Memorization Technique (SMT) by Selectively Strained-Nitride Capping for Sub-65nm High-Performance Strained-Si Device Application

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Abstract

An advanced stress memorization technique (SMT) for device performance enhancement is presented. A high-tensile nitride layer is selectively deposited on the n+ poly-Si gate electrode as a stressor with poly amorphization implantation in advance. And, this high-tensile nitride capping layer will be removed after the poly and S/D activation procedures. The stress modulation effect was found to be enhanced and memorized to affect the channel stress underneath the re-crystallized poly-Si gate electrode after this nitride layer removal. More than 15% current drivability improvement was obtained on NMOS without any cost of PMOS degradation. Combining the high tensile nitride sealing layer deposition after silicide process, it was found to gain additional ~10% improvement to NMOS. The device integrity and reliability were verified with no deterioration by this simple and compatible SMT process, which is a promising local strain approach for sub-65nm CMOS application.

Keywords: SMT, Nitride, Stress, Strained-Si

Introduction

Channel stress control has become a critical technique for electron and hole mobility improvements as down scaling the device dimension. Strained-Si device on SiGe substrate or selective SiGe epitaxy technique [1,2] has been reported to obtain significant on-state current improvement. However, this state-of-the-art process leads the barrier ahead to implement it into the real production. A locally strained channel technique has been reported to modify the poly-Si gate electrode stress by using CVD SiO₂ as capping layer to improve device performance [3]. In addition, recent studies of high tensile capping layer on top of the silicide have demonstrated the NMOSFET driving current improvement capability, but with the PMOS performance degradation [4,5]. Selective implantation was recommended to achieve the capping layer stress relief on top of PMOS portion. However, this implantation step will seriously damage the capping layer quality and results in the risk of reliability worsen [5]. In this paper, we proposed a novel stress memorized technique (SMT) to improve the device performance without PMOS degradation. A high tensile nitride capping layer acts as a temporary stressor to effectively modulate the channel stress. The stress effect is then enhanced and memorized by well-controlled poly amorphization and re-crystallization procedures. This high tensile nitride capping layer will be removed after the annealing step. Therefore, a much thicker capping layer can be used to increase the stress level without any process limitation to impact the subsequent gap filling process steps.

Channel Stress Control by SMT

The process sequence of SMT is illustrated in Fig.1. After the spacer and source/drain formation, a Poly Amorphization Implantation (PAI) of Si gate electrode by Ge is performed in NMOS. The low-temperature and high tensile (>1.5G Pa) Nitride film is deposited as Activation Capping Layer (SiN_{ACL}) to modulate the channel stress. As shown in Fig. 2, the STI and oxidation-induced channel compressive stress can be effectively reduced by this tensile ACL. The selective removal of SiN_{ACL} on PMOS was performed to alleviate the stress-induced device degradation. Poly and source/drain activation were followed by ACL selective removal step. The photographs of poly gate electrode before and after activation are shown in Fig. 3(a) and (b), respectively. The ACL layer located on the NMOS portion area was stripped after the activation steps. The tensile stress is thought to be transferred to the area of NMOS channel underneath of poly through this ACL. After the silicide formation, the low temperature, high-tensile Nitride film is deposited as Contact-Etch-Stop-Layer

(SiN_{CESL}) to add up the stress effect. Finally, the metallization is done for device characterization.

SMT Effects on Device Performance

Figure 4 shows the Ion vs Ioff characteristics of SMT device with different PAI condition compared with the control. Significant improvement is achieved in SMT devices with tensile SiN_{ACL} and PAI. The stress enhanced mobility improvement can be largely increased by high dose PAI. The driving current improvement ranges from 3~11% depending on the PAI condition. The thickness dependence of SiN_{ACL} on drivability is illustrated in Fig.5. Due to the stress enhancement, the improvement can be further increased up to 15% by increasing the nitride thickness. The driving current improvement through the PAI, tensile ACL and ACL thickness effects clearly illustrate that the stress memorization effect is achieved by this temporary stress promoter. Compared to the complicated strain substrate or selective epi SiGe process, this SMT approach shows the benefits of low cost and low risk of reliability. No PMOS performance degradation is achieved through the selective SiN_{ACL} removal prior to the activation annealing, as shown in Fig. 6. Figure 7 shows the Ion vs. Ioff characteristics of SMT device combing the SiN_{ACL} and SiN_{CESL}. Additional 9% current drivability improvement is obtained when combing this tensile CESL into SMT device. The additional improvement indicates that the stress effect can be effectively accumulated to further enhance carrier mobility. As shown in Fig. 8, SMT devices with SiN_{ACL} and SiN_{CESL} show excellent subthreshold characteristics and significant transconductance improvement, which can be contributed to the carrier mobility enhancement by channel stress modulation. Figure 9 shows the drain current improvement dependence on channel stress. Increasing the tensile stress and thickness can increase the channel tensile strain (or less compressive) and results in an increased drain current.

Device Integrity and Reliability

Figure 10 shows the CV curves of the control and SMT devices. The inversion capacitances are almost the same when using SiN_{ACL} and SiN_{CESL}. It indicates that the thermal budget and stress effect of the SMT process do not impact the poly dopant diffusion and de-activation. In addition, the SMT process induced strains do not adversely affect the gate leakage current and junction leakage, as illustrated in Fig.11 and Fig.12, respectively. In Fig. 13, both core and I/O device with SiN_{ACL} show comparable NMOS hot carrier reliability to the control. No reliability concern is observed in PMOS with selectively SiN_{ACL} removal approach. Figure 14 demonstrates that the device with SiN_{CESL} has no negative impacts on the hot carrier lifetime and the negative bias temperature instability even in severe criteria of 1% cumulated failure.

Conclusion

A simple and manufacturable SMT process is proposed for strained-Si device. By combing the PAI, strained nitride capping and the subsequent activation anneal, the stress modulation effect is efficiently enhanced and memorized through the poly re-crystallization. Significant drain current improvement is obtained depending on the PAI condition and SiN_{ACL} stress level. Up to 15% current gain has been demonstrated by SMT process optimization. The improvement gain can further add up ~10% by combing subsequent low-temperature high-tensile SiN_{CESL}. In addition, no adversely impacts are observed on device integrity, hot carrier and NBTI reliability. Therefore, the production-worthy SMT process is very promising for sub-65nm CMOS Application.

Acknowledgement

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Reference

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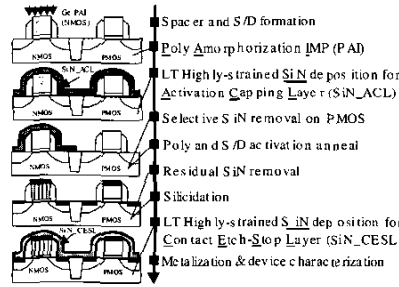


Fig.1 Process sequence of Stress Memorization Technique (SMT).

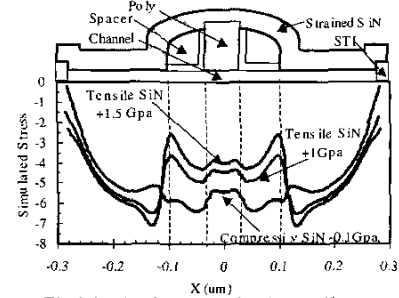


Fig.2 Strained SiN capping layer effect on channel stress distribution (simulation)

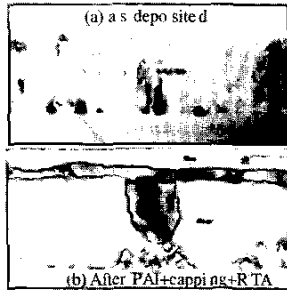


Fig.3 TEM pictures of poly-Si film (a) before and (b) after activation anneal

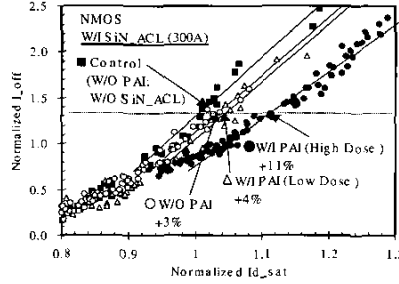


Fig.4 PAI effect on Ion-Ioff curve. Significant improvement is achieved in SMT device with SiN_ACL and high dose PAI

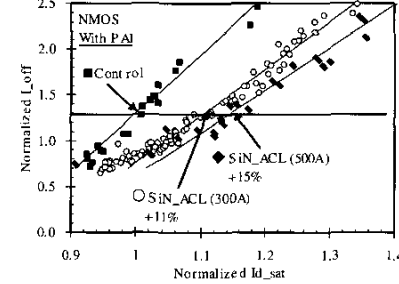


Fig.5 Ion vs. Ioff curves. Improvement increases with increasing thickness of SiN_ACL.

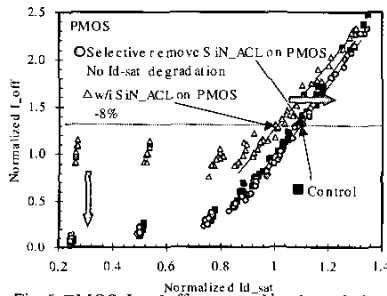


Fig.6 PMOS Ion-Ioff curves. No degradation is observed when selectively remove SiN_ACL on PMOS before RTA.

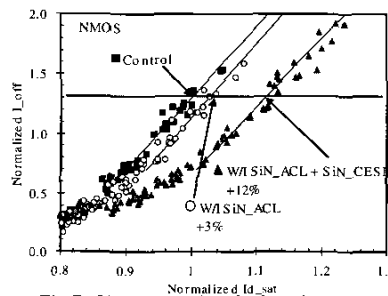


Fig.7 Id-sat can be further improved by combining SiN_CESL into SMT device with SiN_ACL

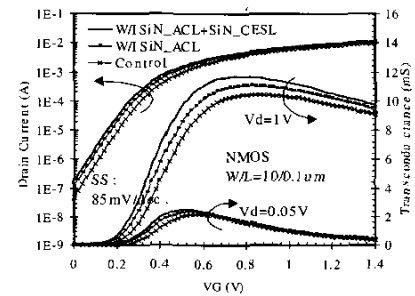


Fig.8 SMT devices exhibit excellent subthreshold characteristics and significant improved transconductance.

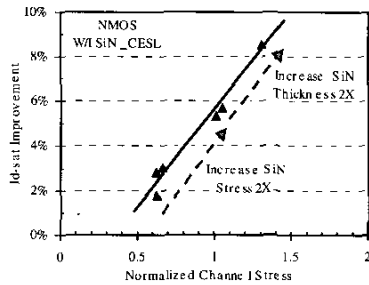


Fig.9 Id-sat Improvement increases with increasing SiN film stress and thickness

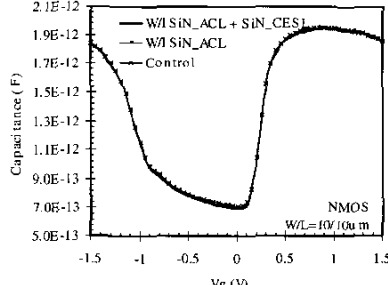


Fig.10 CV curves of control and SMT devices. The inversion capacitance are almost the same

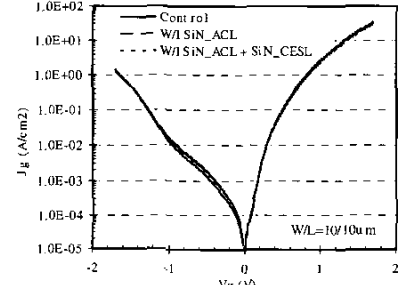


Fig.11 gate leakage current is not adversely affected by SiN_ACL and SiN_CESL

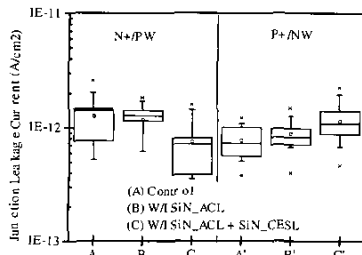


Fig.12 SMT devices show no obvious impacts on junction leakage current

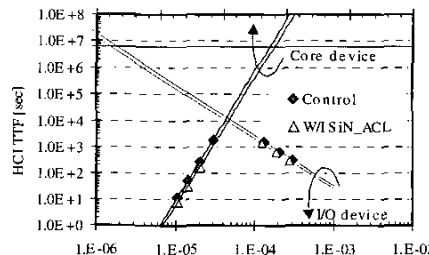


Fig.13 SMT device with SiN_ACL shows little impact on core and I/O HCI reliability

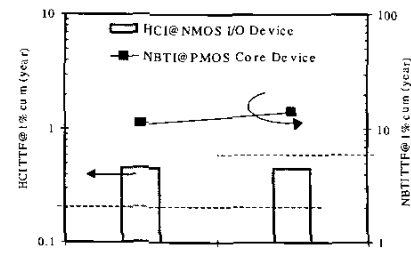


Fig.14 NMOS HCI and PMOS NBTI reliability of device with SiN_CESL are not degraded.