UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNITED MICROELECTRONICS CORPORATION,
AND
UMC GROUP (USA),
Petitioners,
v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,
Patent Owner.

U.S. PATENT NO. 8,587,076

Case IPR2025-01093

DECLARATION OF DR. SANJAY BANERJEE IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,587,076

UMC Ex.1101

TABLE OF CONTENTS

Page

I, Dr. Sanjay Banerjee, declare as follows:

1. My name is Sanjay Banerjee.

2. I have been retained as an expert witness on behalf of United Microelectronics Corporation and UMC Group (USA) (collectively, "Petitioner") for the above-captioned Petition for *Inter Partes* Review ("IPR") ("Petition") of U.S. Patent No. 8,587,076 ("the '076 patent") (Ex.1001). I am being compensated for my time in connection with this Petition at my standard consulting rate of $675 per hour. My compensation is not affected by the outcome of, or my testimony in, this IPR, or any litigation proceedings. I am informed that the assignee for the patent in the present proceeding is Advanced Integrated Circuit Process LLC ("Patent Owner"). I am also informed that the Petition names United Microelectronics Corporation and UMC Group (USA) as real-parties-in-interest.

3. I have been asked to provide my opinions regarding whether claims 1, 2, 3, 6, 7, 8, 10, 11, 12, and 13 of the '076 patent (the "Challenged Claims") are invalid as anticipated, or as obvious to a person having ordinary skill in the art at the time of the alleged invention of the '076 patent ("POSITA").

4. The '076 patent issued on November 19, 2013, from U.S. Patent Application No. 13/547,913, filed on July 12, 2012. The '076 patent claims priority to Japan Application No. 2005-227457, filed on August 5, 2005.

5. I am not currently, and have not at any time in the past been, an employee of any Petitioner or any real-party-in-interest. Other than set out above, I have no affiliation, contractual connection, or financial connection with any Petitioner or any real-party-in-interest, or any of their respective subsidiaries or parents. I similarly have no financial interest in, or affiliation with the Patent Owner.

I. BACKGROUND AND QUALIFICATIONS

6. I am currently the Cockrell Family Chair Professor of Electrical and Computer Engineering at the University of Texas at Austin. At UT Austin, I was also the director of the Microelectronics Research Center from September 1999 through January 2025. I have been a faculty member at UT Austin since 1987.

7. I have also been active in industries related to the relevant field of art. As a Member of the Technical Staff, Corporate Research, Development and Engineering of Texas Instruments Incorporated from 1983–1987, I worked on polysilicon transistors and dynamic random access trench memory cells used by Texas Instruments in the world's first 4-Megabit DRAM, for which I was co-recipient of the Best Paper Award, IEEE International Solid State Circuits Conference, 1986.

8. I received a B. Tech. degree from the Indian Institute of Technology, Kharagpur, and M.S. and Ph.D. degrees from the University of Illinois at Urbana-Champaign, all in Electrical Engineering.

9. I am a leading researcher and educator in various areas of transistor device fabrication technology, including the fabrication, characterization and application of memory devices, transistors, and nanotechnology. My research has been funded by the Texas Advanced Technology Program (ATP), the Texas Higher Education Coordinating Board, the National Science Foundation, the SEMATECH (Semiconductor Manufacturing Technology) consortium, the SRC (Semiconductor Research Corporation) consortium, DARPA, and the Department of Energy, among others.

10. At the University of Texas, I served as the director of the South West Academy of Nanoelectronics from its inception through the end (2006 - 2017), one of three centers in the United States established to develop a replacement for MOSFETs.

11. I have published over 1,200 technical articles, many related to semiconductor fabrication technology, most at highly competitive refereed conferences and rigorously reviewed journals. I have also published 8 books or chapters on transistor device physics and fabrication, and have supervised over 80 Ph.D. and 60 MS students.

12. I have been a member of scientific organizations and committees, including the IEEE Dan Noble Award Committee from 2010–2013, serving as Chair from 2012–2013, the International Technology Roadmap for Semiconductors, the

International Conference on MEMS (Microelectromechanical Systems) and Nanotechnology, the IEEE International Conference on Communications, Computers, Devices, the International Electron Devices Meeting, the International Conference on Simulation of Semiconductor Processes and Devices, and the IEEE Symposium on VLSI (Very-Large-Scale Integration) Technology. I have served as the Session Chair for the "Device Technology" Session conducted at the IEEE International Electron Devices Meeting in 1989–1990. I have also served as the General Chairman for the IEEE University Government Industry Microelectronics Symposium in 1994–1995, and Chair of the IEEE Device Research Conference.

13. I have served on the Technical Advisory Boards of AstroWatt, DSM Semiconductors, Cambrios, Nanocoolers Inc., BeSang Memories, Organic ID and ITU Ventures; Gerson Lehmann Group, NY; Austin Community College; Asia Pacific IIT; Rochester Institute of Technology, and HSMC Foundry.

14. I received the Engineering Foundation Advisory Council Halliburton Award (1991), the Texas Atomic Energy Fellowship (1990–1997), Cullen Professorship (1997–2001) and the Hocott Research Award from UT Austin (2007). I also received the SIA/SRC University Researcher Award (2018), IEEE Grove Award (2014), Distinguished Alumnus Award, IIT (2005), Industrial R&D 100 Award (2004), ECS Callinan Award, 2003, IEEE Millennium Medal, 2000, NSF Presidential Young Investigator Award in 1988, and several SRC Inventor

Recognition and Best Paper Awards. I was a Distinguished Lecturer for IEEE Electron Devices Society, and am a Fellow of the Institute of the Electrical and Electronics Engineers (IEEE), the American Physical Society (APS) and the American Association for the Advancement of Science (AAAS).

15. I am the inventor or co-inventor of over 35 United States patents in various areas of transistor device fabrication technology. I was elected a Fellow of the National Academy of Inventors in 2021.

16. My qualifications and publications are set forth more fully in my curriculum vitae, attached as Ex.1102.

II. MATERIALS AND OTHER INFORMATION CONSIDERED

17. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art and have considered the viewpoint of a POSITA at the time of the alleged invention.

18. I have considered the materials referenced herein, including the ’076 patent (Ex.1001), the file history of the ’076 patent (Ex.1002), the parent and related applications, the file histories of the parent and related applications, the Petition, and other documents listed in the Exhibit List of the Petition, including:

Description	Date of Availability
U.S. Application Publication No. 2002/0063299 to Kamata, et al. (“Kamata”; Ex.1027)	Published May 30, 2002

Description	Date of Availability
Sim, J. H., et al., "Effects of ALD HfO_2 thickness on charge trapping and mobility," Microelectronic Engineering, Vol. 80, pp. 218-221, June 17, 2005 ("Sim"; Ex.1024)	Published June 17, 2005
U.S. Application Publication No. 2006/0091432 to Guha, et al. ("Guha"; Ex.1028)	Filed November 2, 2004
U.S. Application Publication No. 2003/0025135 to Matsumoto, et al. ("Matsumoto"; Ex.1009)	Published February 6, 2003
U.S. Patent 6,504,214 to Yu, et al. ("Yu"; Ex.1048)	Issued January 7, 2003
Koyama, M., et al., "Effects of Nitrogen in HfSiON Gate Dielectric on the Electrical and Thermal Characteristics," Digest of International Electron Devices Meeting, pp. 849-852, Dec. 8-11, 2002 ("Koyama"; Ex.1029)	Published December 8-11, 2002
U.S. Application Publication No. 2005/0051856 to Ono, et al. ("Ono"; Ex.1013)	Published March 10, 2005

19. It is my understanding that the references listed above are prior art to the '076 patent, which is entitled to a priority date not earlier than August 5, 2005. Kamata, Sim, Guha, Matsumoto, Yu, Koyama, and Ono (Exs. 1027, 1024, 1028, 1009, 1048, 1029, and 1013, respectively) were not discussed during the prosecution of the '076 patent.

III. UNDERSTANDING OF PATENT LAW

20. I am not an attorney. For purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law is as listed below.

A. Claim Construction

21. I understand that in an IPR petition filed after November 13, 2018, a claim must be construed under the *Phillips* standard. Under that standard, words of a claim are given their plain and ordinary meaning as understood by a POSITA at the time of invention, in light of the specification and prosecution history, unless those sources show an intent to depart from such meaning, as well as pertinent evidence extrinsic to the patent.

22. I have applied this understanding in my declaration. I do not believe any claim terms require explicit construction in this proceeding to resolve the patentability of the Challenged Claims.

B. Anticipation and Obviousness

23. I have been informed that a patent claim is anticipated if a single prior art reference, such as a patent or a publication, discloses all the limitations of the claimed invention.

24. I have been informed and understand that a patent claim can be considered to have been obvious to a POSITA at the time the application was filed.

This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a POSITA at the time the application was filed. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

25. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to a POSITA. In determining whether a combination based on either a single reference or multiple references would have been obvious, I have been informed that it is appropriate to consider at least the following factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;

- whether a POSITA could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed limitations represent one of a limited number of known design choices, and would have a reasonable expectation of success by a POSITA;
- whether a POSITA would have recognized a reason to combine known limitations in the manner described in the claim;
- whether there is some teaching or suggestion in the prior art to make the modification or combination of limitations claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

26. I understand that a POSITA has ordinary creativity and is not an automaton.

27. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

28. I understand that prior art to the ’076 patent for purposes of my opinion herein includes patents and printed publications in the relevant art that predate the priority date of the ’076 patent.

29. I understand that certain factors—often called “secondary considerations”—may support or rebut an assertion of obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the alleged invention, skepticism of those having ordinary skill in the art at the time of the alleged invention, unexpected results of the alleged invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field.

30. I further understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

IV. SUMMARY OF OPINIONS

31. It is my opinion that claims 1-3, 7-8, and 10-13 are obvious in view of Kamata (Ground I).

32. It is my opinion that claim 6 is obvious in view of Kamata and Sim (Ground II).

33. It is my opinion that claims 1-3, 7-8, and 10-13 are obvious in view of Guha (Ground III).

34. It is my opinion that claim 6 is obvious in view of Guha and Sim (Ground IV).

35. It is my opinion that claims 1-3, 7, 8, 10, and 13 are obvious in view of Matsumoto and Yu (Ground V).

36. It is my opinion that claim 6 is obvious in view of Matsumoto, Yu, and Sim (Ground VI).

37. It is my opinion that claim 1 is obvious in view of Matsumoto and Koyama (Ground VII).

38. It is my opinion that claims 1, 11, and 12 are obvious in view of Matsumoto and Ono (Ground VIII).

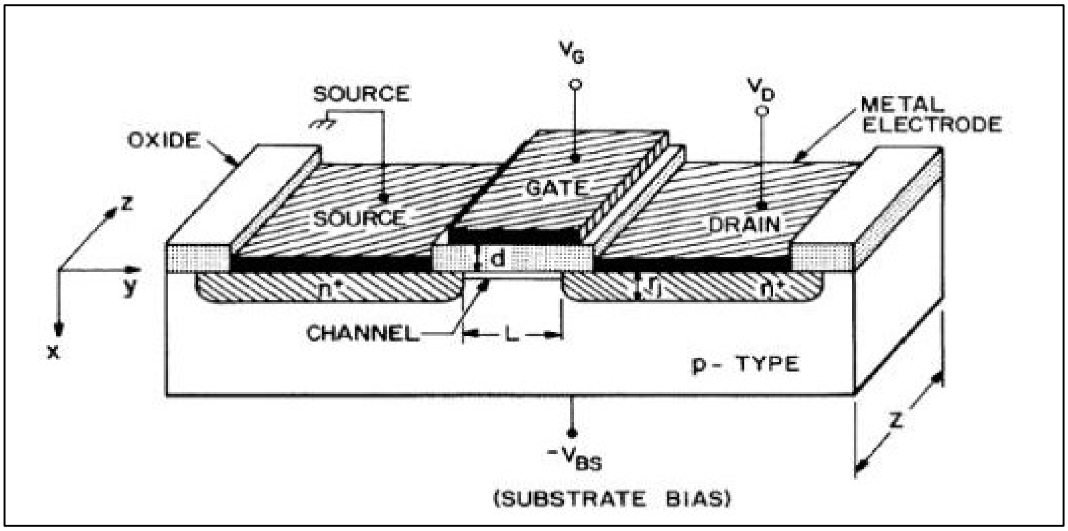
V. OVERVIEW OF THE TECHNOLOGY

39. Broadly speaking, a semiconductor device is an electrical device made of semiconductor material like silicon or germanium. This includes many types of

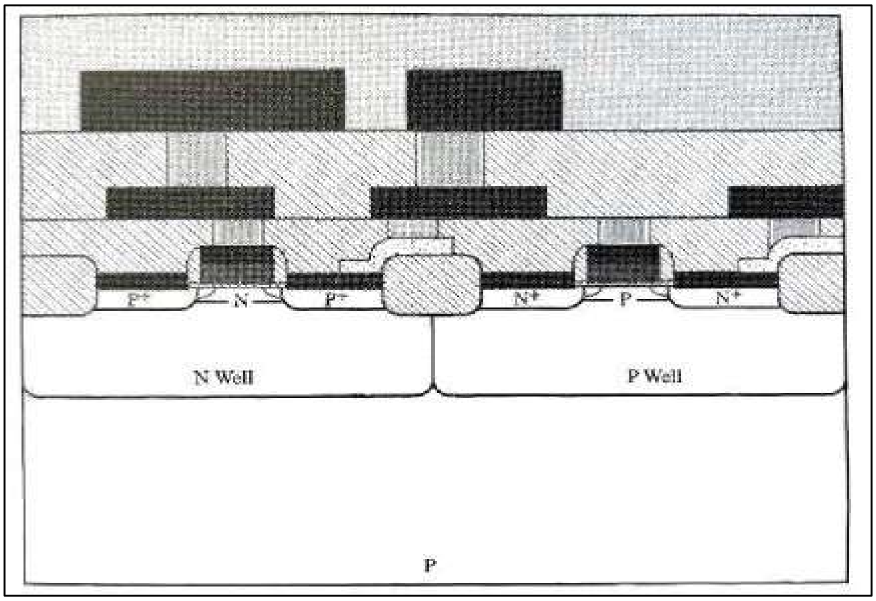
devices like light-emitting diodes (LEDs) and metal oxide semiconductor (MOS) transistors. Field effect transistors are just one type of semiconductor devices and have been in commercial use for decades, as discussed in more detail below.

A. MISFET/MOSFET

40. A metal insulating semiconductor field-effect transistor (MISFET), commonly referred to as a metal oxide semiconductor field-effect transistor (MOSFET) if the insulator is an oxide, is a transistor that switches from an OFF state to an ON state when a voltage greater than the threshold voltage is applied to a gate terminal. In the ON, or active state, current flows from a source to a drain through a channel region. For the transistor types at issue in this IPR, the channel region is located under the gate electrode (which can be made of stacked metal layers) and the gate insulating layer (often called a gate oxide or gate dielectric), and between the source and drain. Sze-1981, Ex.1413, 433-34, Fig. 3 (below); Plummer, Ex.1215, 71-76, Figs. 1-11 (further below).



Sze-1981, Ex.1413, Fig. 3



Plummer, Ex.1215, Fig. 1-11

41. MOSFETs are characterized by the material used in the source and drain. A MOSFET with source/drain regions made from “p-type” material is known as a PMOS or p-FET, while a MOSFET with source/drain regions made from “n-type” material is known as a NMOS or n-FET. Thus, MOSFETs generally include a

gate electrode, a gate insulating layer, and "the silicon wafer, also called the substrate, body or bulk." Weste, Ex.1212, 8. An nMOS transistor "is built with a p-type body and has regions of n-type semiconductor adjacent to the gate called the source and drain." *Id.*, 8 (emphasis omitted), FIG. 1.8(a). A pMOS transistor "is just the opposite, consisting of p-type source and drain regions with an n-type body." *Id.*

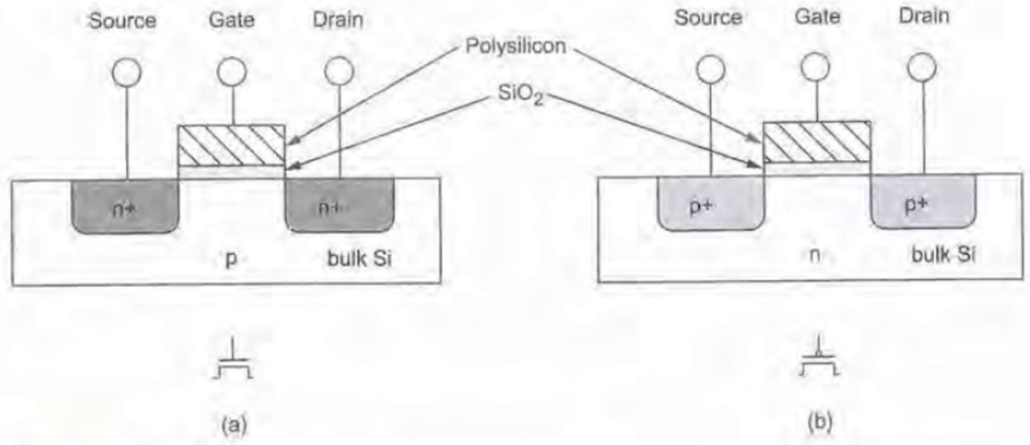


FIG 1.8 nMOS transistor (a) and pMOS transistor (b)

Weste, Ex.1212, FIG. 1.8(b) (above, right)

42. In the mid-1980s, complementary MOS (CMOS) devices became popular, which have both PMOS (p-FET) and NMOS (n-FET) transistors on the same substrate or integrated circuit (IC). In such devices, the active areas (and associated transistors) are generally formed in regions called "wells," and a transistor can even have more than one well, as seen below. *See* Weste, Ex.1212, 117-118, FIG. 3.2 (below).

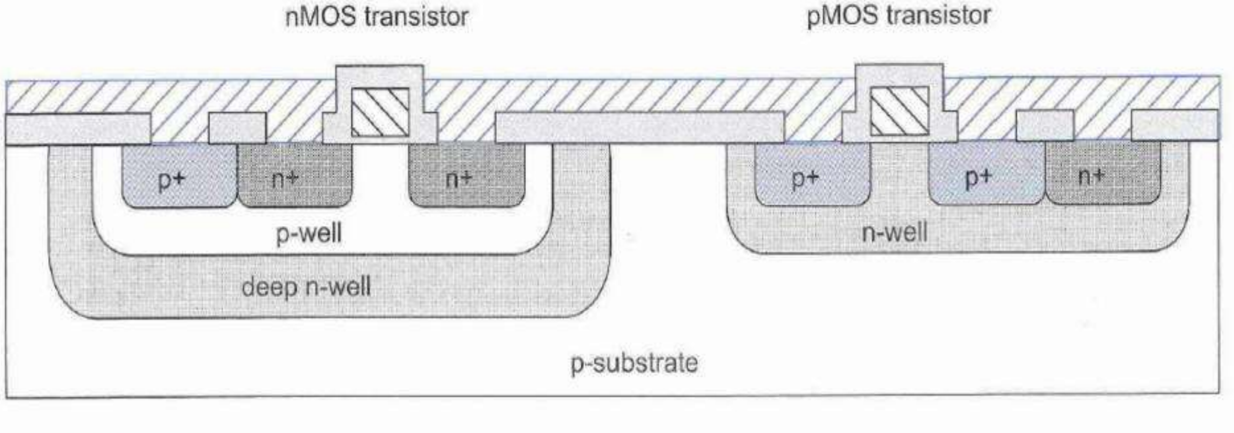


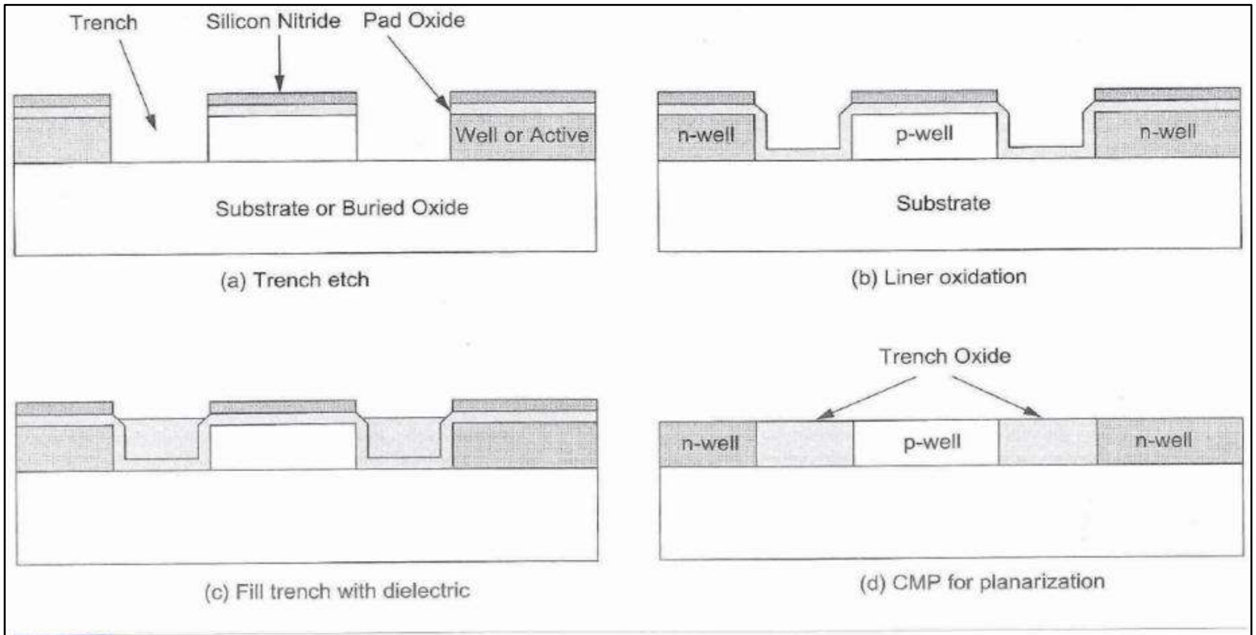
FIG 3.2 Well structure in triple-well process

Weste, Ex.1212, Fig. 3.2

43. Impurities known as "dopants" are added to the active areas and wells to add charge carriers and tailor the electrical properties of these regions, such as their conductivity. The wells have opposite dopant types to the dopants of the source/drain. As such, an n-FET is formed in a p-well, and a p-FET is formed in an n-well. *See* Weste, Ex.1212, 8, FIG. 1.8(b).

44. With respect to dopants, charge carriers can be electrons (which are negatively charged) or holes (which are positively charged). When a region is doped with p-type dopants (like boron), the holes are majority carriers and the electrons are minority carriers. *See* Weste, Ex.1212, 7; Plummer, Ex.1215,, 17. When a region is doped with n-type dopants (like arsenic), the electrons are majority carriers and the holes are minority carriers. *See* Weste, Ex.1212, 7; Plummer, Ex.1215, 17 ("The electrons or holes are introduced on a one for one basis by the dopants.").

45. One issue with ICs relates to forming multiple devices on the same chip, and often it is necessary to isolate two structures from each other to ensure proper operation on the chip. One example of this isolation is forming a shallow trench isolation on the substrate between devices. *See* Weste, Ex.1212, 117. In the example below, a trench is etched between a p and n-well to form the shallow trench isolation. *Id.*, 119, Fig. 3.3 (below).



(a) Trench etch

(b) Liner oxidation

(c) Fill trench with dielectric

(d) CMP for planarization

FIG 3.3 Shallow trench isolation

Weste, Ex.1212, Fig. 3.3

46. Once the dopants are added, or implanted, into the silicon substrate, they need to be annealed, for example to repair the silicon crystal lattice from any damage caused by the dopant implantation. Plummer, Ex.1215, 81-82. “Because the ion implantation process creates damage, most dopants are not electrically active at the end of the implantation.” *Id.*, 470. A rapid thermal anneal, often at temperatures

over 1000 degrees Celsius, can activate the dopants and repair some of the damage done by implantation. *Id.*, 81. Annealing can also cause diffusion of the implanted dopants throughout the substrate (and in certain circumstances, other layers of the device). The interaction of the implanted dopants between the source/drain, the gate electrode and the gate insulating layer, and the channel were all well understood by a POSITA long before the priority date of the challenged patents. In fact, a POSITA would often use the various interactions of the manufacturing process, for example the shape of the source/drain after dopant implantation and annealing, to improve and optimize the performance of the semiconductor device, as discussed further below.

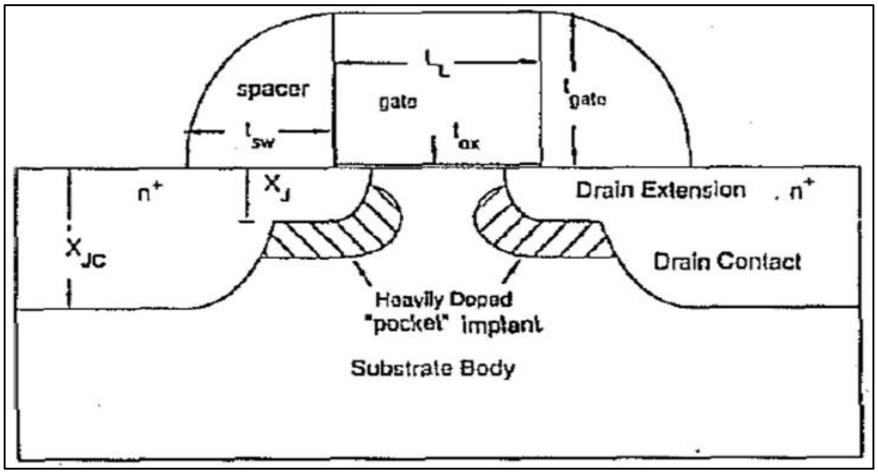
47. For example, varying the amount of dopants at different positions in the semiconductor device can have significant impacts on the device's performance. Where a source/drain may be heavily doped, other areas may only be lightly doped. As one example, the prior art has recognized that as transistors continue to scale down in size, using source and drain extensions may provide certain benefits, and these extensions can have varying dopant levels, including what are commonly referred to as lightly doped drain (LDD) and highly doped drain (HDD). Plummer, Ex.1215, 77; Rodder, Ex.1323, 2:61-62, 3:65-67.

48. Source/drain extensions were known to assist in suppressing short channel effects of scaled-down transistors by varying the dopants and having a

gradual transition in the electrical field between the source, the source extension, the channel, the drain extension, and the drain. Plummer, Ex.1215, 77-78 (using a LDD "allows the drain voltage to be dropped over larger distance than would be the case if an abrupt N^+P junction were formed" and even "modest reductions in the field strength obtained through the LDD structure can make a significant difference in device reliability").

49. As I discuss further below, sidewall structures placed on the edge of gate electrodes can serve many purposes, including to control the shape and position of source/drain extensions after annealing of the implanted dopants, as well as the overlap of the extension regions and the gate/gate insulating film. *See* Plummer, Ex.1215, 78.

50. As another example of varying dopants, the prior art also taught using pocket or halo implants to further mitigate the short channel effect as transistor sizes decreased. Pocket implants are placed below the channel region, as shown below. Wolf-4, Ex.1214, 219-20, Fig. 5-27 (below).



Wolf Vol. 4, Ex.1214, Fig. 5-27

51. In this example, the pocket implants are doped opposite of the source/drain and source/drain extension. Wolf-4, Ex.1214, 219 ("Precise control of the placement and dose of this implant within the transistor-structure is needed to obtain the intended enhancements.").

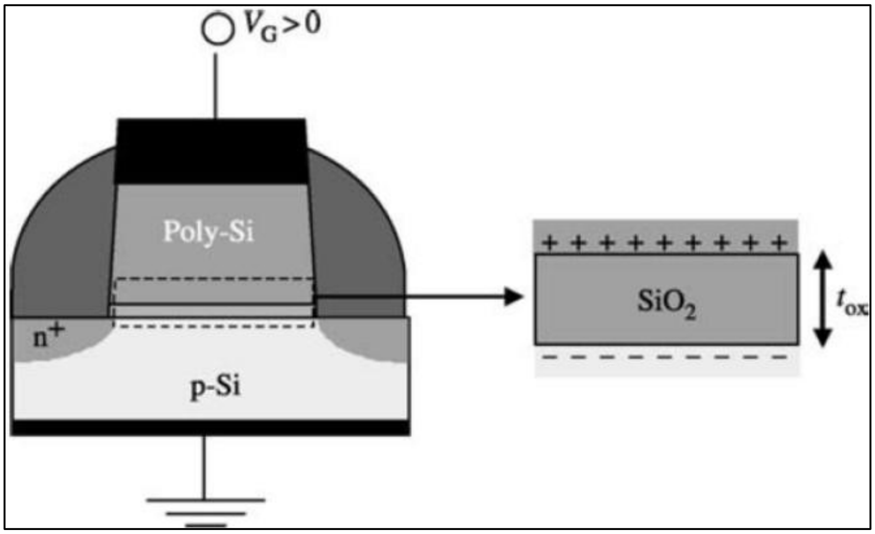
B. Gate Insulating Films & High-k Materials

52. The gate insulating film or gate dielectric isolates the gate electrode from the channel. Plummer, Ex.1215,, 288. Silicon dioxide was primarily used as the gate dielectric material for many years (*id.*, 53), but silicon dioxide films presented problems when reduced in thickness for smaller and smaller transistors. In particular, "in ultrathin SiO_2 gate layers (thickness typically below 3 nm) charge carriers can flow through the gate dielectric by quantum mechanical tunnelling mechanism." Houssa, Ex.1213, 5; *see also* Wolf-4, Ex.1214, 4-5.

53. The MOS transistor, from an electrical perspective, "behaves like parallel plate capacitor when gate voltage VG is applied to the gate charges on the metal are compensated by opposite charges in the semiconductor, these latter charges forming the channel connecting the source and the drain of the transistor as illustrated in figure 1.1.4." Houssa, Ex.1213, 8, Fig. 1.1.4 (below). The capacitance *C* can thus be represented by the following equation:

$$C = \frac{A\varepsilon_r\varepsilon_0}{t_{ox}} \qquad (1.1.1)$$

54. In this equation, "*A* is the capacitor area, ε_r the relative dielectric constant of the material (3.9 for SiO_2), ε_0 the permittivity of free space (8.85 x 10^{12} F m^{-1}) and t_{ox} the gate oxide thickness." Houssa, Ex.1213, 8. From this formula, the gate oxide thickness has an inverse relationship to capacitance: decreasing the gate oxide thickness increases the capacitance of the structure, with a corresponding "increase in the number of charges in the channel for a fixed value of VG." *Id.*



Houssa, Ex.1213, Fig. 1.1.4

55. In practical uses, however, problems occur when decreasing the gate oxide thickness of silicon dioxide past a certain point. Houssa, Ex.1213, 8. As one prior art textbook proposed, "[a]n alternative way of increasing the capacitance is to use an insulator with a higher relative dielectric constant than SiO_2 (it should be noticed that the relative dielectric constant is also represented by the letter k and one speaks about high-k materials)." *Id.*, 8-9. "One could then use a thicker gate layer and, hopefully, reduce the leakage current flowing through the structure and also improve the reliability of the gate dielectric." *Id.*

56. Equivalent oxide thickness (EOT) is one measure of high-k gate dielectrics. The EOT of a high-k material "is defined as the thickness of the SiO_2 layer that would be required to achieve the same capacitance density as the high-k

material in consideration" (Ex.1213, 9), which can be represented by the following equation:

$$\frac{t_{\text{eq}}}{\varepsilon_{\text{r,SiO}_2}} = \frac{t_{\text{high-}\kappa}}{\varepsilon_{\text{r,high-}\kappa}} \qquad (1.1.2)$$

57. In this equation, "$t_{\text{high-k}}$ and $\varepsilon_{\text{r,high-k}}$ are the thickness and relative dielectric constant of the high-k material, respectively." *Id*. In one example shown by Houssa, "using ZrO_2 as gate dielectric ($\varepsilon_r \approx 20$) would allow us to use a 5.1 nm thick layer in order to achieve a capacitance equivalent to a 1 nm thick SiO_2 layer; the equivalent oxide thickness of this ZrO_2 layer is thus 1 nm." *Id*.

58. But make no mistake, more than just a hope, the use of high-k gate dielectrics were a well-known, well-understood, and well-documented component to improve transistor performance as a substitute for silicon dioxide gate dielectrics, especially as transistors continued to decrease in size in the early 2000s. Long before 2005, numerous industry publications and other prior art readily recognized the advantages of using high-k materials as a gate dielectric.

59. In 2002, for example, numerous industry papers identified high-k materials, and hafnium oxide HfO_2 in particular, as a significant contributor to increased transistor performance. A paper by Rim et al. titled "Mobility Enhancement in Strained Si NMOSFETs with HfO_2 Gate Dielectrics" recognized that POSITAs had already been looking to high-k materials to solve known

problems: "[g]ate leakage reduction in ultra thin gate dielectric is the main motivation for the search of high-k materials." Rim-2002, Ex.1109, at Introduction; *see also id.*, Conclusion ("Strained Si NFETs with high-K dielectrics exhibit significantly enhanced NFET mobility, even over the universal mobility of the SiO_2/bulk Si devices, and hold the promise for the best trade-off between mobility and gate leakage reduction, which is especially attractive for low power, high performance CMOS technology."). Another article at the same industry conference concluded that "[h]igh-temperature FG annealing improved channel carrier mobility as well as subthreshold slopes in both N and PMOSFET with HfO_2 gate dielectrics," which are "advantageous in achieving large on current while suppressing off current, and give more flexibility in Vt adjustment." Onishi-2002, Ex.1107, Conclusion.

60. Yet another article at the same conference by Pidin et al., titled "Low Standby Power CMOS with HfO_2 Gate Oxide for 100-nm Generation," concluded that HfO_2 was particularly suited for low standby current applications. Pidin-2002, Ex.1108, Conclusion ("55-nm CMOS with 3-nm HfO_2 gate dielectric was fabricated using conventional process flow with high-temperature anneal of ≥1000°C and cobalt silicide. Gate current reduction of more than 3 orders of magnitude was achieved and low off-state current devices were obtained demonstrating very promising characteristics of HfO_2 for low standby current applications.").

61. But more than just the structure and use of high-k materials, the industry had already begun optimizing the process for making transistors with high-k gate dielectrics, with one article from the 2002 VLSI Symposium comparing two gate first approaches using HfO_2, one via physical vapor deposition and another via chemical vapor deposition. *See* Lee-2002, Ex.1105, Conclusion ("Compared with PVD TaN devices, the CVD TaN/HfO_2 devices exhibit lower leakage current and CV hysteresis, superior interface properties, higher transconductance, and superior effective electron and hole mobility.").

62. Numerous other prior art references recognized the ability of high-k gate dielectrics to make up for the shortcomings of too-thin silicon dioxide gate dielectrics. One article in the Journal of Applied Physics titled "High-k Gate Dielectrics: Current Status and Materials Properties Considerations" recognized that already by 2001 "much work has been done on high-k metal oxides as a means to provide a substantially thicker (physical thickness) dielectric for reduced leakage and improved gate capacitance." Wilk, Ex.1018, 5250; *see also* Wolf-4, Ex.1214, 146-47 ("The use of high-k dielectrics as the gate dielectric in submicron MOSFET structures also improves other device characteristics," including in threshold voltage Vt and in the subthreshold-swing St.").

63. For example, as shown by Figure 5 below in Wilk, using high-k materials in place of silicon dioxide for the gate dielectric improved both power consumption and gate leakage current.

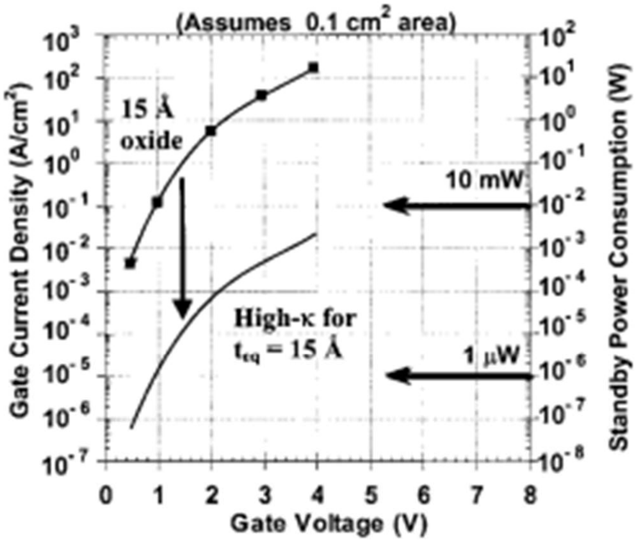
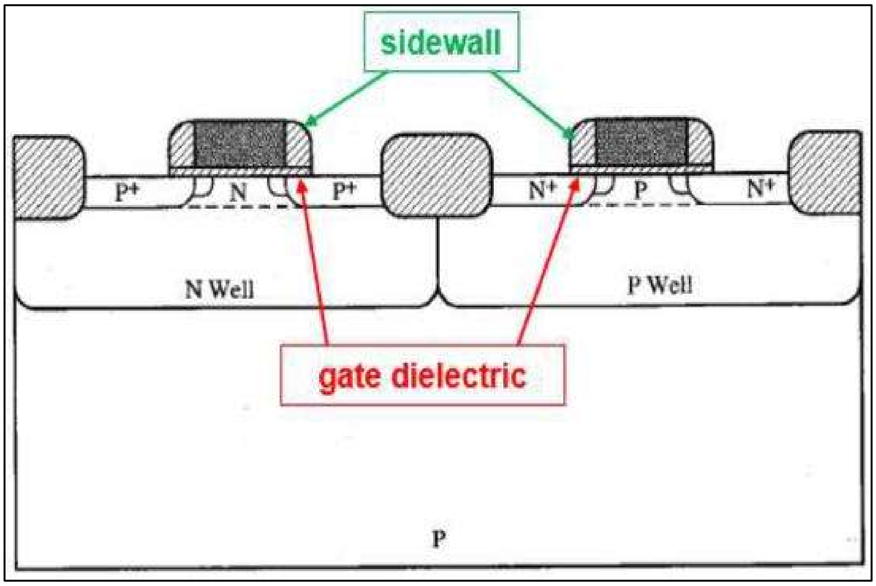


FIG. 5. Power consumption and gate leakage current density for a chip which has a 15 Å thick SiO_2 gate dielectric compared to the potential reduction in leakage current by an alternate dielectric exhibiting the same equivalent oxide thickness. Assumes at total gate area of 0.1 cm^2.

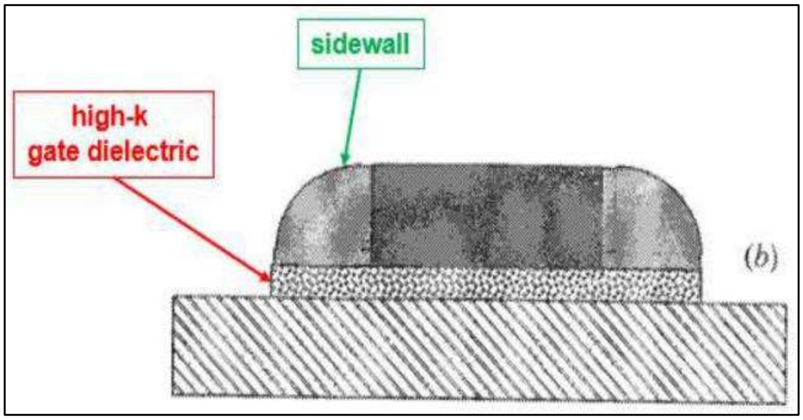
Wilk, Ex.1018, Fig. 5.

64. Not only did the prior art recognize the use of high-k materials as a substitute for silicon dioxide gate dielectrics, but the prior art also showed it was common to extend the gate dielectric out from underneath the gate electrode to underneath the sidewalls. For example, in Figure 2-34 below in Plummer, the gate dielectric is wider than the gate electrode.



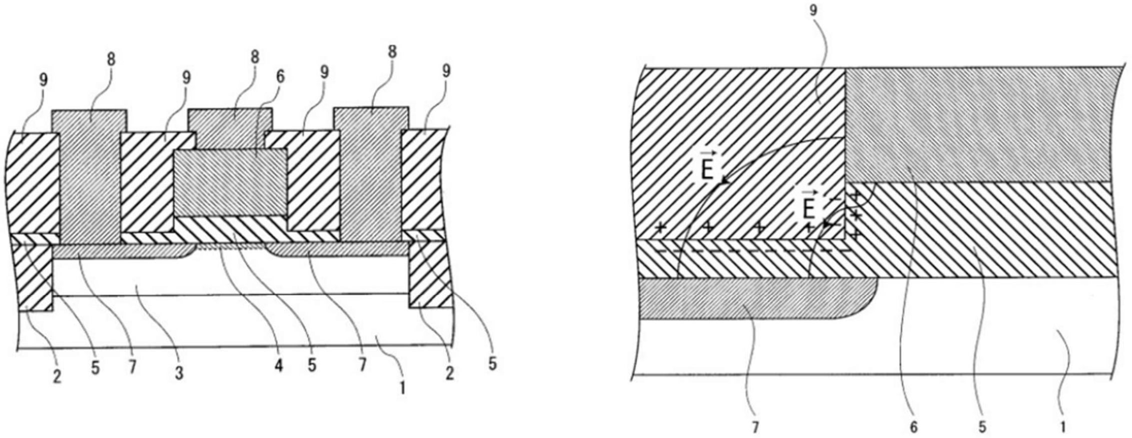
Plummer, Ex.1215, Fig. 2-34

65. As another textbook example, Houssa shows using HfO_2 as the high-k gate dielectric, with and without extending the gate dielectric underneath the sidewalls. Houssa explains that by extending the gate dielectric "with the approach of figure 5.1.9(b), the etch requirements are relaxed but they will require LDD implants through the high-k layer." Houssa, Ex.1213, 510, Fig. 5.1.9(b).



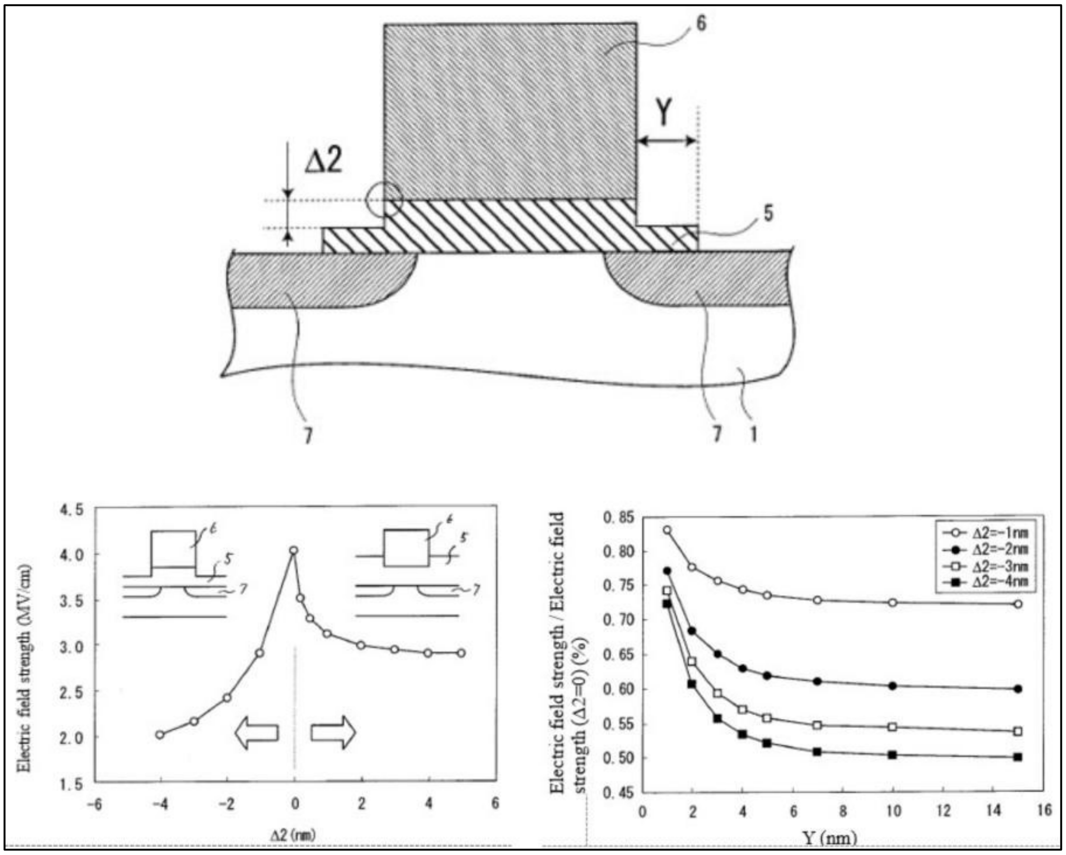
Houssa, Ex.1213, Fig. 5.1.9(b)

66. Japanese Publication No. 2005/064190 by Ono, et al. ("JP-Ono") published on March 11, 2005 and described some of the known benefits of expanding the high-k gate dielectric wider than the gate electrode, including that "protruding the gate insulating film outside the gate electrode during processing results in higher values of the electric field." JP-Ono, Ex.1340, ¶7. Further, JP-Ono suggests that extending the gate dielectric over the source/drain region, as well as reducing the thickness of the gate dielectric over the source/drain regions compared with under the gate electrode, "mitigate[s] the electric field at the lower end corner of the gate electrode 6" and "suppresses problems such as insulation breakdown and decreased reliability of the gate insulating film." *Id.*, Abstract. Specifically, JP-Ono detailed how thinning the gate dielectric over the source/drain region minimizes the electric field at the edge of the gate. *Id.*, ¶¶29-32, Fig.1-2.



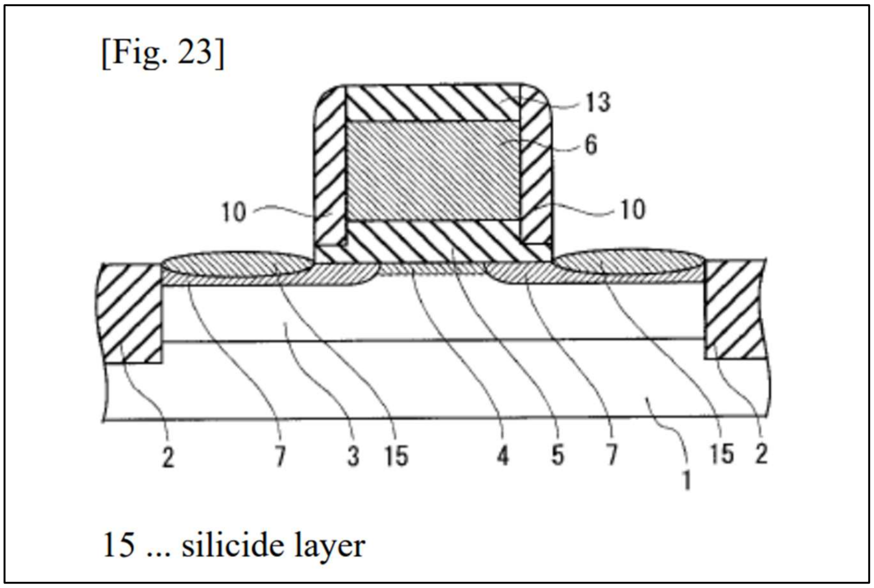
JP-Ono, Figures 1 (left), 2 (right)

67. Further, JP-Ono studied how varying the thickness and length of the gate dielectric over the source/drain regions affects the electric field distribution. Figure 4 shows that when the gate dielectric over the source/drain region is the same thickness as under the gate, e.g. at 0 Δ2, the electric field is strongest. JP-Ono, Ex.1340, ¶¶29-32, Fig.1-2. As the gate dielectric becomes thinner compared with under the gate electrode, e.g. when Δ2 is negative, the electric field weakens more than with a thicker gate dielectric, which favors a thinner dielectric over the source/drain regions. *Id.*, ¶35. Figure 24 further shows that the electric field is further reduced as the gate dielectric protrudes farther from the corner of the gate, i.e., as Y increases. *Id.*, ¶87.



JP-Ono, Figs. 3 (top), 4 (bottom-left), 24 (bottom-right)

68. These improvements are explicitly taught in a FET having a gate sidewall made of “materials like silicon oxide, silicon nitride, or silicon oxynitride,” as shown Figure 23 below. JP-Ono, Ex.1340, ¶83.

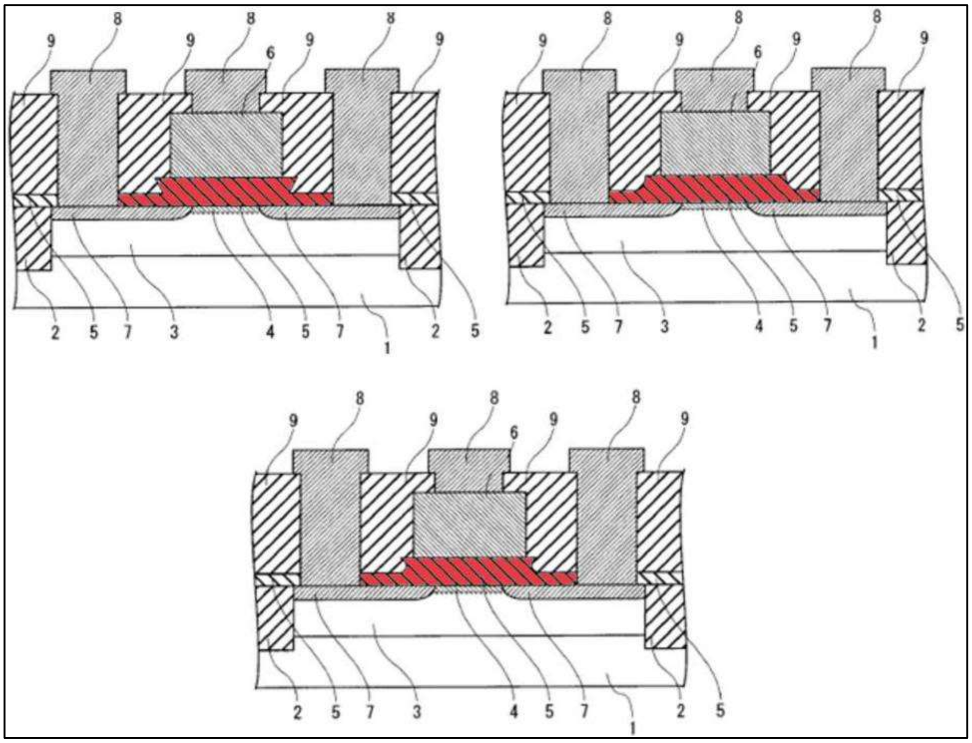


JP-Ono, Ex.1340, Fig. 23

69. Thus, JP-Ono teaches a POSITA the benefits of changing not only the location of the gate dielectric, e.g. outside the gate electrode, but also the shape of the gate dielectric, e.g. with thinner ends over the source/drain regions than underneath the gate electrode. In reference to Figure 23, JP-Ono explained that "it is not essential for the side of the gate insulating film 5 to be located inside or outside of the outer surface of the gate-side wall 10," but instead, the gate dielectric can be located both farther than the end of the sidewall, or closer than the end of the sidewall, with similar benefits. JP-Ono, Ex.1340, ¶83 ("Therefore, it is preferable that the side of the gate insulating film does not protrude too far outward [or inward] from the outer surface of the gate-side wall.").

70. JP-Ono demonstrated several different shapes for the protruding portions of the gate dielectric in Figures 36-44, as can be seen by some examples

below in red. JP-Ono, Ex.1340, Figs. 38, 41-42 (below). "By changing the shape of the gate insulating film near the lower corner of the gate electrode, as shown in the various examples here, it is possible to adjust the capacitance formed between the gate electrode 6 and the source-drain region 7, allowing for optimization." *Id.*, ¶108. Although shown without any sidewalls, JP-Ono explained that "gate-side wall 10 may be removed after processing the gate insulating film, or it may be left as it is." *Id.*, ¶103.



JP-Ono, Ex.1340, Figs. 38 (top-left), 41 (top-right), 42 (bottom)

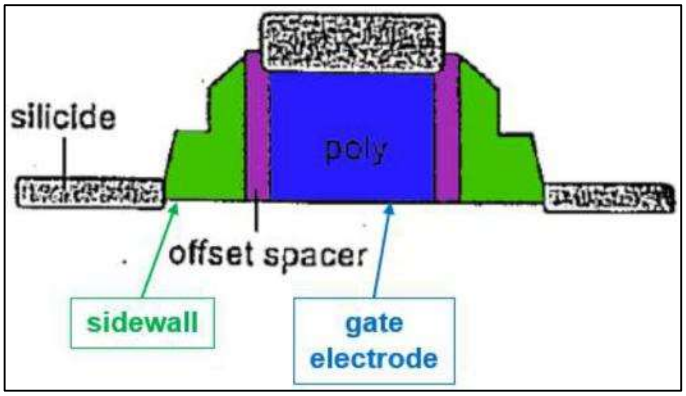
C. Sidewall Structures

71. Varying the sidewall structure on the sides of the gate electrode is another way a POSITA had to further optimize device performance in the prior art.

Sidewalls, also referred to as spacers or sidewall spacers, are formed on the side of the gate electrode for a variety of reasons. As discussed above, various sidewall structures may be used on the gate electrode to control the shape and position of source/drain extensions after annealing of the implanted dopants, as well as the overlap of the extension regions and the gate/gate insulating film. *See* Houssa, Ex.1213, 511; Weste, Ex.1212, 122; Wolf-4, Ex.1214, 9, 217, 219; Plummer, Ex.1215,, 78. Alternatively, sidewall spacers can prevent shorts between the source/drain and the gate, for example if the source/drain regions have silicide portions. Plummer, Ex.1215,, 742. These spacers are often made with silicon dioxide or silicon nitride, or combinations of multiple oxide and nitride layers. Houssa, Ex.1213, 511-12.

72. Varying the sidewall structure to control the source/drain extensions is one example of device optimization. As one textbook noted, "it has also been reported that the amount of overlap of the SDE-region with the gate-edge is also critical for optimum device performance." Wolf-4, Ex.1214, 217. As shown in Wolf's Figure 5-25 below, a POSITA knew that varying the size of the spacer at the gate electrode would affect formation of the source/drain extension and the resulting overlap with the gate edge: "an offset-spacer is fabricated on the side of the gate after the gate-poly is etched (but before the SDE implant step is carried out," with

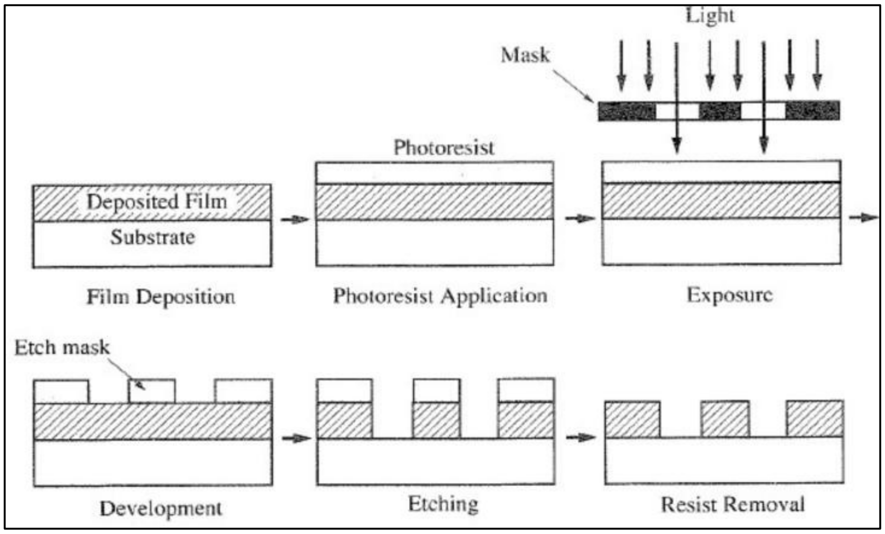
the spacer width "varied from zero (no-spacer) to some upper-bound (e.g., 50-nm)" to control gate overlap and optimize device performance. *Id.*



Wolf-4, Ex.1214, Fig. 5-25

D. Etching

73. The process of manufacturing a semiconductor device, particularly one with varying transistor structures, often involves a series of material deposition and etching, including by deposition of thin films with selective etching to pattern a desired structure. Plummer, Ex.1215,, 609-11. For example, a mask may be used in selective portions of a semiconductor device to "mask" or protect the underlying structure from further processing. As seen below, some areas may be masked while other areas are left unprotected such that a subsequent etching step etches the unmasked areas, while leaving the masked areas relatively intact. *Id.*, 609-10; Fig. 10-1.



Plummer, Ex.1215, Fig. 10-1

74. A POSITA can further optimize the structure of the semiconductor device by varying the etching process, as some processes are more selective than others. While the ideal etch profile "has perfectly straight sidewalls exactly under the edge of the mask," as seen above in Figure 10-1, in practice etching has both lateral and vertical components, as seen below in Figure 10-2.

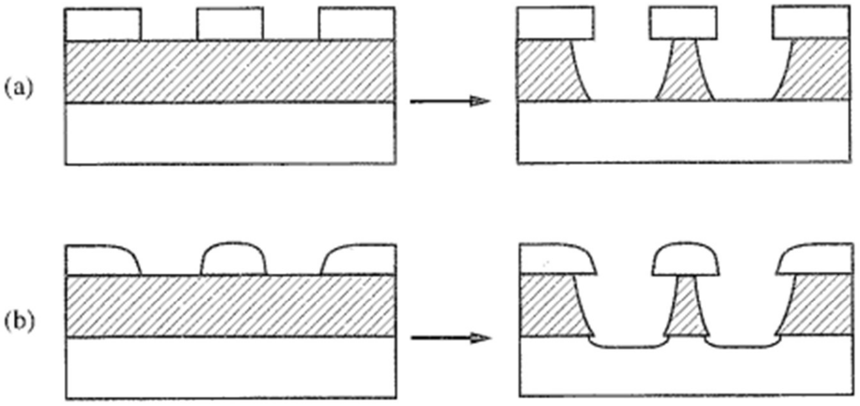
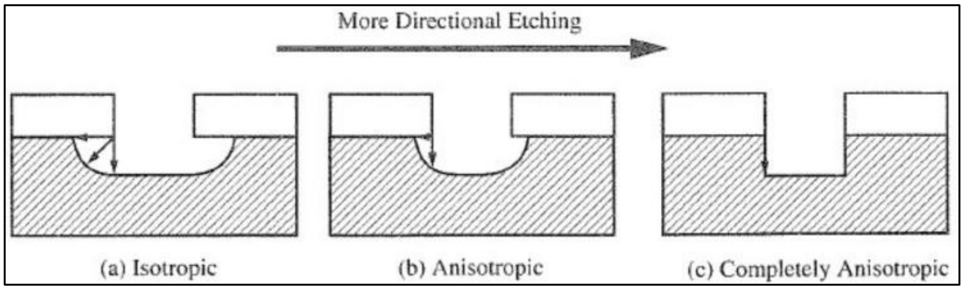


Figure 10-2 Actual etch profiles that can occur. (a) Lateral etching under mask. (b) Rounded photoresist which is further eroded during etching, leading to even more lateral etching. (b) also illustrates etch selectivity.

Plummer, Ex.1215, Fig. 10-2.

75. Etching is accomplished through both wet and dry processes, where wet etching often entails immersing the wafers in liquid like hydrofluoric acid to perform chemical etching, while dry etching uses plasma instead to etch material through both a physical and chemical process. Plummer, Ex.1215,, 609, 612.

76. Under certain circumstance, etching can also be targeted to etch directionally. Anisotropic etching, for instance, is considered a vertical etch with little to no etching in the lateral direction, while isotropic etching has more equal etching rates both vertically and laterally. Plummer, Ex.1215, 610-13. These differences can be seen below in Figure 10-3.



Plummer, Ex.1215, Fig. 10-3

Id., Fig. 10-3.

E. Replacement Metal Gate Stacks

77. While the industry recognized the benefits of high-k gate dielectrics, the prior art also recognized that using metal gates on top of high-k gate dielectrics further enhanced transistor performance, particularly as transistor sizes became smaller. When formed on top of high-k gate dielectrics like HfO_2, metal gate stacks addressed issues like Fermi-level pinning, eliminated polysilicon gate depletion, provided lower resistance, enhanced switching speeds, and improved overall transistor performance.

78. For example, a 2002 article by Samavedam et al. titled "Metal Gate MOSFETs with HfO_2 Gate Dielectric" recognized "[m]etal gates will eliminate gate depletion and address other issues like boron penetration and increased gate resistance, which will be aggravated as the poly gate thickness is scaled down."). Samavedam-2002, Ex.1110, Introduction; *see also id.*, Conclusion ("We have successfully fabricated and characterized HfO_2 n-MOSFETs with TaSiN and PVD

TIN gates and p-MOSFETs with CVD and PVD TiN gates using a conventional CMOS process. Metal-gated HfO_2 n-MOSFETs show a 10^4X gate leakage reduction compared to poly/SiO_2 devices. Reasonable Ion/Ioff performance and reliability were observed in PVD TiN/HfO_2 PMOS.”); *see also* Lee-2002, Ex.1105, Introduction (“As CMOS devices are scaled into sub-0.1 um regime, poly-depletion effects and boron penetration become significant concerns. Therefore, metal gate electrodes are being explored to replace the polysilicon gate.”). Just two years later, a 2004 article titled “55nm high mobility SiGe(:C) pMOSFETs with HfO_2 gate dielectric and TiN metal gate for advanced CMOS” concluded that “[f]or the first time, MOS transistors with compressively strained SiGe(:C) channel, metal gate and high-k dielectric are demonstrated down to 55nm gate length,” with significant improvements: “SiGe(:C) surface channel pMOSFETs with HfO_2 gate dielectric exhibit a 10^4 gate leakage reduction and a 65% mobility enhancement at high transverse effective field (1MV/cm) when compared to the universal SiO_2/Si reference.” Weber-2004, Ex.1111.

79. Other prior art references further recognized the problem of using polysilicon gates with high-k gate dielectrics specifically, or decreased transistor size in general. As gate dielectrics grew smaller consistent with transistor sizes, the polysilicon depletion effect worsened. Saito631, Ex.1518, 1:31-34; Hou, Ex.1519, 1:36-44. And where a high-k material is substituted for the silicon dioxide gate

dielectric with a polysilicon gate electrode, diffusion of the polysilicon dopants into the high-k material can cause a large threshold voltage offset. Colombo, Ex.1520, ¶5; Kavalieros277, Ex.1515, ¶3. As discussed above, metal gate stacks were considered the next step to address these problems. Saito631, Ex.1518, 1:31-34; Iriyama, Ex.1521, 1:28-34, 1:41-42; ITRS_FEP, Ex.1512, 2-3, 20; ITRS_PIDS, Ex.1216, 1, 3, 27, Fig. PIDS5.

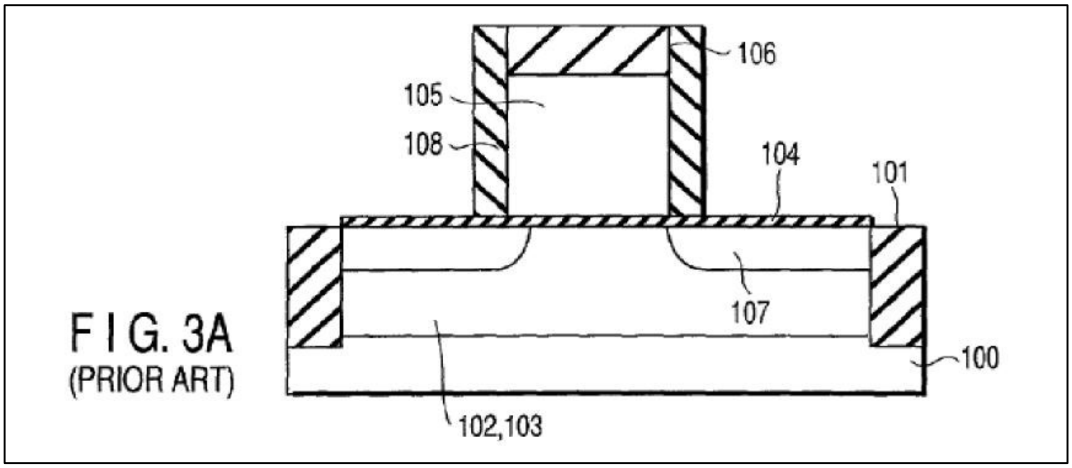
80. In particular, the prior art recognized that metal gates for PMOS and NMOS transistors would need separate metal gate stacks, and replacement metal gates (or gate-last processes) were well known to provide significant benefits compared with gate-first approaches. A material's "work function" is "the minimum energy required to bring an electron from the Fermi level to the vacuum level." Wolf-3, Ex.1229, 117. However, in MOS/MIS structures, the metal is in direct contact with a dielectric, not with the vacuum. Moreover, work functions of metal gates are highly dependent on material properties and interfaces. To differentiate this, an "effective work function" of the metal gate is commonly used to refer to the metal work function as measured (e.g., through the threshold voltage of the device).

81. In a CMOS device, PMOS transistors require a work function greater than about 4.8 eV, while NMOS transistors require a work function of less than about 4.6 eV. Hou, Ex.1519, 1:17-22; Colombo, Ex.1520, ¶¶20-21; ITRS_FEP, Ex.1512, Tbl. FEP4a ($|E_{c,v} – \varphi_m|$ (eV) < 0.2). Where the same polysilicon gate electrode can

be doped to adjust the work function for both NMOS and PMOS transistors, this is not the case for metal gates. Different metal gate stacks must be used. *See* Kavalieros277, Ex.1515, ¶3 ("When making a CMOS device that includes metal gate electrodes, it may be necessary to make the NMOS and PMOS gate electrodes from different materials.").

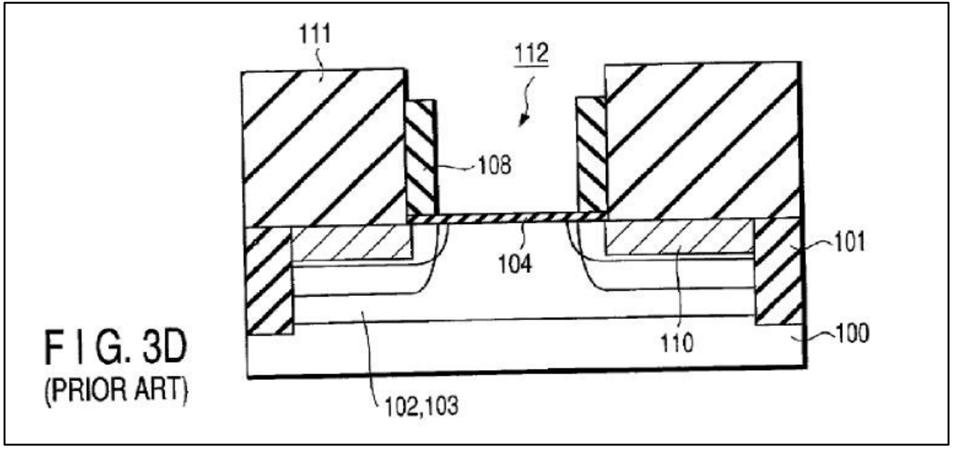
82. Some of the metals considered in the prior art for the PMOS metal gate stack showed less thermal stability than necessary, adversely affecting device performance when subjecting the metal to the high temperatures used to anneal the dopants in the source/drain regions. Hou, Ex.1519, 1:45-57; Iriyama, Ex.1521, 1:41-48.

83. One solution already considered by the prior art was replacement metal gates ("RMG"), which is a "gate-last" approach because a dummy gate is often manufactured first and then replaced by the metal gate. By making the metal gate last, the POSITA avoids subjecting the metal gate stacks to high temperatures during the source/drain annealing (because the annealing is done before placement of the metal gate). As seen below from one prior art reference, source/drain regions (107), the polysilicon dummy gate (105), a SiN film (106), and sidewalls (108) are formed for the NMOS and PMOS transistors before the replacement metal gate. Matsuo, Ex.1522, ¶¶9-10, 16, FIG. 3A.



Matsuo, Ex.1522, FIG. 3A

84. Before the dummy gate is replaced, the source/drain regions are doped and annealed. *See* Matsuo, Ex.1522, ¶10, FIGS. 3B-C; *see also* Hou, Ex.1519, 2:8-11; Iriyama, Ex.1521, 1:59-2:6. As one of the last steps, the dummy gates are removed to allow for placement of the metal gate stack. Matsuo, Ex.1522, ¶¶11-13, FIG. 3D.



Matsuo, Ex.1522, FIG. 3D

85. In this example, after removal of the dummy gate, both the NMOS and PMOS metal gate electrodes are formed, as seen below. Matsuo, Ex.1522, ¶¶12-16,

FIG. 3J. First, gate dielectric (113) is formed, and then metal layers 114, 116, and 117 after. *Id.*, ¶¶12-16. This sequence can prevent damage to metal gate stacks susceptible to deterioration by high temperature annealing. Iriyama, Ex.1521, 2:22-29.

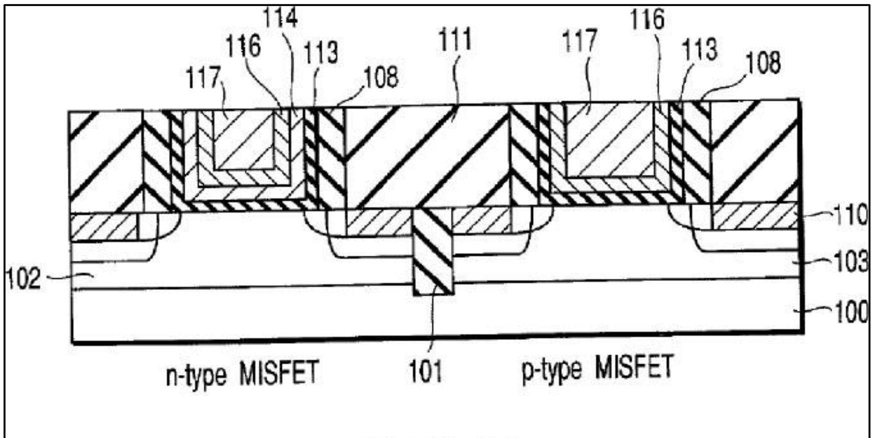


FIG. 3J
(PRIOR ART)

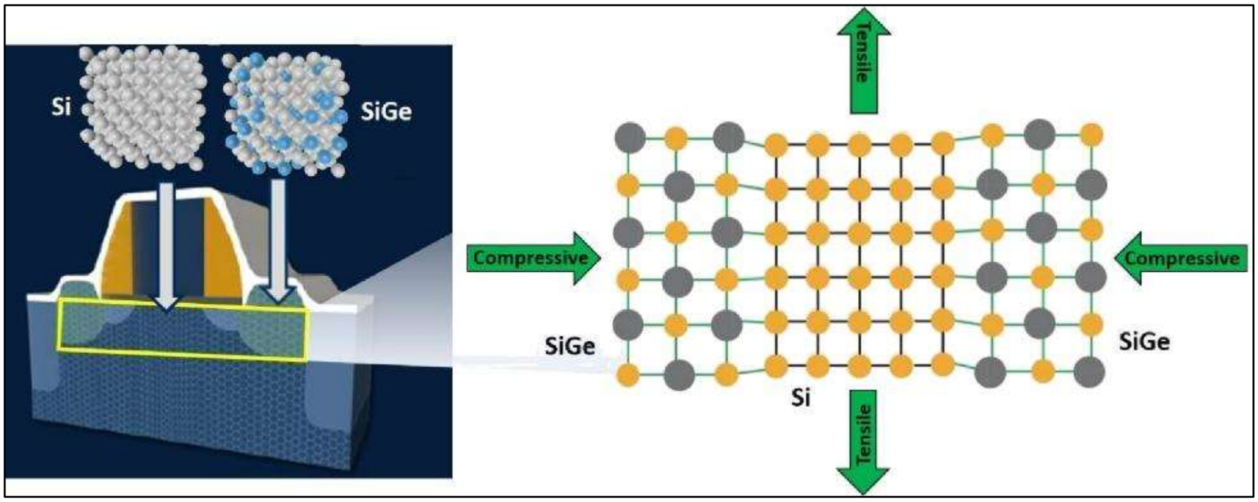
Matsuo, Ex.1522, FIG. 3J

86. In Fig. 3J above, the metal layer 114 is directly formed on the gate dielectric 113 for NMOS gate electrode (shown on the left), but a different metal gate stack is used for the PMOS gate electrode (shown on the right), which does not include metal layer 114. Matsuo, Ex.1522, ¶21. The two gate electrodes thus have different metal work functions, one for NMOS and one for PMOS. *Id.*, ¶21, FIG. 3J; Hou, Ex.1519, 2:11-14; Iriyama, Ex.1521, 2:10-12; Mistry2007, Ex.1516, 247; Mistry_Presentation, Ex.1517, 16, 18.

F. Strained Silicon

87. In the early 2000s, strained silicon technology was recognized as another mechanism to improve transistor performance as transistor sizes continued to shrink. Until the large-scale adoption of strained silicon, PMOS transistors used to be slower than NMOS transistors and much effort was spent on improving PMOS transistor performance compared with NMOS transistors. But the prior art quickly realized that compressively strained PMOS transistors could be improved by as much as 50%, leading to a reversal in efforts spent trying to improve NMOS transistors compared with PMOS transistors.

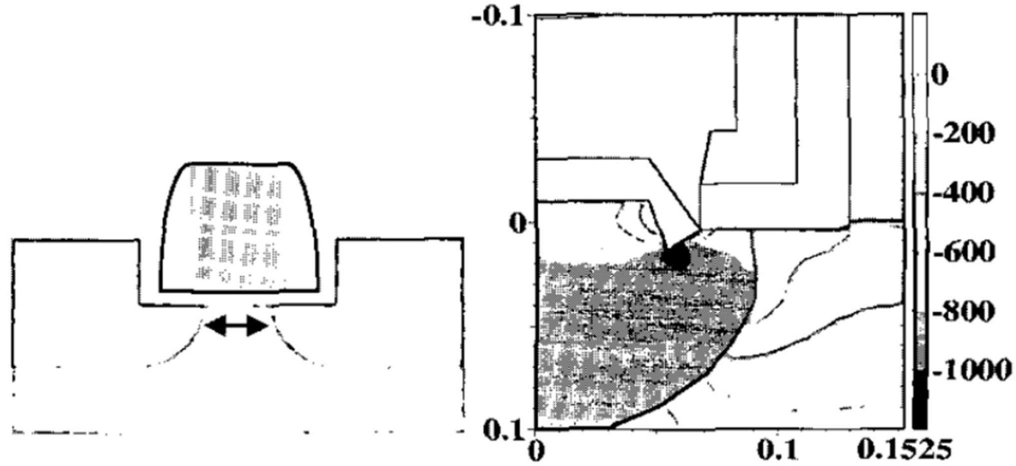
88. Germanium is one source of compressive stress in PMOS transistors. The Ge atoms are larger in size than Si atoms, such that silicon-germanium ("SiGe") can be used in the source/drain regions of PMOS transistors to apply compressive stress to the PMOS channel region. *See* Thompson2004, Ex.1523, 1790-96; Sun-2007, Ex.1524, 2. By 2005, SiGe source/drain regions increased PMOS "hole mobility by as much as 50%" (James, Ex.1525, 2), doubling PMOS operating speeds.



89. Numerous prior art references recognized the benefits of strained silicon, for both PMOS and NMOS transistors. For example, in a 2004 paper titled "35% Drive Current Improvement from Recessed-SiGe Drain Extensions on 37 nm Gate Length PMOS," Chidambaram et al. recognized that "Epitaxial SiGe, grown in recessed Si, has been used to compressively strain the PMOS channel and increase the hole mobility." Chidambaram-2004, Ex.1104, Introduction; *see id*., Abstract ("A highly compressive SiGe layer, in close proximity to the channel, results in large hole mobility improvements."). Another 2004 article by Mistry et al. proclaimed that "[t]he use of strain to improve mobility has been known for 50 years," concluding that "[u]niaxial strained silicon has been implemented in a high volume manufacturing 90nm logic technology for the first time, with impressive performance results and improved power scaling." Mistry-2004, Ex.1106.

90. Where a PMOS transistor benefits from compressive strain, NMOS transistors benefit from tensile stress along the channel region. As seen in Figs. 2-4

from Mistry-2004, compressive stress from SiGe source/drain regions on PMOS transistors and tensile stress on NMOS transistors from a high tensile stress nitride overlayer were well known to improve transistor performance.



(a) (b)

Fig. 2 (a) Epitaxial S/D Transistor structure. (b) Stress simulations: the resulting stress is dominantly uniaxial along the [110] current flow direction X and Y-axes show dimensions in µm. Contours show stress in MPa.

Fig. 3 TEM of NMOS transistor showing high tensile stress nitride overlayer.

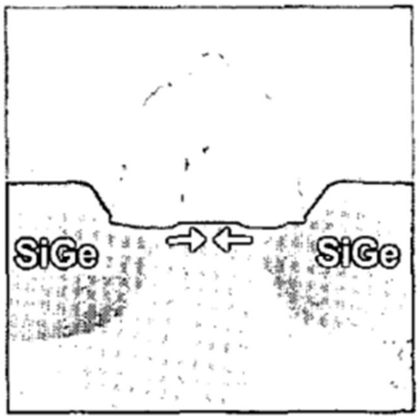


Fig. 4 TEM of PMOS showing SiGe heteroepitaxial S/D inducing uniaxial strain.

Mistry-2004, Ex.1106, FIGS. 2-4.

91. In another article that same year by Chen et al. titled "Stress Memorization Technique (SMT) by Selectively Strained-Nitride Capping for Sub-

65nm High-Performance Strained-Si Device Application," the prior art recognized that "[c]hannel stress control has become a critical technique for electron and hole mobility improvements as down scaling the device dimension." Chen-2004, Ex.1103, Introduction. The article further recognized the tradeoffs inherent in stressing both PMOS and NMOS transistors on the same chip. *Id.* ("In addition, recent studies of high tensile capping layer on top of the silicide have demonstrated the NMOSFET driving current improvement capability, but with the PMOS performance degradation.").

92. Searching for a cost-conscious method to effectively stress the NMOS transistor without degrading PMOS performance, the article proposed (1) selectively applying a high tensile nitride activation capping layer to the NMOS transistor, and (2) applying a low temperature, high-tensile nitride film as a contact etch stop layer to both the NMOS and PMOS transistors. Chen-2004, Ex.1103, Channel Stress Control by SMT; *see id.*, Introduction ("In this paper, we proposed a novel stress memorized technique (SMT) to improve the device performance without PMOS degradation. A high tensile nitride capping layer acts as a temporary stressor to effectively modulate the channel stress. The stress effect is then enhanced and memorized by well-controlled poly amorphorization and re-crystallization procedures. This high tensile nitride capping layer will be removed after the annealing step. Therefore, a much thicker capping layer can be used to increase the

stress level without any process limitation to impact the subsequent gap filling process steps."); *id.*, Channel Stress Control by SMT ("After the silicide formation, the low temperature, high-tensile Nitride film is deposited as Contact-Etch-Stop-Layer (SIN-CESL) to add up the stress effect.").

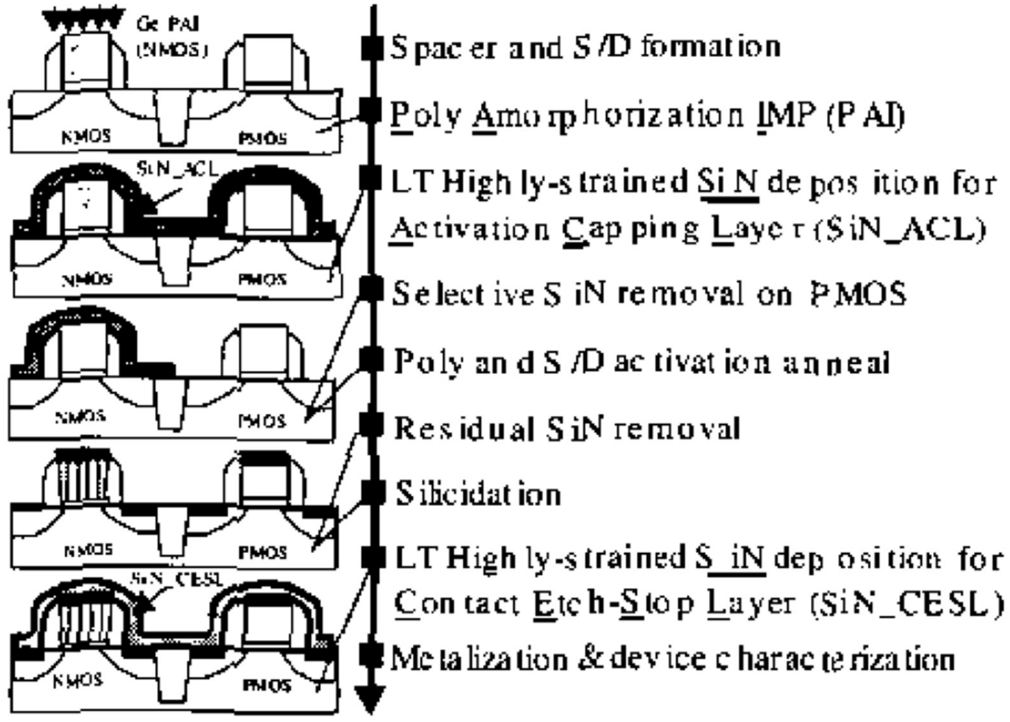


Fig.1 Process sequence of Stress Memorization Technique (SMT).

Chen-2004, Ex.1103, Fig. 1.

93. Additional prior art references taught straining both PMOS and NMOS transistors. *See* Murthy151, Ex.1526, ¶¶5, 48, 72; James, Ex.1525, 2. For example, it was known to create tensile strain with epitaxial source/drain regions, similar to SiGe for PMOS transistors, but it requires using an atom smaller than silicon, like

carbon, to grow a material like silicon carbide (SiC) instead of SiGe,. *See* Murthy151, Ex.1526, ¶¶5, 48, 72; James, Ex.1525, 2; Bohr, Ex.1527, ¶45.

94. As either an alternative or a supplement to source/drain epitaxy, the semiconductor industry was also already depositing compressive and tensile stress-inducing films over PMOS and NMOS devices to induce a desired strain, as shown above. *See also* James, Ex,1525, 2, 4; Morin-2007, Ex.1528, 355-56, 367; Hsu823, Ex.1506, ¶3; Jung, Ex.1529, Abstract, ¶90 ("In addition to being deposited as part of a structure to control electron mobility, as shown in FIG. 1B, a stress-tuned silicon nitride film can be deposited for other purposes . . . , for example . . . , to provide an etch stop layer . . . ."). A contact etch stop layer ("CESL") made of silicon nitride was frequently used, and if prepared under certain conditions, a silicon nitride CESL may apply stress to the channel and increase device performance. Hsu823, Ex.1506, ¶3; *see also* Ex.1531, Ke, ¶3 ("A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device."); Jung, Ex.1529, ¶90 ("In addition to being deposited as part of a structure to control electron mobility, as shown in FIG. 1B, a stress-tuned silicon nitride film can be deposited for other purposes in various steps in the fabrication process, for example (and not by way of limitation), to provide an etch stop layer . . . , as well as to enhance channel mobility in various portions of the device structure."); Morin-2007, Ex.1528, 355-56. It was well known that a silicon nitride CESL may provide

tensile stress, compressive stress, or no stress at all, depending on the process used to apply the layer. *See, e.g.*, Jung, Ex.1529, ¶¶17, 99-100, 131-32, Tbls. IV-V, VII, Fig. 15.

95. As evidenced by the prior art, strained silicon has been well known long before the priority date of the challenged patents. *See*, *e.g.*, Sun-2007, Ex.1524, 1 ("Strain is a relatively old topic in semiconductor physics."). In fact, strained silicon was already commercially used in at least three generations of devices by 2007. *See* Thompson2004, Ex.1523, 1790-91 (Intel's 90nm devices); Bai-2004, Ex.1532, 657-58 (Intel's 65nm devices); Mistry2007, Ex.1516, 247-48 (Intel's 45nm devices); Mistry_Presentation, Ex.1517, 1-19 (same).

G. Stress Buffering Layers

96. Not only were tensile stress contact etch stop layers and SiGe source/drains well known in the prior art, but using buffer layers to mitigate the unwanted effects of those stress layers were also well understood concepts in the prior art.

97. If a tensile contact etch stop layer is deposited over a PMOS device, it generally applies a tensile stress to the channel region. Morin-2007, Ex.1528, 355-56, 367; Doris, Ex.1429, ¶¶ 5, 13; Hsu823, Ex.1506, ¶37. Where the PMOS device is already compressively stressed, for example with epitaxial SiGe source/drain regions, the tensile stress from the contact etch stop layer offsets some portion of the

compressive stress, reducing improvements from the SiGe. Morin-2007, Ex.1528, 355-56, 367; Kavalieros729, Ex.1419, ¶¶2, 26; Doris, Ex.1429, ¶5. The tensile stress may even degrade performance, particularly in PMOS devices without SiGe source/drains. Morin-2007, Ex.1528, 355-56, 367.

98. A POSITA would have understood how to mitigate or negate performance decreases on the PMOS devices from tensile stress. First, a POSITA may choose to apply both a SiGe source/drain to a PMOS device as well as a tensile contact etch stop layer over both the NMOS and PMOS devices to optimize performance of both devices. If the compressive stress from the SiGe is greater than the tensile stress from the contact etch stop layer, the overall compressive stress may still increase PMOS performance, though it may be lessened by the contact etch stop layer. The tradeoff is that the tensile stress improves NMOS transistor performance.

99. A POSITA knew of other ways to mitigate the performance loss. For example, the tensile stress could be reduced for the PMOS device by using a stress-relief layer as a buffer between the SiGe and the tensile contact etch stop layer. Murthy556, Ex.1430, 9:27-29, FIGS. 2, 9, 13-15; Doris, Ex.1429, ¶42, Figs. 1-2, 14-15; Alvarez, Ex.1406, Abstract, ¶43, FIG. 9; Lee870, Ex.1431, ¶29, ¶¶46-67 (pFET performance degradation "is reduced/eliminated due to the inclusion of the stress relief layer 64 under the nitride layer 70 that reduces the tensile stress in the channel region"), FIGS. 2-5; Cheng810, Ex.1432, ¶¶22-31, Figs. 1B-1F (describing similar);

Baik, Ex.1433, ¶37 ("the tensile stresses of the [stressor layer] ha[ve] relatively little or no adverse impact [on] the adjacent PMOS device" because the intermediate layer "reduce[s] the amount of stresses induced in the PMOS device by acting as a physical barrier").

100. A number of prior art references taught that using an intermediate layer "buffers the large stress inherent silicon nitride layer." Murthy556, Ex.1430, 9:27-29; Alvarez, Ex.1406, ¶¶49, 66, 68, 77, FIGS. 9-11. As seen below, Alvarez depicts on example with a stress-inducing layer 216 (shown in blue below) that is buffered by stress-control layer 226 (shown in purple) to mitigate the adverse effects of the stress layer on the PMOS devices 224b and 224c (while still improving performance of the NMOS devices).

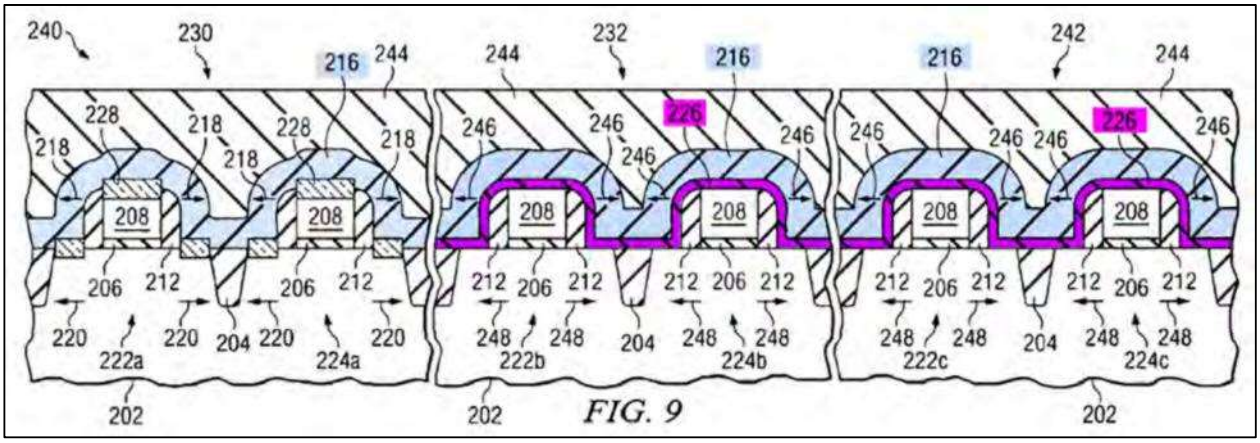


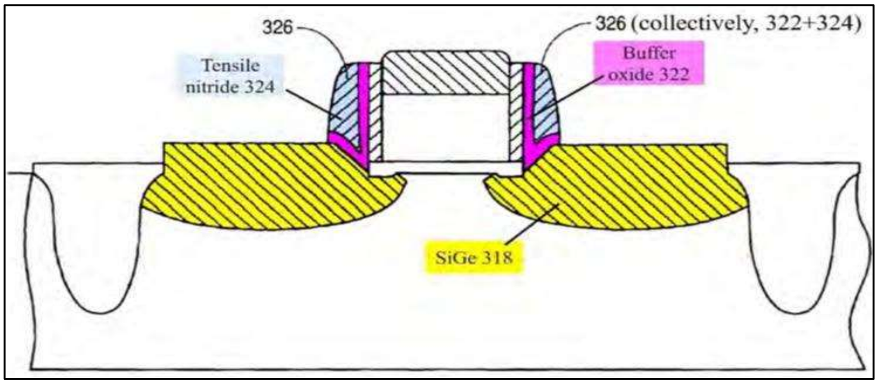
FIG. 9

Alvarez, Ex.1406, FIG. 9

101. While the buffer layer above in Figure 9 is shown to be selectively applied, the prior art also explained that these layers could be applied to multiple areas, similar to the one Alvarez discloses (e.g., dual-purpose stress-controlling and

masking layer), as a way to save manufacturing cost or complexity. Alvarez, Ex.1406, ¶¶43, 45, 47, 49, 53-55, 78, FIGS. 7-9. This is particular advantageous where "different types of transistors . . . hav[e] different operating parameters and requirements" and/or "due to the performance requirements of transistors in the particular regions." *Id.*, ¶¶27, 32, FIGS. 7-9. Leaving the buffer layer over both the NMOS and PMOS, for example, can reduce the number of fabrication steps and lower the cost of manufacturing. *Id.*, ¶[0075]; *see also id.*, ¶¶74, 78.

102. In another example shown below, a buffer layer can be formed immediately between the SiGe source/drain regions and the gate electrode, particularly when raised SiGe source/drain regions are used. *See* Murthy556, Ex.1430, 9:11-15, 9:30-35, FIGS. 7-9; *see also* Miyashita, Ex.1435, ¶¶[0052]-[0053], FIGS. 1U-1W; Koutny, Ex.1434, ¶¶88, 108 (silicon dioxide liner 485A between tensile stress-inducing layer 504A and source/drain "reduces the cumulative stress" caused by the tensile layer); Doris, Ex.1429, ¶¶34, 42; Cheng810, Ex.1432, ¶30; Lee870, Ex.1431, ¶67.



Murthy556, Ex.1430, FIG. 9 (annotated)

103. These buffer layers can prevent "the tension from materially adversely influencing the charge carrier mobility in the pFET," such that the pFET "experiences a performance improvement" through "enhanc[ed] hole mobility in the pFET channel" compared to no buffer layer. Doris, Ex.1429, ¶¶34-35, Figs. 2, 14, 15. Using low-stress dielectric films like silicon oxides can create "a neutral buffer layer" between a compressively stressed source/drain and a tensile contact etch stop layer, which allows the compressively stressed region "to have maximum influence on the pFET channel mobility and minimizes the influence of the tensile barrier etch stop layer." *Id.*, ¶42; *see also* Lee870, Ex.1431, ¶¶29, 46-67 (explaining that an intermediate stress relief layer "with neutral stress or opposite stress relative to the [CESL]" reduces or eliminates any pFET performance degradation because it "reduces the tensile stress in the channel region"), FIGS. 2-5; Cheng810, Ex.1432, ¶¶22-31, Figs. 1B-1F.

H. System-on-Chip Design Advancements

104. Threshold voltage is an important characteristic when considering what a particular transistor will be used for. Threshold voltage is the minimum voltage applied at the gate to create a conductive channel between the source and drain—i.e., the ON or active voltage of the transistor. Van Zant, Ex.1211, 526, 474 ("Every MOS transistor is designed to operate at a specific threshold voltage."). Because PMOS and NMOS transistors use different dopants for the source/drain and source/drain extensions, a POSITA understands that PMOS and NMOS transistors have opposite gate voltages. That is, NMOS transistors require a positive voltage at the gate to induce the active state (and thus a positive threshold voltage), while PMOS transistors require a negative voltage at the gate to induce the active state (and thus a negative threshold voltage). *See, e.g.,* Weste, Ex.1212, 74, 293-296, 302.

105. Threshold voltage has three main components: flatband voltage (V_{FB}), voltage drop across the gate oxide (V_o), and semiconductor potential at the semiconductor surface during strong inversion ($\psi s(inv)$). Sze-2002, Ex.1223, 175, 178, 194. For a given semiconductor and dielectric material, substrate doping, oxide thickness t_{ox}, and the metal work function Φ_m can be used to predictably tune a transistor's threshold voltage. Houssa, Ex.1213, 535, 537. When the substrate doping and gate oxide thickness are carefully engineered to control channel mobility

and the gate capacitance, respectively, the gate electrode work function can be altered to optimize or fine-tune the threshold voltage further.

106. Consumer devices often have multiple transistors on the same chip, including transistors of the same conductivity types but with different threshold voltages, to cope with various demands on standby power and operation speed. For example, a device may include transistors for low operating power (LOP), transistors for low stand-by power (LSTP), and/or transistors for high performance (HP). ITRS-PIDS, Ex.1216, 5. HP transistors have the highest operating speed, the shortest gate length, the thinnest gate oxide, and the lowest threshold voltage among the three. ITRS-PIDS, Ex.1216, 11, 17, 21. LSTP transistors are designed for low performance and low leakage current and therefore have thicker gate oxides and higher threshold voltage, while LOP transistors are between the HP and LSTP devices in terms of performance, leakage current, and threshold voltage. *Id.*

107. As recognized by the prior art, instead of making different chips for different purposes, HP, LOP, and LSTP transistors can be formed on a single chip by varying the manufacturing process parameters. Because "[a]n increasing number of mixed-signal and system-on-a-chip applications require dual on-chip power-supply-voltages[,]" different transistors of the same type (e.g., PMOS or NMOS) are needed for different power-supply-voltages. Wolf-4, Ex.1214, 121. For example, "[t]he higher-voltage may be used for the analog and input/output (I/O) circuitry,

and the lower-voltage for the core-digital-logic devices." *Id.* And because analog and I/O regions must handle higher operating voltages, "the analog and I/O devices require thicker gate oxides than the core logic devices." *Id.* As such, forming different transistors with different gate oxide thickness can be used where needed, for instance where both higher-voltage and lower-voltage transistors are desired on the same chip.

108. The prior art teaches different processes to vary oxide thickness across different transistors on the same chip. *See, e.g.,* Karve, Ex.1226, 3:45-4:36 (describing formation of nMOS with thicker gate oxide than core nMOS), Figs. 5-6, 8; Luo, Ex.1227, 5:61-7:58 (describing formation of nMOS-DGO and nMOS core devices). As explained by one textbook, one process is to include two oxidation steps "with a masked etch-step in between to remove the first oxide from regions intended to have thinner oxide." Wolf-4, Ex.1214, 121. Yet another process uses nitrogen implants to impede oxide growth in certain areas, which occurs because "the rate of thermal-oxidation on silicon is reduced by nitrogen implants." *Id.* "Hence, nitrogen implantation into the silicon substrate prior to the oxidation process can be used to facilitate the implementation of such 'dual-gate-oxide' ICs." *Id.*

VI. THE '076 PATENT

109. The '076 patent issued on November 19, 2013, from U.S. Patent Application No. 13/547,913, filed on July 12, 2012. Ex.1001, cover. The '076

patent claims priority to Japan Application No. 2005-227457, filed on August 5, 2005. *Id.*

A. Claims

110. The '076 patent has 13 claims, including one independent claim numbered 1, and dependent claims numbered 2-12. Ex.1001, 21:39-22:43. Claims 1, 2, 3, 6, 7, 8, 10, 11, 12, and 13 are the Challenged Claims.

111. The Challenged Claims are reproduced below:

> **1. Preamble:** A semiconductor device comprising:
>
> **1[a]:** a gate insulating film formed on an active region in a substrate and including Hf;
>
> **1[b]:** a gate electrode formed on the gate insulating film;
>
> **1[c]:** a insulating sidewall formed on each side surface of the gate electrode; and
>
> **1[d]:** wherein a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length, and
>
> **1[e]:** an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode.

Ex.1001, 21:39-22:6.

> **2:** The semiconductor device of claim 1, further comprising a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film.

Ex.1001, 22:7-9.

> **3.** The semiconductor device of claim 1, wherein the gate insulating film is formed of a Hf based oxide.

Ex.1001, 22:10-11.

> **6.** The semiconductor device of claim 1, wherein a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.

Ex.1001, 22:18-20.

> **7.** The semiconductor device of claim 1, wherein an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall.

Ex.1001, 22:21-23.

> **8.** The semiconductor device of claim 1, wherein the insulating sidewall has a double layer structure including an oxide film and a nitride film.

Ex.1001, 22:24-26.

> **10.** The semiconductor device of claim 1, wherein a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length.

Ex.1001, 22:30-33.

> **11.** The semiconductor device of claim 1, wherein the end of the gate insulating film located under the insulating sidewall has a tapered surface.

Ex.1001, 22:34-36.

> **12.** The semiconductor device of claim 1, wherein the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof

Ex.1001, 22:37-39.

> **13.** The semiconductor device of claim 1, wherein the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length.

Ex.1001, 22:40-43.

B. Summary of the Specification

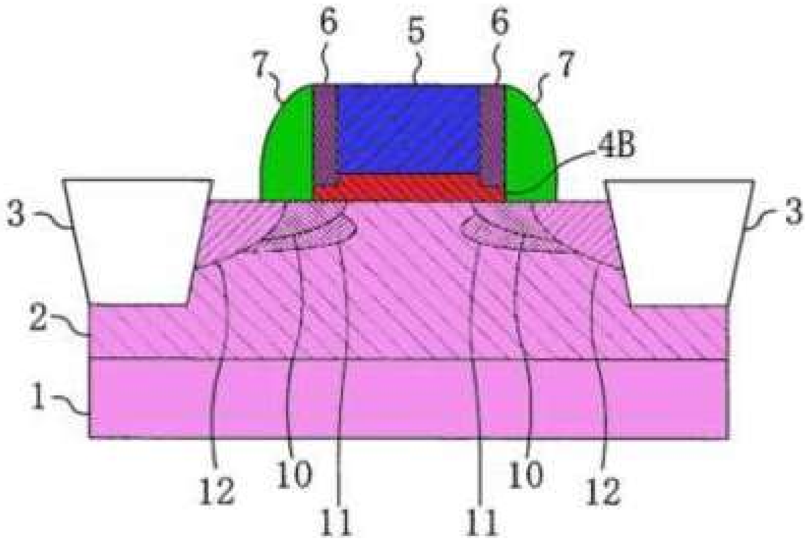
112. The ’076 patent is directed to “a structure of a MISFET (metal insulator semiconductor field-effect transistor) and a method for fabricating the MISFET and, more particularly, relates to techniques for improving the driving power and reliability of a MISFET.” ’076 patent, Ex.1001, 1:20-22. According to the ’076 patent, in prior art devices, the “side end portions” of the high-k film “are in direct contact with sidewalls,” which caused the reliability of the gate insulating film to degrade. *Id.*, 1:64-2:8.

113. The inventors of the ’076 patent purported to have solved this problem via “a MISFET structure in which a high dielectric constant gate insulating film is kept remaining under sidewalls to prevent end portions of the high dielectric constant gate insulating film from being in contact with the sidewalls, and a method for forming the MISFET structure.” *Id.*, 2:13-19. The ’076 patent discloses several exemplary embodiments in which the high-k gate insulating film extends at least partially under the insulating sidewall, and is thinner under the insulating sidewall than under the gate electrode, including devices with a single sidewall (e.g., the first and fourth embodiments) and devices with double sidewalls (*e.g.*, the second and third embodiments) to which the ’076 patent’s claims are directed.

114. More specifically, the Challenged Claims recite a semiconductor device with a gate insulating film formed on an active region in a substrate and

including Hf, a gate electrode formed on the gate insulating film, and a insulating sidewall formed on each side surface of the gate electrode, wherein a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length. ’076 patent, Ex.1001, 21:39-22:6. Claim 1 of the ’076 patent further requires an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode. *Id.*

115. Dependent Challenged Claims 2 and 8, for example, depend from claim 1 and specify that the semiconductor device further includes a buffer insulating film between the substrate and the gate insulating film (claim 2) and that the insulating sidewall has a double layer structure including an oxide film and a nitride film (claim 8). ’076 patent, Ex.1001, 22:7-9 & 22:24-26. Thus, Figure 2 (below) of the ’076 patent, which corresponds to the second embodiment of the ’076 patent, illustrates an exemplary device covered by claim 1:



’076 Patent, Ex.1001, Fig. 2 (annotated)

116. As illustrated above in Figure 2, the high-k gate insulating film (shaded red) extends under first (i.e., inner or offset) sidewall 6 (shaded purple) and has a wider width than gate electrode 5 (shaded blue). Further, the claimed insulating sidewall of claim 1 is made up of both sidewalls 6 and 7 such that an end of the gate insulating film underneath the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode.

117. Although the ’076 patent does not expressly disclose a buffer insulating film in the context of the second or third embodiments, an example of a buffer insulating film between the substrate and the high dielectric constant gate insulating film, as required by dependent claim 2, is illustrated in Figure 9. *See* ’076 patent, Ex.1001, FIG. 9, element 25.

C. Summary of the Prosecution History

118. During prosecution of the application that led to the ’076 patent, the Examiner issued a prior art rejection over U.S. Patent No. 6,992,358 to Hieda. Ex.1002, 129-33. In response, the Applicant amended pending claim 21 (which issued as claim 1) to add the following limitation: “an end of the gate insulating film under the insulating sidewall ~~is located to retract~~ retracted from an outer end of the insulating sidewall toward the gate electrode.” *Id.*, 155. Following submission of a terminal disclaimer, the Examiner allowed the amended claims. *Id* , 157-59, 173-74.

VII. LEVEL OF ORDINARY SKILL IN THE ART

119. I understand that there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including the educational level of active workers in the field at the time of the alleged invention, the sophistication of the technology, the type of problems encountered in the art, and the prior art solutions to those problems.

120. In determining the characteristics of a hypothetical person of ordinary skill in the art of the ’076 patent at the time of the alleged invention, I considered several things, including the type of problems encountered in this field, and the rapidity with which innovations were made. I also considered the sophistication of the technology involved, and the educational background and experience of those actively working in the field, and the level of education that would be necessary to

understand the ’076 patent. Finally, I placed myself back in the relevant periods of time, and considered the state of the art and the level of skill of the engineers working in this field in those times.

121. It is my opinion that a POSITA at the time of the ’076 patent would have had at least a Master’s degree in electrical engineering, physics, chemistry, materials science, or a related field, and three years of work experience in semiconductor design and manufacturing, including with respect to planar transistors, or equivalent work experience. Additional graduate education might compensate for a deficiency in experience, and vice-versa.

122. I also note that my opinions provided in this Declaration would not change in view of any minor modifications to this level of skill.

VIII. CLAIM CONSTRUCTION

123. It is my opinion that for purposes of this proceeding, the claim terms need not be construed to resolve the prior art issues presented in this Petition.

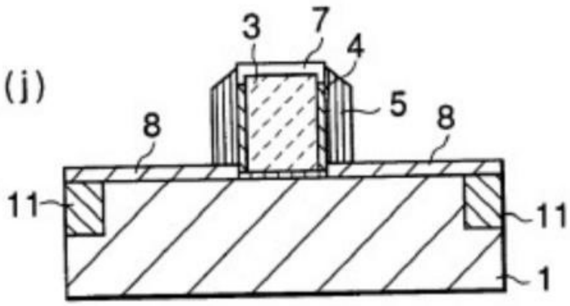
124. Nothing in this section should be construed as expressing any opinion as to whether the claims constitute patentable subject matter under 35 U.S.C. § 101, or whether they satisfy the definiteness, enablement, best mode, or written description requirements under 35 U.S.C. § 112.

IX. OVERVIEW OF THE PRIOR ART

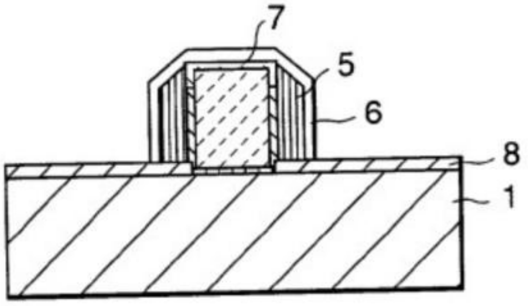
A. Kamata (Ex.1027)

125. Kamata discloses multiple semiconductor devices, including MIS type transistors with a variety of sidewall films. (*See* Kamata, Ex.1027, Abstract, ¶¶3, 5, 16.) Kamata teaches manufacturing its devices through the steps of: "forming a gate insulating film on a silicon substrate; forming a gate electrode on the gate insulating film; forming a first insulating film to cover the gate insulating film and the gate electrode; [and] forming a second insulating film on the first insulating film . . . ." (Kamata, Ex.1027, ¶¶22-30.) Specifically, Kamata includes a high-k dielectric film: "The gate insulating film may be . . . a high dielectric constant film such as an oxide film with higher dielectric constant than the silicon oxide, containing at least an element selected from a group of Ti, Zr, Hf, Ta, La, Al Ba, Sr, Y, Pr and Gd, and a silicate film containing such an element." (Kamata, Ex.1027, ¶52.)

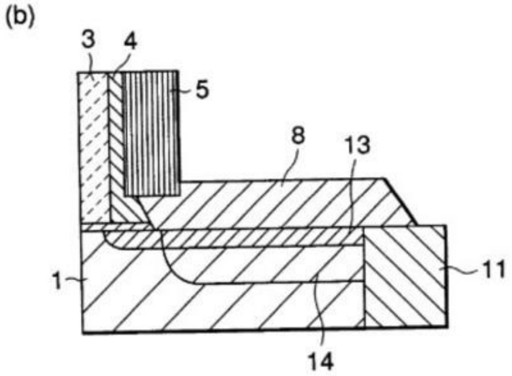
126. Several embodiments are relevant to the '076 Patent, including the first (Figure 1B(j)), fourth (Figure 5(c)), and ninth (Figure 10(b)) embodiments, shown below.



Kamata, Fig. 1B(j)
(First Embodiment)



Kamata, Fig. 5(c)
(Fourth Embodiment)



Kamata, Fig. 10(b)
(Ninth Embodiment)

127. In each of these embodiments, the gate film extends from underneath the gate electrode to underneath a portion of the sidewall. In the first and fourth embodiments, the gate film extends under sidewall 4, and under sidewall 4 and a portion of sidewall 5 for the ninth embodiment. (*See also* Kamata, Ex.1027, ¶25 ("forming a first insulating film to cover the gate insulating film and the gate electrode").)

B. Sim (Ex.1024)

128. In the same field as Kamata and the ’076 patent, Sim relates to the use of high-k dielectrics in semiconductor devices. Sim, Ex.1024, Abstract (“Scaling the physical thickness of the HfO_2 dielectric causes less charge trapping and higher mobility.”). ’076 patent, Ex.1001, 1:18-19 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”).

129. Sim explained that “[h]afnium-based high-k dielectrics and metal gate electrodes have been aggressively investigated to ensure continued scaling of CMOS technology, but several drawbacks such as low mobility and charge trapping have been identified.” Sim, Ex.1024, 218. Sim’s authors examined and addressed these drawbacks by testing films of different thickness and “systematically evaluat[ing] the effects of high-k film thickness on charge trapping and channel carrier mobility.” *Id.* Specifically, Sim explained that “scaling the high-k dielectric is a simple, but very effective means of improving mobility and other reliability characteristics.” *Id.* Sim concluded that “[s]caling the physical thickness of the HfO_2 dielectric to below 20Å causes less charge trapping and higher mobility.” *Id.*, 221.

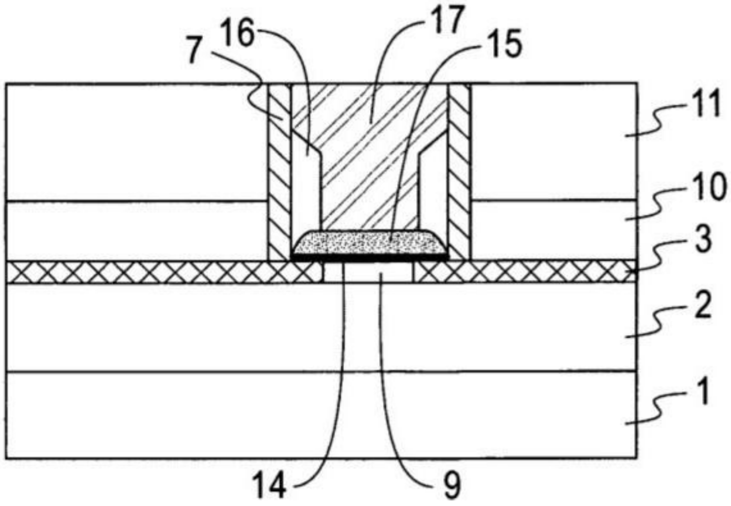
C. Guha (Ex.1028)

130. Guha, titled “Damascene Gate Field Effect Transistor With an Internal Spacer Structure,” is directed at semiconductor devices like Field Effect Transistors. (*See also* Guha, Ex.1028, ¶¶1 (“The invention relates to a MOSFET device having

a damascene gate with an internal spacer structure and a process of forming the device."), 4 ("The invention relates to a MOSFET with improved device performance and method of fabricating the device.").)

131. My analysis focuses on the structure shown in Figure 12, although Guha also discloses that its other processes include common steps. (Guha, Ex.1028, ¶42 (stating that the structure of Figures 10-12 start with the structure of Figure 7; see also Guha, Ex.1028, ¶54 ("Any disclosed embodiment may be combined with one or several of the other embodiments shown and/or described. This is also possible for one or more features of the embodiments.").)

132. Guha's Figure 12 embodiment is shown below.



Guha, Figure 12

133. As seen in Figure 12, Guha teaches a semiconductor device with gate electrode 17, gate spacer structure 16, and isolating spacer structure 7. (Guha, Ex.1028, ¶¶43-45.) A gate insulating film, dielectric layer 15, is formed on gate-

isolating layer 14, both extending from underneath the gate electrode 17 to underneath the gate spacer structure 16. (Guha, Ex.1028, ¶¶38, 43-44.) Dielectric layer 15 "preferably compris[es] a high-K dielectric material, [which] is a material that exhibits a dielectric constant of approximately above 10 or more. Examples of such materials, include, but are not limited to hafnium oxide, hafnium silicate, aluminum oxide or zirconium oxide." (Guha, Ex.1028, ¶¶38, 43) Further, Guha teaches that "[t]he gate-isolating layer 14 acts as a buffering layer between channel 9 and the dielectric material to be deposited thereon," and thus is "used to prevent mobility degradation in the silicon channel that may be caused by scattering mechanisms in the dielectric layer." (Guha, Ex.1028, ¶37).

D. Matsumoto (Ex.1009)

134. Similar to the '076 patent, Matsumoto relates "to a semiconductor device" and more specifically to an improved MOSFET (Metal Oxide Semiconductor Field Effect Transistor), and methods for manufacturing the same. Matsumoto, Ex.1009, Abstract, ¶2. Matsumoto discloses a semiconductor device having a gate electrode, insulating sidewalls on the side of the gate electrode, and a gate insulating film that extends from under the gate electrode to the under the insulating sidewalls.

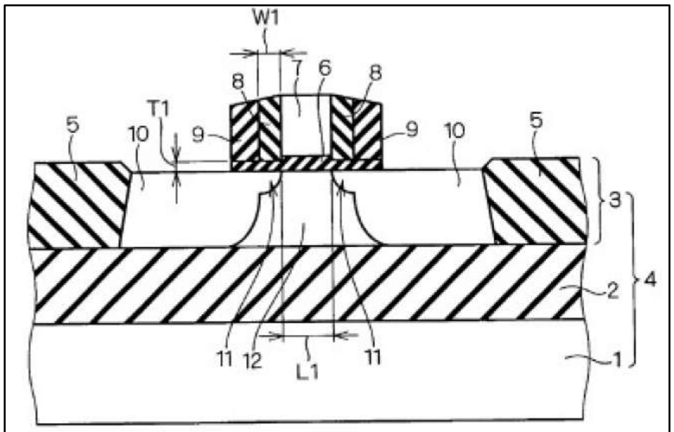
135. Although Matsumoto discloses several embodiments and modifications, many of the fabrication steps are discussed in relation to the first

embodiment. *See, e.g.*, Matsumoto, Ex.1009, ¶123 ("The remaining structure of the semiconductor device according to the second preferred embodiment is similar to the corresponding structure of the above-stated semiconductor device according to the first preferred embodiment shown in FIG. 1."), 137 ("Referring first to FIG. 18, the gate electrode 7 is formed by the process described in the first preferred embodiment …."). Moreover, Matsumoto repeatedly explains, and a POSITA would have understood, that the teachings of one embodiment (or modification thereof) could be readily applied to other embodiments. *See, e.g.*, Matsumoto, Ex.1009, 140 ("The technique of the fourth preferred embodiment is applicable to any one of the first to third preferred embodiments."), 141 ("The technique of the first modification of the fourth preferred embodiment is applicable to any one of the first to fourth preferred embodiments."), 143 ("The technique of the second modification of the fourth preferred embodiment is applicable to any one of the first to fourth preferred embodiments and the first modification of the fourth preferred embodiment.").

136. According to Matsumoto, the "increased base width of a parasitic bipolar transistor reduces the gain of the parasitic bipolar transistor, thereby to suppress malfunctions and operating characteristic variations of the MOSFET. Additionally, a decreased amount of overlap between the gate electrode and the extensions as viewed in plan suppresses a gate overlap capacitance to achieve the

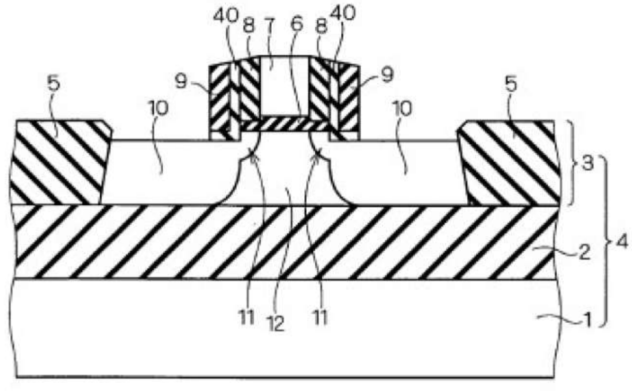
increase in operating speed and the reduction in power consumption." Matsumoto, Ex.1009, ¶15.

137. As shown in Figure 1 below, Matsumoto's first embodiment has a gate insulating film 6 extends from under the gate electrode 7 to under both sidewalls 8 and 9, just like Figure 3 of the '076 patent. *See* Matsumoto, Ex.1009, ¶103.



Matsumoto, Fig. 1

138. As shown in Figure 22 below, Matsumoto's fourth embodiment includes a gate insulating film 6 extending from under the gate electrode 7 to under only the sidewall film 8, comparable to Figure 2 of the '076 patent. *See* Matsumoto, Ex.1009, ¶¶138-140.

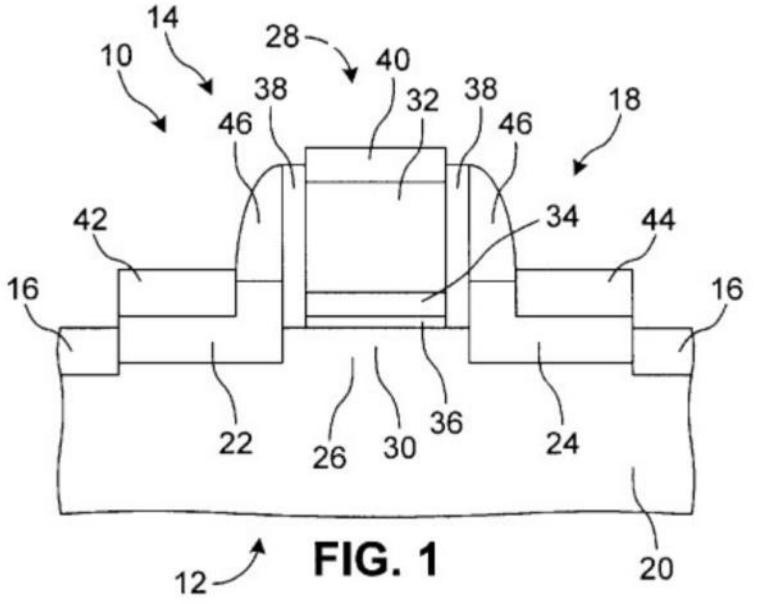


Matsumoto, Fig. 22

E. Yu (Ex.1048)

139. U.S. Patent No. 6,504,214, titled "MOSFET Device Having High-K Dielectric Layer," to Yu, et al. ("Yu"; Ex.1048), was filed on January 11, 2002, and issued on January 7, 2003.

140. Similar to numerous of the prior art discussed so far, Yu discloses a MOSFET with a high-k gate insulating film between the gate electrode and the substrate. (Yu, Ex.1048, Abstract.) An example is seen below.



Yu, Fig. 1

141. Yu further discloses that buffer interface 36 between the substrate 20 and high-k gate dielectric 34. (Yu, Ex.1048, 3:59-62; Figure 1.) Yu's buffer interface 36 "can be a thin layer of oxide," such as "a layer of silicon oxide that is about 0.5 nm to about 0.7 nm thick." (Yu, Ex.1048, 4:58-61; see also Yu, Ex.1048, 3:62-63.) Yu teaches specific benefits of a buffer layer between the high-k gate film and the substrate: "The buffer interface 36 acts to reduce diffusion and/or penetration of atoms from the high-K dielectric material into the layer of semiconductor material 20 that could lead to a degradation in channel mobility. In addition, the buffer interface 36 may act to retard reaction of the high-K material with the layer of semiconductor material 20." (Yu, Ex.1048, 3:64-4:2.)

F. Koyama (Ex.1029)

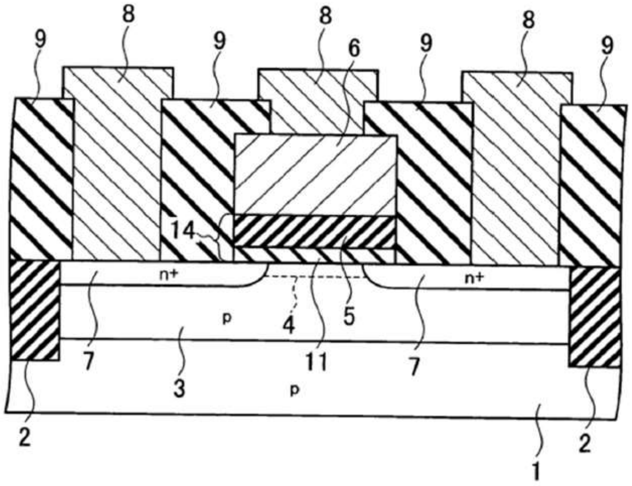
142. "Effects of Nitrogen in HfSiON Gate Dielectric on the Electrical and Thermal Characteristics" to Koyama, et al. ("Koyama"; Ex.1029) was published in 2002. Koyama studied high-k dielectrics for semiconductor devices, the same field as Kamata and the '076 patent. (Ex.1001, 1:18-19 ("The present invention relates to a semiconductor device and a method for fabricating the semiconductor device."); Kamata, Ex.1027, ¶3 ("This invention relates to a semiconductor device and a method of manufacturing the same.").)

143. Koyama described that as early as 2002, "Hf(Zr) silicates are considered to be prospective high-K materials due to their modest dielectric constants and good interface properties." (Koyama, Ex.1029, 849.) Proposing to use a "HfSiON gate dielectric with excellent thermal stability," Koyama compared "the effects of nitrogen on the improved thermal stability and electrical characteristics of this dielectric." (Koyama, Ex.1029, 849.) Koyama concluded that "nitrogen [in HfSiON] enhances the dielectric constant of silicates" and "boron penetration is substantially suppressed in the HfSiON during high temperature annealing." (Koyama, Ex.1029, 849.) These results "strongly suggest that HfSiON is the most probable material for first generation high-K gate dielectrics." (Koyama, Ex.1029, 850.)

G. Ono (Ex.1013)

144. Ono also relates to semiconductor devices, including field effect transistors. Ex.1013, Abstract, ¶¶3-7. Ono is therefore in the same field as Matsumoto and the ’076 patent in my opinion. Ex.1001, 1:8-9 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); Matsumoto, Ex.1009, ¶2 (“The present invention relates to a semiconductor device and a method of manufacturing the same.”).

145. Ono discloses two base embodiments of a semiconductor device each of which includes a semiconductor substrate, source and drain regions arranged at the surface of the semiconductor substrate, a gate insulator film on the substrate, and a gate electrode on the gate insulator film. Ex.1013, ¶¶8-9. As shown below in Figure 77, Ono’s semiconductor device includes a gate stack comprising gate insulator film 11 and gate insulator film 5 made of “HfO_2 film.” *Id.*, ¶¶ 207, 209.



Ono, Fig. 77

146. Gate electrode 6 is formed on gate insulator film 5, as shown in Figure 77 above, and may have gate sidewalls positioned adjacent to it. Ex.1013, ¶¶207, 181 ("sidewalls may be provided to the gate electrode"). In one example modification to adjust and optimize the electrical performance of the device, Ono teaches that "the sidewalls of the gate insulator film may curve." *Id.*, ¶¶200, 216. Ono also discloses several examples in which a length of the gate insulating film is varied in relation to the gate electrode, the sidewall of the gate insulating film is "slanted," and the gate insulator films have curved end portions. *See e.g.*, *id.*, FIGS. 86-123, ¶216.

X. SPECIFIC GROUNDS FOR PETITION

A. Ground I

147. In my opinion, Kamata renders obvious Challenged Claims 1-3, 7, 8, and 10-13 of the '076 patent (Ground I).

1. Independent Claim 1

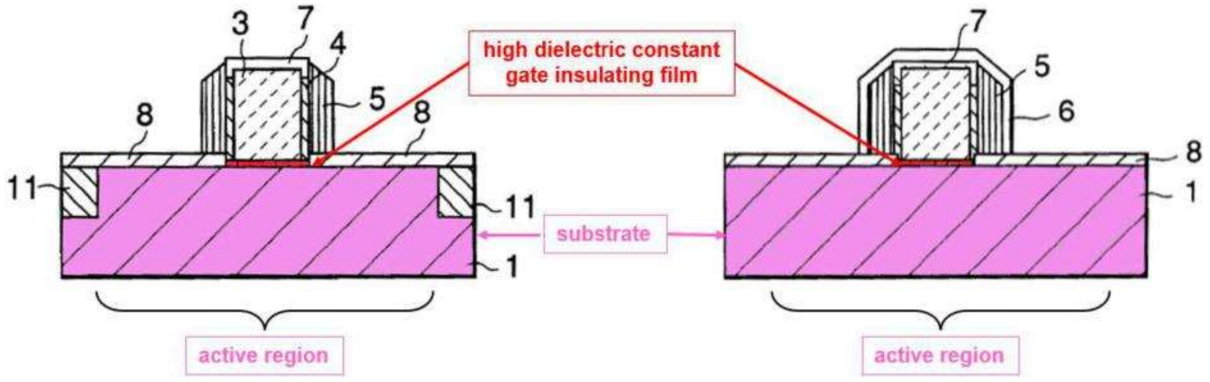
a. Preamble: "A semiconductor device comprising:"

148. Kamata discloses a semiconductor device in at least its first, fourth, and ninth embodiments. Kamata's title is "Semiconductor Device and Manufacturing Method" and it further states that the invention "relates to a semiconductor device." Kamata, Ex.1027, ¶¶3, 8; see also Kamata, Ex.1027, ¶¶32, 50 (first embodiment), 35, 68 (fourth embodiment), 93-94 (ninth embodiment).)

b. Limitation 1[a]: "a gate insulating film formed on an active region in a substrate and including Hf;"

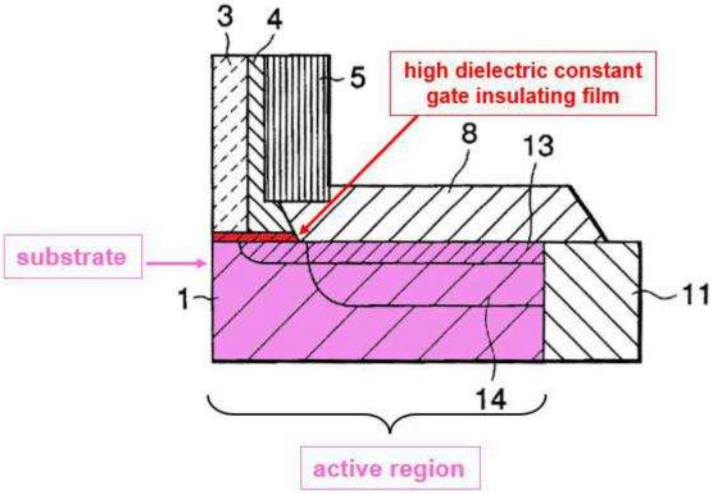
149. Kamata's first, fourth, and ninth embodiments each disclose limitation 1[a]: "a gate insulating film formed on an active region in a substrate and including Hf." Each of Kamata's devices has "a semiconductor substrate 1 made of silicon" (*see, e.g.*, Kamata, Ex.1027, ¶50) and is manufactured by "forming a gate insulating film on a silicon substrate." (Kamata, Ex.1027, ¶23; *see also* Kamata, Ex.1027, ¶¶68 ("parts [of the fourth embodiment] that are same as or similar to those of the first embodiment are denoted respectively by the same reference symbols"), 94 ("portions [of the ninth embodiment] that are same as or similar to those FIGS. 1A through 2C are denoted respectively by the same reference symbols").)

150. Kamata further discloses that "shallow trench isolation zones (STI) 11 are formed on a semiconductor substrate 1 made of silicon to define an element region 1a (FIG. 1A(a))." (Kamata, Ex.1027, ¶50; *see also* Kamata, Ex.1027, ¶¶68, 94.) A POSITA would understand that element region 1a, bordered by the shallow trench isolation, is an "active region in a substrate." (Kamata, Ex.1027, ¶¶99-100 (referring to "active region 1a") This is similar to the '076 patent. (See Ex.1001, 1:41-43 ("region of the well 102 surrounded by the STI serves as an active region of a substrate 101").) Thus, Kamata's active region in a substrate is shaded pink in the annotated figures below.



Kamata, Fig. 1B(j)
(First Embodiment)

Kamata, Fig. 5(c)
(Fourth Embodiment)



Kamata, Fig. 10(b)

(Ninth Embodiment)

151. As shown above, each embodiment of Kamata's semiconductor device includes film 2 (shaded red) formed on the active region underneath the gate electrode and extending beneath the sidewall. (*See, e.g.*, Kamata, Ex.1027, ¶¶23, 56, 68, 94). Kamata further discloses use of high-k material in the gate film: "[t]he gate insulating film may be . . . a high dielectric constant film such as an oxide film with

higher dielectric constant than the silicon oxide, containing at least an element selected from a group of Ti, Zr, Hf, Ta, La, Al Ba, Sr, Y, Pr and Gd, and a silicate film containing such an element." (Kamata, Ex.1027, ¶52). Kamata further discloses that "[t]he film may be a single crystal film, a poly crystal film or an amorphous film such as TiO_2, Ti_2O_5, BST, Si_3N_4, Al_2O_3, Y_2O_3, La_2O_3, HfO_2, ZrO_2, Pr_2O_3, $SrTiO_3$ and Gd_2O_3." (Kamata, Ex.1027, ¶53.) Additionally, Kamata teaches that the gate film can be "a mixture of SiO_2, TiO_2, Ti_2O_5, BST, Si_3N_4, Al_2O_3, Y_2O_3, La_2O_3, HfO_2, ZrO_2, Pr_2O_3, $SrTiO_3$ or Gd_2O_3, with Ti, Zr, Hf, Ta, La, Al Ba, Sr, Y, Pr or Gd." (Kamata, Ex.1027, ¶53.)

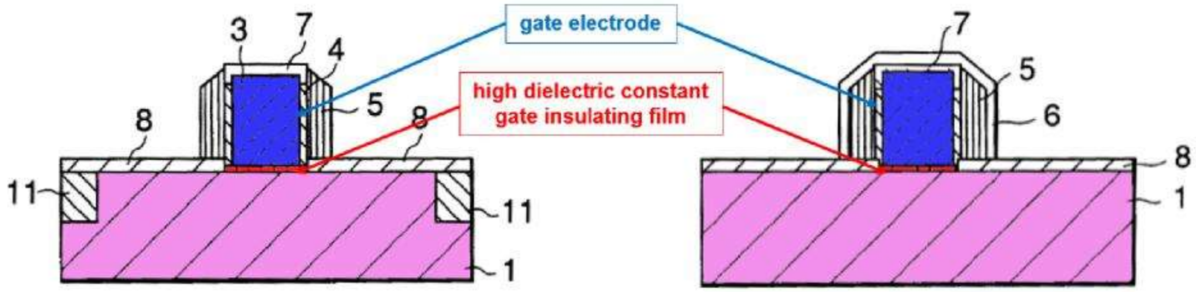
152. Using high-k materials as the gate film was well known to a POSITA to solve known problems, particularly to address the well-understood issues with using silicon dioxide gate dielectrics as semiconductor devices continued to shrink in size. (See Houssa, Ex.1213, 3-12; Wolf Vol 4., Ex. 1214, 4-5, 146-47.) Further, a POSITA would have been motivated to select HfO_2 given its known benefits, e.g., "its superior thermal stability with poly-Si and reasonable band alignment." (Lee-2000, Ex.1337, 2.4.1; *see also* Houssa, Ex. 1213, 207 (HfO_2 "combines a high k (15–26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ..."); Lee-1999, Ex.1349, 134 ("Excellent dielectric properties ... suggest that HfO_2 is a promising material for the future gate dielectric application.").)

153. Thus, a POSITA would have been motivated to use high-k material for the gate film, such as the hafnium oxide disclosed by Kamata or otherwise known in the art, for a semiconductor device. Kamata therefore teaches limitation 1[a]: "a gate insulating film formed on an active region in a substrate and including Hf." (See, e.g., Kamata, Ex.1027, ¶73 (referring to "gate insulating film 2"), ¶¶8-10 (showing the semiconductor device includes "a gate insulating film formed on a surface of the silicon substrate"), claim 1.) At a minimum, limitation 1[a] is obvious.

c. Limitation 1[b]: "a gate electrode formed on the gate insulating film;"

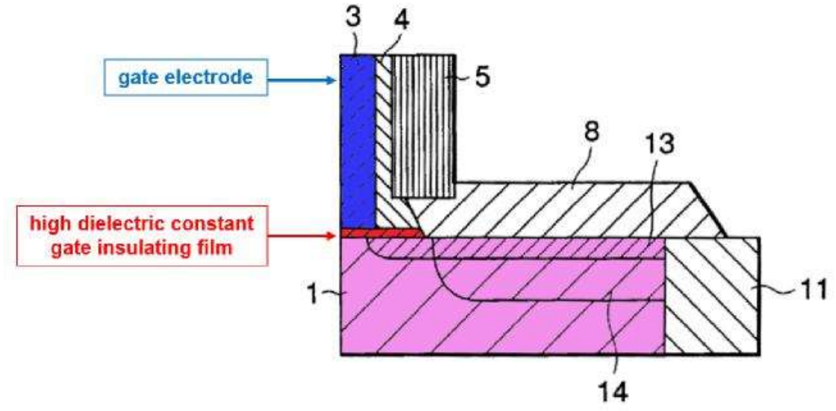
154. Kamata's first, fourth, and ninth embodiments each disclose limitation 1[b]: "a gate electrode formed on the gate insulating film." Kamata teaches "forming a gate electrode on the gate insulating film." (Kamata, Ex.1027, ¶24; *see also, e.g.*, Kamata, Ex.1027, ¶¶8-11, claim 1 (reciting device with "gate electrode formed on the gate insulating film")).

155. As seen in the annotated figures, the semiconductor devices of Kamata have a gate electrode 3 (shaded blue) formed on gate insulating film 2 (the "high dielectric constant gate insulating film," shaded red). (Kamata, Ex.1027, ¶50 ("Then, a gate electrode 3 is formed by depositing polycrystalline silicon (FIG. 1A(b)) and, after a lithography step, the gate electrode is processed by means of an anisotropic etching technique using plasma such as RIE (reactive ion etching (FIG. 1A(c))."); *see also* Kamata ¶¶68, 94, Figures 1A(a)-(c).)



**Kamata, Figures 1B(j)
(First Embodiment)**

**Kamata, Figure 5(c)
(Fourth Embodiment)**



Kamata, Figure 10(b)

(Ninth Embodiment)

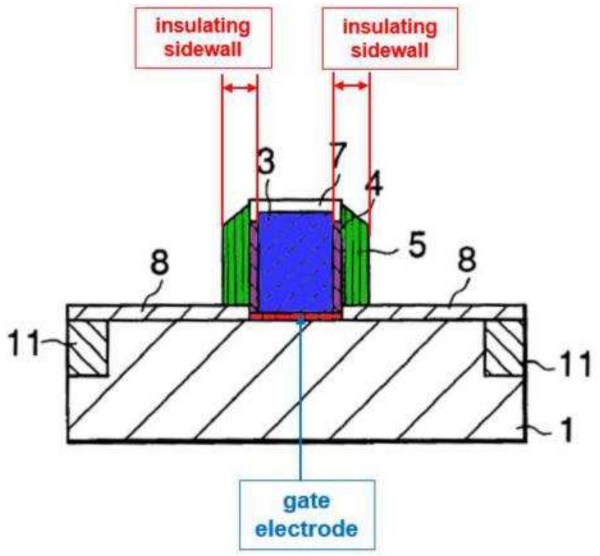
d. Limitation 1[c]: "a insulating sidewall formed on each side surface of the gate electrode;"

156. Kamata's first, fourth, and ninth embodiments each teaches limitation 1[c]: "a insulating sidewall formed on each side surface of the gate electrode."

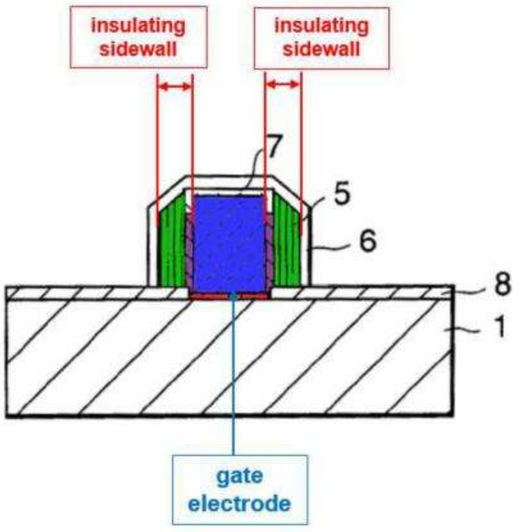
157. Kamata discloses "forming a first insulating film to cover the gate insulating film and the gate electrode; forming a second insulating film on the first insulating film [and] selectively leaving the second insulating film on a side surface

of the gate electrode with the first insulating film interposed therebetween . . . .” (Kamata, Ex.1027, ¶¶25-27; *see also* claim 1). Kamata calls these insulating films “sidewall films” 4 and 5. (See Kamata, Ex.1027, ¶¶57 (referring to film 5 as “sidewall film 5”), 74 (referring to film 4 as “sidewall film 4”).) Specifically, sidewall film 4 is a silicon oxide film (see, e.g., Kamata, Ex.1027, ¶58 (referring to “silicon oxide film 4”), and sidewall film 5 is a silicon nitride film. (See Kamata, Ex.1027, ¶¶50 (referring to “silicon nitride film (Si3N4) 5”).) A POSITA is well aware that silicon oxide and silicon nitride films are insulators, particularly when used as sidewall films. (Wolf Vol 4., Ex. 1214, 9, 75; Plummer, Ex.1215, 79-80.)

158. Sidewall film 4 and sidewall film 5 are collectively the “insulating sidewall,” consistent with the ’076 patent. The ’076 patent refers to an “insulating sidewall” broadly to cover multiple sidewall structures, including a single component (6:3-4), a composition of two components (2:58-63), and as a composition having multiple layers (20:43-52).



Kamata, Fig. 1B(j)
(First Embodiment)



Kamata, Fig. 5(c)
(Fourth Embodiment)

159. Figure 10(b), annotated below, shows Kamata's ninth embodiment device similarly includes sidewall film 4 (shaded purple) and sidewall film 5 (shaded green). These films together are the claimed insulating sidewall formed on the gate electrode's side surfaces (shaded blue). (See Kamata, Ex.1027, ¶¶8-16, 57, 74; see also Kamata, Ex.1027, ¶¶50, 58, 94.[1])

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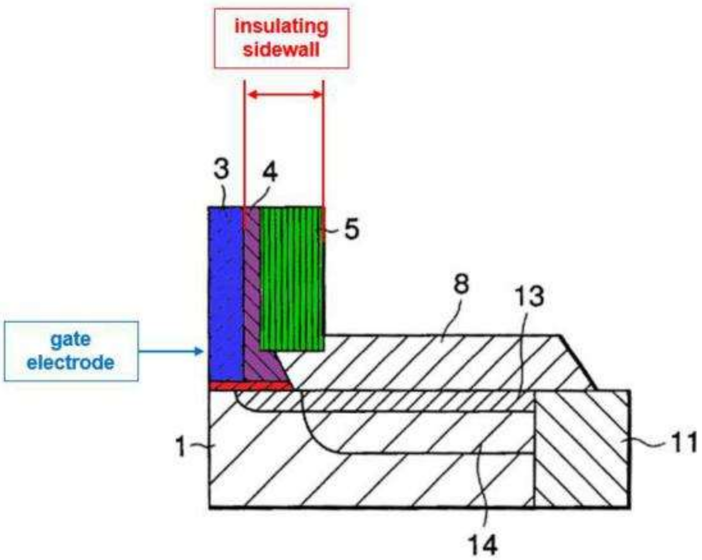
[1] Although Figure 10(b) shows only one sidewall of the semiconductor device of Kamata's ninth embodiment, a POSITA would understand that the device includes the same corresponding structure on the other surface of the gate electrode.



Kamata, Fig. 10(b)

(Ninth Embodiment)

e. Limitation 1[d]: "wherein a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length,"

160. The semiconductor devices of Kamata's first, fourth, and ninth embodiments each teaches Limitation 1[d]: "wherein a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length."

161. In the first and fourth embodiment, semiconductor devices (Figures 1B(j) and 5(c)), the width of high-k gate insulating film 2 along the gate length[2]

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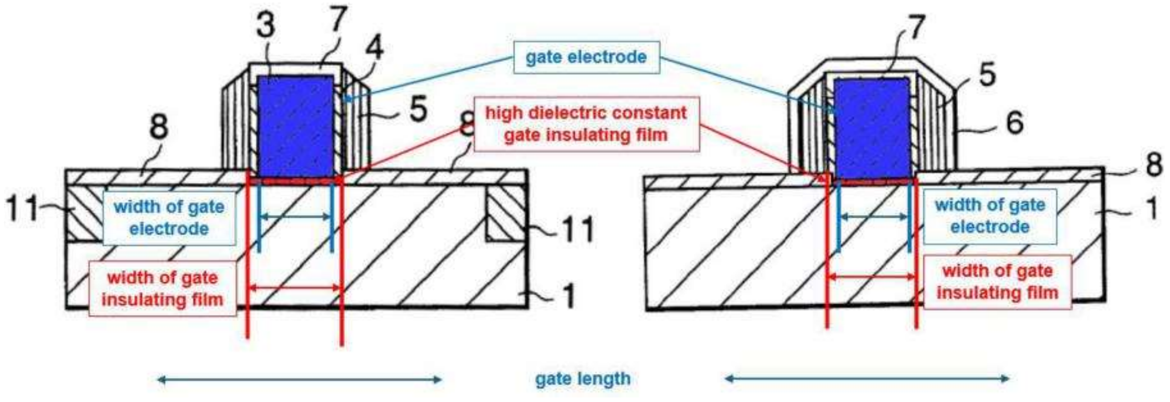
[2] The '076 patent uses the term "along the gate length" to refer to a direction, specifically from the source to the drain regions.

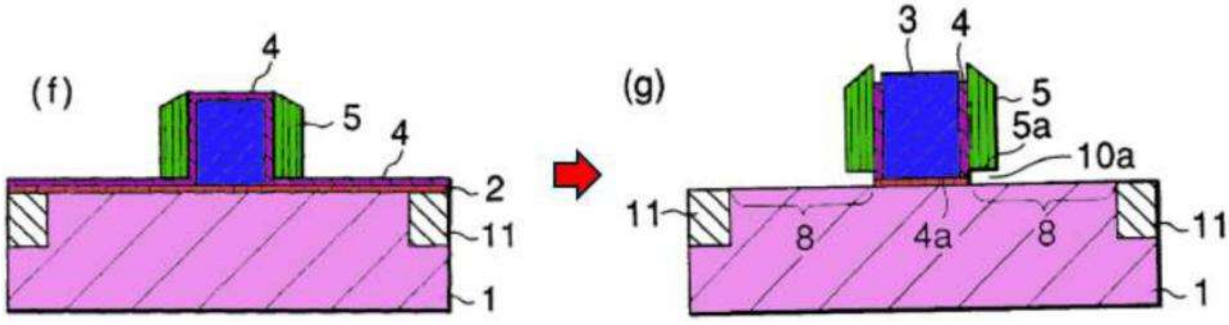
(shaded red), is larger than the width of gate electrode 3 (shaded blue).



Kamata, Fig. 1B(j) (First Embodiment)

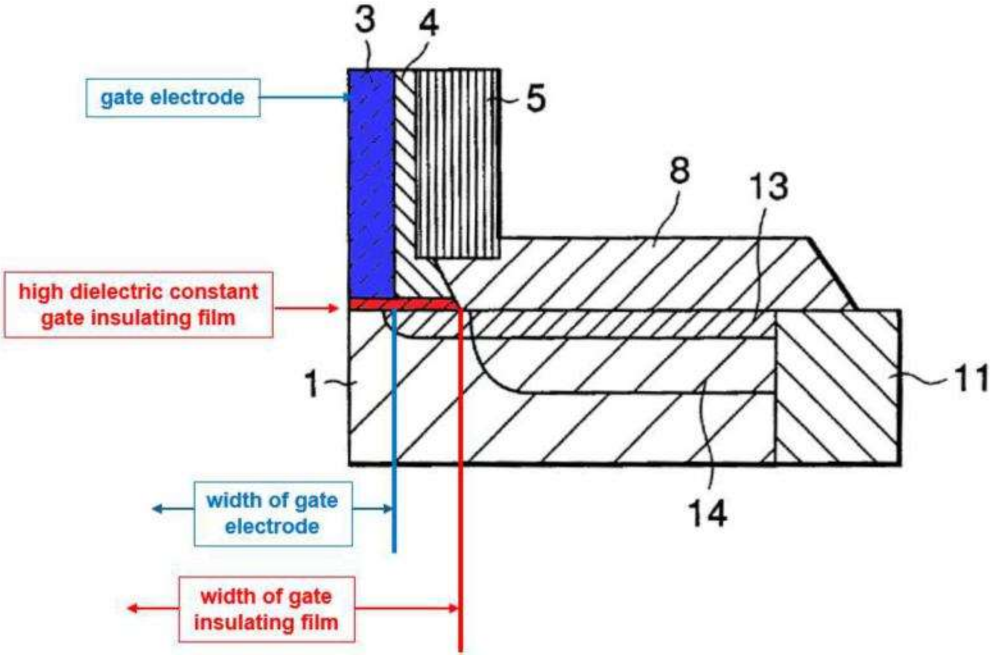
Kamata, Fig. 5(c) (Fourth Embodiment)

162. Kamata's manufacturing process confirms this structure. Gate electrode 3 and sidewall film 5 are first formed on silicon oxide film 2 and sidewall film 4, and subsequently, silicon oxide film 2 and sidewall film 4 are etched together. This structure results in gate insulating film 2 extending underneath the gate electrode as well as underneath sidewall film 4, as shown in Figures 1A(f) and 1B(g) below. (See Kamata, Ex.1027, ¶¶50, 56 (discussing formation of gate electrode 3 and sidewall films 4 and 5), 68 (fourth embodiment).)



Kamata, Fig. 1A(f) (annotated left), Fig. 1B(g) (annotated right)

163. As seen below for the ninth embodiment, the high-k film 2 (shaded red) protrudes from underneath the gate electrode 3 to underneath both sidewall films 4 and 5. (See Kamata, Ex.1027, ¶¶50 (describing formation of gate electrode 3), 93 (describing forming deep diffusion region 14 after forming sidewalls), 94, Figure 10(b) (below).) While Figure 10(b) only shows one side of the gate electrode, a POSITA would have understood that the other side has similar structure. Accordingly, the width of high-k film 2 along the gate length (shaded red) is larger than the width of the gate electrode (shaded blue).



Kamata, Fig. 10(b)

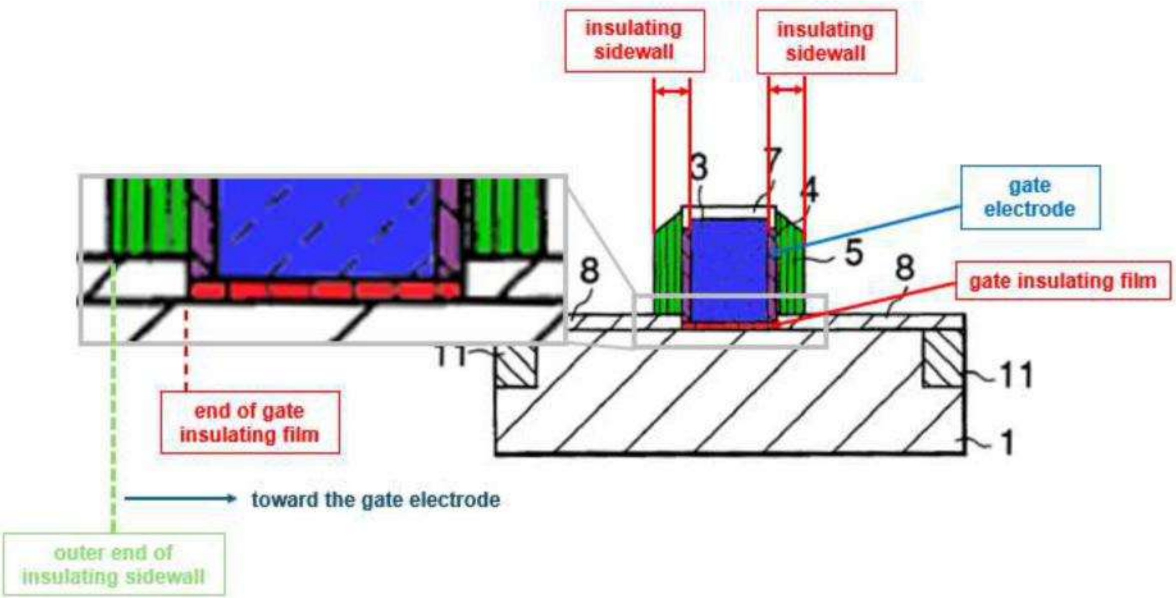
(Ninth Embodiment)

f. Limitation 1[e]: "an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode."

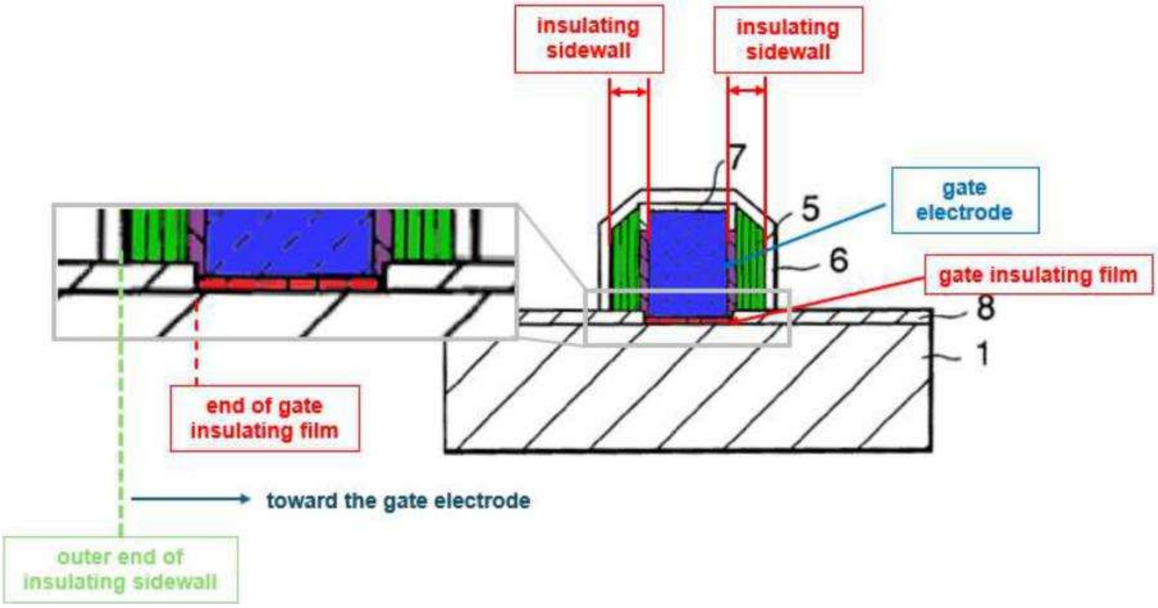
164. The devices of Kamata's first, fourth, and ninth embodiments each disclose "an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode."

165. It is important to note that the claim term "retract" first appeared in claim 21 of the application leading to the '076 patent, which ultimately issued as claim 1. The term "retract" does not appear in the '076 patent specification, or any of the other patents in the same family.

166. In Kamata's first and fourth embodiments, shown in Figures 1B(j) and 5(c) below, the high-k gate insulating film 2 is a continuous layer extending from underneath the gate electrode (shaded blue) to underneath the insulating sidewall film 4 (shaded purple), which together with insulating sidewall film 5, forms the claimed "insulating sidewall." (Kamata, Ex.1027, ¶¶50 and 56 (together describing formation of gate electrode 3 and sidewalls 4 and 5), 68 (fourth embodiment).)



Kamata, Fig. 1B(j) (with enlargement)
(First Embodiment)

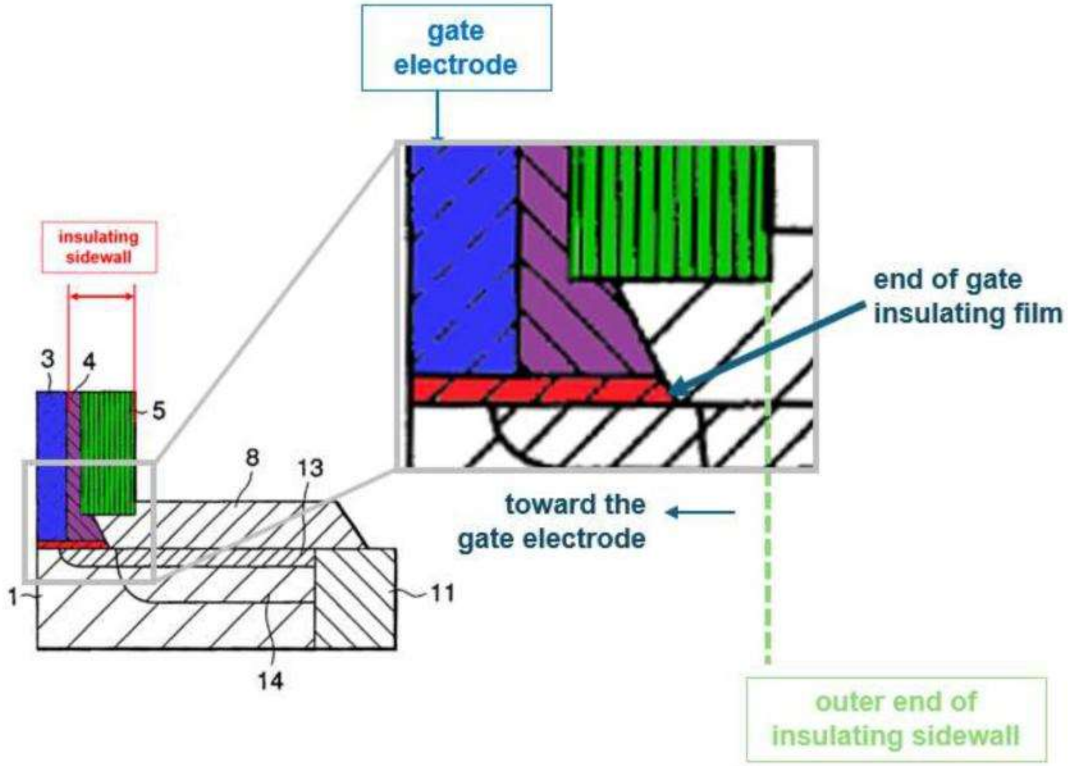


Kamata, Fig. 5(c) (with enlargement)

(Fourth Embodiment)

167. In Kamata's first and fourth embodiments, the end of the gate insulating film is perpendicular to the substrate surface and is located inward from the end of sidewall film 5 (the outer end of the "insulating sidewall") toward the gate electrode. Thus, the end of the high-k gate dielectric teaches "an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode."

168. Kamata's ninth embodiment meets this limitation 1[e] as well. As seen in Figure 10(b) the high-k gate insulating film 2 is also a continuous layer extending from underneath the gate electrode (shaded blue) to underneath sidewalls 4 (shaded purple) and 5 (shaded green), which are collectively the "insulating sidewall." (Kamata, Ex.1027, ¶¶50 and 56 (together describing formation of gate electrode 3 and sidewall 5), 93 (describing deep diffusion region 14 formation after sidewall film formation), 94.)



Kamata, Fig. 10(b) (with enlargement)

(Ninth Embodiment)

169. The gate insulating film does not extend to the outer end of the sidewall. Instead, the end of gate insulating film 2 (shaded red) is tapered and located a distance inward from the end of sidewall toward the gate electrode. Thus, the end of high-k gate dielectric in the ninth embodiment meets limitation 1[e]: "retracted from an outer end of the insulating sidewall toward the gate electrode."

2. Dependent Claim 2: "The semiconductor device of claim 1, further comprising a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film."

170. Kamata's first, fourth, and ninth embodiments each disclose the limitations of claims 2: "further comprising a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film."

171. Kamata teaches that "[i]t is desired that a SiO_x ($0<x\leqq2$) layer ... is interposed between the gate insulating film and the silicon substrate." (Kamata, Ex.1027, ¶¶54, 68 (relating fourth embodiment to first embodiment), 94 (relating ninth embodiment to first embodiment).) This SiO_x layer is a "buffer insulating film" made of "silicon oxide" and is located between the substrate and the high-k gate insulating film 2.

3. Dependent Claim 3: "The semiconductor device of claim 1, wherein the gate insulating film is formed of a Hf based oxide."

172. Kamata's first, fourth, and ninth embodiments each teaches or renders obvious the limitations of claim 3: "wherein the gate insulating film is formed of a Hf based oxide."

173. Kamata specifically discloses the gate insulating film may be made with "a high dielectric constant film such as an oxide film with higher dielectric constant than the silicon oxide, containing at least an element selected from a group of Ti, Zr, Hf, Ta, La, Al Ba, Sr, Y, Pr and Gd, and a silicate film containing such an

element." (Kamata, Ex.1027, ¶52). As one exemplary material, Kamata teaches that "[t]he film may be . . . HfO_2." (Kamata, Ex.1027, ¶53.) HfO_2 is a "Hf based oxide."

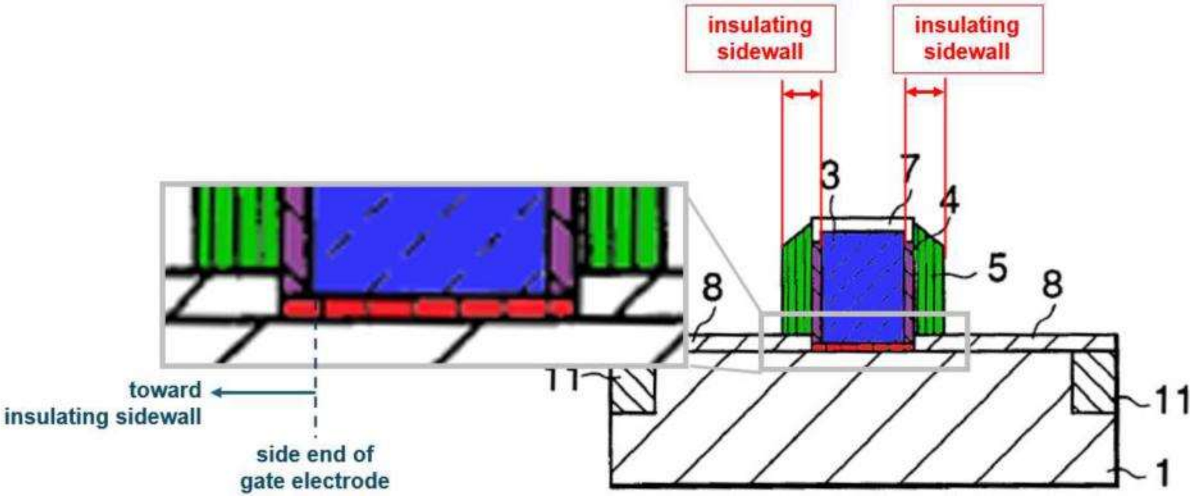
174. As explicitly suggested by Kamata, a POSITA would have been motivated to use a Hf-based oxide as a high-k gate insulating film for semiconductor devices. By 2005, i.e., the earliest priority date of the '076 patent, a POSITA was well aware that hafnium-based gate dielectrics, including HfO_2, was a popular high-k material. HfO_2 was known to have superior thermal stability and band gap alignment. (See, e.g., Lee-2000, Ex.1337, 2.4.1 ("Recently, HfO_2 films have emerged as the most promising gate dielectric material for sub 100nm technology due to its superior thermal stability with poly-Si and reasonable band alignment ...."); Houssa, Ex.1213, 207 (HfO_2 "combines a high k (15–26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ..."); Lee-1999, Ex.1349, 134 ("Excellent dielectric properties such as high dielectric constant, low leakage current, good thermal stability, negligible dispersion and excellent reliability were demonstrated. These results suggest that HfO_2 is a promising material for the future gate dielectric application.").)

4. Dependent Claim 7: "The semiconductor device of claim 1, wherein an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall."

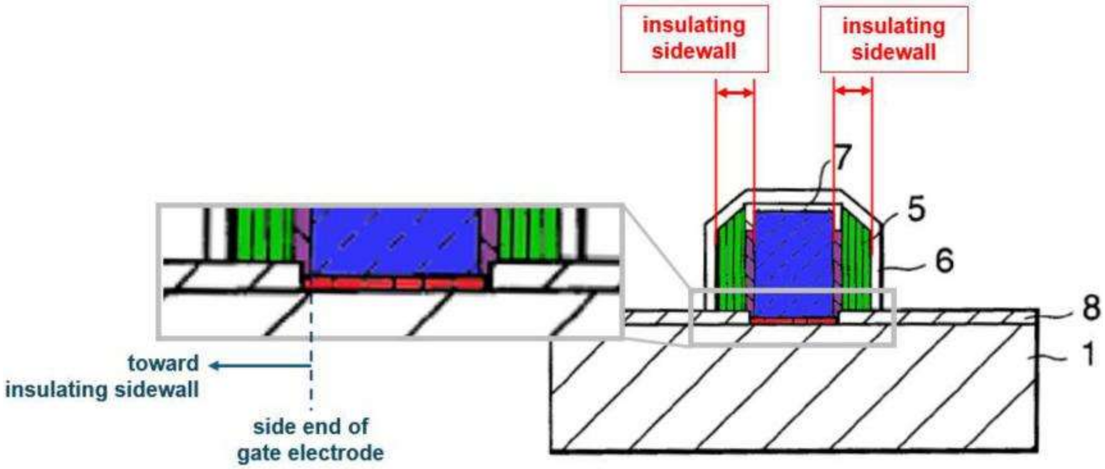
175. Kamata's first, fourth, and ninth embodiments each teaches the limitations of claim 7: "wherein an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall."

176. As discussed above for limitation 1[d], the end of the high-k gate insulating film protrudes a distance outward from the gate electrode and towards an outer end of the sidewall. And specifically, the end of the high-k gate insulating film extends from underneath the gate electrode to underneath the sidewall, with the distance between the end of the gate insulating film and the sidewall being set by Kamata's fabrication process, including the width of sidewall films 4 and 5.

177. Starting with the first and fourth embodiment devices, as discussed above for limitation 1[d], the end of high-k gate insulating film 2 is perpendicular to the substrate surface and is not coextensive with the outer end of sidewall film 5. Instead, the end of the gate insulating film is located at a distance inward from the outer end of sidewall film 5, as well as a distance outward from the gate electrode. Thus, the end of gate insulating film 2 in the first and fourth embodiments meet the limitation of claim 7 "wherein an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall," consistent with the '076 patent and Applicant's prosecution statements. (Ex.1001, 20:63-21:7.)



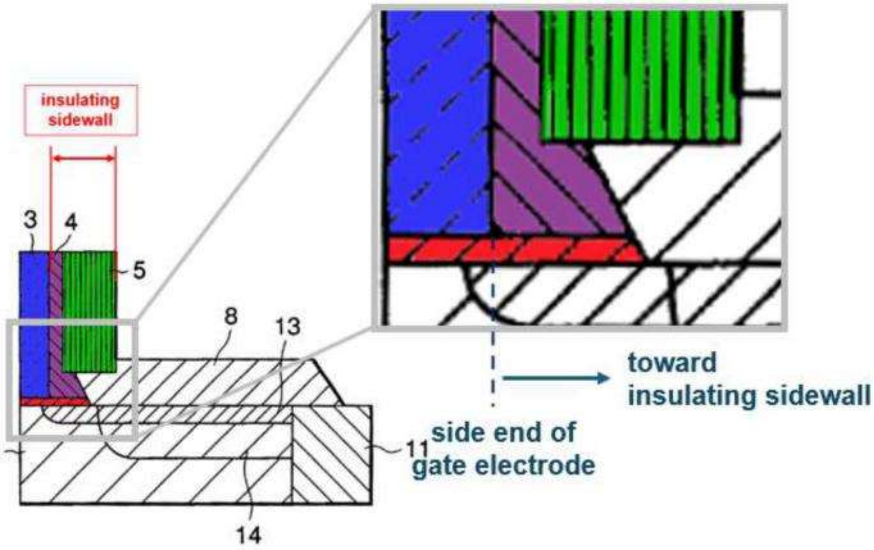
Kamata, Figure 1B(j) with enlargement



Kamata, Figure 5(c) with enlargement

178. For the ninth embodiment, the end of gate insulating film 2 is tapered, but it is also similarly located at a distance inward from the outer end of the sidewall film 5, as well as a distance outward from the gate electrode. The end of high-k gate dielectric in the ninth embodiment "protrudes from a side end of the gate electrode

toward the insulating sidewall," consistent with the '076 patent and Applicant's prosecution statements. (Ex.1001, 20:63-21:7.)



Kamata, Figure 10(b) with enlargement

5. Dependent Claim 8: "The semiconductor device of claim 1, wherein the insulating sidewall has a double layer structure including an oxide film and a nitride film."

179. Kamata's first, fourth, and ninth embodiment devices each discloses the limitations of claim 8: "wherein the insulating sidewall has a double layer structure including an oxide film and a nitride film." As discussed above for limitation 1[c], the "insulating sidewall" includes sidewall film 4, which is a silicon oxide film, and sidewall film 5, which is a silicon nitride film. (Kamata, Ex.1027, ¶¶50, 58.) To the extent this is not an explicit disclosure, a POSITA would understand sidewall films 4 and 5 are each a "layer" of the insulating sidewall, consistent with the '076 patent.

(See Kamata, Ex.1027, ¶¶16 (referring to "multilayer type sidewall films"), 50, 58; Ex.1001, 20:43-52.)

6. Dependent Claim 10: "The semiconductor device of claim 1, wherein a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length."

Dependent Claim 13: "The semiconductor device of claim 1, wherein the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length."

180. The semiconductor devices of Kamata's first, fourth, and ninth embodiments each teaches claims 10 and 13: "a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length" [claim 10] and "the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length" [claim 1313].

181. In the first and fourth embodiment semiconductor devices (Figures 1B(j) and 5(c)), the width of high-k gate insulating film 2 along the gate length[3] (shaded red), is larger than the width of gate electrode 3 (shaded blue).

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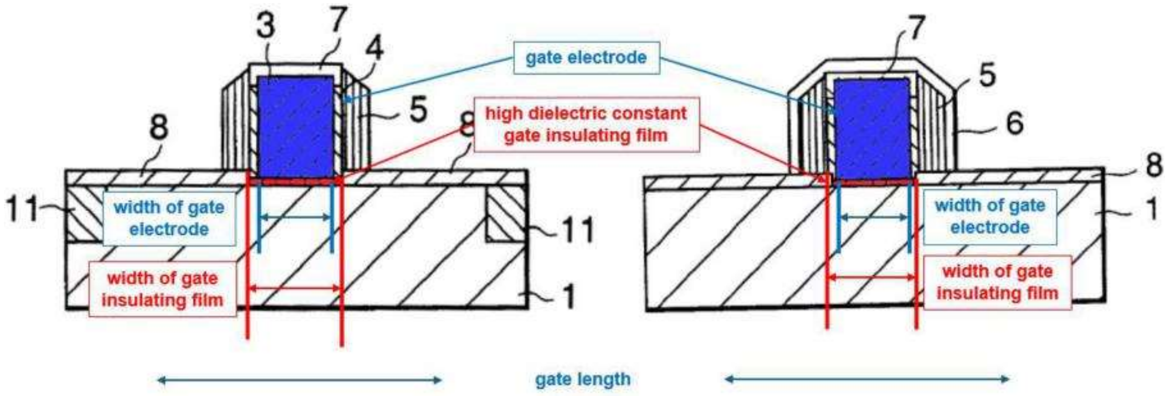
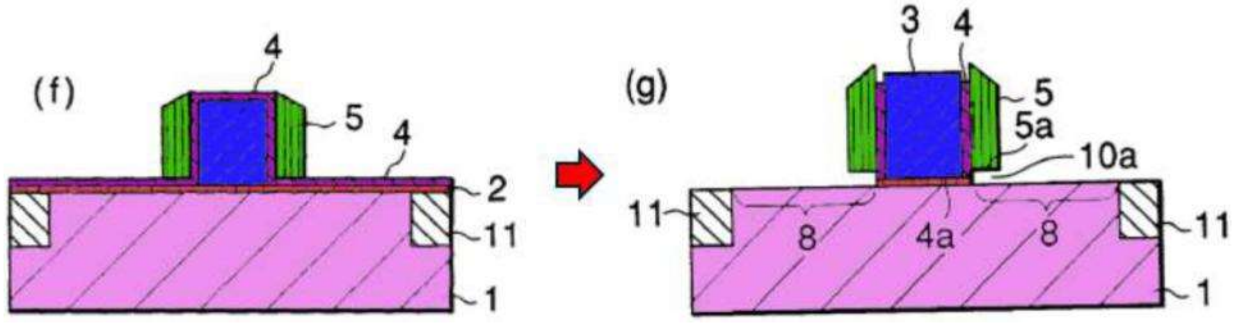
[3] The '076 patent uses the term "along the gate length" to refer to a direction, specifically from the source to the drain regions.



Kamata, Fig. 1B(j) (First Embodiment)

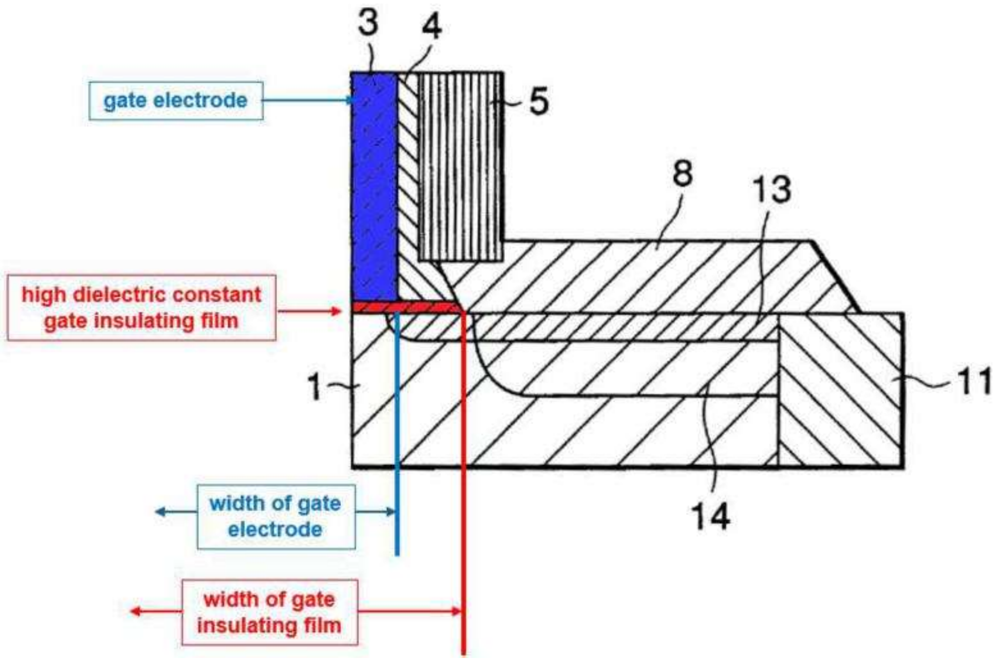
Kamata, Fig. 5(c) (Fourth Embodiment)

182. Kamata's manufacturing process confirms this structure. Gate electrode 3 and sidewall film 5 are first formed on silicon oxide film 2 and sidewall film 4, and subsequently, silicon oxide film 2 and sidewall film 4 are etched together. This structure results in gate insulating film 2 extending underneath the gate electrode as well as underneath sidewall film 4, as shown in Figures 1A(f) and 1B(g) below. (See Kamata, Ex.1027, ¶¶50, 56 (discussing formation of gate electrode 3 and sidewall films 4 and 5), 68 (fourth embodiment).)



Kamata, Fig. 1A(f) (annotated left), Fig. 1B(g) (annotated right)

183. As seen below for the ninth embodiment, the high-k film 2 (shaded red) protrudes from underneath the gate electrode 3 to underneath both sidewall films 4 and 5. (See Kamata, Ex.1027, ¶¶50 (describing formation of gate electrode 3), 93 (describing forming deep diffusion region 14 after forming sidewalls), 94, Figure 10(b) (below).) While Figure 10(b) only shows one side of the gate electrode, a POSITA would have understood that the other side has similar structure. Accordingly, the width of high-k film 2 along the gate length (shaded red) is larger than the width of the gate electrode (shaded blue). Claim 13 refers to the width of the gate electrode in the middle position of height. While the figures in Kamata show perfectly vertical sidewalls of the gate electrode, a POSITA would know that these are schematic drawings, and that in practice there will be a slight tapering of the gate electrode due to the finite anisotropy of the Reactive Ion Etching (RIE) of the gate electrode. Hence, the width of the gate electrode in the middle position of height will be slightly less than at the bottom of the gate electrode. Because the gate insulating film is wider than the gate electrode at the bottom, it will also be wider than the gate electrode in the middle portion.



Kamata, Fig. 10(b)

(Ninth Embodiment)

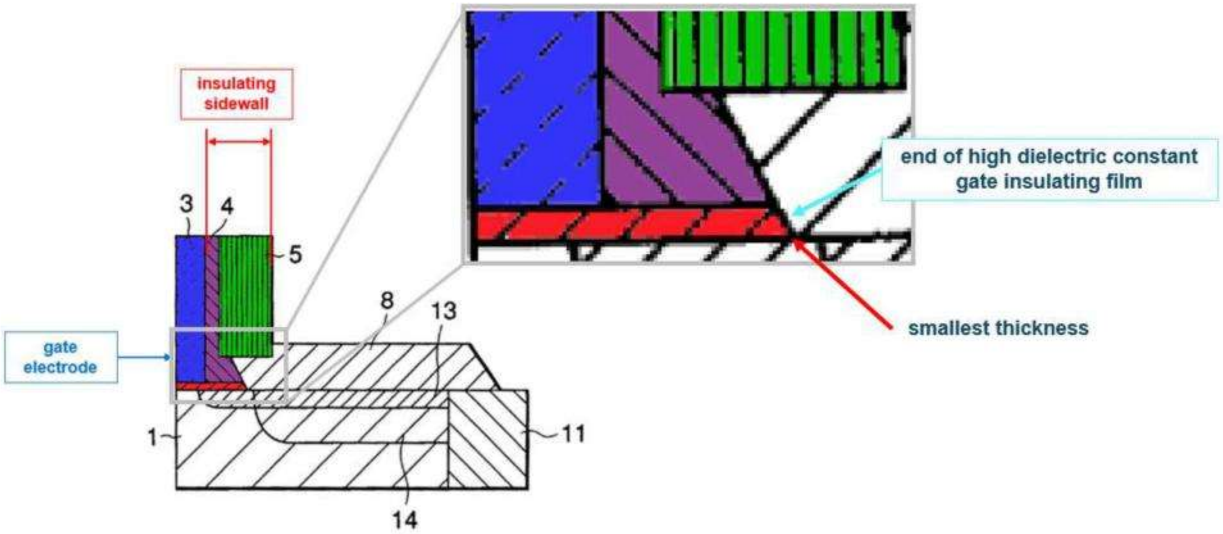
7. **Dependent Claim 11: "The semiconductor device of claim 1, wherein the end of the gate insulating film located under the insulating sidewall has a tapered surface."**

Dependent Claim 12: "The semiconductor device of claim 1, wherein the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof."

184. Claims 11 and 12 relate to the thickness and shape of the high-k gate insulating film. Kamata's ninth embodiment discloses the limitations of dependent claims 11 and 12.

185. As shown in Figure 10(b), gate insulating film 2 extends underneath the gate electrode to underneath sidewall films 4 and 5 (together the claimed "insulating sidewall"), but the end of the gate insulating film 2 tapers down in thickness. The

thickness of the film at the end is smaller than the thickness underneath the gate electrode.



Kamata, Fig. 10(b) (with enlargement)

(Ninth Embodiment)

186. Further, the thickness of the gate insulating film becomes "smaller toward the end," [claim 12] which also discloses an end having "a tapered surface," [claim 11]. (See Kamata, Ex.1027, ¶93; see also Kamata, Ex.1027, ¶¶18, 85 (describing formation of slanted surfaces in embodiment having same slanted gate dielectric and slanted epitaxially grown film 8).) If the Patent Owner claims that one cannot depend on the figures alone to meet these claims, a POSITA would know that an RIE process never achieves infinite anisotropy. Hence, for a finite anisotropy, RIE using a mask will always lead to narrower width at the top of the layer being

etched, compared to the bottom of the layer, leading to the sort of tapering shown in the Kamata figures.

B. Ground II

187. In my opinion, the combination of Kamata and Sim renders obvious Challenged Claim 6 of the ’076 patent (Ground II).

1. Dependent Claim 6: “The semiconductor device of claim 1, wherein a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.”

188. While Kamata discloses HfO_2 as a high-k gate insulating film (see Kamata, Ex.1027, ¶53), it does not specify that the film “has a thickness of 2 nm or less” as recited by claim 6. Sim discloses this limitation, as I discuss further below. The combination of Kamata (first/fourth/ninth embodiments) and Sim thus meet the limitation of claim 6: “wherein a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.”

189. Sim is titled “Effects of ALD HfO_2 thickness on charge trapping and mobility,” and was published on June 17, 2005. Sim studied the use of high-k dielectrics in semiconductor devices, including specifically HfO_2. (Sim, Ex.1024, Abstract (“Scaling the physical thickness of the HfO_2 dielectric causes less charge trapping and higher mobility.”).) Sim is thus related to and in the same field as Kamata and the ’076 patent. (Ex.1001, 1:17-18 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”);

Kamata, Ex.1027, ¶3 ("This invention relates to a semiconductor device and a method of manufacturing the same.").)

190. Sim teaches a gate insulating film having a thickness 2 nm or less. Sim describes that "[h]afnium-based high-k dielectrics and metal gate electrodes have been aggressively investigated to ensure continued scaling of CMOS technology, but several drawbacks such as low mobility and charge trapping have been identified." (Sim, Ex.1024, 218.) Sim examined these advantages and drawbacks by testing different thickness films, "systematically evaluat[ing] the effects of high-k film thickness on charge trapping and channel carrier mobility." (Sim, Ex.1024, 218.) Sim concluded that "scaling the high-k dielectric is a simple, but very effective means of improving mobility and other reliability characteristics," and "[e]ven within 100μs, a 33Å HfO_2 sample shows significant current reduction while a 18Å HfO_2 sample is free from transient charging within the detection limits." (Sim, Ex.1024, 218-219.) Sim further concluded that "[s]caling the physical thickness of the HfO_2 dielectric to below 20Å causes less charge trapping and higher mobility." (Sim, Ex.1024, 221.) 20Å or Angstroms is equal to 2 nm, as required by claim 11.

191. Applying Sim disclosure that using HfO_2 as the gate dielectric with a thickness less than 20 Angstroms to Kamata's first, fourth, and ninth embodiments meets the limitations of claim 6. Moreover, Kamata's ninth embodiment discloses tapering the thickness of the gate insulating film at the ends, which would be even

smaller in thickness than the gate film underneath the gate electrode. Thus, the combination of Kamata and Sim teaches "wherein a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less."

192. A POSITA would have been motivated to use Sim's gate insulating film with a thickness of 20Å (2 nm) or less to Kamata. Kamata specifically discloses hafnium oxide as an exemplary high-k gate dielectric, the same film studied in Sim. And Sim concludes that reducing hafnium oxide to below 20Å enhances mobility and reduces charge trapping, which improves performance and scalability of semiconductor devices. (Sim, Ex.1024, 219, 221.) Both Kamata and Sim emphasize these goals. (Kamata, Ex.1027, ¶5; Sim, Ex.1024, 218.) A POSITA would also expect success in combining Sim and Kamata, as the atomic layer deposition (ALD) process from Sim is a well-established gate film manufacturing method (and compatible with Kamata's fabrication methods). By 2005, ALD was a well-known and widely adopted manufacturing technique for depositing high-k material like HfO_2 as gate insulating films.

193. Thus, the combination would have been nothing more than the use of a well-known techniques and structures (Sim's ALD to make HfO_2 gate films with less than 20Å thickness) to improve similar devices (Kamata's semiconductor devices with a hafnium oxide gate dielectric) in a predictable manner. A POSITA would have had a reasonable expectation of success because Sim teaches a well-

known process, atomic layer deposition (ALD), for making high-k gate films. (Sim, Ex.1024, 218; Houssa, Ex.1213, 17-19.)

C. Ground III

194. In my opinion, Guha renders obvious Challenged Claims 1-3, 7-8, 10-13 of the ’076 patent (Ground III).

1. Independent Claim 1

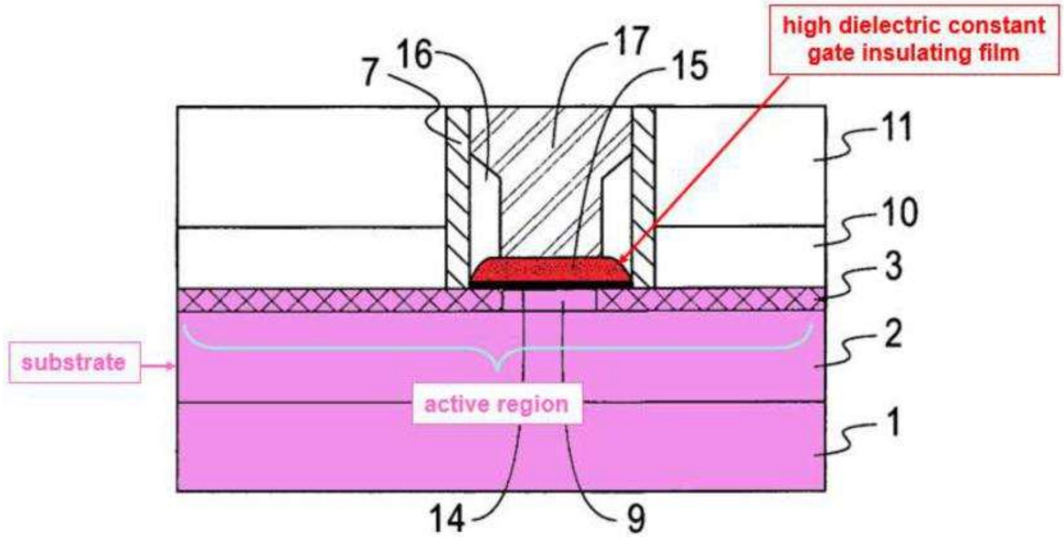
a. Preamble: “A semiconductor device comprising:”

195. Guha’s Figure 12 device is a “semiconductor device.” Guha describes MOSFETs, which is semiconductor device. (Guha, Ex.1028, ¶¶1 (“The invention relates to a MOSFET device having a damascene gate with an internal spacer structure and a process of forming the device.”), 4 (“The invention relates to a MOSFET with improved device performance and method of fabricating the device. ”).) Guha’s semiconductor device includes substrate 1 and channel layer 3, each “compris[ing] any semiconducting material.” (Guha, Ex.1028, ¶¶22-23, ¶¶43-45 (relating Figure 9’s first embodiment to Figure 12).

b. Limitation 1[a]: “a gate insulating film formed on an active region in a substrate and including Hf;”

196. Guha’s semiconductor device meets limitation 1[a] and includes a gate insulating film formed on an active region in a substrate and including Hf. Guha manufactures “an initial stacked structure that comprises a substrate 1 having a bottom insulator 2, also referred to as buried oxide layer, located thereon. The initial

stacked structure also includes a channel layer 3 on top of the bottom insulator 2, and an oxide layer 4, also referred to as pad protection layer, located atop the channel layer 3." (Guha, Ex.1028, ¶21). Substrate 1 "may be of the n or p-type depending on the desired device to be fabricated." (Guha, Ex.1028, ¶22; see also Ex.1028, ¶43.)[4] Channel layer 3 is manufactured over buried oxide layer 2, which alternatively "can be omitted." (Guha, Ex.1028, ¶22; see also Guha, Ex.1028, ¶43.) Guha's substrate 1, channel layer 3, and buried oxide layer 2 (if present) are collectively the claimed "substrate" (shaded pink below).



Guha, Fig. 12 (annotated)

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[4] At paragraph 43, Guha indicates that the Figures 10-12 embodiment is built on the device shown in Figure 7. As such, my discussion of these preceding figures applies to Figure 12 as well. (Guha, Ex.1028, ¶43).

197. Guha teaches that "the substrate may further contain active device regions." (Guha, Ex.1028, ¶22; see also Guha, Ex.1028, ¶43.) "[S]ource/drain extensions, also referred to as source/drain (S/D) junctions, are formed by implanting dopants through the pad protection layer 4 into the channel layer 3, with the dummy gate 5 acting as an implantation mask. Following ion implantation, the S/D extensions are annealed to activate dopants. A channel 9 (see FIG. 3), having a predetermined channel length substantially equal to the length of the dummy gate 5, is thus defined between the S/D extensions." (Guha, Ex.1028, ¶26; see also Ex.1028, ¶43.) Thus, a POSITA would have understood that Guha's device has "an active region in a substrate," and that a portion of channel layer 3 forms the active region.

198. Guha's Figure 12 includes another optional layer, gate-isolating layer 14 (shaded black above) formed on the "active region in a substrate." Dielectric layer 15 (shaded red), "comprising a high-k dielectric material," is "formed only on the gate-isolating layer 14" on the active region. (Guha, Ex.1028, ¶¶37¬38, 43.) "A high-K material is a material that exhibits a dielectric constant of approximately above 10 or more. Examples of such materials, include, but are not limited to hafnium oxide, hafnium silicate, aluminum oxide or zirconium oxide." (Guha, Ex.1028, ¶38; see also Guha, Ex.1028, ¶43 ("This can be achieved, for example, by a directional deposition process such as thermal evaporation of a metal such as hafiium [sic], zirconium, aluminium [sic], among others, and subsequent chemical

conversion to a high-k dielectric such as metal oxides, silicates or other appropriate high-k materials, allowing a further reduction in sidewall capacitance").)

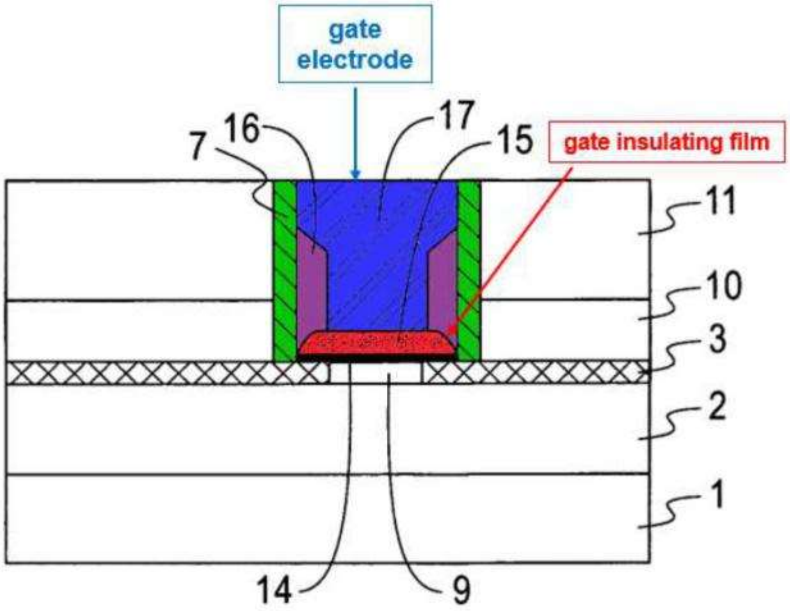
199. A POSITA would have been motivated to choose a hafnium-based gate dielectric, such as hafnium oxide or hafnium silicate, because of their known benefits, e.g., HfO_2's "superior thermal stability with poly-Si and reasonable band alignment," and HfSiON's "improved thermal stability and electrical characteristics." Lee-2000, Ex.1337, 2.4.1; Koyama, Ex.1029, 849; *see also see also* Houssa, Ex. 1213, 207 (HfO_2 "combines a high k (15–26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ..."); Lee-1999, Ex.1349, 134 ("Excellent dielectric properties ... suggest that HfO_2 is a promising material for the future gate dielectric application.").) Using high-k materials as the gate film was well known to a POSITA to solve known problems, particularly to address the well-understood issues with using silicon dioxide gate dielectrics as semiconductor devices continued to shrink in size. (See Houssa, Ex.1213, 3-12; Wolf Vol 4., Ex. 1214, 4-5, 146-47.)

200. Therefore, a POSITA would have understood Guha's dielectric layer 15 to be "a gate insulating film formed on an active region in a substrate and including Hf."

c. Limitation 1[b]: "a gate electrode formed on the gate insulating film;"

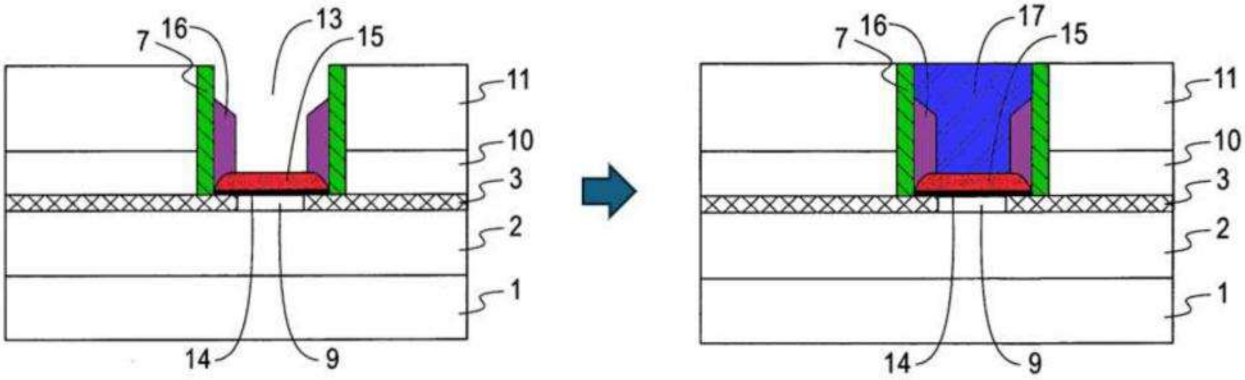
201. Guha's semiconductor device discloses limitation 1[b], a gate electrode formed on the gate insulating film. Guha forms gate electrode 17 by filling cavity 13 with conductive material. (Guha, Ex.1028, ¶45.) "[T]he conductive material may be formed from vapor phase deposition, such as tungsten or titanium nitride, or by depositing amorphous silicon and reacting it with a metal such as nickel to form a silicide, and subsequently thinning it down to the dielectric layer 15, and possibly removing the conductive material and the dielectric layer 15 lying outside of cavity 13, e.g., by CMP. Polysilicon may also be used, for example, either in-situ doped or doped by a conventional ion-implantation and annealing technique, as long as the annealing temperatures and conditions are compatible with the dielectric layer 15 and the second overlayer 11." (Guha, Ex.1028, ¶41). "[B]y means of the gate spacer structure 16, the interface between the bottom of the gate 17 and the dielectric layer 15 is better defined and offers a better control over the channel 9." (Guha, Ex.1028, ¶45.) Accordingly, a POSITA would have understood that gate 17 is "a gate electrode formed on the gate insulating film." (Guha, Ex.1028, ¶¶41, 45.)

202. As seen below, Guha shows gate electrode 17 (shaded blue) formed on high-k dielectric layer 15 (shaded red).



Guha, Fig. 12 (annotated)

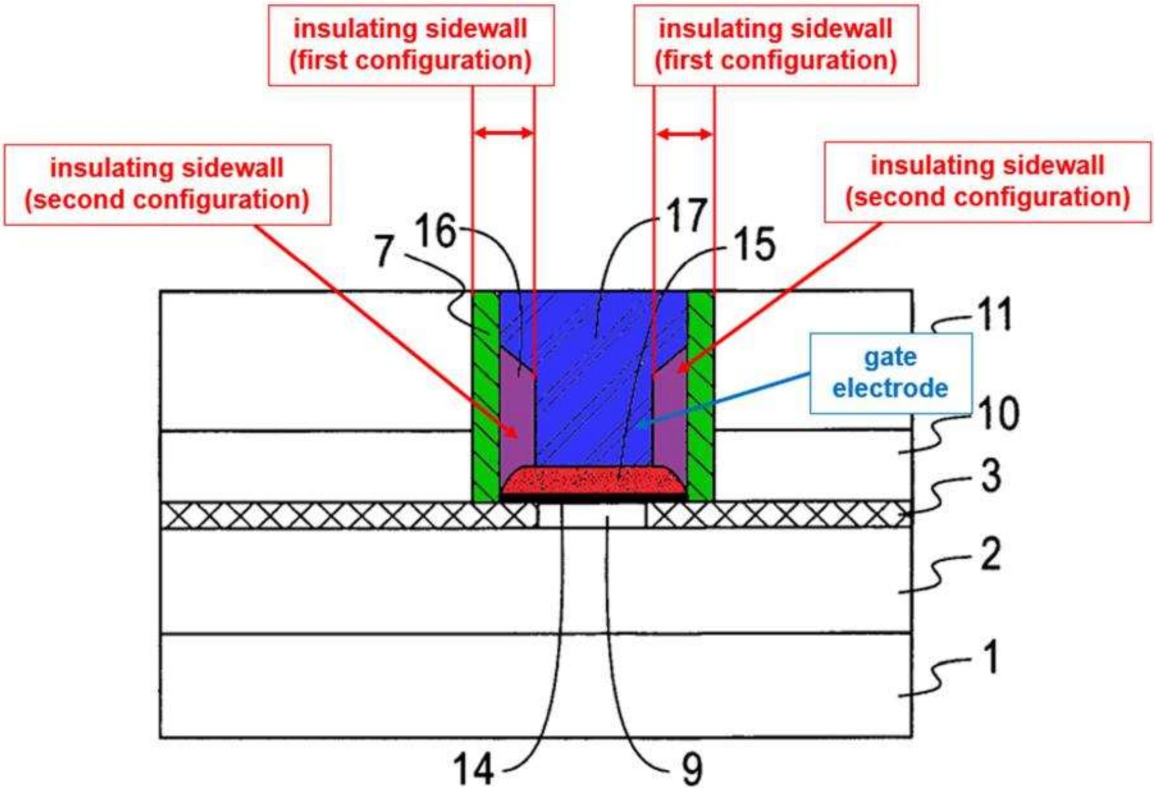
203. Guha's manufacturing process confirms this structure. Guha teaches that cavity 13 is "filled with a conductive material to form the gate 17" by "depositing the material into the cavity 13 and onto the dielectric layer 15." (Guha, Ex.1028, ¶¶41, 44 (associating gate formation in Figure 12 with first embodiment process), 45.) The gate electrode is thus formed over dielectric layer 15.



Guha, Figs. 11 (left) and 12 (right) (annotated)

d. Limitation 1[c]: "a insulating sidewall formed on each side surface of the gate electrode;"

204. Guha's Figure 12 discloses limitation 1[c], a insulating sidewall formed on each side surface of the gate electrode. (See Guha, Ex.1028, ¶¶28 (forming isolating spacers 7), 44 (forming spacers 16), 43 (associating Figure 12 to process steps of Figures 1-7).) Guha discloses a semiconductor device with gate spacers 16 (shaded purple) and isolating spacers 7 (shaded green) on the side surfaces of gate electrode 17 (shaded blue), as shown below.



Guha, Fig. 12 (annotated)

205. "Isolating spacer structure 7 can be composed of any insulating material including, for example, an oxide, nitride, oxynitride or any combination thereof; as

long as the material can be selectively etched with respect to the material of the dummy gate spacers 8. Isolating spacer structure 7 can be formed by deposition of an insulating material and subsequent etching. A preferred material would be silicon nitride." (Guha, Ex.1028, ¶¶28, 43.)

206. "'[I]nternal' gate spacers 16, or more generally, a gate spacer structure, is formed inside the cavity 13 . . . , for example, by depositing a spacer material, e.g. an oxide or other suitable material, in the cavity 13 and etching the deposited material anisotropically, e.g. by RIE, such that the portion of the dielectric layer 15 above channel 9 is exposed, leaving the gate spacer structure 16 on the sidewalls of the cavity 13. This arrangement of the gate spacer structure 16 provides a narrowing of the cavity 13 above the channel 9." (Guha, Ex.1028, ¶¶40, 43.) In Figure 12, "the gate spacer structure 16 contacts both the dielectric layer 15 and the isolating spacer structure 7." (Guha, Ex.1028, ¶44.)

207. Guha's spacers are synonymous with "sidewalls," as "spacer" and "sidewall" are often used interchangeably. A POSITA would also have understood Guha's spacers to be "sidewalls" as used in the '076 patent. (See, e.g., Guha, Ex.1028, ¶¶40 (describing "gate spacer structure 16 on the sidewalls of the cavity"), 44.)

208. Furthermore, as discussed previously, a POSITA would have understood gate spacers 16 and isolating spacers 7 to be insulating. Guha discloses

that gate spacers 16 are formed of "an oxide or other suitable material." (Guha, Ex.1028, ¶¶40, 43.) Specifically, "by means of the gate spacer structure 16, the interface between the bottom of the gate 17 and the dielectric layer 15 is better defined and offers a better control over the channel 9." (Guha, Ex.1028, ¶45.) In order to provide these specific benefits, a POSITA would have understood the gate spacers 16 to be made of an insulating material, like silicon oxide, rather than conductive material. That is to say, if gate spacer 16 was formed of a conductive material, it would function similar to the gate electrode (which it itself comprised of a semiconductor or conductive material), potentially removing any of the benefits disclosed in Guha of a separate gate spacer structure 16. A POSITA also knew that gate spacers are typically formed of an insulating material like silicon dioxide. (Wolf Vol 4., Ex. 1214, 9, 75; Plummer, Ex.1215, 79-80.)

209. Guha specifically discloses that isolating spacers 7 are "composed of any insulating material including, for example, an oxide, nitride, oxynitride or any combination thereof," with the "preferred material [being] silicon nitride." (Guha, Ex.1028, ¶¶28.)

210. As shown in Figure 12, gate spacer structure 16 and isolating spacer structure 7 collectively disclose limitation 1[c], an "insulating sidewall formed on each side surface of the gate electrode," consistent with the '076 patent. (Ex.1001,

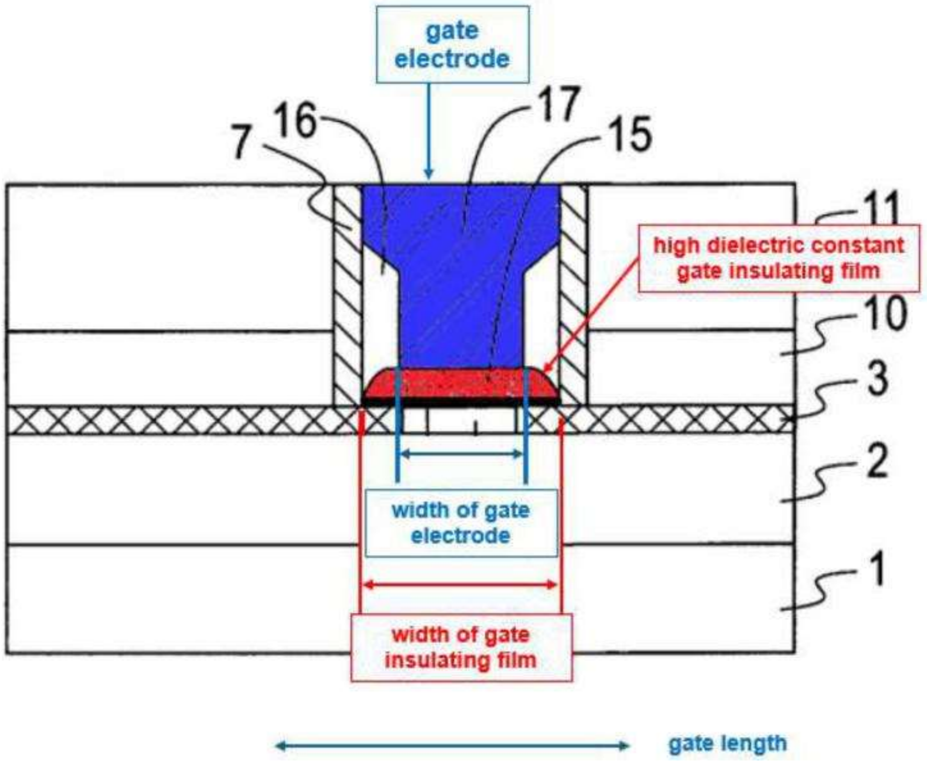
2:58-63 ("insulating sidewall" includes two sidewalls).) As discussed further below, I will refer to this as the first insulating sidewall configuration.

211. But Guha also discloses that isolating structure 7 is optional and may "not be necessary." (Guha, Ex.1028, ¶¶34-35; see also Guha, Ex.1028, ¶44 ("In other embodiments where the isolating spacer structure 7 is absent, the gate spacer structure 16 will contact the overlayer 11 instead.").) Where the isolating spacer structure 7 is absent, gate spacer 16 by itself is an "insulating sidewall formed on each side surface of the gate electrode" (limitation 1[c]), consistent with the '076 patent. (Ex.1001, 6:3-4 (disclosing "insulating sidewall" as a single component).) As discussed further below, I will refer to this as the second insulating sidewall configuration.

212. Both the first and second insulating sidewall configurations meet limitation 1[c].

e. Limitation 1[d]: "wherein a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length,"

213. Guha teaches the limitation 1[d]. As seen in Figure 12, the width of dielectric layer 15 (shaded red) is larger than the width of gate electrode 17 (shaded blue), thereby disclosing the limitations of claims 16 and 17. (Guha, Ex.1028, ¶¶41, 43-45 (describing formation of gate spacers 16 in the cavity followed by deposition of the gate electrode).)

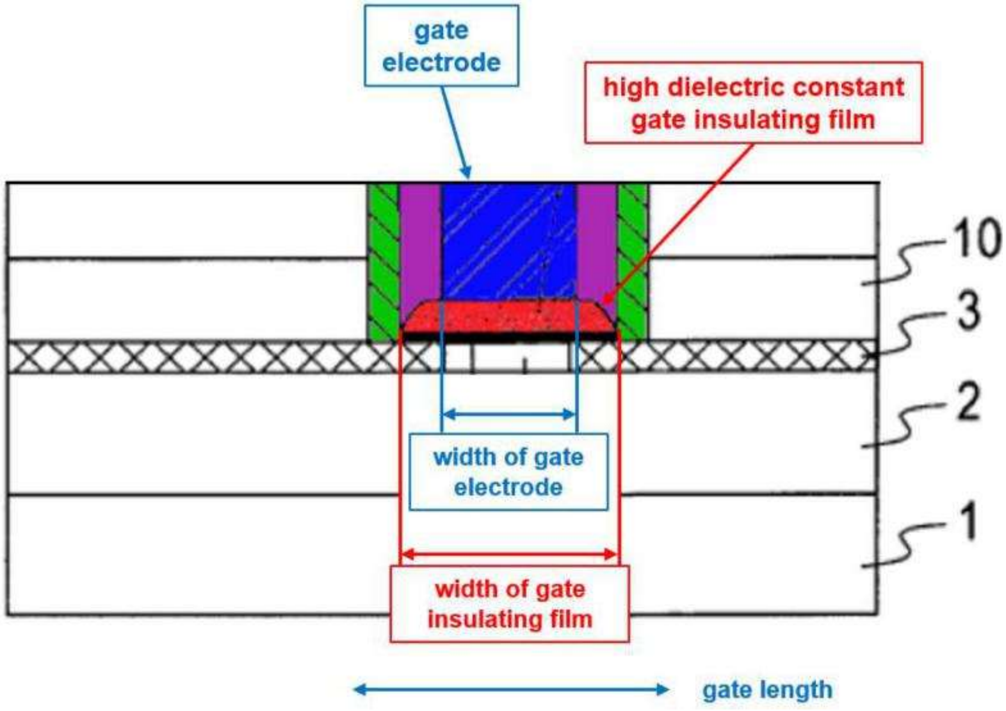


Guha, Fig. 12 (annotated)

214. If Patent Owner argues that the width of the gate electrode at the top of the electrode is equal to the width of dielectric layer 15, and therefore fails to disclose claim 1, I disagree. Claim 1 does not require that the width of the gate electrode is smaller than the width of the gate insulating film throughout the entire electrode, only that "*a width* of the gate insulating film along a gate length is larger than *a width* of the gate electrode along the gate length."

215. But even if the claim required this, Guha teaches "internal spacer 16a and 16b may also have a rectangular cross-section, e.g., by polishing or removing the upper curved region to form a horizontal portion of the internal surface." (Guha, Ex.1028, ¶47.) A POSITA would understand that, based on this disclosure, the

expanded upper portion of the gate electrode could be removed with the slanted upper portion of gate spacers 16, which results in a rectangular cross-section with a gate electrode that has a uniform width along the entire height of the electrode. As shown in modified Figure 12 below, the width of the gate electrode consistent, and claim 1 is met.



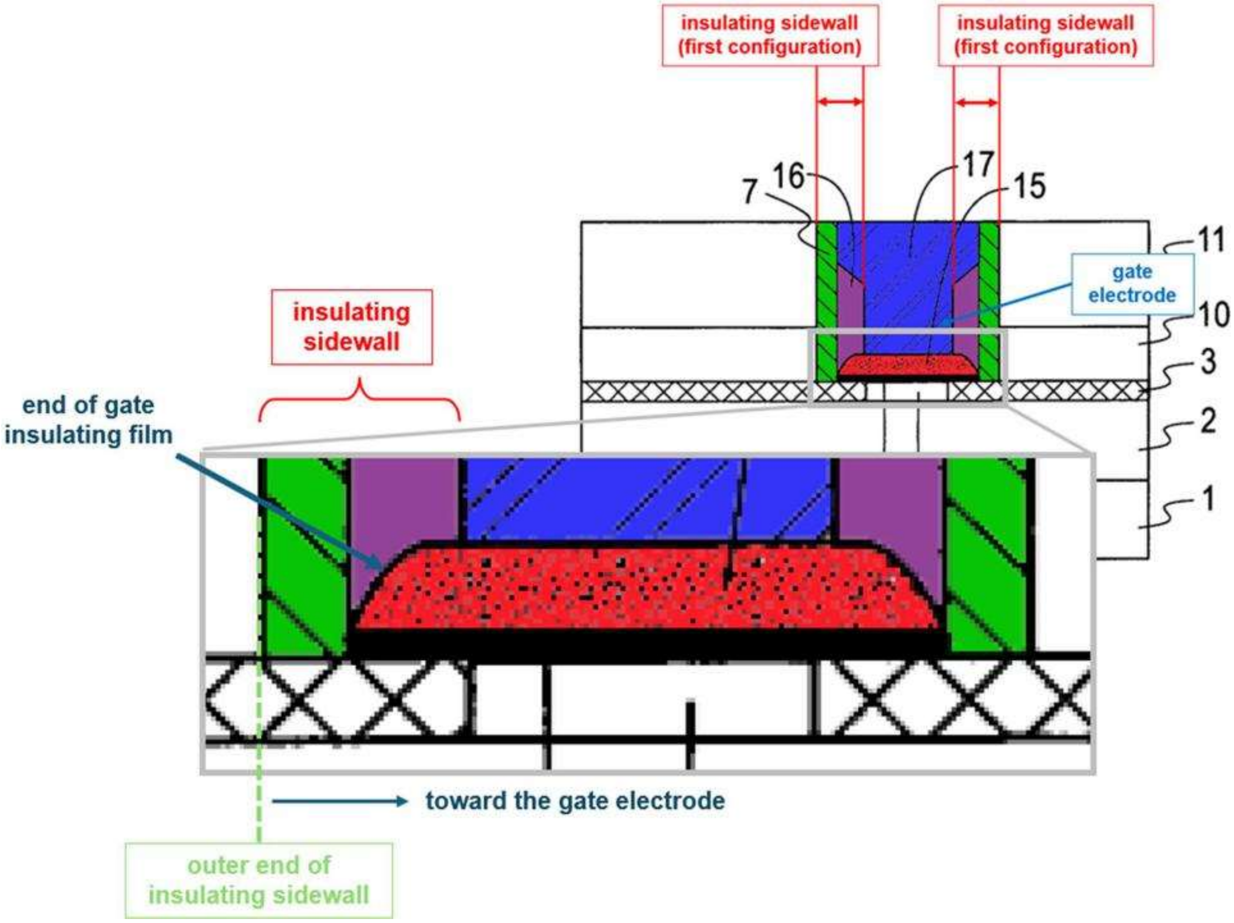
Guha, Fig. 12 (modified and annotated)

f. Limitation 1[e]: "an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode."

216. Guha discloses limitation 1[e] under both the first and second insulating sidewall configuration. As discussed above and seen in Figure 12, Guha's gate insulating film (shaded red) has a rounded end that protrudes from under the gate

electrode (shaded blue) to under spacers 16 (shaded purple). The tapered end of the gate insulating film is not concurrent with the side end of the gate electrode.

217. In the first insulating sidewall configuration, as seen in Figure 12 below, dielectric layer 15 is continuous layer extending from underneath gate electrode 17 (shaded blue) to underneath gate spacer 16 (shaded purple). his structure is formed because dielectric layer 15 is deposited in cavity 13 after isolating spacer 7, but before gate spacer structure 16. (Guha, Ex.1028, ¶¶43-45 (describing formation of gate spacer 16, dielectric layer 15, and gate electrode 17).).



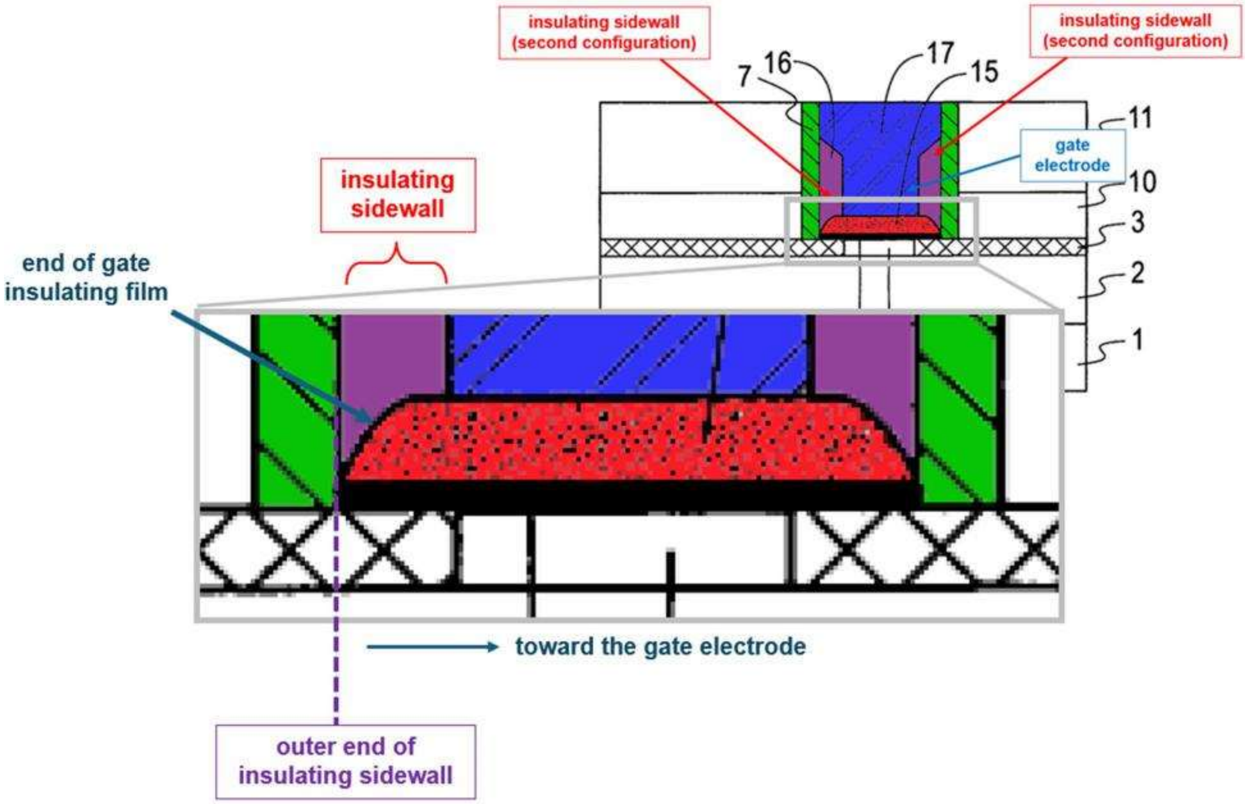
Guha, Fig. 12 (annotated under first configuration, and enlarged)

218. Guha's first insulating sidewall configuration thus teaches limitation 1[e]: "an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode."

219. Because dielectric layer 15 is deposited in cavity 13 after isolating spacer 7, but before gate spacer structure 16, dielectric layer 15 does not extend underneath isolating spacer 7 (which is the outer end of the collective insulating sidewall structure). As shown in Figure 12 above, the end of the gate insulating film is tapered and located inward from the outer end of the "insulating sidewall" (outer end of isolating spacer 7). The distance between the end of the gate insulating film and the sidewall is determined by Guha's fabrication process, including the width of isolating spacer 7. Guha discusses deposition of the gate dielectric using thermal evaporation of a metal such as hafnium, followed by chemical conversion to an oxide (HfO_2) using oxidation. As well known to a POSITA, the evaporation process will lead to such tapering of layer 15 due to the arrival angles (i.e step coverage) of the deposited species being more restricted near the corners. Thus, the end of dielectric layer 15 ("the high dielectric constant gate insulating film") is "under the insulating sidewall [and] is retracted from an outer end of the insulating sidewall toward the gate electrode," as required by limitation 1[e], consistent with the '076 patent and Applicant's statements during prosecution. (Ex.1001, 20:63-21:7; Ex.1002, 151-52.). Limitation 1[e] is thus met under the first insulating sidewall configuration.

220. In the second configuration, Guha discloses "an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode" as required by limitation 1[e]. At least part of dielectric layer 15 does not contact the outer end of spacer 16 (shaded purple below). Therefore, an end of dielectric layer 15 (the "high dielectric constant gate insulating film") is not located underneath the outer end of the gate spacer 16.

221. Both the shape at the end of dielectric layer 15 and the distance between the end of dielectric layer 15 and the insulating sidewall are determined by specific process parameters, including step coverage, deposition rate, and aspect ratio. Thus, the end of dielectric layer 15 in Guha is "under the insulating sidewall [and] is retracted from an outer end of the insulating sidewall toward the gate electrode." as required by Limitation 1[e], consistent with the '076 patent and Applicant's statements during prosecution. (Ex.1001, 20:63-21:7; Ex.1002, 151-52.)



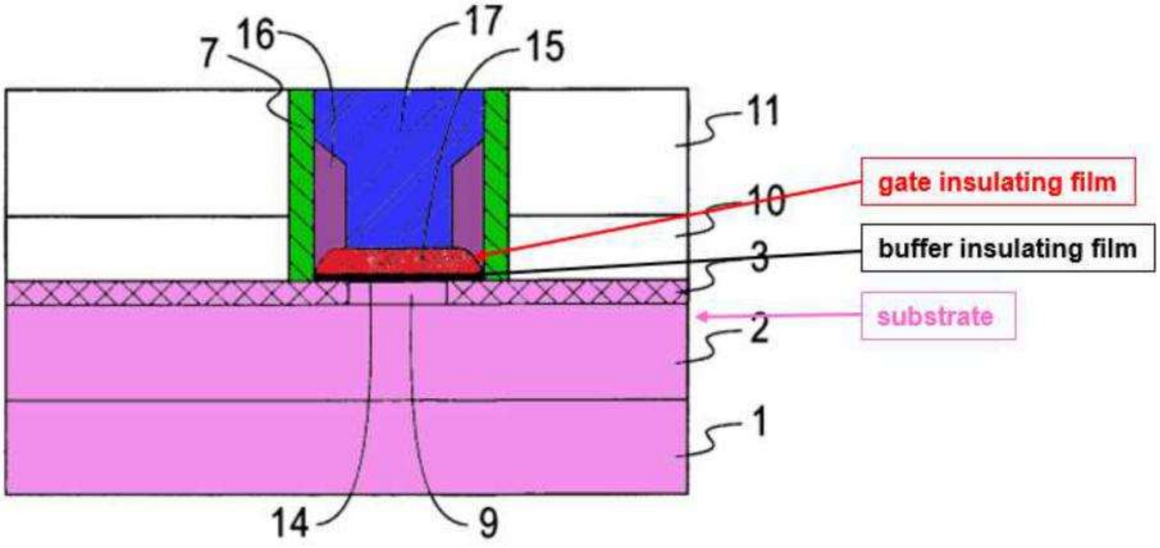
2. Dependent Claim 2: "The semiconductor device of claim 1, further comprising a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film."

222. Guha discloses dependent claim 2, a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film. For Figure 12, "[i]n this embodiment, the structure of FIG. 7 is subjected to a deposition step in which the dielectric layer 15 is formed only on the gate-isolating layer 14 at the bottom of the cavity 13. This can be achieved, for example, by a directional deposition process such as thermal evaporation of a metal such as hafiium [sic], zirconium, aluminium [sic], among others, and subsequent chemical

conversion to a high-k dielectric such as metal oxides, silicates or other appropriate high-k materials, allowing a further reduction in sidewall capacitance. As shown in FIG. 10, the dielectric layer 15 covers only the bottom of the cavity 13." (Guha, Ex.1028, ¶43.)

223. Guha's gate-isolating layer 14 can be "formed at the bottom of the cavity 13," on the substrate. (Guha, Ex.1028, ¶37). "The gate-isolating layer 14 acts as a buffering layer between channel 9 and the dielectric material to be deposited thereon. A preferred material for the gate-isolating layer 14 is silicon oxide, which can be thermally grown, and thinned if necessary. Other materials, however, may also be suitable. This gate-isolating layer, for example, is used to prevent mobility degradation in the silicon channel that may be caused by scattering mechanisms in the dielectric layer." (Guha, Ex.1028, ¶37.)

224. As seen below, Guha's gate-isolating layer 14 (shaded black) is shown in Figure 12. As discussed above in limitation 1[a], channel 9 is part of the substrate (shaded pink), and gate-isolating layer 14 is therefore "a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film" as required by claim 2.



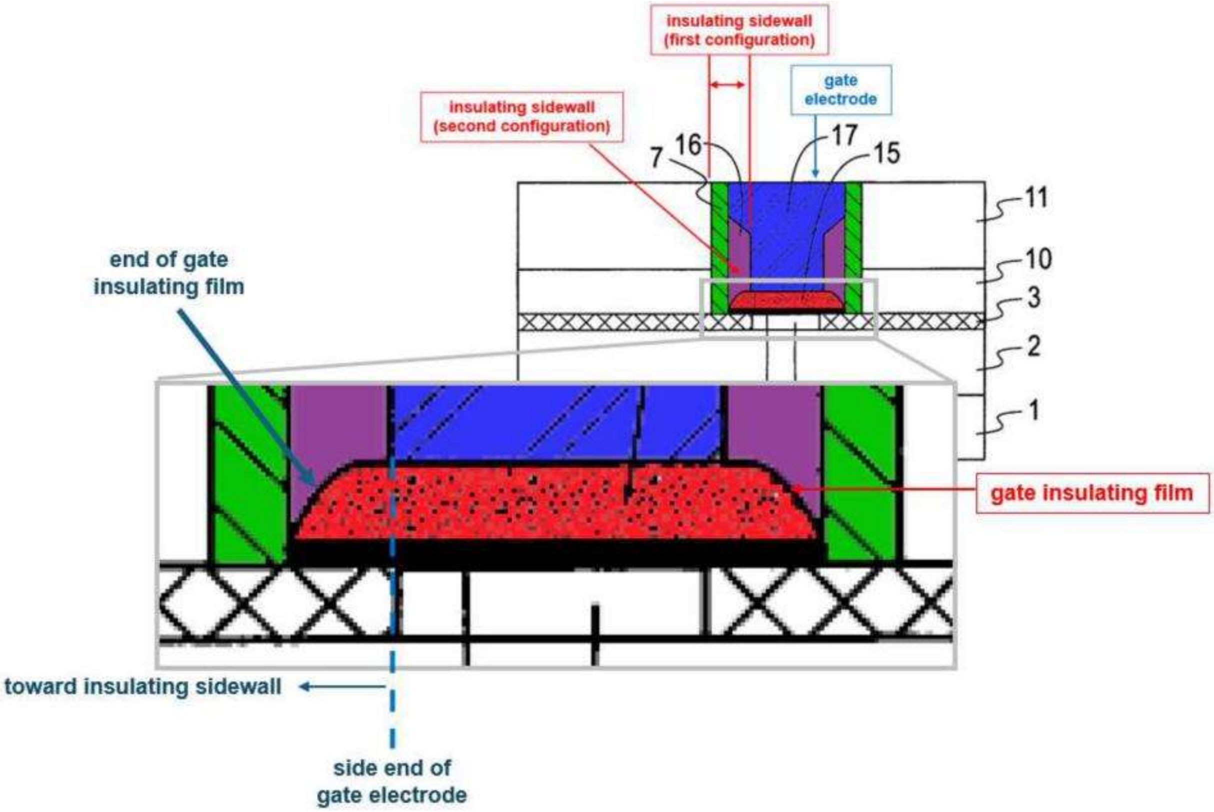
Guha, Fig. 12 (annotated)

3. Dependent Claim 3: "The semiconductor device of claim 1, wherein the gate insulating film is formed of a Hf based oxide."

225. Guha discloses claim 3, or at a minimum, renders this claim 3 obvious. Guha discloses high-k dielectric layer 15 "preferably compris[es] a high-k dielectric material," with exemplary materials to "include, but are not limited to hafnium oxide, hafnium silicate, aluminum oxide or zirconium oxide." (Guha, Ex.1028, ¶¶38, 43.) Hafnium oxide is "a Hf based oxide" as recited by claim 6. Thus, a POSITA would have been motivated to use hafnium oxide from Guha's list of gate materials given its known benefits, including thermal stability, band alignment, and ability to scale. (Lee-2000, Ex.1337, 2.4.1; Houssa, Ex.1213, 207; Lee-1999, Ex.1349, 134.)

4. Dependent Claim 7: "The semiconductor device of claim 1, wherein an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall."

226. Guha discloses the limitation of claim 7 under both the first and second insulating sidewall configurations. As shown in Figure 12, Guha's gate insulating film (shaded red) has a rounded end that protrudes from under the gate electrode (shaded blue) to under spacer 16 (shaded purple). The tapered end of the gate insulating film is not concurrent with the side end of the gate electrode.



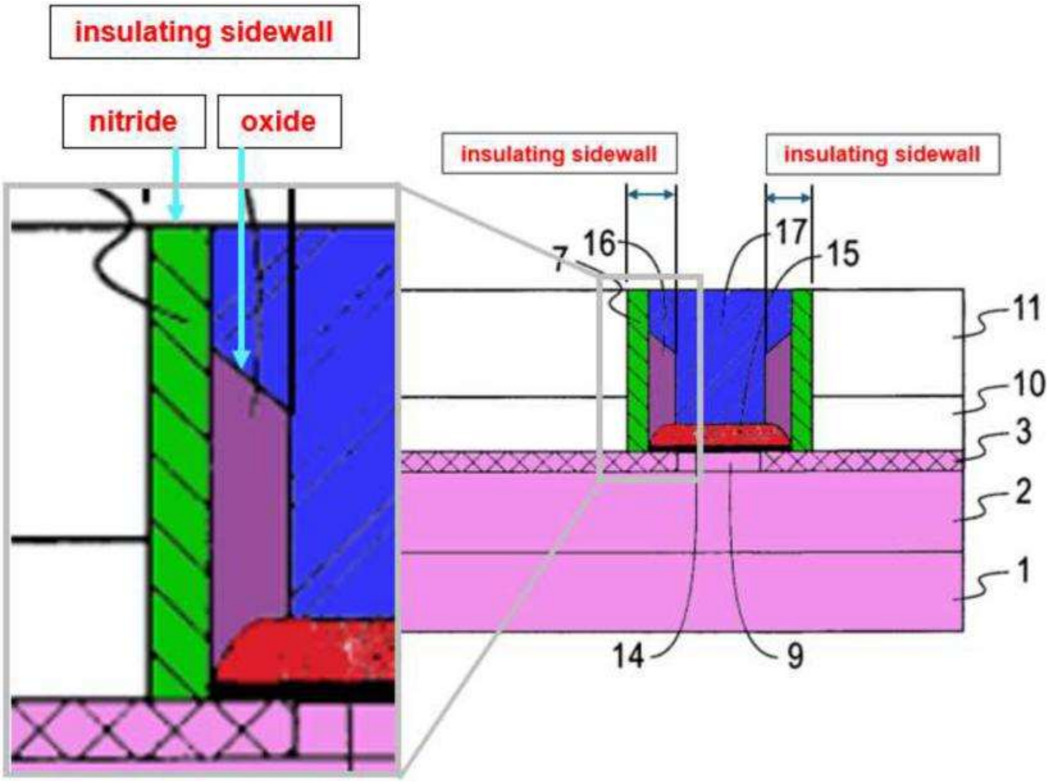
Guha, Fig. 12 (annotated and enlarged)

227. In Figure 12, the end of high-k gate dielectric layer 15 "protrudes from a side end of the gate electrode toward the insulating sidewall" in both the first

configuration (collectively gate spacers 16 and isolating spacers 7) and the second configuration (gate spacers 16 alone).

5. Dependent Claim 8: "The semiconductor device of claim 1, wherein the insulating sidewall has a double layer structure including an oxide film and a nitride film."

228. Guha discloses the limitation of claim 8, wherein the insulating sidewall has a double layer structure including an oxide film and a nitride film, at least under the first insulating sidewall configuration (gate spacer 16 and isolating spacer 7), because spacers 16 and 7 are two layers (a "double layer structure") of the claimed insulating sidewall.



Guha, Fig. 12 (annotated and enlarged)

229. Guha discloses that gate spacer 16 is a "material, e.g. an oxide or other suitable material." (Guha, Ex.1028, ¶40.) Gate spacer 16 is thus "an oxide film."

230. Guha further discloses that isolating spacer 7 "can be composed of any insulating material including, for example, an oxide, nitride, oxynitride or any combination thereof." (Guha, Ex.1028, ¶28.) "A preferred material would be silicon nitride." (Guha, Ex.1028, ¶28.) Isolating spacer 7 is thus a nitride film.

231. Similar to the prior art discussed previously, a POSITA would consider gate spacer 16 (made of silicon oxide) and isolating spacer 7 (preferably made of silicon nitride) to be "layers" of the sidewall structure, consistent with the '076 patent. (See, e.g., Guha, Ex.1028, ¶¶28 (formation of isolating spacers 7), 44 (formation of gate spacers 16); Ex.1001, 20:43-52.)

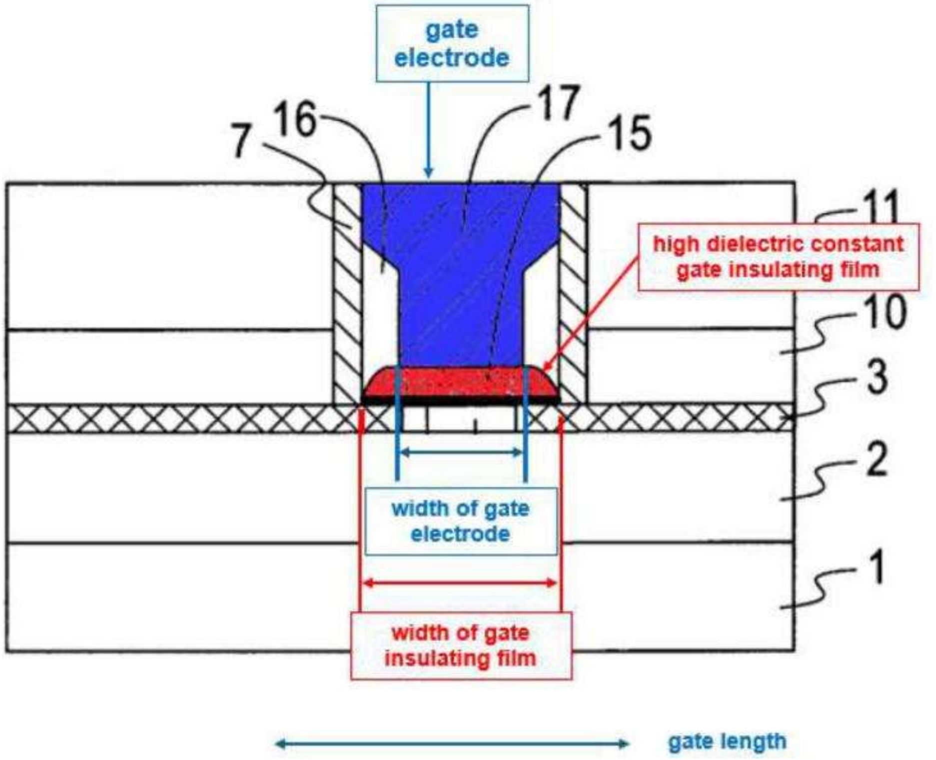
6. Dependent Claim 10: "The semiconductor device of claim 1, wherein a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length."

Dependent Claim 13: "The semiconductor device of claim 1, wherein the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length."

232. For the same reasons discussed above for limitation 1[d], Guha discloses the limitations of claims 10 and 13. As seen in Figure 12, the width of dielectric layer 15 (shaded red) is larger than the width of gate electrode 17 (shaded blue), thereby disclosing the limitations of claims 10 and 13. (Guha, Ex.1028, ¶¶41,

43-45 (describing formation of gate spacers 16 in the cavity followed by deposition of the gate electrode).)

233. The width of Guha's gate electrode is the same at its middle position as at its bottom, and both are narrower than the width of the gate insulating film. Thus, the width of the dielectric layer 15 is larger than the width of the gate electrode at its middle.

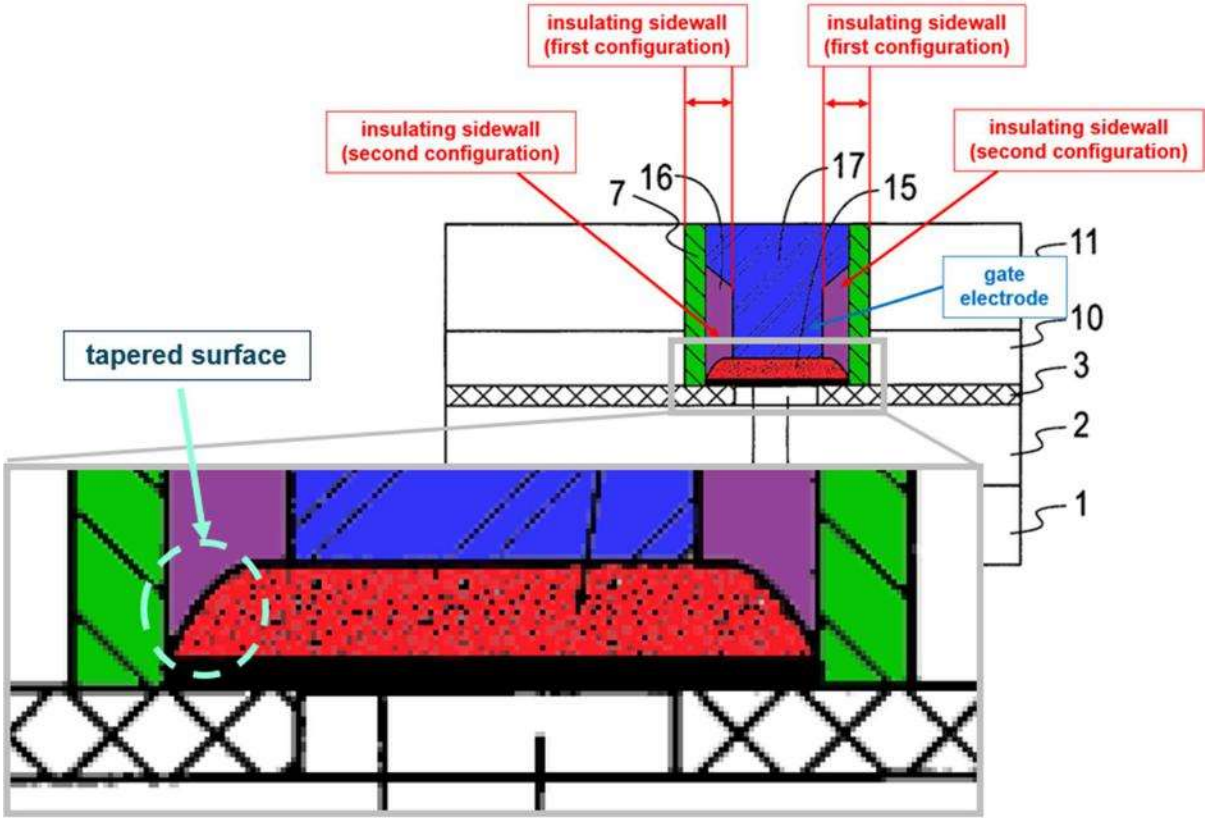


Guha, Fig. 12 (annotated)

7. Dependent Claim 11: "The semiconductor device of claim 1, wherein the end of the gate insulating film located under the insulating sidewall has a tapered surface."

8. Dependent Claim 12: "The semiconductor device of claim 1, wherein the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof."

234. Guha discloses that "the edge where the dielectric layer 15 meets the isolating spacer structure 7 ... is rounded either upwards or downwards (e.g., similar to a cusp)." (Guha, Ex.1028, ¶43.) Figure 12 shows an example of dielectric layer 15 that is rounded downward.



Guha, Fig. 12 (annotated and enlarged)

235. In Figure 12, the high-k gate insulating film is tapered such that it becomes smaller towards the ends for reasons discussed earlier. The film is at its smallest thickness under spacer 16 next to where it meets spacer 7. Under both the first and second insulating sidewall configurations, Guha teaches that the "end of the gate insulating film located under the insulating sidewall has a tapered surface," as required by claim 11, and "has a thickness which becomes smaller toward the end thereof," as required by claim 12, because the end of the gate insulating film 15 under spacer 16 is tapered. The tapered end portion of dielectric layer 15 is "located under the insulating sidewall" in both the first configuration (gate spacers 16 and isolating spacers 7 collectively) and second configuration (gate spacers 16 alone). Moreover, Guha discloses deposition of the gate dielectric using thermal evaporation of a metal such as hafnium, followed by chemical conversion to an oxide (HfO_2) using oxidation. As well known to a POSITA, the evaporation process will lead to such tapering of layer 15 due to the arrival angles (i.e step coverage) of the deposited species being more restricted near the corners. Accordingly, Guha teaches the limitation of claims 11 and 12.

D. Ground IV

236. In my opinion, the combination of Guha and Sim renders obvious Challenged claim 6 of the ’076 patent (Ground IV).

1. Dependent Claim 6: "The semiconductor device of claim 1, wherein a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less."

237. Guha uses "hafnium oxide" as a high-k gate dielectric film (Guha, Ex.1028, ¶38), but does not expressly disclose the gate insulating film located underneath the insulating sidewall has a thickness of "2 nm or less." Sim provides this teaching, as discussed above. Thus, the combination of Guha and Sim renders claim 6 obvious.

238. As discussed above, Sim relates to semiconductor devices (Sim, Ex.1024, Abstract), and is in the same field as Guha and the '076 patent. (Ex.1001, 1:17-18 ("The present invention relates to a semiconductor device and a method for fabricating the semiconductor device."); Guha, Ex.1028, ¶1 ("The invention relates to a MOSFET device having a damascene gate with an internal spacer structure and a process of forming the device.").)

239. Sim explicitly teaches using a HfO_2 gate insulating film with a thickness 2 nm or less. Specifically, Sim concluded that "[s]caling the physical thickness of the HfO_2 dielectric to below 20Å causes less charge trapping and higher mobility." (Sim, Ex.1024, 221.) 20Å or Angstroms is equal to 2 nm, as recited by claim 6.

240. Applying Sim's teaching to Guha's semiconductor devices yield a device where the high-k gate insulating film is less than 2 nm, as required by claim

6. This is even more true for Guha's tapered end of the gate insulating film, since the tapered end is even smaller than the film underneath the gate electrode. Thus, the combination of Guha and Sim discloses " a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less."

241. For similar reasons discussed above, a POSITA would have been motivated to use Sim's gate insulating film with a thickness of 20Å (2 nm) or less in Guha's Figure 12 semiconductor device. Guha already contemplates hafnium oxide as an example high-k gate dielectric, the same film studied in Sim. Sim concludes that reducing the thickness of hafnium oxide to below 20Å enhances mobility and reduces charge trapping, which increases the performance and scalability of semiconductor devices. (Sim, Ex.1024, 219, 221.) These improvements assist making transistors smaller and more reliable, which both Guha and Sim highlight as objectives. (Guha, Ex.1028, ¶2; Sim, Ex.1024, 218.)

242. Sim's empirical evidence showing that reducing HfO_2 thickness as a gate dielectric to 2 nm or less enhances mobility and minimizes charge trapping aligns with Guha's scaling objectives, reinforcing the benefits of this combination. The combination would also have been nothing more than the use of a known technique and structure (Sim's HfO_2 gate dielectric layer less than 20Å in thickness) to improve similar devices (Guha's Figure 12 semiconductor device having a hafnium oxide gate dielectric) in a predictable manner. A POSITA would have had

a reasonable expectation of success because Sim uses a well-known process, atomic layer deposition (ALD), for manufacturing high-k films. (Sim, Ex.1024, 218; Houssa, Ex.1213, 17-19.)

E. Ground V

243. In my opinion, the combination of Matsumoto and Yu renders obvious Challenged Claims 1-3, 7, 8, 10, and 13 of the ’076 patent (Ground V).

1. Motivation to Combine

244. A POSITA would have been motivated to combine two features of Yu with Matsumoto. First, Matsumoto and Yu are both directed to semiconductor devices and are in the same field of endeavor as the ’076 patent. (Ex.1001, 1:18-19 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); Matsumoto, Ex.1009, ¶2 (“The present invention relates to a semiconductor device and a method of manufacturing the same.”); Yu, Ex.1048, Abstract (“A MOSFET device and method of fabrication.”).)

a. First Combination – Hafnium Based Oxide

245. A POSITA would have combined Yu with Matsumoto by using a Hf based oxide, such as HfO_2, as the gate dielectric in Matsumoto’s semiconductor device.

246. Matsumoto already provides a list of exemplary materials to use as its gate insulating film, including “a metal oxide film such as Al2O3 or a ferroelectric film such as Ta2O5 and BST.” (Matsumoto, Ex.1009, ¶107.) A POSITA would have

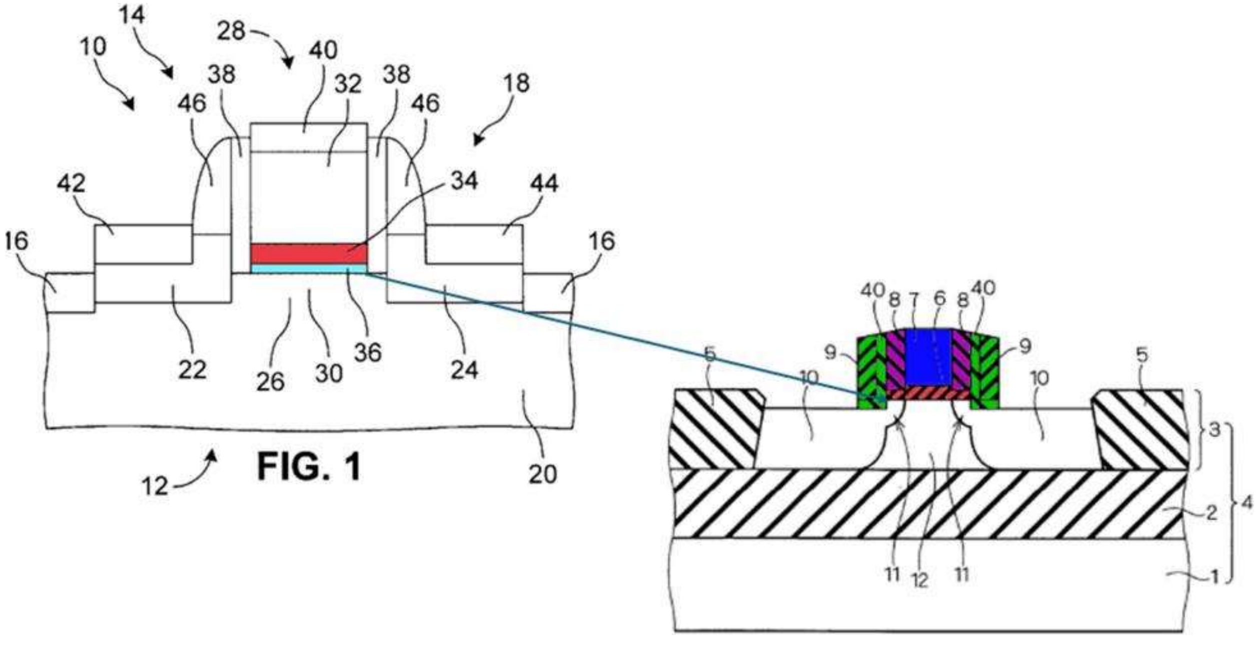
understood these films to be high-k dielectrics. (See, e.g., Wilk, Ex.1018, Table 1; Campbell, Ex.1338, 88-89.) In addition to "aluminum oxide (e.g., Al2O3)" and "barium strontium titanate (BST)" as identified in Matsumoto, Yu teaches that its gate dielectric 34 may comprise "hafnium oxide (e.g., HfO_2)," which is another known high-k film. (Yu, Ex.1048, 3:15-30; see also Wilk. Ex.1018, Table 1.)

247. HfO_2 is a known high-k material with superior thermal stability and excellent electrical properties. Matsumoto explicitly seeks to improve the electrical characteristics of its gate insulating film, which aligns with Yu's teaching of HfO_2 as a high-performance dielectric material. Thus, in my opinion, a POSITA would have been motivated to use a Hf-based oxide as a gate insulating layer, such as HfO_2 as taught by Yu, in Matsumoto's device given HfO_2's known benefits, e.g., "its superior thermal stability with poly-Si and reasonable band alignment." (Lee-2000, Ex.1337, 2.4.1; see also Houssa, Ex. 1213, 207 (HfO_2 "combines a high k (15–26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ..."); Lee-1999, Ex.1349, 134 ("Excellent dielectric properties ... suggest that HfO_2 is a promising material for the future gate dielectric application.").) HfO_2 also could be scaled down to a smaller EOT. (See Houssa, Ex.1213, 207.)

b. Second Combination – Buffer Layer

248. A POSITA applying Yu’s teachings to Matsumoto’s semiconductor device would also have included a buffer interface layer between the high-k gate insulating film and the substrate, as taught by Yu.

249. Yu’s buffer interface 36 (shaded aqua), which “can be a layer of silicon oxide” (Yu, Ex.1048, 4:58-61, 3:62-63) would have been used by a POSITA between the substrate and Matsumoto’s high-k dielectric (shaded red) in the combined device, as seen below. Yu’s buffer interface 36 is directly relevant to the semiconductor device of Matsumoto, ensuring compatibility with Matsumoto’s high-k gate dielectric.



Yu, Fig. 1 (left); Matsumoto, Fig. 22 (right) (annotated)

250. Yu's buffer layer enhances Matsumoto's objective of reducing device malfunctions and improving operational stability by mitigating adverse interactions between the high-k gate dielectric and the substrate. Accordingly, a POSITA would have been motivated to combine Matsumoto and Yu as discussed above. Yu itself suggests the motivation, teaching that a buffer interface (a) "acts to reduce diffusion and/or penetration of atoms from the high-k dielectric material into the layer of semiconductor material 20 that could lead to a degradation in channel mobility" and (b) "may act to retard reaction of the high-k material with the layer of semiconductor material 20." (Yu, Ex.1048, 3:64-4:2; see also Yu. Ex.1048, 4:65-67 ("The buffer interface material layer 62 assists in reducing integration issues that may arise when attempting form a layer of high-k material on a semiconductor layer."))

251. One objective of Matsumoto is "to provide a semiconductor device which achieves reductions in malfunctions and operating characteristic variations." (Matsumoto, Ex.1009, ¶13.) Based on Yu's suggestion to use a buffer layer to achieve these same benefits, a POSITA would have been motivated to use Yu's buffer interface to further improve Matsumoto's channel mobility device performance, of semiconductor devices such as the transistors disclosed by Matsumoto and Yu.

252. It would be nothing more than applying predictable methods to use Yu's buffer layer. Matsumoto's existing process steps disclose forming a silicon

oxide film via CVD or thermal oxidation, as well as suggesting using some high-k materials instead. Yu teaches that when using high-k materials, a silicon oxide buffer reduces diffusion and interface defects. (Yu, Ex.1048, 3:64-4:2.) Given Matsumoto's disclosure of alternative high-k materials, a POSITA would have expected predictable improvements by using Yu's buffer layer. Thus, combining Matsumoto and Yu would have involved nothing more than known techniques and structures (Yu's buffer interface) to improve similar devices (Matsumoto's transistor having a high-k gate dielectric film) in a predictable manner. A POSITA would have had a reasonable expectation of success because Yu instructs a POSITA on conventional techniques to create buffer layers between the high-k gate dielectric film and the substrate. (Yu, Ex.1048, 4:61-65 ("The buffer interface material layer 62 can be formed by a low temperature (about 500° C.) thermal oxidation process, a remote plasma deposition process, an atomic layer deposition (ALD) process or the like.").)

253. Matsumoto also discloses similar methods for forming a layer of silicon oxide above the substrate. (Matsumoto, Ex.1009, ¶107 ("Next, a silicon oxide film 13 is formed entirely on the upper surface of the silicon layer 3 and the upper surface of the isolating insulation film 5 by a CVD process or a thermal oxidation process.").) A POSITA, wanting to gain the benefits of using high-k materials as a gate dielectric and wanting to further improve performance by using a buffer layer

between the substrate and the high-k gate dielectric, would have simply applied Matsumoto's (or Yu's) disclosure of forming a silicon oxide layer underneath the high-k materials for the gate dielectric.

2. Independent Claim 1

a. Preamble: "A semiconductor device comprising:"

254. The combination of Matsumoto and Yu discloses a "semiconductor device." Matsumoto is titled "Semiconductor device and method of manufacturing same," and discloses that "[t]he present invention relates to a semiconductor device." (See, e.g., Matsumoto, Ex.1009, ¶¶2, 102, 137; see also Matsumoto, Ex.1009, Abstract ("A semiconductor device ...."); Yu, Ex. 1048, 1:7-11.)

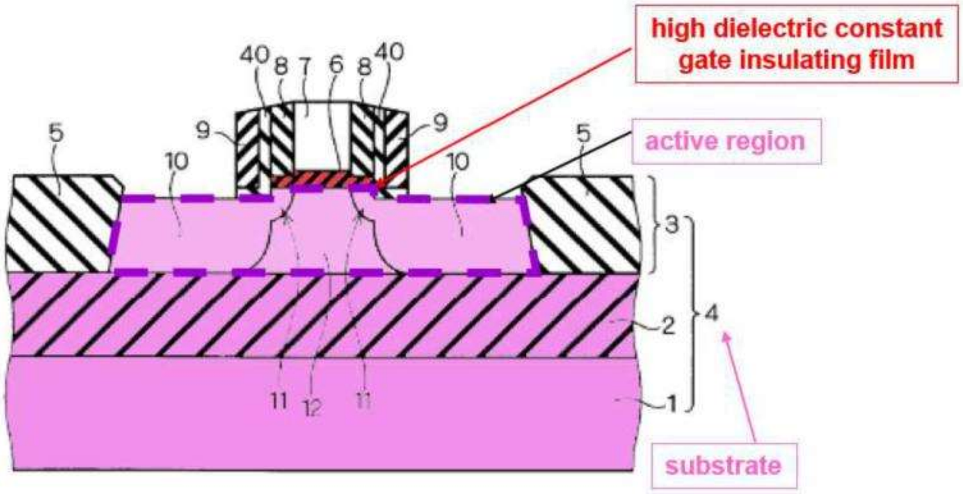
b. Limitation 1[a]: "a gate insulating film formed on an active region in a substrate and including Hf;"

255. The combination of Matsumoto and Yu discloses limitation 1[a]: "a gate insulating film formed on an active region in a substrate and including Hf."

256. Matsumoto discloses a substrate, comprising a multi-layer SOI substrate 4 (shaded pink) made up of silicon substrate 1, BOX layer 2, and single-crystalline silicon layer 3 "stacked in the order named." (Matsumoto, Ex.1009, ¶102; see also Matsumoto, Ex.1009, ¶137 (relating process steps of first embodiment through forming gate electrode to fourth embodiment), ¶140 (relating fourth embodiment to first embodiment).)

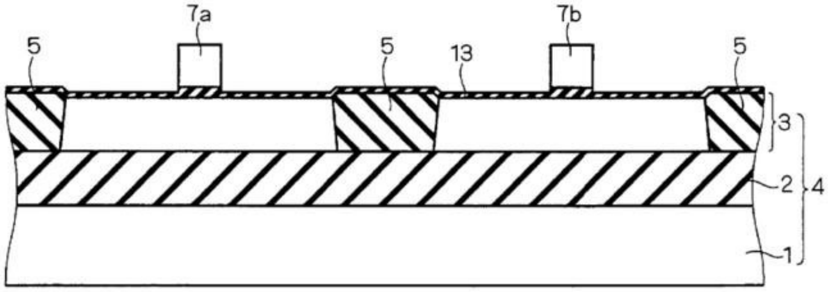
257. Matsumoto further discloses an active region, teaching that "isolating insulation film 5 extends from the upper surface of the silicon layer 3 to the upper surface of the BOX layer 2," and that the "MOSFET is formed in a device region defined by the isolating insulation film 5." (Matsumoto, Ex.1009, ¶¶102-03.) The device region is an "active region in a substrate" and includes source/drain regions 10. (Matsumoto, Ex.1009, ¶¶103-05, 139).

258. This is also consistent with the '076 patent. (See Ex.1001, 1:41-42 ("The region of the well 102 surrounded by the STI serves as an active region of a substrate 101"), 7:28-45 (active region includes source/drain regions surrounded by STI structures).) The active region for Figure 22 (outlined below in magenta) in a substrate (shaded pink) is seen in Matsumoto's fourth embodiment below.



Matsumoto, Fig. 22 (annotated)

259. Matsumoto's film 6 would be understood as the claimed gate insulating film. (Matsumoto, Ex.1009, ¶103 (referring to film 6 as a "gate insulation film").) In both first and fourth embodiments, Matsumoto teaches "silicon oxide film 6 is formed partially on the upper surface of the silicon layer 3" in the device region and that gate electrode 7 "is formed partially on the silicon oxide film 6." (Matsumoto, Ex.1009, ¶103 (first embodiment), ¶137 (in fourth embodiment, "gate electrode 7 is formed by the process described in the first embodiment").) This is accomplished by forming film 13 on the substrate, as shown in Figure 4, below.



Matsumoto, Fig. 4

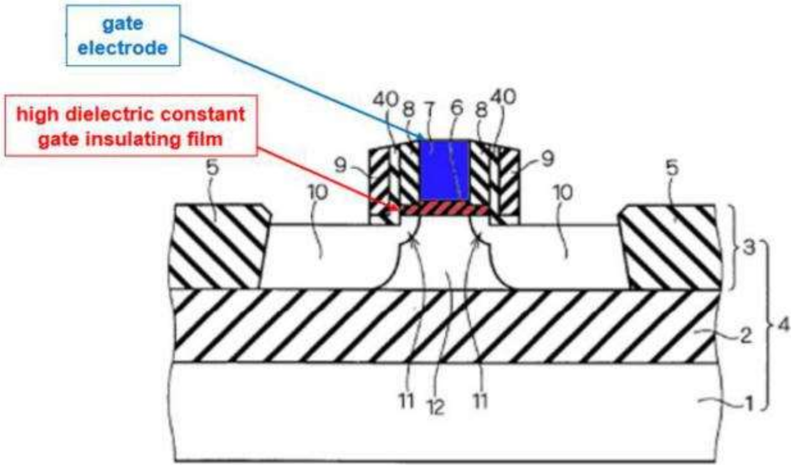
260. After sidewalls are formed, film 13 is etched to form film 6. (See Matsumoto, Ex.1009, ¶138, Figures 18-19, 22.)

261. As discussed above for "First Combination," the material used for Matsumoto's gate insulating film 6 is HfO_2, as taught by Yu. (See also Matsumoto, Ex.1009, ¶107 (film 6 can be a high-k film); Yu, Ex.1048, 3:15-30.) Thus, the combination of Matsumoto and Yu teaches "a gate insulating film formed on an active region in a substrate and including Hf."

c. Limitation 1[b]: "a gate electrode formed on the gate insulating film;"

262. The combination of Matsumoto and Yu discloses limitation 1[b]: "a gate electrode formed on the gate insulating film."

263. In Matsumoto's fourth embodiment, "gate electrode 7 made of polysilicon is formed partially" on insulating film 6. (Matsumoto, Ex.1009, ¶103 (first embodiment), ¶107 (describing formation of high-k insulating film and gate electrode), ¶¶137¬138 (in fourth embodiment, "gate electrode 7 is formed by the process described in the first embodiment").) The gate electrode (shaded blue) is formed over the high dielectric constant gate insulating film (shaded red), as shown in Figure 22 below.

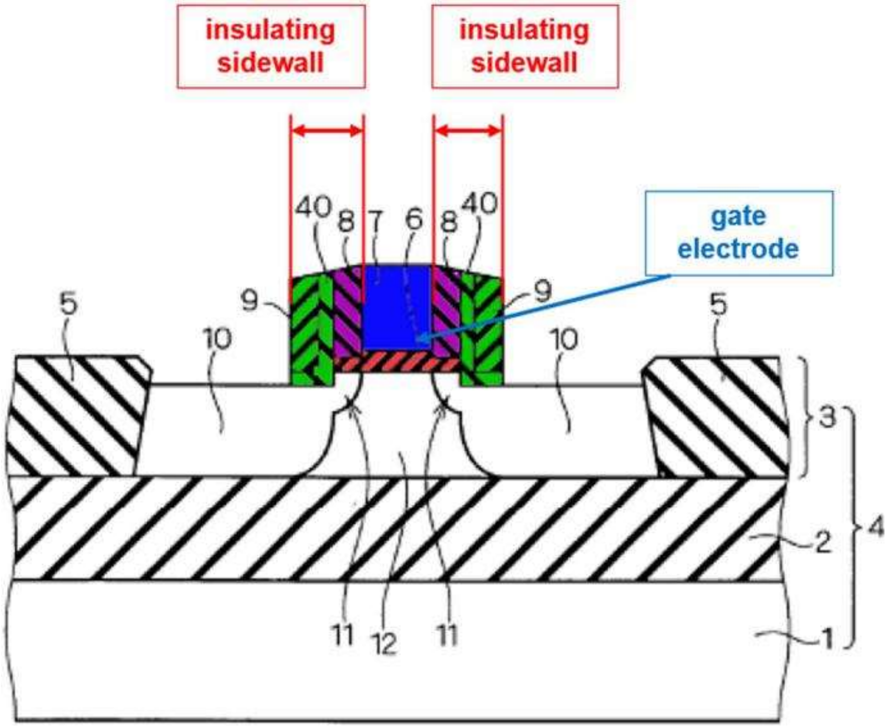


Matsumoto, Figure 2

d. Limitation 1[c]: "a insulating sidewall formed on each side surface of the gate electrode;"

264. The combination of Matsumoto and Yu teaches limitation 1[c]: "a insulating sidewall formed on each side surface of the gate electrode."

265. In Figure 22, silicon oxide film 40 and silicon nitride film 9 are formed "on the outer side surfaces of" film 8. (See Matsumoto, Ex.1009, ¶139.)



Matsumoto, Fig. 22 (annotated)

266. In Matsumoto's fourth embodiment, silicon oxide film 8, silicon oxide film 40, and silicon nitride film 9 are collectively "an insulating sidewall formed on each side surface of the gate electrode" (Limitation 1[c]), consistent with the '076 patent.

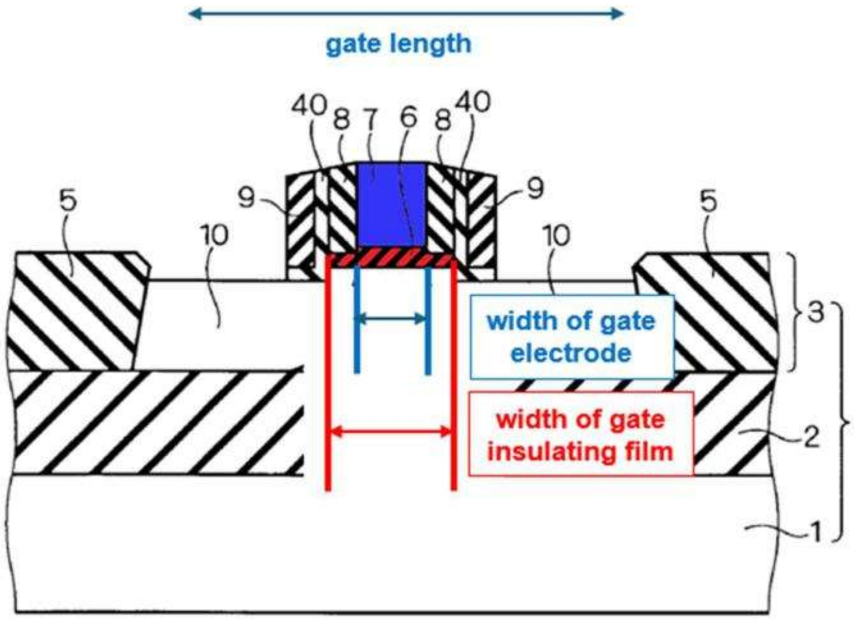
267. Matsumoto describes film 9 as a "sidewall insulation film." (Matsumoto, Ex.1009, ¶114 (describing nitride films 9a/9b "serving as sidewall insulation films").) While film 8 and film 40 are not described as a sidewall, a POSITA would nevertheless consider films 8 and 40 sidewalls as claimed in the '076 patent. (Matsumoto, Ex.1009, ¶¶104, 110, 139, 40 ("the semiconductor device further includes a second sidewall formed on the side surface of the gate electrode, with the first sidewall therebetween").) A POSITA would have known that silicon oxide (for films 8 and 40) and silicon nitride (for film 9) are both insulators and common material used to manufacture sidewalls. As such, films 8, 40, and 9 make up the claimed "insulating sidewall." Alternatively, a POSITA would consider film 8 alone to be the claimed "insulating sidewall," consistent with the '076 patent. Ex.1001, 6:9.

e. Limitation 1[d]: "wherein a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length,"

268. The combination of Matsumoto and Yu teaches limitation 1[d] "a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length."

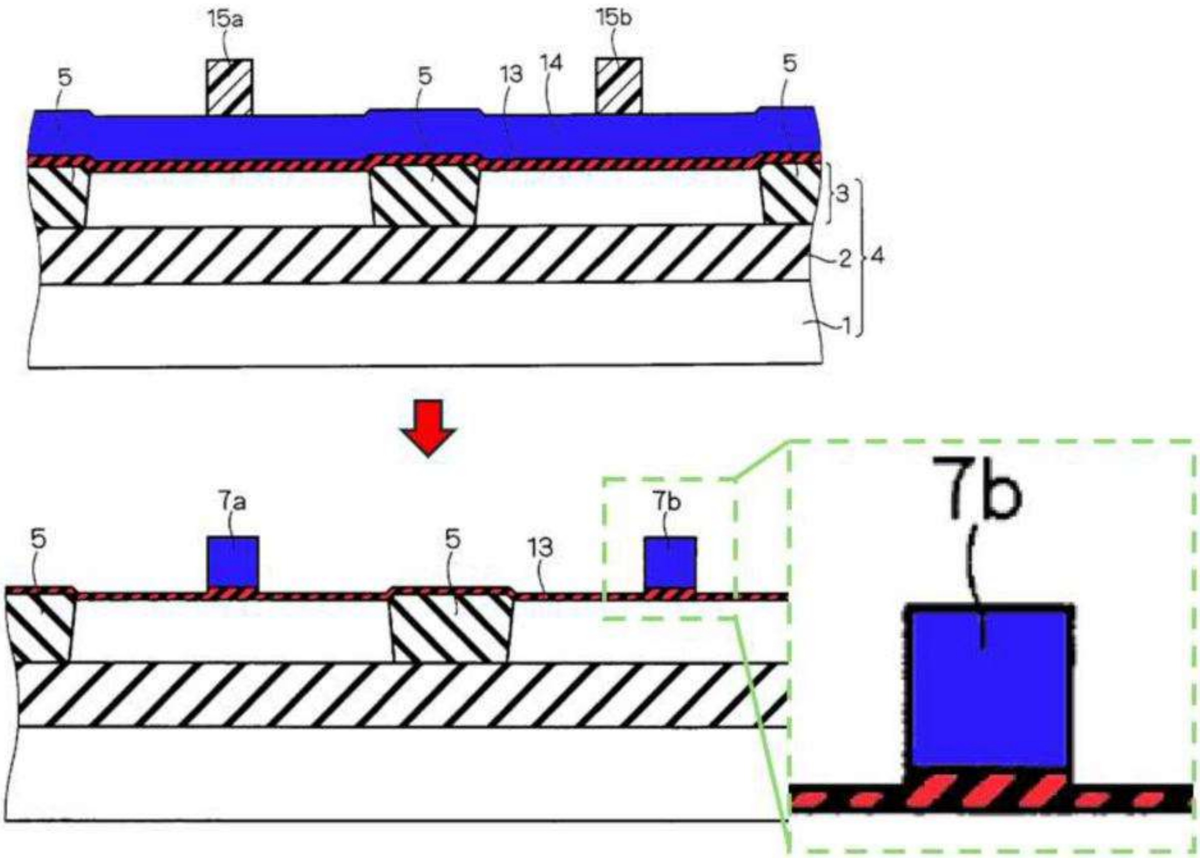
269. In Matsumoto's fourth embodiment, the gate insulating film 6 (shaded red) extends from underneath the gate electrode 7 to underneath film 8. Thus, the

width of gate insulating film 6 (shaded red) along the gate length is larger than the width of gate electrode 7 (shaded blue).



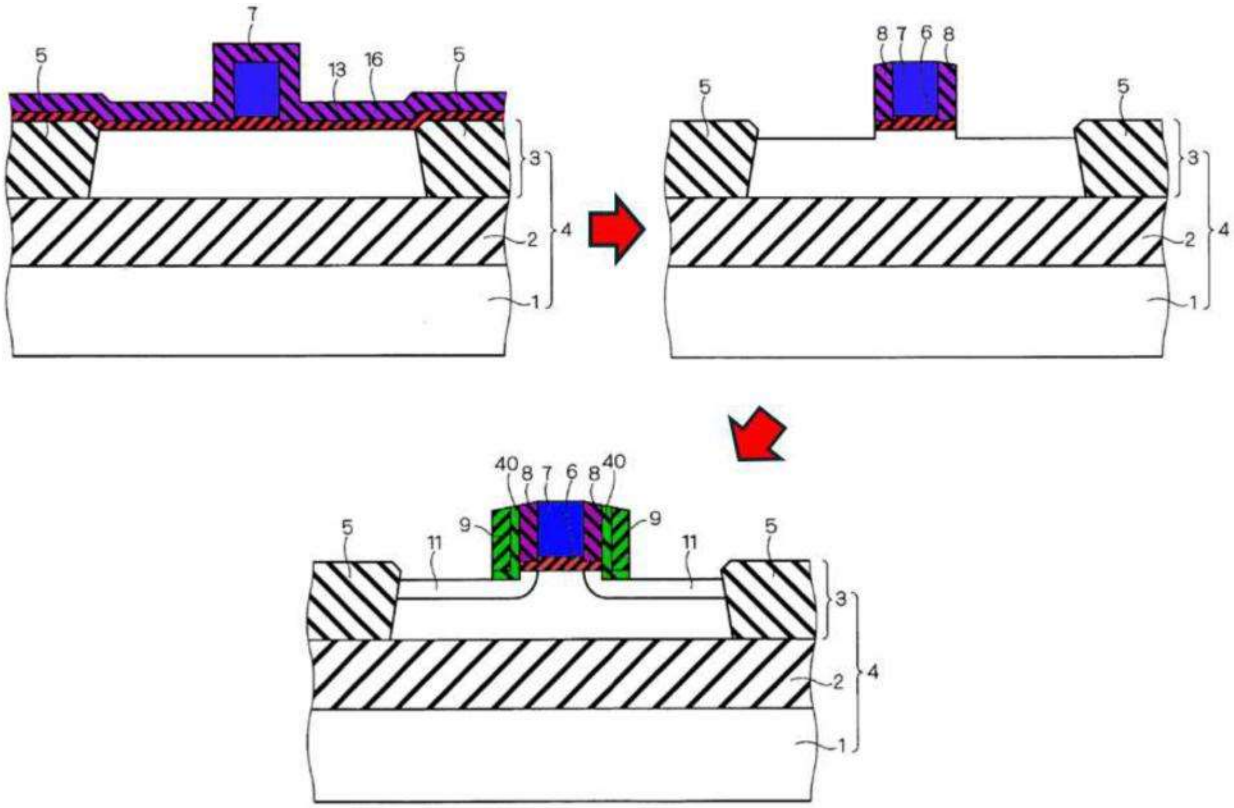
Matsumoto, Fig. 22 (annotated)

270. Matsumoto's manufacturing process confirms the width of the gate insulating film is larger than the gate electrode. As seen below in Figures 3-4, dielectric film 13 that forms the gate insulating film is formed continuously as one layer. (Matsumoto, Ex.1009, ¶107.)



Matsumoto, Figs. 3 (annotated top) and 4 (annotated and enlarged, bottom)

271. After forming the gate electrode, sidewalls 8 are formed, as seen in Figures 18-19. (Matsumoto, Ex.1009, ¶138.) The etching process that forms films 8 (shaded purple) "is continued to overetch the upper surface of the silicon layer 3 exposed by the etching of the silicon oxide film 16." (Matsumoto, Ex.1009, ¶138.) As seen below in Figure 19, the high-k dielectric film (shaded red) is formed underneath the gate and sidewall film 8. Film 40 and film 9 (shaded green) are then formed on the outer surfaces of film 8, as seen in Figure 21. (Matsumoto, Ex.1009, ¶139.)



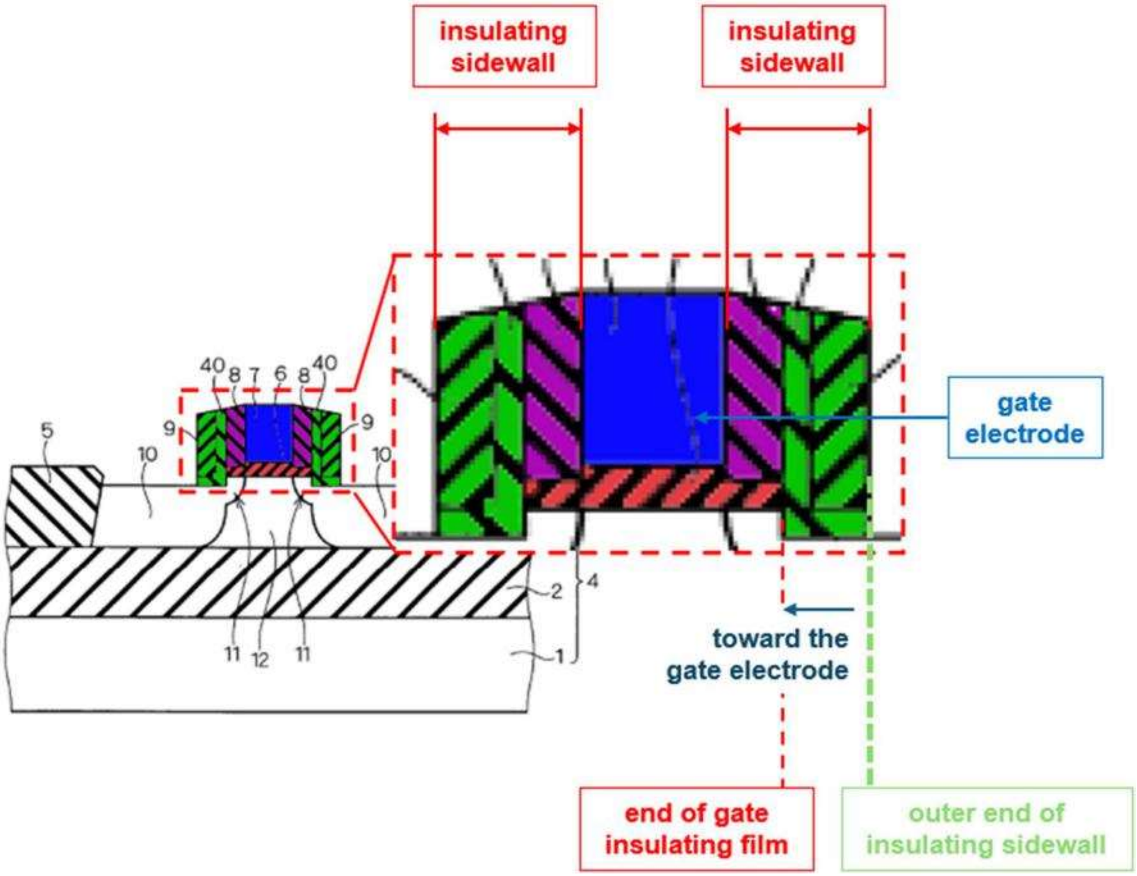
Matsumoto, Figs. 18 (top-left), 19 (top-right), and 21 (bottom) (annotated)

272. Because the high-k dielectric film 6 (shaded red) extends both underneath the gate electrode 7 and underneath part of the "insulating sidewall" (specifically, film 8), which is formed on the side of the gate electrode, the width of the gate insulating film is greater than the gate electrode.

f. Limitation 1[e]: "an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode."

273. The combination of Matsumoto and Yu discloses limitation 1[e]: "an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode."

274. As seen in Figure 22, the end of high-k gate insulating film 6 is perpendicular to the substrate's surface, and located inward from the outer end of sidewall 9 (the outer end of the collective "insulating sidewall") toward the gate electrode. Thus, the end of the gate insulating film is "retracted from an outer end of the insulating sidewall toward the gate electrode."



Matsumoto, Fig. 22 (annotated and enlarged)

3. Dependent Claim 2: "The semiconductor device of claim 1, further comprising a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film."

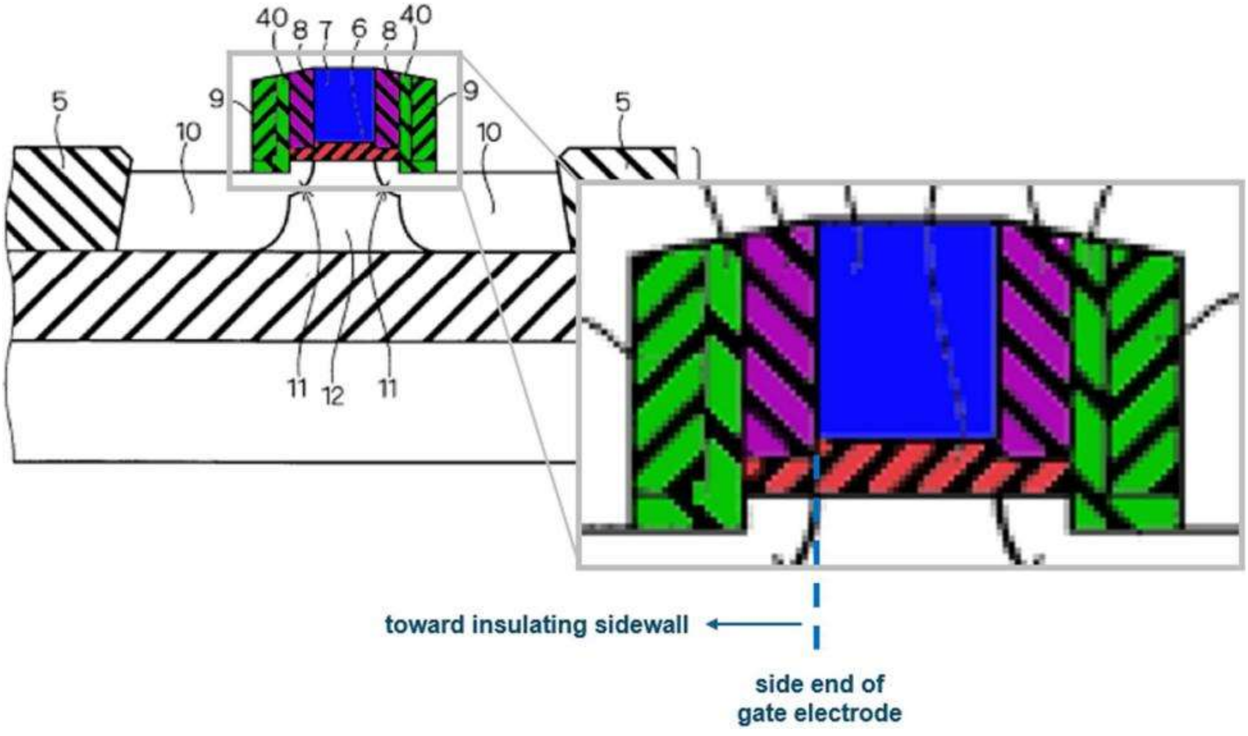
275. When Matsumoto and Yu are combined, Yu's buffer interface 36, which Yu teaches "can be a layer of silicon oxide," is located between the high-k dielectric and the substrate in Matsumoto's semiconductor device. (Yu, Ex.1048, 4:58-61, 3:62-63.) Buffer interface 36 is thus a "buffer insulating film formed of a silicon oxide film."

4. Dependent Claim 3: "The semiconductor device of claim 1, wherein the gate insulating film is formed of a Hf based oxide."

276. The combination of Matsumoto and Yu teaches the limitations of claim 3: "the gate insulating film is formed of a Hf based oxide." Matsumoto itself suggest using high-k materials as gate dielectrics, and considering the well-documented of HfO_2 in particular, a POSITA would have naturally viewed Yu's teachings together with Matsumoto to improve Matsumoto's semiconductor device. As discussed above in Section X.E.1.b, Yu teaches that gate dielectric 34 may be formed of "hafnium oxide (e.g., HfO_2)." (Yu, Ex.1048, 3:15-30.) The combination of Matsumoto and Yu would result in Matsumoto's gate insulating film being formed of a Hf-based oxide— namely, HfO_2—as suggested by Yu.

5. Dependent Claim 7: "The semiconductor device of claim 1, wherein an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall."

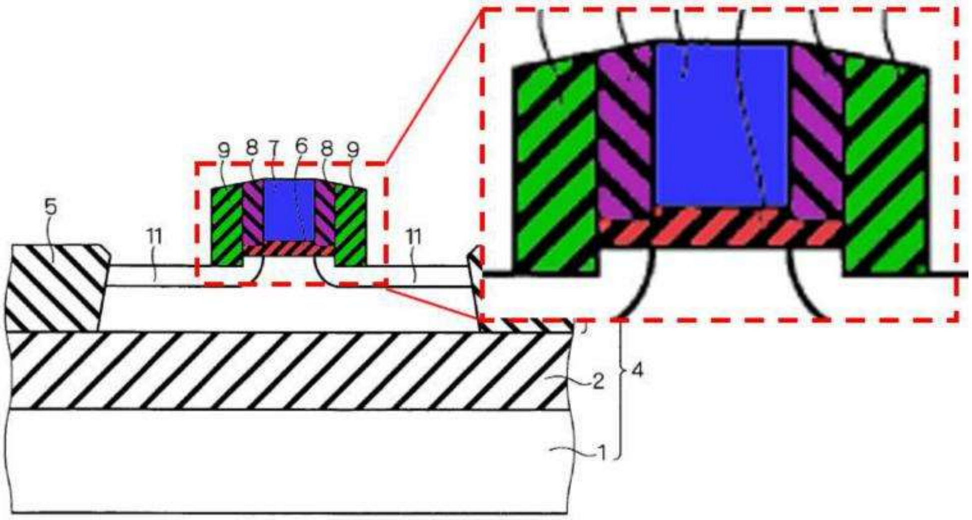
277. The combination of Matsumoto and Yu teaches the limitations of claim 7: "an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall." As discussed above in limitation 1[D], Matsumoto's gate insulating film 6 (shaded red) protrudes from underneath the gate electrode 7 to underneath sidewall 8 (part of the collective "insulating sidewall" comprising films 8, 40, and 9). It thus "protrudes from a side end of the gate electrode toward the insulating sidewall."



Matsumoto, Fig. 22 (annotated and enlarged)

6. Dependent Claim 8: "The semiconductor device of claim 1, wherein the insulating sidewall has a double layer structure including an oxide film and a nitride film."

278. Claim 8 requires a double layer structure for the insulating sidewall. Matsumoto discloses this claim. Specifically, Matsumoto discloses modifying the fourth embodiment to omit layer 40, as seen in Figure 23 below.



Matsumoto, Fig. 23 (annotated and enlarged)

279. In this modification, after silicon oxide film 8 is formed, "silicon nitride films 9 are formed directly on the upper surface of the silicon layer 3." (Matsumoto, Ex.1009, ¶141.) A POSITA would have considered each silicon oxide film 8 and silicon nitride films 9 to be a "layer" of the claimed insulating sidewall structure, consistent with the '076 patent. (Ex.1001, 20:43-52.) Thus, as seen in Figure 23, Matsumoto teaches that "the insulating sidewall" (here, the structure of silicon oxide film 8 and silicon nitride film 9) "has a double layer structure including an oxide film and a nitride film," as required by claim 14.

280. Matsumoto explains the modification "is applicable to any one of the first to fourth preferred embodiment," and as such, the analysis of claim 1 for Figure 22 applies equally to Figure 23. (Matsumoto, Ex.1009, ¶141 ("The technique of the first modification of the fourth preferred embodiment is applicable to any one of the first to fourth preferred embodiments.").) The modified fourth embodiment of Matsumoto with a silicon oxide and nitride film thus meets each limitation of claim 1.

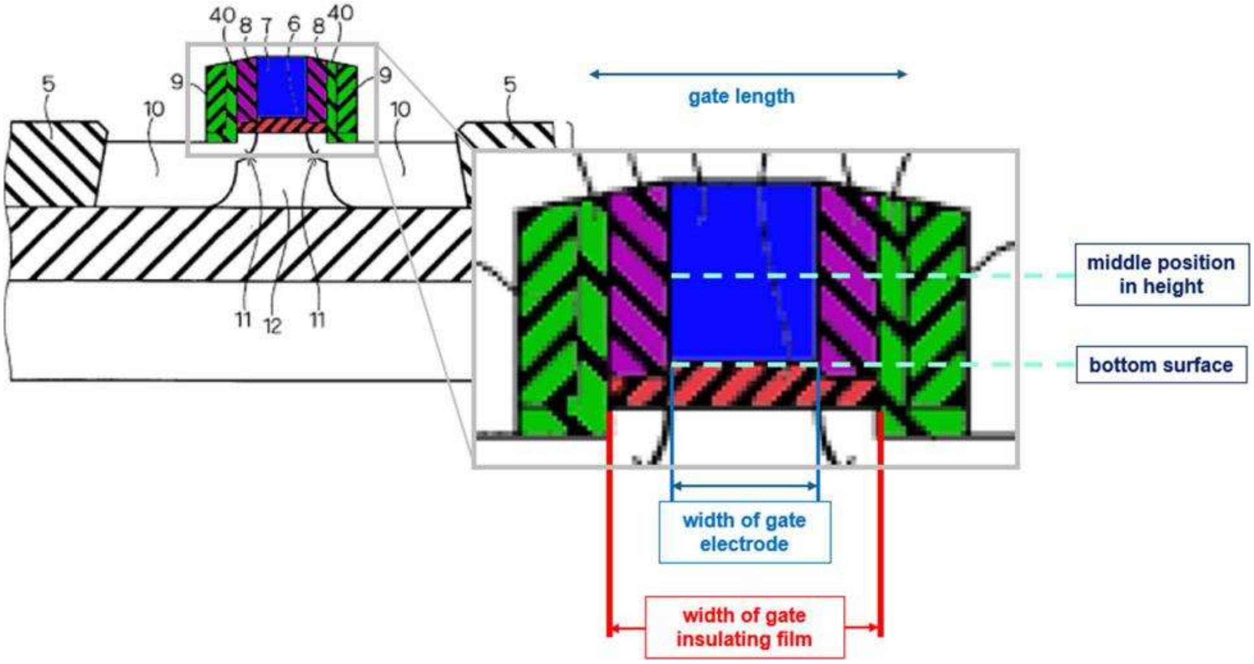
7. Dependent Claim 10: "The semiconductor device of claim 1, wherein a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length."

Dependent Claim 13: "The semiconductor device of claim 1, wherein the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length."

281. The combination of Matsumoto and Yu discloses claims 10 and 13: "a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length" [claim 10] and "the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length" [claim 13].

282. As I discuss above for limitation 1[d], Matsumoto's gate insulating film 6 extends from underneath the gate electrode to underneath film 8, which is part of

the collective "insulating sidewall" comprising films 8, 40, and 9. This can be seen below in Matsumoto's Figure 22.



Matsumoto, Fig. 22 (annotated and enlarged)

283. From Figure 22, the width of Matsumoto's gate electrode 7 is constant across the entire electrode. The width of the high-k gate insulating film 6 (shaded red) is larger than the gate electrode 7 (shaded blue). As discussed above in limitation 1[d]. the manufacturing process of Matsumoto's fourth embodiment, confirms the structures disclosed in Figure 22. As I discussed in other grounds, the finite anisotropy of the gate electrode RIE process is likely to make the gate electrode slightly narrower in the middle position than at the bottom, thus satisfying Claim 13 further.

F. Ground VI

284. In my opinion, the combination of Matsumoto, Yu, and Sim renders obvious Challenged Claim 6 of the ’076 patent (Ground VI).

1. Dependent Claim 6: “The semiconductor device of claim 1, wherein a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.”

285. The combination of Matsumoto and Yu teaches every limitation of claim 1, but does not disclose that “a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less” as required by claim 6. As discussed in Ground II, Sim provides this teaching, and the combination of Matsumoto, Yu, and Sim renders claim 6 obvious. Sim relates to semiconductor devices (Sim, Ex.1024, Abstract), and is in the same field as Matsumoto, Yu, and the ’076 patent. (Ex.1001, 1:18-19 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”) Matsumoto, Ex.1009, ¶2 (“The present invention relates to a semiconductor device and a method of manufacturing the same.”);Yu, Ex.1048, Abstract (“A MOSFET device and method of fabrication.”).)

286. As discussed above for the “First Combination” and limitation, the combination of Matsumoto and Yu uses a HfO_2 film for the high-k gate insulating film. A POSITA would have been motivated to use a thickness of 2 nm or less for

the gate film, as taught by Sim. The resulting combination includes a Hf-based high-k gate dielectric having "a thickness of 2 nm or less."

287. Sim explicitly teaches using a HfO_2 gate insulating film with a thickness 2 nm or less. Specifically, Sim concluded that "[s]caling the physical thickness of the HfO_2 dielectric to below 20Å causes less charge trapping and higher mobility." (Sim, Ex.1024, 221.) 20Å or Angstroms is equal to 2 nm, as recited by claim 6.

288. Applying Sim's teaching to Matsumoto and Yu yield a device where the high-k gate insulating film is less than 2 nm, as required by claim 6. For similar reasons discussed above, a POSITA would have been motivated to use Sim's gate insulating film with a thickness of 20Å (2 nm) or less. Matsumoto contemplates using a high-k gate dielectric and Yu discloses using HfO_2, the same film studied in Sim. Sim concludes that reducing the thickness of hafnium oxide to below 20Å enhances mobility and reduces charge trapping, which increases the performance and scalability of semiconductor devices. (Sim, Ex.1024, 219, 221.) These improvements align with the continued desire to make transistors smaller and more reliable, which all of Matsumoto, Yu, and Sim emphasize as objectives. (Matsumoto, Ex.1009, ¶13; Yu, Ex.1048, 1:39-41; Sim, Ex.1024, 218.)

289. The combination would also have been nothing more than the use of a known technique and structure (Sim's HfO_2 gate dielectric layer less than 20Å in

thickness) to improve similar devices (the combined device of Matsumoto and Yu having a hafnium oxide gate dielectric) in a predictable manner. A POSITA would have had a reasonable expectation of success because Sim uses a well-known process, atomic layer deposition (ALD), for manufacturing high-k films. (Sim, Ex.1024, 218; Houssa, Ex.1213, 17-19; see also Matsumoto, Ex.1009, ¶107 (disclosing depositing gate insulating film "by a CVD process or a thermal oxidation process.").)

G. Ground VII

290. In my opinion, the combination of Matsumoto and Koyama renders obvious Challenged Claim 1 of the '076 patent (Ground VII).

291. While Matsumoto teaches each and every limitation of claim 1, it does not explicitly disclose "a gate insulating film ... including Hf" in limitation 1[a]. This limitation is taught by Koyama. As I discussed above, Koyama studied using high-k materials as gate dielectrics for semiconductor devices (Koyama, Ex.1029, Title); it is thus in the same field as Matsumoto and the '076 patent. (Ex.1001, 1:18¬19 ("The present invention relates to a semiconductor device and a method for fabricating the semiconductor device."); Matsumoto, Ex.1009, ¶2 ("The present invention relates to a semiconductor device and a method of manufacturing the same.").)

292. In the combination of Matsumoto's fourth embodiment and Koyama, Matsumoto's gate insulating film 6 is made of HfSiON, as suggested by Koyama. The combination of Matsumoto and Koyama thus discloses "a gate insulating film ... including Hf." The disclosures of Matsumoto that I analyzed in Ground 5, in combination with Koyama's suggested to use HfSiON as a gate insulating film, render obvious claim 1 obvious.

293. Matsumoto already suggests a number of exemplary high-k films for use as a gate dielectric. Matsumoto teaches that "[a] silicon oxynitride film, a metal oxide film such as Al2O3 or a ferroelectric film such as Ta2O5 and BST may be formed in place of the silicon oxide film 13." (Matsumoto, Ex.1009, ¶107). As such, a POSITA would have found it obvious to use HfSiON as the gate insulating film in Matsumoto, as suggested by Koyama, because of its compatibility with high-k applications and its well-known advantages, including thermal stability and reduced leakage.

294. Koyama described that as early as 2002, "Hf(Zr) silicates are considered to be prospective high-K materials due to their modest dielectric constants and good interface properties." (Koyama, Ex.1029, 849.) Proposing to use a "HfSiON gate dielectric with excellent thermal stability," Koyama compared "the effects of nitrogen on the improved thermal stability and electrical characteristics of this dielectric." (Koyama, Ex.1029, 849.) Koyama concluded that "nitrogen [in

HfSiON] enhances the dielectric constant of silicates" and "boron penetration is substantially suppressed in the HfSiON during high temperature annealing." (Koyama, Ex.1029, 849.) These results "strongly suggest that HfSiON is the most probable material for first generation high-K gate dielectrics." (Koyama, Ex.1029, 850.)

295. By heeding Koyama's teaching to use HfSiON as a gate dielectric for its enhanced thermal stability and to minimize electron trapping, a POSITA would have had confidence in achieving the desired performance improvements by applying those teachings to Matsumoto's fourth embodiment. Further, a POSITA would have had a reasonable expectation of success, and the results of the combination would have been predictable, for all the reasons discussed above about the wide-spread use of high-k gate dielectrics.

H. Ground VIII

296. In my opinion, the combination of Matsumoto and Ono renders obvious Challenged Claims 1, 11, and 12 of the '076 patent (Ground VIII).

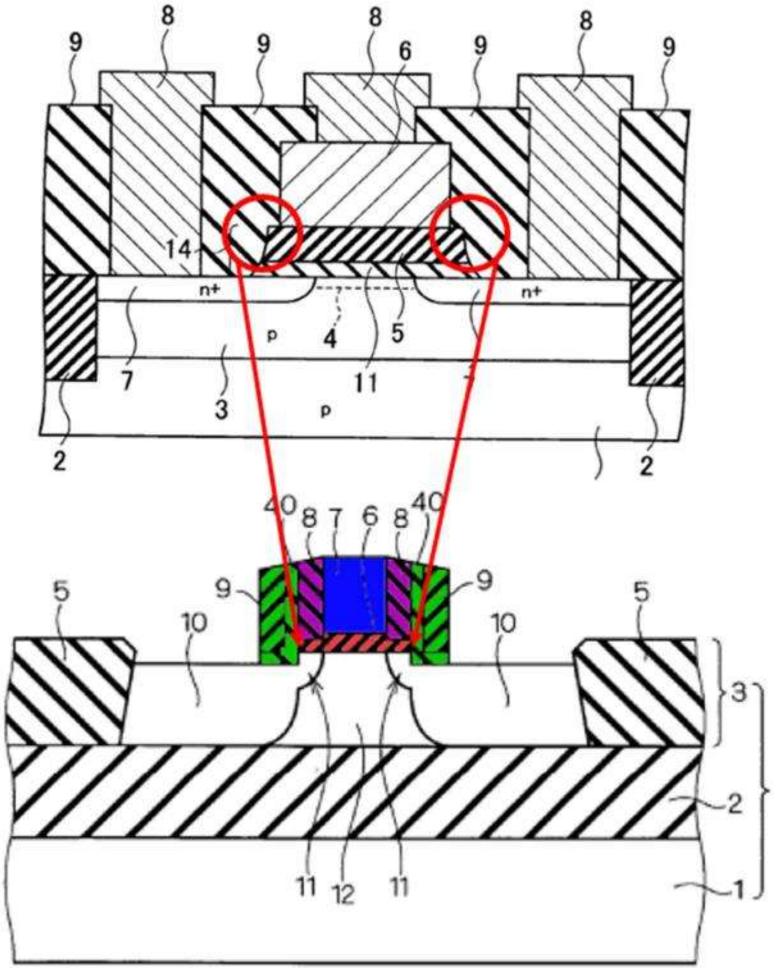
1. Motivation to Combine

297. A POSITA would have been motivated to combine the teachings of Matsumoto and Ono.

298. As discussed extensively already, a POSITA would have been motivated to select a Hf-based oxide as the gate insulating film in Matsumoto's

semiconductor device, as shown by Ono. (Ono, Ex.1013, ¶209 (describing use of a "HfO_2 film").) Further, a POSITA would have been motivated to select HfO_2 given its known benefits, e.g., "its superior thermal stability with poly-Si and reasonable band alignment." (Lee-2000, Ex.1337, 2.4.1; *see also* Houssa, Ex. 1213, 207 (HfO_2 "combines a high k (15–26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ..."); Lee-1999, Ex.1349, 134 ("Excellent dielectric properties ... suggest that HfO_2 is a promising material for the future gate dielectric application.").)

299. Additionally, a POSITA would have also been motivated to use Ono's disclosures of curving the end of the gate insulating film to Matsumoto's device, as illustrated below.



Ono, Figure 107 (top); Matsumoto, Figure 22 (bottom)

300. As taught by Ono, it was well known that modifying the end of the gate insulating film—such as curving or rounding it—optimizes electrical capacitance and improves device performance. This is an express goal of Matsumoto, which seeks to reduce parasitic capacitance and enhance gate controllability, defined objectives that support using the demonstrated benefits of Ono's curved gate insulating film ends. Thus, a POSITA would have been motivated combine Ono and Matsumoto in the manner described above.

301. Ono itself suggests this combination, disclosing that using curved side surfaces for gate insulating films "reduc[es] the scattering of carriers as well as enhanc[es] the controllability of the gate electrode with respect to the potential of the channel region" and therefore provides "an advantage of optimization." (Ono, Ex.1013, ¶216; see also Ono, Ex.1013, ¶200 (noting, for first embodiment, that by using curved side surfaces, "the electrical capacitance between the gate electrode 6 and the source/drain regions 7 may be adjusted," resulting in "an advantage of optimization").

302. Ono's curved sidewall can further be utilized in gate insulating films that overhang the gate electrode. It was understood that by extending the gate insulating film past the gate electrode, "the capacitive coupling between the source/drain regions 7 and the gate electrode 6 is strengthened, therefore advantages of reducing the resistance of the source/drain regions 7, controlling the parasitic capacitance as well as allowing high-speed operations are obtained." (Ono, Ex.1013, ¶¶215-216.)

303. Ono's suggestion to adjust the length and shape of the gate insulating film (e.g., to be slanted or curved) align with Matsumoto's goals of reducing overlap capacitance, improving speed, and lowering power consumption by minimizing the overlap between the gate electrode and the extension regions. (Matsumoto, Ex.1009, ¶47.) A POSITA would have been further motivated to curve the end of

Matsumoto's gate insulating film to enhance controllability of the gate and to optimize parasitic resistance and parasitic capacitance, which improves device performance. (See Ono, Ex.1013, ¶108.)

304. Applying Ono's disclosures to Matsumoto's fourth embodiment would have been nothing more than applying a known technique and structure (Ono's curved sidewalls and HfO_2 film for a gate insulating film) to improve similar devices (Matsumoto's transistor using a high-k gate insulating film) in the same way (modifying the dielectric layer to control capacitance). For example, Matsumoto and Ono both disclose forming high-k gate insulating films that extend under the gate electrode and the insulating sidewall using conventional techniques. (Matsumoto, Ex.1009, ¶114; Ono, Ex.1013, ¶167.) Given these known techniques, applying Ono to Matsumoto would have been within the skills of a POSITA and a POSITA would have had a reasonable expectation of success in making the combination.

2. Independent Claim 1

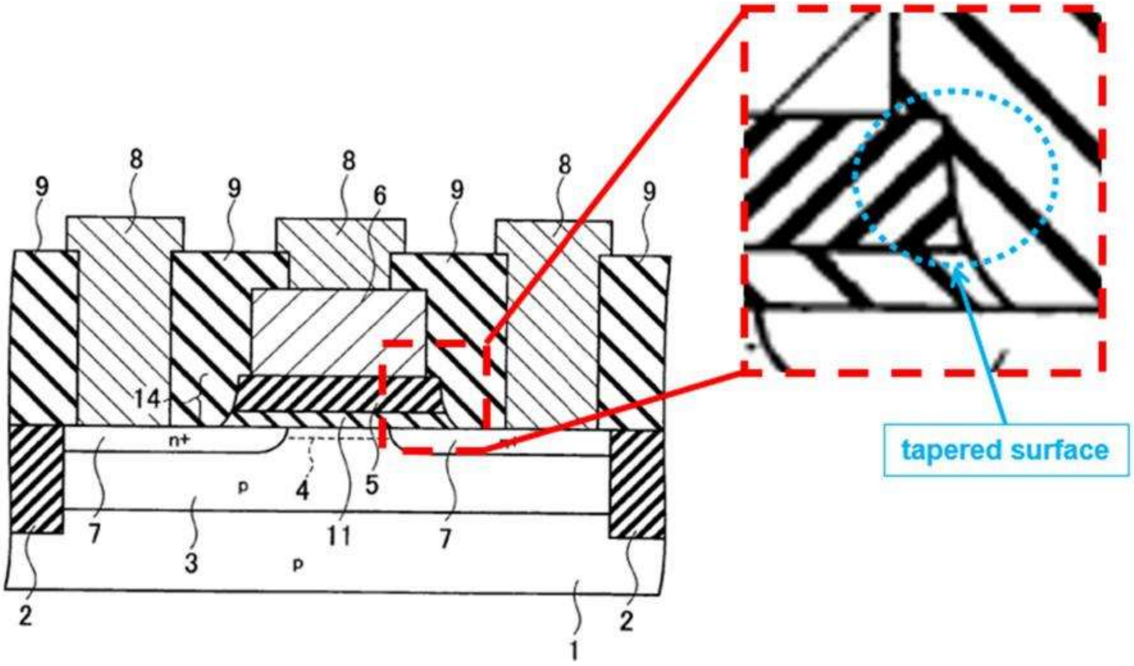
305. For the reasons I discussed in Ground V above, Matsumoto teaches each limitation of claim 1, except it does not expressly disclose "a gate insulating film ... including Hf" (Limitation 1[a]). In the combination of Matsumoto's fourth embodiment and Ono, Matsumoto's gate insulating film 6 comprises HfO_2, as suggested by Ono. (Ono, Ex.1013, ¶209.) Thus, the combination of Matsumoto and Ono renders obvious claim 1.

3. Dependent Claim 11: "The semiconductor device of claim 1, wherein the end of the gate insulating film located under the insulating sidewall has a tapered surface."

Dependent Claim 12: "The semiconductor device of claim 1, wherein the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof."

306. The combination of Matsumoto and Ono teaches the limitations of claims 11 and 12: "the end of the gate insulating film located under the insulating sidewall has a tapered surface" [claim 11] and "the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof" [claim 12].

307. Ono's suggestion of a curved end for the gate insulating film, for example in Figure 107, results in a tapered structure with decreasing thickness towards the ends. The combination of Matsumoto and Ono includes curved ends for gate insulating film with under the claimed "insulating sidewall," specifically, under sidewall film 8. When used in Matsumoto, this curved shape has a gate insulating film thickness that decreases toward the end, as seen below in Ono's Figure 107.



Ono, Fig. 107 (annotated and enlarged)

308. As seen above, the end of the gate insulating film in Ono's Figure 107 tapers at the end and thus has a thickness that is smallest at its end. Thus, the combination discloses the limitations of both claims 11 and 12.

XI. CONCLUSION

309. For the aforementioned reasons, in my opinion, to a POSITA, the Challenged Claims of the '076 patent are rendered obvious by the prior art.

310. I understand that the Patent Owner has not asserted secondary considerations of non-obviousness. I reserve the right to respond to any such assertions.

311. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be

true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the results of the proceedings.

Date: June 6, 2025　　　Respectfully submitted,

Sanjay Banerjee

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Sanjay Banerjee, Ph.D.