

## Mobility Enhancement in Strained Si NMOSFETs with HfO<sub>2</sub> Gate Dielectrics

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### Abstract

Integration of strained Si and high-K gate dielectric is demonstrated for the first time. While providing a >1000× gate leakage reduction, strained Si NMOSFETs with HfO<sub>2</sub> gate dielectric exhibit 60% higher mobility than the unstrained Si device with HfO<sub>2</sub> gate dielectrics, and 30% higher mobility than the conventional Si NMOSFETs with SiO<sub>2</sub> gate dielectric (universal MOSFET mobility).

### Introduction

Gate leakage reduction in ultra thin gate dielectric is the main motivation for the search of high-K materials [1, 2]. Electrical results on various candidate materials such as HfO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> have shown leakage reduction by orders of magnitude, but have also highlighted the integration challenges such as charge trapping-related  $V_T$  instability and mobility degradation. On the other hand, dramatic mobility enhancements have been reported in strained Si MOSFETs [3-6]. Biaxial tensile strain in Si splits the conduction band degeneracy, reducing the intervalley phonon scattering and increasing the electron mobility. In this report, we demonstrate that integration of high-K dielectrics with strained Si significantly enhances electron mobility. Furthermore, we use the analysis of the effective mobility characteristics to gain understanding of the mechanisms that limit mobility in the high-K dielectric/Si interface.

### Fabrication and Electrical Characteristics

Strained Si and HfO<sub>2</sub> gate dielectrics were integrated using a standard CMOS process modified for the material compatibility [5]. Fig. 1 shows a schematic illustration of the device structure. A thin layer of tensile-strained Si was epitaxially grown on a ~1.5 μm thick layer of relaxed SiGe (15% [Ge]) by UHV/CVD. Devices were also fabricated on the control CZ Si substrates for comparison. After the device isolation and well implants, a 3 nm-thick HfO<sub>2</sub> layer was deposited by ALD [1] on a thin (sub-1 nm) interfacial oxynitride. The control devices were fabricated at the same time with a 2.2 nm-thick conventional nitrided SiO<sub>2</sub> on both CZ Si and strained Si substrates (Table 1). After polysilicon gate deposition and patterning, the fabrication process continued with the spacer formation, source/drain implant, activation anneal, and silicidation. The XTEM micrograph of the gate stack is shown in Fig. 2.

The split  $C-V$  technique was used to measure the gate to inversion channel capacitance as shown in Fig. 3. The inversion equivalent oxide thickness ( $EOT_{inv}$ ) was 2.8 and 3.1 nm for HfO<sub>2</sub> and SiO<sub>2</sub>, respectively. The  $C-V$ 's in the HfO<sub>2</sub> devices exhibited shift in the positive gate bias direction due to the fixed and trapped charges, consistent with previous reports [1].

Gate leakage current is shown as a function of the gate bias in Fig. 4. Although the  $T_{inv}$  is ~0.3 nm thinner in the HfO<sub>2</sub> devices, a significant leakage reduction is observed due to the higher dielectric constant. Compared with SiO<sub>2</sub> at an equivalent  $T_{inv}$  and gate over-drive, HfO<sub>2</sub> provides more than 1000× reduction in gate leakage current (Fig. 5).

Long channel NFET  $I_D-V_{GS}$  characteristics are shown in Fig. 6. The strained Si device with HfO<sub>2</sub> gate dielectric ("HfO<sub>2</sub>/SS") exhibits an excellent subthreshold slope of ~80 mV/dec, comparable to the SiO<sub>2</sub> control devices. Near the threshold, the subthreshold slope is slightly degraded in the HfO<sub>2</sub> devices possibly due to the combination of charge trapping and lower mobility near and below the threshold. However, the comparison of  $I_D-V_{DS}$  characteristics at equivalent gate over-drives (Fig. 7) show that the output current of the HfO<sub>2</sub>/SS device slightly higher (comparable when  $T_{inv}$  difference

is accounted for) than the CZ Si device with SiO<sub>2</sub> ("SiO<sub>2</sub>/CZ") due to the higher mobility in the HfO<sub>2</sub>/SS device above the threshold.

### NMOSFET Mobility Characteristics

Effective electron mobility was extracted using  $I-V$  and  $C-V$  measurements on large area NFETs [7]. Inversion charge density  $Q_{inv}$  was calculated by integrating the gate-to-channel capacitance, and the vertical effective field  $E_{eff}$  was calculated by [7]:

$$E_{eff} = \frac{1}{\epsilon_{Si}} \cdot \left( Q_{dpt} + \frac{1}{2} \cdot Q_{inv} \right)$$

where  $Q_{dpt}$  is the integrated maximum depletion charge.

Fig. 8 shows the comparison of effective mobility. The mobility of the SiO<sub>2</sub>/CZ device closely follows the universal mobility [7] as expected, and the high mobility in the strained Si device with SiO<sub>2</sub> ("SiO<sub>2</sub>/SS") is consistent with the reported enhancement of NFET mobility in strained Si NFETs [5]. The mobility of the CZ Si device with HfO<sub>2</sub> ("HfO<sub>2</sub>/CZ") is degraded compared to the universal mobility, consistent with the previously reported results ([1] for example). However, the mobility of the HfO<sub>2</sub>/SS device is enhanced over the universal MOSFET mobility for  $E_{eff}$  of >1 MV/cm. At 1.4 MV/cm, the HfO<sub>2</sub>/SS device exhibits a 30% higher mobility than the universal mobility and the SiO<sub>2</sub>/CZ control device, and a 60% higher mobility than the HfO<sub>2</sub>/CZ control device. This represents, to our best knowledge, the best mobility characteristics achieved in FETs with high-K dielectrics. The amount of strain-induced mobility enhancement in the HfO<sub>2</sub> device is comparable to that observed in the SiO<sub>2</sub> devices. Strained Si devices with Al<sub>2</sub>O<sub>3</sub> were also fabricated, and exhibited similar enhancements over the previously reported mobility of the Al<sub>2</sub>O<sub>3</sub>/CZ devices [1, 2].

### Analysis of HfO<sub>2</sub>-limited Mobility

The mobility characteristics of the HfO<sub>2</sub>/SS devices suggest that the Coulomb scattering due to the trapped and fixed charges in the dielectric may be the dominating mechanism responsible for mobility degradation observed in the NFETs with high-K dielectrics. MOSFET mobility can be expressed as a Matthiessen's sum of the mobilities limited by various mechanisms such as Coulomb, phonon, and surface roughness scattering (inset in Fig. 8) [7]:

$$1/\mu_{total} = 1/\mu_{Coul} + 1/\mu_{phonon} + 1/\mu_{surf.rough}$$

It has been experimentally shown that strain in Si enhances the electron mobility in the intermediate to high  $E_{eff}$  range where the mobility is limited by phonon and surface roughness scattering [5]. The large mobility enhancement exhibited by the HfO<sub>2</sub>/SS device over the HfO<sub>2</sub>/CZ device strongly suggests the absence of another mobility-limiting scattering mechanism related to HfO<sub>2</sub> in such  $E_{eff}$  range. In other words, if there were a mechanism that limits the mobility at high effective fields (such as increased phonon or roughness scattering), one would not expect to see the dramatic, strain-induced mobility enhancement over the universal mobility.

Fig. 9 shows the mobility component limited by the HfO<sub>2</sub>-related scattering mechanisms. These mobility components were computed for the CZ Si and SS devices by taking the difference of the measured mobility of the SiO<sub>2</sub> and HfO<sub>2</sub> devices (inset in Fig. 9). The HfO<sub>2</sub>-limited mobilities extracted from strained Si and CZ Si are comparable in magnitude within the accuracy of the analysis, and show a positive power dependence on carrier density, characteristic of Coulomb scattering-limited mobility that becomes less dominant with increasing amount of screening by free carriers.

Integration of strained Si and high-K dielectrics provides an improved trade-off between device performance and gate leakage.

Fig. 10 illustrates such trade-off by comparing the gate leakage and mobility at a given effective field and carrier concentration for the particular set of devices studied in this work. The HfO<sub>2</sub>/SS device improves the mobility over the conventional SiO<sub>2</sub>/CZ device while reducing the gate leakage.

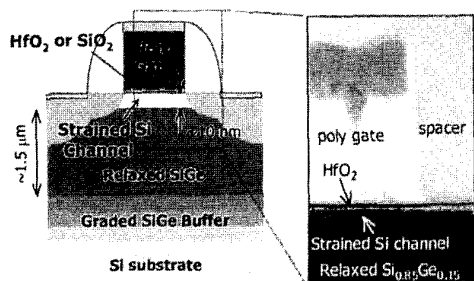
### Conclusion

Strained Si NFETs with high-K dielectrics exhibit significantly enhanced NFET mobility, even over the universal mobility of the SiO<sub>2</sub>/bulk Si devices, and hold the promise for the best trade-off

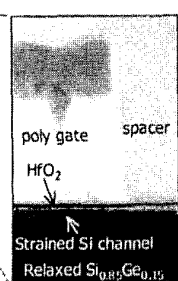
between mobility and gate leakage reduction, which is especially attractive for low power, high performance CMOS technology.

### References

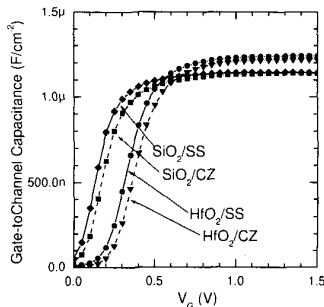
- [1] E. Gusev, *et al.*, *IEDM Tech. Dig.*, p. 451, 2001.
- [2] D. Buchanan, *et al.*, *IEDM Tech. Dig.*, p. 223, 2000.
- [3] J. Welser, *et al.*, *IEDM Tech. Dig.*, p. 947, 1994.
- [4] T. Mizuno, *et al.*, *Symp. on VLSI Tech.*, p. 210, 2000.
- [5] K. Rim, *et al.*, *Symp. on VLSI Tech.*, p. 59, 2001.
- [6] N. Sugii, *et al.*, *IEDM Tech. Dig.*, p. 737, 2001.
- [7] S. Takagi, *et al.*, *IEEE Trans. Elec. Dev.*, **41**, p. 2357, 1994.



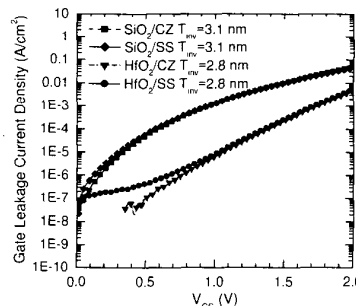
**Fig. 1** A schematic illustration of a strained Si FET with high-K gate dielectrics.



**Fig. 2** XTEM micrograph of the gate stack in a strained-Si NFET with HfO<sub>2</sub> gate dielectric.



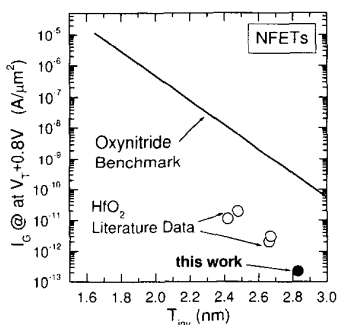
**Fig. 3** Gate-to-channel  $C-V$  characteristics measured by the split  $C-V$  technique.



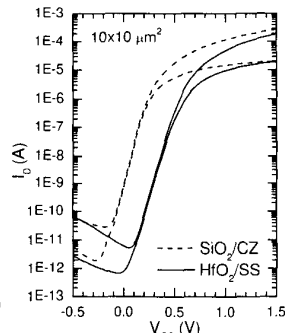
**Fig. 4** Comparison of gate current characteristics.

**Table 1.** Experimental matrix and comparison of mobility (in cm<sup>2</sup>/V·s) at  $E_{eff} = 1.4 \text{ MV/cm}$ .

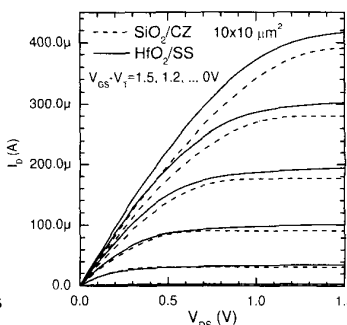
Gate Dielec.	Substrate	
	CZ Si	Strained Si
SiO <sub>2</sub>	SiO <sub>2</sub> /CZ 173	SiO <sub>2</sub> /SS 271
HfO <sub>2</sub>	HfO <sub>2</sub> /CZ 134	HfO <sub>2</sub> /SS 218



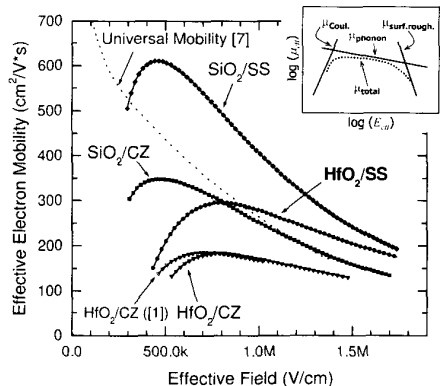
**Fig. 5** Gate leakage comparison at constant gate over-drive and  $T_{inv}$ . HfO<sub>2</sub> provides a gate leakage reduction by > 1000×.



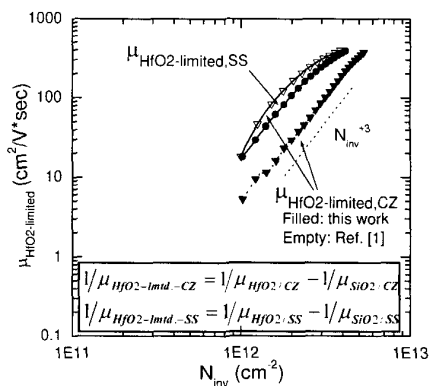
**Fig. 6**  $I_D-V_{GS}$  characteristics of the HfO<sub>2</sub>/SS NFET. Good subthreshold slopes (80 mV/dec) are observed.



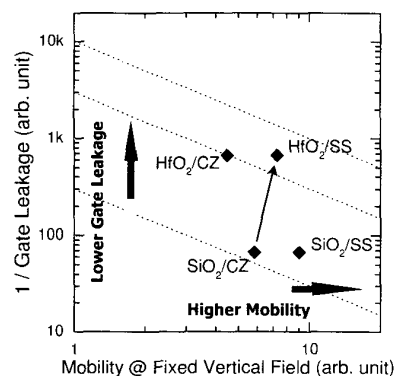
**Fig. 7**  $I_D-V_{DS}$  characteristics of the HfO<sub>2</sub>/SS NFET. Current is comparable to that of SiO<sub>2</sub>/CZ NFET when  $T_{inv}$  difference is taken into account.



**Fig. 8** Effective mobility of NFETs as a function of vertical effective field. The HfO<sub>2</sub>/SS device exhibits mobility enhancement over the control and the universal mobility at  $E_{eff} > 1 \text{ MV/cm}$ . The inset shows the various components of MOSFET mobility.



**Fig. 9** Mobility limited by HfO<sub>2</sub>-related Coulomb scattering as a function of inversion carrier density. Mobility values extracted from the SS and CZ Si devices are comparable in magnitude and show similar carrier density dependence.



**Fig. 10** Gate leakage vs. NFET mobility at a given vertical field and carrier concentration. The HfO<sub>2</sub>/SS device exhibited higher mobility and lower gate leakage although  $T_{inv}$  of HfO<sub>2</sub> was 0.3 nm thinner than SiO<sub>2</sub>.