

# High Quality Ultra Thin CVD HfO<sub>2</sub> Gate Stack with Poly-Si Gate Electrode

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## Abstract

We have developed and demonstrated an *in-situ* rapid thermal CVD (RTCVD) process for the fabrication of high quality ultra thin CVD HfO<sub>2</sub> gate stack that is compatible with conventional self-aligned poly-Si gate technology. These poly-Si gated HfO<sub>2</sub> gate stack show excellent interface properties, EOT=10.4Å, and leakage current  $J_g=0.23\text{mA/cm}^2$  @  $V_g=-1\text{V}$  which is several orders of magnitude lower than RTO SiO<sub>2</sub> with poly-Si gate. In addition, the HfO<sub>2</sub> gate stack is thermally stable in direct contact with n<sup>+</sup>-poly Si gate under typical dopant activation conditions. These films also show excellent reliability under high-field electrical stress. We have also fabricated and demonstrated NMOSFETs, and studied boron penetration in HfO<sub>2</sub> gate stack with p<sup>+</sup>-poly Si gate.

## Introduction

In an attempt to develop advanced gate dielectric film replacing SiO<sub>2</sub>, many high-K materials have been investigated to meet the requirements for sub-100 nm technology. Key issues related to the development of high-K gate stack with conventional dual-gate poly-Si CMOS process are the thermal stability of high-K materials in direct contact with silicon and poly-Si at high temperatures, high quality interfaces with channel and gate electrode, reasonable barrier height to achieve low leakage current, and suppressed boron penetration. The compatibility of high-K gate stack with conventional poly-Si dual-gate CMOS process has received considerable attention. Recently, HfO<sub>2</sub> films have emerged as the most promising gate dielectric material for sub 100nm technology due to its superior thermal stability with poly-Si and reasonable band alignment [1], [2]. Kang et al. used PVD sputtered HfO<sub>2</sub> and poly-Si electrode to fabricate the MOS devices with the CET (Capacitance Equivalent Thickness) of 16.3Å and good leakage current [3].

In this paper, we report the electrical and chemical properties, thermal stabilities, reliability characteristics, and NMOSFET characteristics of ultra thin (EOT=10.4Å) CVD HfO<sub>2</sub> with conventional poly-Si gate process.

## Experiment

The MOS capacitors used in our study with the HfO<sub>2</sub> gate stack were fabricated on Si substrates using an *in-situ* RTP multiprocessing whose process procedure is shown in Fig 1. After the standard RCA cleaning with final HF dip, the NH<sub>3</sub>-based interface layer was grown at 700°C for 10sec. The CVD HfO<sub>2</sub> films were deposited at 500°C for 3min using O<sub>2</sub> and C<sub>16</sub>H<sub>36</sub>HfO<sub>4</sub> with N<sub>2</sub> as a carrier gas. The *in-situ* post-deposition annealing was performed in an N<sub>2</sub> ambient at 700~900°C for 30sec to improve the film quality and reduce the leakage current. The amorphous Si gate (~1600Å) was deposited directly on the HfO<sub>2</sub> at 540°C, followed by either POCl<sub>3</sub> doping at 900°C or ion implantation of Phosphorus for NMOS and BF<sub>2</sub> for PMOS. The gate dopants were activated at 900 ~ 1000°C for 30 ~ 60sec. The NMOSFETs were also fabricated with conventional self-aligned poly-Si gate process.

The EOT (Equivalent Oxide Thickness) is extracted from the simulation program considering quantum mechanical (QM) and poly-depletion effects. The chemical properties and thermal stability of ultra-thin HfO<sub>2</sub> gate stacks with poly-Si capping were investigated by an *in-situ* XPS (X-ray Photoelectron Spectroscopy) in an integrated CVD film growth and analysis system.

## Results and Discussion

### 1. High quality HfO<sub>2</sub> gate stack with conventional n<sup>+</sup>-poly Si gate process

The importance of the NH<sub>3</sub>-based interface layer on the high-K dielectric to improve the interfacial properties and reduce the final EOT was reported in [4]. The NH<sub>3</sub>-based interface layer provides strong resistance to oxidation of the silicon substrate during the CVD of HfO<sub>2</sub> and, more importantly, during the post-deposition annealing. It is found that N<sub>2</sub> post deposition annealing is very effective to improve the film quality and reduce the leakage current. By using these processes, we have achieved HfO<sub>2</sub> gate stack with EOT=10.4Å and

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$J_g=0.23\text{mA/cm}^2$  @ $V_g=-1\text{V}$ , as shown in Fig. 2. The negligible difference between the measured HFCV and the simulated LFCV and a smooth transition in depletion region indicate extremely low interface state density. The flat band voltage of  $n^+$ -poly Si-gated  $\text{HfO}_2$  gate stack is  $-0.8\text{V}$ , which is similar to that of the  $\text{SiO}_2$  with  $n^+$ -poly Si gate and the same substrate doping concentration. The  $\text{HfO}_2$  gate stack with  $n^+$ -poly Si gate shows  $>10^4$  times lower leakage current @ $V_g=-1\text{V}$  than that of  $\text{SiO}_2$  for  $\text{EOT}<15\text{\AA}$  (Fig. 3).

The hysteresis characteristics in HFCV of the  $\text{HfO}_2$  gate stack is compared with different gate electrode by monitoring the amounts of flat band voltage shift (Fig. 4). The  $V_{\text{FB}}$  shifts after 4 sweeps between  $\pm 2\text{V}$  for  $n^+$ -poly Si gate devices are extremely low:  $2\text{mV}$  for  $\text{POCL}_3$  doped and  $5\text{mV}$  for P-implanted, compared to  $32\text{mV}$  for TiN/Al gate, indicating hysteresis characteristics are strongly affected by gate material. These films also show negligible frequency dependence in HFCV (Fig. 5) over the range of  $10\text{kHz}-1\text{MHz}$ , indicating negligible slow interface traps in  $\text{HfO}_2$  gate stack.

The thermal stability of the CVD  $\text{HfO}_2$  gate stack with  $n^+$ -poly Si gate is studied by monitoring the changes in both C-V and I-V of the gate stack as a function of several gate activation conditions (Fig. 6). As can be seen from Fig. 6, negligible changes in both C-V and I-V are observed, indicating that  $\text{HfO}_2$  is thermally stable after  $950^\circ\text{C}$  anneal in direct contact with  $n^+$ -poly Si gate.

The thermal stability of CVD  $\text{HfO}_2$  gate stack is also examined by *in-situ* XPS analysis in an integrated CVD film growth and surface analysis system. After the CVD of  $\text{HfO}_2$  and  $\text{N}_2$  post-deposition anneal, poly-Si was deposited at  $600^\circ\text{C}$ , followed by  $\text{N}_2$  anneal at  $900, 950^\circ\text{C}$ . As shown in Fig. 7, CVD  $\text{HfO}_2$  films remain stable after poly-Si deposition and annealing in UHV  $\text{N}_2$  ambient up to  $950^\circ\text{C}$ , and show no evidence of the formation of undesirable Hf metal or Hf silicide phases. No changes in C-V and I-V were found after forming gas sintering ( $450^\circ\text{C}$ ,  $30\text{min}$ ) either. The HRXTEM of the  $\text{HfO}_2$  gate stack with  $n^+$ -poly Si gate in Fig. 8 shows extremely thin interface layer below CVD  $\text{HfO}_2$  and sharp interfaces, with  $\text{HfO}_2$  film remaining amorphous after gate activation at  $950^\circ\text{C}$  for  $60\text{sec}$ . The dielectric constant of the CVD  $\text{HfO}_2$  layer is estimated to be 24.

## 2. Reliability, Boron penetration, and NMOSFET characteristics

The  $\text{HfO}_2$  with  $n^+$ -poly Si gate displays fairly weak temperature dependence of the I-V characteristics (Fig. 9), indicating that trap-assisted conduction in this film is not the dominant mechanism. The reliability characteristics of  $\text{HfO}_2$  gate stack was studied by investigating the SILC (Stress Induced Leakage Current)

and charge trapping characteristics under constant voltage stress. The SILC was measured under negative constant voltage stress with  $E=16\text{MV/cm}$ . After applying stress for  $1000\text{sec}$ , the increase of leakage current is negligible at low electric field ( $V_g=-0.5\text{V}$ ) (Fig. 10(a)). The negligible charge trapping in  $\text{HfO}_2$  gate stack is observed during constant voltage stress with  $E=16\text{MV/cm}$  (Fig. 10(b)). Under extremely high field stressing ( $E>20\text{MV/cm}$ ), both soft and hard breakdown, as well as SILC could be seen. As a result, it is very difficult to obtain long-term TDDDB on CVD  $\text{HfO}_2$  gate stack. Fig. 11 shows boron penetration characteristics in  $p^+$ -poly  $\text{HfO}_2$  gate stack on n-type Si substrates. Up to  $1000^\circ\text{C}$ ,  $10\text{sec}$  annealing, negligible flat band voltage shift was found, suggesting no boron penetration. However, upon  $1000^\circ\text{C}$ ,  $30\text{sec}$  annealing, boron penetration is observed. Fig. 12 shows Id-Vd characteristics of NMOSFET with  $\text{HfO}_2$  gate stack and  $n^+$ -poly Si gate. Fig. 13 shows Id-Vg characteristics of  $\text{HfO}_2$  with excellent sub-threshold swing of  $73\text{mV/dec}$

## Summary

In this paper, we report ultra thin high quality CVD  $\text{HfO}_2$  poly-Si gated stack with  $\text{EOT}=10.4\text{\AA}$  and  $J_g=0.23\text{mA/cm}^2$  @ $V_g=-1\text{V}$ . This film shows good interface properties, extremely small hysteresis ( $<5\text{mV}$ ) and negligible frequency dependence in HFCV, and excellent reliability characteristics. The thermal stability of the  $\text{HfO}_2$  with  $n^+$ -poly Si gate is confirmed by the electrical measurements, *in-situ* XPS analysis and the HRXTEM. NMOSFETs fabricated with  $\text{HfO}_2$  gate stack demonstrate good drive current and excellent sub-threshold swing. Boron penetration in these films is also investigated. Our results suggest that CVD  $\text{HfO}_2$  gate stack is very promising for possible direct insertion into standard dual-gate CMOS process.

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## References

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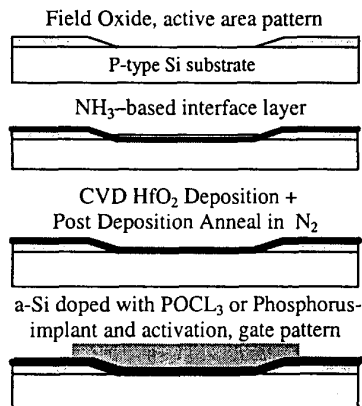


Fig. 1. In-situ RTP fabrication process for HfO<sub>2</sub> gate stack.

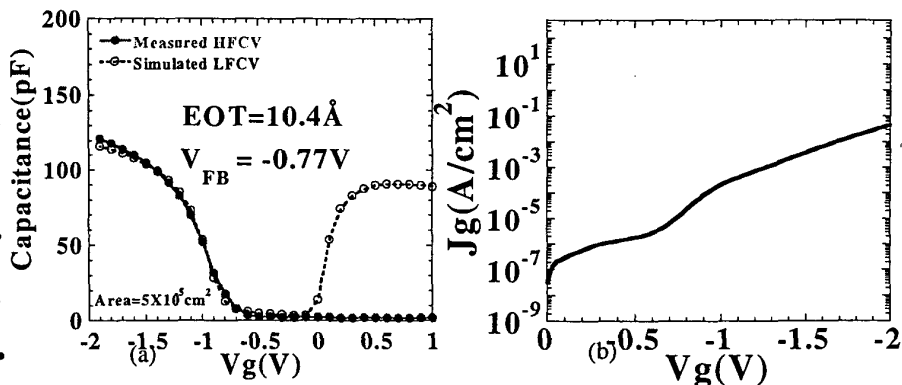


Fig. 2. (a) Measured HFCV and Simulated LFCV and (b) Jg-Vg of HfO<sub>2</sub> gate stack with a-Si gate doped with Phosphorus-implantation.

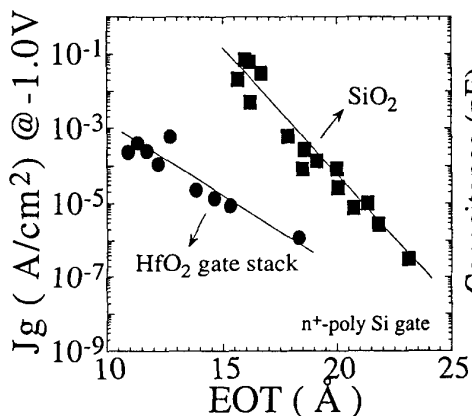


Fig. 3. Current density @ Vg=-1V as a function of EOT for HfO<sub>2</sub> and SiO<sub>2</sub> with n<sup>+</sup>-poly Si gate.

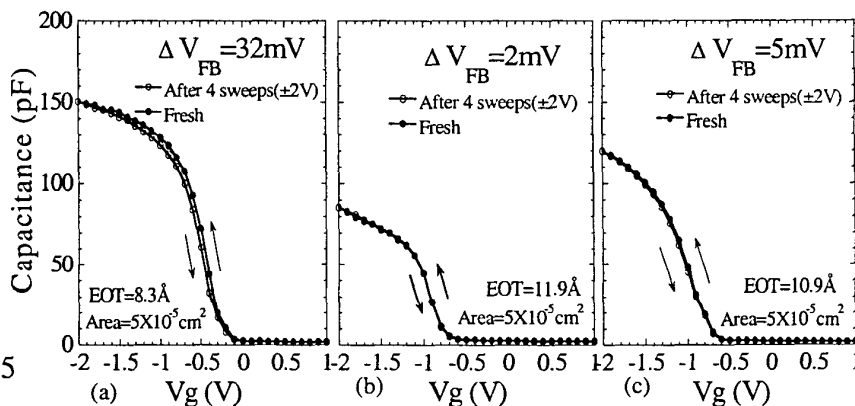


Fig. 4. Hysteresis in HFCV of HfO<sub>2</sub> gate stack with (a)TiN/Al gate, (b)a-Si gate doped with POCL<sub>3</sub> (c)a-Si doped with Phosphorus-implantation.

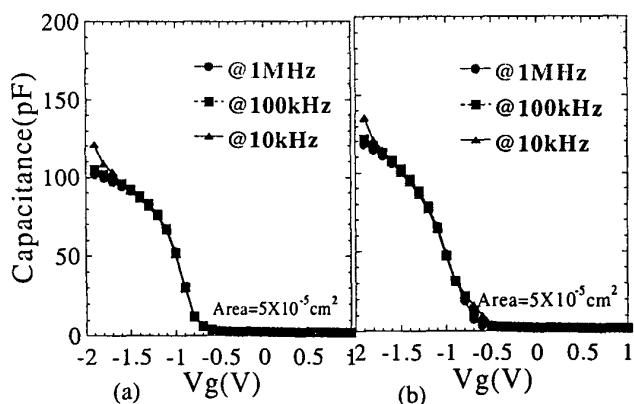


Fig. 5. Frequency dependence in HFCV of HfO<sub>2</sub> gate stack with (a)a-Si gate doped with POCL<sub>3</sub> (b)a-Si gate with Phosphorus-implantation.

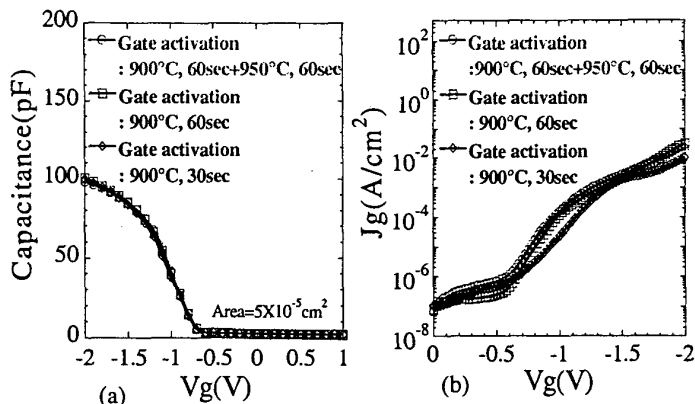


Fig. 6. Thermal stability of HfO<sub>2</sub> gate stack with n<sup>+</sup>-poly Si gate : effects of different Phosphorus activation temperature and time on (a) HFCV and (b) Jg-Vg.

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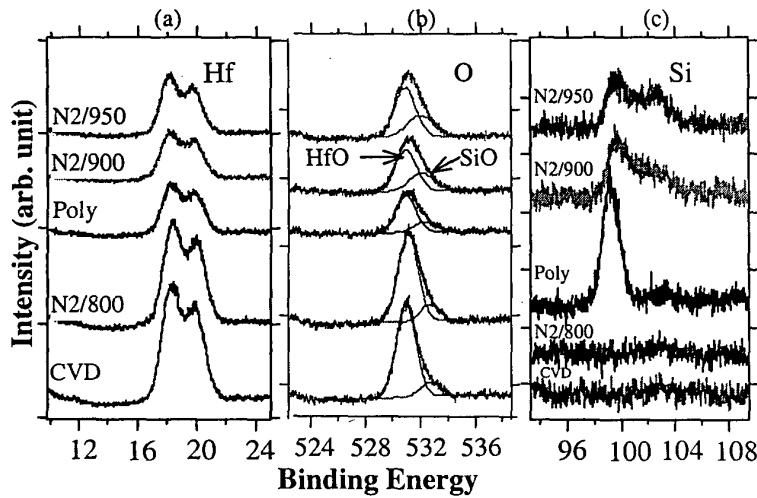


Fig. 7. XPS analysis of (a) Hf 4f, (b) O 1s and (c) Si 2p of HfO<sub>2</sub> gate stack deposited on clean Si(100) at 450°C for 2min followed by N<sub>2</sub> annealing at 800°C for 1min, poly-Si deposition at 600°C and N<sub>2</sub> annealing at 900°C and 950°C for 30sec.

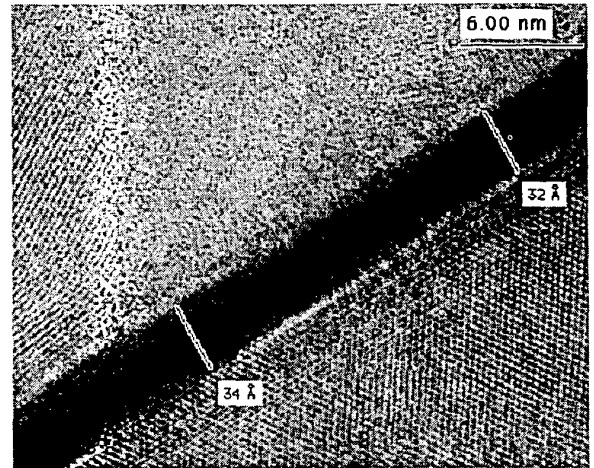


Fig. 8. TEM picture of HfO<sub>2</sub> gate stack with a-Si gate doped with P-implant (Gate Activation : 900°C, 60sec + 950°C, 60sec).

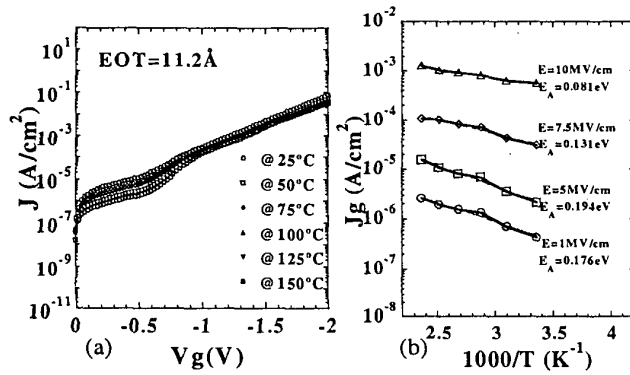


Fig. 9. (a) J<sub>g</sub>-V<sub>g</sub> at different temperature (b) Arrhenius's plot of temperature dependent leakage current of HfO<sub>2</sub> gate stack with a-Si gate doped with Phosphorus implantation.

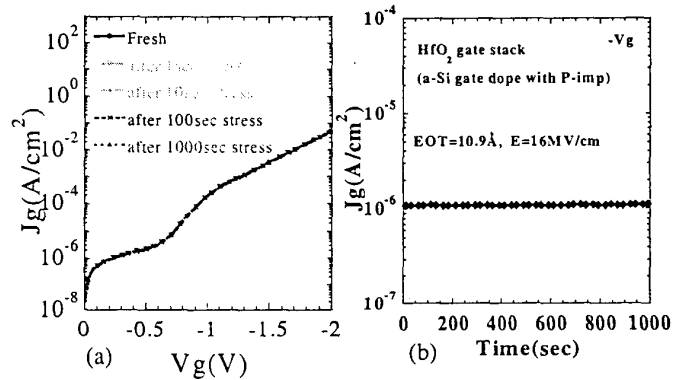


Fig. 10. (a) J<sub>g</sub>-V<sub>g</sub> after constant voltage stress (b) J<sub>g</sub>-Time during during constant voltage stress of HfO<sub>2</sub> gate stack with a-Si gate doped with Phosphorus implantation.

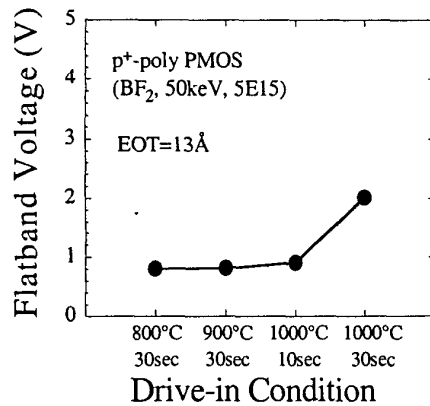


Fig. 11. Boron penetration characteristics of HfO<sub>2</sub> gate stack by flatband voltage shift during gate activation.

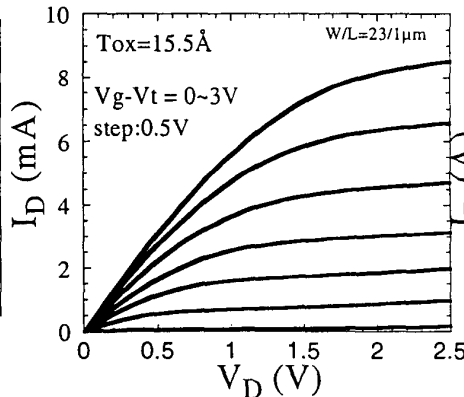


Fig. 12. Id-V<sub>d</sub> characteristics of NMOSFET (HfO<sub>2</sub> gate stack with n<sup>+</sup>-poly Si gate).

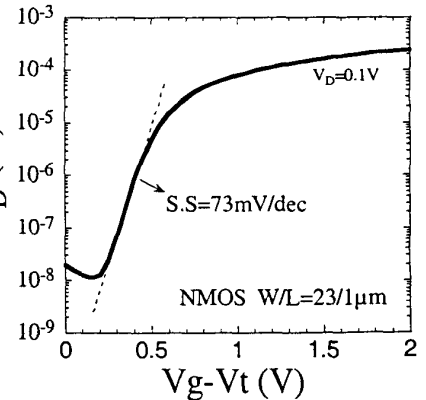


Fig. 13. Id-V<sub>g</sub> characteristics of NMOSFET (HfO<sub>2</sub> gate stack with n<sup>+</sup>-poly Si gate).

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