

Self-Aligned Ultra Thin HfO₂ CMOS Transistors with High Quality CVD TaN Gate Electrode

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Abstract

In this paper, we have demonstrated and characterized self-aligned, gate-first CVD TaN gate n- and p-MOS transistors with ultra thin (EOT=11~12Å) CVD HfO₂ gate dielectrics. These transistors show no sign of gate deletion and excellent thermal stability after 1000°C, 30s N₂ anneal. Compared with PVD TaN devices, the CVD TaN/HfO₂ devices exhibit lower leakage current, smaller CV hysteresis, superior interface properties, higher transconductance, and superior electron and hole mobility.

Introduction

As CMOS devices are scaled into sub-0.1 um regime, poly-depletion effects and boron penetration become significant concerns. Therefore, metal gate electrodes are being explored to replace the polysilicon gate. Refractory PVD metals have been studied for CMOS gate electrode with high-K gate dielectrics [1-4]. However, PVD may produce plasma damages on thin dielectric and dielectric/Si interface, resulting in gate dielectric long-term reliability and channel mobility degradations. In addition, PVD metal gates suffer from poor conformality which makes it unsuitable for future generation devices such as double-gate FinFET [5] or vertical replacement-gate [6] structures. It has been reported that CVD TaN films deposited using TBTDET (tertbutylimidotrisdiethylamido tantalum) exhibit excellent thermal stability with underlying ultra thin SiO₂ up to 1000°C and extremely thermally stable work function, suggesting that CVD TaN can be used as gate electrode on ultra thin gate oxide in a self-aligned gate-first CMOS processing [7].

In this paper, we have demonstrated and characterized self-aligned, gate-first CVD TaN gate CMOS transistors with ultra thin (EOT=11~12Å) CVD HfO₂ gate dielectrics for the first time. These transistors show no sign of gate deletion and excellent thermal stability after 1000°C, 30s N₂ anneal. Compared with PVD TaN devices, the CVD TaN/HfO₂ devices exhibit lower leakage current and CV hysteresis, superior interface properties, higher transconductance, and superior effective mobility.

Experiment

Both n-MOS and p-MOS were fabricated using standard self-aligned gate-first CMOS process. After LOCOS formation and standard pre-gate cleaning, NH₃ interface treatment was performed by RTP at 700°C, 10sec. This interface layer was required to achieve good EOT and leakage of high-K gate stack [8]. 40Å of CVD HfO₂ was deposited in a hot-wall MOCVD system using C₁₆H₃₆O₄Hf (t-buto Hf) and O₂ at 300°C, followed by a post-deposition N₂ annealing at 700°C, 30sec. CVD TaN layer (~200nm) was then deposited using TBTDET TaN precursor at 600°C [7]. For comparison, same thickness (~200nm) of PVD TaN was deposited on the CVD HfO₂ using reactive sputtering in nitrogen ambient. After gate lithography, both TaN gates were RIE etched using CF₄-based chemistry. Conventional self-aligned source/drain formation process was used to fabricate MOSFETs with S/D activation annealing at 950°C, 30sec.

Results and Discussion

HRXTEM and EDS were used to monitor the metal penetration of as-deposited PVD and CVD TaN on ultra thin CVD HfO₂ (physical thickness 40Å). Fig. 1 shows clearly the penetration of Ta through the HfO₂ during PVD process while no Ta was detected underneath the CVD TaN gate electrode. The presence of Ta in HfO₂ and the HfO₂/Si interface as a result of physical sputtering process would have detrimental effects on dielectric reliability as well as channel carrier mobility.

Comparison of high-frequency CV and simulated low-frequency CV between PVD TaN and CVD TaN devices for both n- and p-MOS is shown in Fig. 2. All devices received 950°C, N₂ + 400°C F/G anneal. As can be seen, PVD TaN devices show CV humps near the flat-band voltage while CVD TaN show excellent fit, indicating superior interface properties of CVD TaN devices. The D_{it} (interface states density) calculated using Terman method was 7E10 for CVD TaN and 1E11 for PVD TaN gate. The larger D_{it} in PVD TaN devices is caused by Ta penetration into the HfO₂/Si interface and plasma damage during the PVD TaN deposition. The sputtering induced damage is not completely cured even after high temperature (950°C) and forming gas annealing. EOT of 12.0~12.3Å for CVD TaN gate and 11.1~11.3Å for PVD TaN gate devices were extracted from a C-V simulation program taking quantum effects into account. Sputtering-induced oxide thinning may be responsible for thinner EOT observed for PVD TaN devices.

Fig. 3 and Fig. 4 show the C-V and J-V characteristics of n- and p-MOSFETs (W/L=100/100um) respectively. The measured CV data are in good agreement with a CV simulation taking quantum effects into account. Both PVD and CVD TaN devices show symmetric CV characteristics with respect to accumulation and inversion and C_{inv}/C_{max} = 1, indicating no sign of gate depletion. Leakage current of CVD TaN electrode was found to be 1 to 1.5 orders of magnitude lower than that of PVD TaN electrode, particularly at low V_g. This could be due to Ta penetration and PVD damage during sputtering process.

Negligible hysteresis ($\Delta V_{FB} < 30\text{mV}$) of HFCV was observed on CVD TaN gate stack with voltage sweeping from -2V to +2V for even as-deposited device, while PVD TaN gate stack shows large hysteresis ~150mV [Fig. 5]. In addition, CVD TaN devices show much smaller temperature dependence of J_g [Fig. 6]. These results suggest smaller density of traps in CVD TaN devices.

Figs. 7-8 show well behaved Id-V_g and G_m-V_g curves for n- and p-MOSFETs respectively with good subthreshold swings of 70 mV/decade for both n-MOS and p-MOS. However, G_m of CVD TaN gate stack are significantly larger than that of PVD TaN gate stacks. The Id-V_d characteristics of n- and p-MOSFETs are plotted in Fig. 9, with CVD TaN devices showing significantly higher drive current for the same V_d and V_g-V_t. Fig. 10 examines the electron and hole mobilities. The effective electron mobility of CVD TaN and PVD TaN gate device are 170cm²/V·S and 80cm²/V·S and hole mobilities are 60cm²/V·S and 48cm²/V·S, respectively. The lower carrier mobilities of PVD TaN devices are attributed to poor interface quality due to the combined effects of Ta penetration into the HfO₂/Si interface and sputtering induced damage [9].

Conclusion

We have demonstrated and characterized self-aligned, gate-first CVD TaN gate n- and p-MOS transistors with ultra thin (EOT=11~12Å) CVD HfO₂ gate dielectrics for the first time. Compared with PVD TaN devices, the CVD TaN/HfO₂ devices exhibit lower leakage current and CV hysteresis, superior interface properties, higher transconductance, and superior effective electron and hole mobility.

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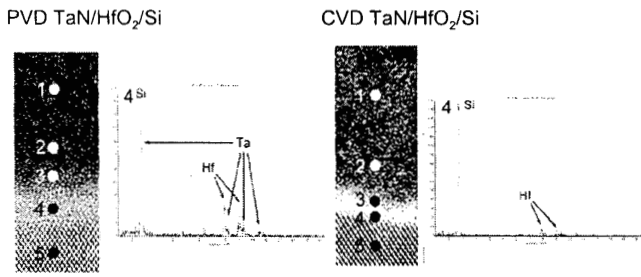


Fig. 1 HRXTEM and EDS of PVD TaN/HfO₂/Si and CVD TaN/HfO₂/Si gate stack. PVD TaN shows Ta penetration.

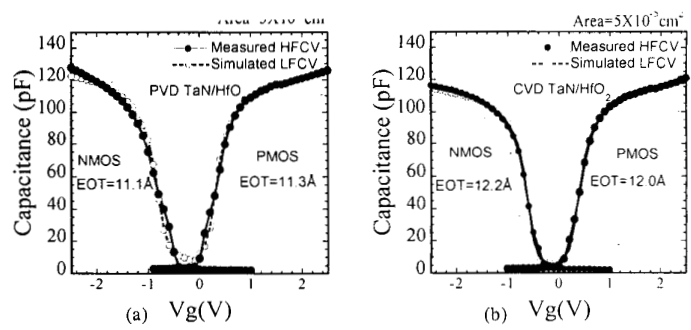


Fig. 2 HFCV and simulated LFCV of n- and p-MOS (after 950°C N2 and 400°C F/G anneal) for (a) PVD TaN/HfO₂ (b) CVD TaN/HfO₂. CVD TaN/HfO₂ shows excellent fit with simulated LFCV while PVD TaN/HfO₂ shows CV hump near the flat band voltage.

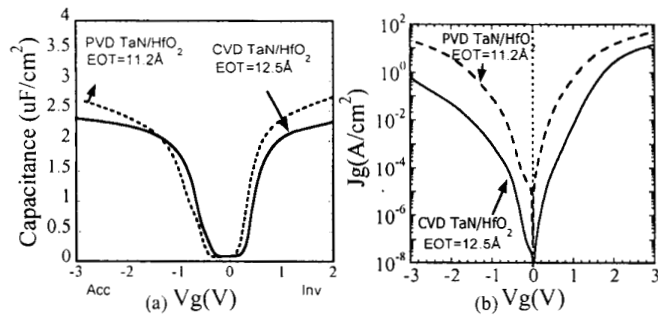


Fig. 3 n-MOS transistor CV (a) and IV (b) (with S/D grounded) of CVD HfO₂ with PVD TaN, CVD TaN gate electrode.

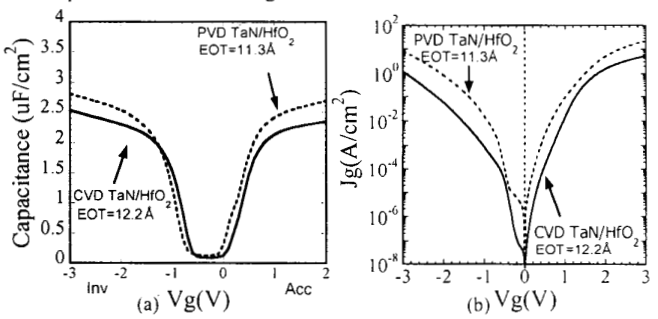


Fig. 4 p-MOS transistor CV (a) and IV (b) (with S/D grounded) of CVD HfO₂ with PVD TaN, CVD TaN gate electrode.

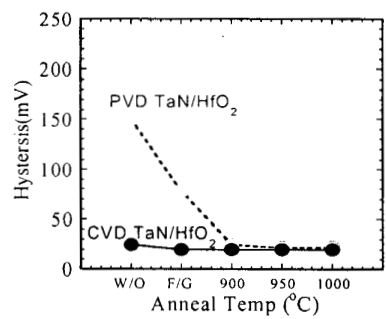


Fig. 5 CV hysteresis characteristics for CVD and PVD TaN gate HfO₂ capacitors with +2V~-2V sweep.

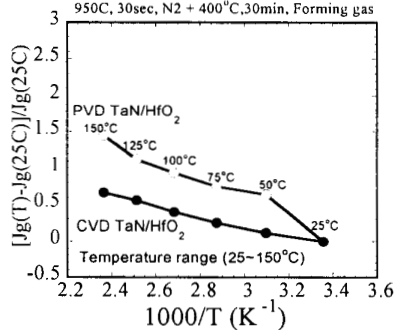


Fig. 6 Temperature dependence of Jg.

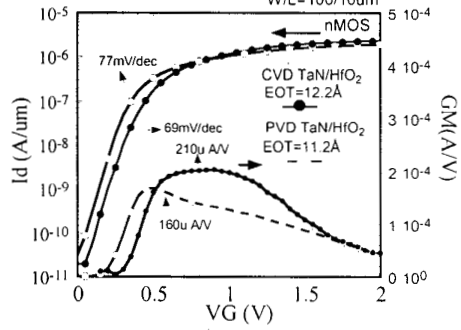


Fig. 7 n-MOSFET Id-Vg characteristics for both CVD TaN and PVD TaN gate electrode.

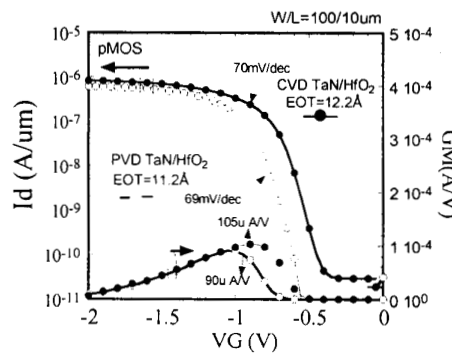


Fig. 8 p-MOSFET Id-Vg characteristics for both CVD TaN and PVD TaN gate with HfO₂.

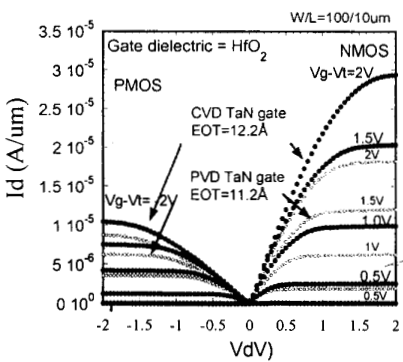


Fig. 9 n- and p-MOSFETs Id-Vd characteristics for both CVD TaN and PVD TaN gate HfO₂ devices.

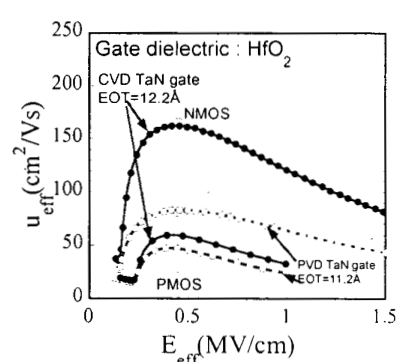


Fig. 10 Effective electron and hole mobility comparison between CVD TaN and PVD TaN HfO₂ devices.