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Date: June 6, 2025

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNITED MICROELECTRONICS CORPORATION,
AND
UMC GROUP (USA),
Petitioners,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,
Patent Owner.

Case No. IPR2025-01093
Patent No. 8,587,076

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,587,076 UNDER 35 U.S.C. §§ 311, 312 AND 37 C.F.R. § 42.104

TABLE OF CONTENTS

Page

TABLE OF CONTENTS ii
TABLE OF EXHIBITS vii
I. Introduction 1
II. Certification of Grounds for Standing 1
III. Identification of Challenge and Requested Relief 2
A. Prior Art 2
B. Grounds for Challenge 3
IV. THE ’076 PATENT 4
A. Applicant Admitted Prior Art 4
B. Technical Background 6
1. MISFET/MOSFET 6
2. Gate Insulating Film 7
3. Sidewall Structures 11
4. Etching Properties 12
C. ’076 Patent Overview 14
D. Prosecution History 16
1. ’076 Patent 16
2. ’180 Patent 17
3. JP Application 17
E. Claim Construction 19
F. Level of Ordinary Skill in the Art 19

V. Ground I: Kamata Renders Claims 1-3, 5-6, 13, 14, 16-19, and 21-22 Obvious 20

A. Overview 20

B. Independent Claim 1 21

1. Preamble 21

2. Limitation 1[a] 21

3. Limitation 1[b] 25

4. Limitation 1[c] 26

5. Limitation 1[d] 28

6. Limitation 1[e] 30

C. Claim 2 33

D. Claim 3 34

E. Claim 7 34

F. Claim 8 36

G. Claims 10 and 13 37

H. Claims 11-12 38

VI. Ground II: Kamata-Sim Combination Renders Claim 6 Obvious 39

VII. Ground III: Guha Renders Claims 1-3, 7-8, 10-13 Obvious 41

A. Overview 41

B. Independent Claim 1 41

1. Preamble 41

2. Limitation 1[a] 42

3. Limitation 1[b] 44

4. Limitation 1[c] 46
5. Limitation 1[d] 48
6. Limitation 1[e] 51

C. Claim 2 54

D. Claim 3 55

E. Claim 7 55

F. Claim 8 56

G. Claims 10 and 13 57

H. Claims 11-12 59

VIII. Ground IV: Guha-Sim Combination Renders Claim 6 Obvious 60

IX. Ground V: Matsumoto-Yu Combination Renders Claims 1-3, 7-8, 10, & 13 Obvious 61

A. Overview 61

B. Motivation to Combine 63

1. First Combination 64
2. Second Combination 64

C. Independent Claim 1 66

1. Preamble 66
2. Limitation 1[a] 66
3. Limitation 1[b] 68
4. Limitation 1[c] 69
5. Limitation 1[d] 71
6. Limitation 1[e] 73

D. Claim 2 74

E. Claim 3 75

F. Claim 7 75

G. Claim 8 76

H. Claims 10 and 13 77

X. Ground VI: Matsumoto-Yu-Sim Combination Renders Claim 6 Obvious 78

XI. Ground VII: Matsumoto-Koyama Combination Renders Claim 1 Obvious 80

A. Motivation to Combine 80

B. Independent Claim 1 81

XII. Ground VIII: Matsumoto-Ono Combination Renders Claims 1 and 11-12 Obvious 82

A. Overview 82

B. Motivation to Combine 85

C. Independent Claim 1 87

D. Claims 11-12 88

XIII. MANDATORY NOTICES 89

A. Real Party-in-Interest (37 C.F.R. §42.8(b)(1)) 89

B. Related Matters (37 C.F.R. §42.8(b)(2)) 89

C. Lead and Back-up Counsel (37 C.F.R. §42.8(b)(3)) 90

D. Service Information (37 C.F.R. §42.8(b)(4)) 90

E. Payment of Fees (37 C.F.R. §42.103) 90

XIV. CONCLUSION 91

CERTIFICATE OF COMPLIANCE WITH WORD COUNT 92

CERTIFICATE OF SERVICE 93

Appendix: Challenged Claims Listing.. 94

TABLE OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 8,587,076 to Hirase et al. (the "'076 patent")
1002	Prosecution History of the '076 patent ("the Prosecution History")
1003-1008	RESERVED
1009	U.S. Patent Application Publication No. 2003/0025135 to Matsumoto, et al. ("Matsumoto")
1010-1012	RESERVED
1013	U.S. Publication 2005/0051856 to Ono, et al. ("Ono")
1014-1017	RESERVED
1018	Wilk, G. D., et al., "High-k gate dielectrics: Current status and materials properties considerations," Journal of Applied Physics, Vol. 89, No. 10, pp. 5243-5275, May 15, 2001 ("Wilk")
1019-1023	RESERVED
1024	Sim, J. H., et al., "Effects of ALD HfO_2 thickness on charge trapping and mobility," Microelectronic Engineering, Vol. 80, pp. 218-221, June 17, 2005 ("Sim")
1025-1026	RESERVED
1027	U.S. Patent Application Publication No. 2002/0063299 to Kamata, et al. ("Kamata")
1028	U.S. Patent Application Publication No. 2006/0091432 to Guha, et al. ("Guha")
1029	Koyama, M., et al., "Effects of Nitrogen in HfSiON Gate Dielectric on the Electrical and Thermal Characteristics," Digest of International Electron Devices Meeting, pp. 849-852, Dec. 8-11, 2002 ("Koyama")

Exhibit No.	Description
1030-1047	RESERVED
1048	U.S. Patent 6,504,214 to Yu, et al. ("Yu")
1049-1100	RESERVED
1101	Declaration of Sanjay Banerjee, PhD
1102	Curriculum Vitae of Sanjay Banerjee, PhD
1103	"Stress Memorization Technique (SMT) by Selectively Strained-Nitride Capping for Sub-65nm High-Performance Strained-Si Device Application," Chen et al., 2004 Symposium on VLSl Technology Digest of Technical Papers (2004) ("Chen-2004")
1104	"35% Drive Current Improvement from Recessed-SiGe Drain Extensions on 37 nm Gate Length PMOS," Chidambaram et al., 2004 Symposium on VLSl Technology Digest of Technical Papers (2004) ("Chidambaram-2004")
1105	"Self-Aligned Ultra Thin HfO_2 CMOS Transistors with High Quality CVD TaN Gate Electrode," Lee et al., 2002 Symposium On VLSl Technology Digest of Technical Papers (2002) ("Lee-2002")
1106	"Delaying Forever: Uniaxial Strained Silicon Transistors in a 90nm CMOS Technology," Mistry et al., 2004 Symposium on VLSl Technology Digest of Technical Papers (2004) ("Mistry-2004")
1107	"Effects of High-Temperature Forming Gas Anneal on HfO_2 MOSFET Performance," Onishi et al., 2002 Symposium On VLSl Technology Digest of Technical Papers (2002) ("Onishi-2002")

Exhibit No.	Description
1108	"Low Standby Power CMOS with HfO_2 Gate Oxide for 100-nm Generation," 2002 Symposium On VLSl Technology Digest of Technical Papers (2002) ("Pidin-2002")
1109	"Mobility Enhancement in Strained Si NMOSFETs with HfO_2 Gate Dielectrics," Rim et. al., 2002 Symposium On VLSl Technology Digest of Technical Papers (2002) ("Rim-2002")
1110	"Metal Gate MOSFETs with HfO_2 Gate Dielectric," Samavedam et al., 2002 Symposium On VLSl Technology Digest of Technical Papers (2002) ("Samavedam-2002")
1111	"55nm high mobility SiGe(:C) pMOSFETs with HfO_2 gate dielectric and TiN metal gate for advanced CMOS," Weber et al., 2004 Symposium on VLSl Technology Digest of Technical Papers (2004) ("Weber-2004")
1112	Japanese Patent Publication JP2005-064190 to Ono (with English Abstract and Japanese Publication) ("JP-Ono Abstract")
1113-1210	RESERVED
1211	Van Zant, "Microchip Fabrication" (Fifth Ed. 2004) ("Van Zant")
1212	Weste, "CMOS VLSI Design: A Circuits and Systems Perspective" (Third Edition, 2005) ("Weste")
1213	Houssa, M., "High-k Dielectrics" to Houssa (IOP Publishing Ltd. 2004) ("Houssa")
1214	Wolf, S., "Silicon Processing for the VLSI Era, Volume 4 – Deep-Submicron Process Technology" ("Wolf-4")

Exhibit No.	Description
1215	Plummer, J. et al., "Silicon VLSI Technology: Fundamentals, Practice and Modeling" (Prentice Hall 2000) ("Plummer")
1216	"International Technology Roadmap for Semiconductors: Process Integration, Devices, and Structures" (2007 Edition) ("ITRS-PIDS")
1217-1222	RESERVED
1223	"Semiconductor Devices: Physics and Technology" by Sze (Second Edition, 2002) ("Sze-2002")
1224-1225	RESERVED
1226	U.S. Patent No. 7,709,331 to Karve, et al. ("Karve")
1227	U.S. Patent No. 8,017,469 to Luo, et al. ("Luo")
1228	RESERVED
1229	Wolf, "Silicon Processing for the VLSI Era, Volume 3 – The Submicron MOSFET" (1995) ("Wolf-3")
1230-1304	RESERVED
1305	Translated Excerpts from JP File History
1306-1307	RESERVED
1308	File History of U.S. Patent 8,253,180 ("'180 File History")
1309-1322	RESERVED
1323	U.S. Patent No. 6,306,712 to Rodder, et al. ("Rodder")
1324-1325	RESERVED
1326	Declaration of June Ann Munford
1327-1336	RESERVED

Exhibit No.	Description
1337	Lee, S. J., et al. "High Quality Ultra Thin CVD HfO_2 Gate Stack with Poly-Si Gate Electrode," Digest of International Electron Devices Meeting, pp. 31-34, Dec. 10-13, 2000 ("Lee-2000")
1338	Campbell, "The Science and Engineering of Microelectronic Fabrication", Second Edition (2001) ("Campbell")
1339	RESERVED
1340	Japanese Patent Publication JP2005-064190 to Ono with certified translation ("JP-Ono")
1341-1348	RESERVED
1349	Lee, B.H., et al., "Ultrathin Hafnium Oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application," Digest of International Electron Devices Meeting, pp. 133-36, Dec. 5-8, 1999 ("Lee-1999")
1350-1405	RESERVED
1406	U.S. Patent Application Publication No. 2007/0249069 A1 to Alvarez et al. ("Alvarez").
1407-1412	RESERVED
1413	S.M. Sze, Physics of Semiconductor Devices (2d ed. 1981) (excerpted). ("Sze-1981")
1414-1418	RESERVED
1419	U.S. Patent Application Publication No. 2006/0286729 A1 to Kavalieros et al. ("Kavalieros729")
1420-1428	RESERVED
1429	U.S. Patent Application Publication 2004/0262784 A1 to Doris et al. ("Doris)

Exhibit No.	Description
1430	U.S. Patent No. 6,797,556 B2 to Murthy et al. (“Murthy556”)
1431	U.S. Patent Application Publication No. 2007/0134870 A1 to Lee et al. (“Lee870”)
1432	U.S. Patent Application Publication No. 2005/0260810 A1 to Cheng et al. (“Cheng810”)
1433	U.S. Patent Application Publication No. 2009/0020820 A1 to Baik et al. (“Baik”)
1434	U.S. Patent Application Publication No. 2008/0293207 A1 to Koutny et al. (“Koutny”)
1435	U.S. Patent Application Publication No. 2010/0075476 A1 to Miyashita. (“Miyashita”)
1436-1505	RESERVED
1506	U.S. Patent Application Publication 2007/0235823 A1 to Hsu et al. (“Hsu823”).
1507-1511	RESERVED
1512	International Technology Roadmap for Semiconductors: Front End Processes (2007 ed.). (“ITRS_FEP”)
1513-1514	RESERVED
1515	U.S. Patent Application Publication No. 2006/0022277 A1 to Kavalieros et al. (“Kavalieros277”)

Exhibit No.	Description
1516	K. Mistry, et al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging," Technical Digest of the of the 2007 IEEE International Electron Devices Meeting (IEDM), pp. 247-50 (Dec. 2007) ("Mistry2007")
1517	K. Mistry, et al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging," presented at 2007 IEEE International Electron Devices Meeting (IEDM), pp. 1-37 (Dec. 2007) ("Mistry_Presentation")
1518	U.S. Patent No. 6,881,631 B2 to Saito et al. ("Saito631")
1519	U.S. Patent No. 7,812,414 B2 to Hou et al. ("Hou")
1520	U.S. Patent Application Publication No. 2005/0258468 A1 to Colombo et al. ("Colombo")
1521	U.S. Patent No. 6,849,511 B2 to Iriyama et al. ("Iriyama")
1522	U.S. Patent Application Publication No. 2002/0037615 A1 to Matsuo. ("Matsuo")
1523	S.E. Thompson et al., "A 90-nm Logic Technology Featuring Strained Silicon," IEEE Transactions on Electron Devices, vol. 51. No. 11, pp. 1790-97 (Nov. 2004). ("Thompson-2004")

Exhibit No.	Description
1524	Y. Sun et al., "Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors," Journal of Applied Physics, vol. 101, Art. No. 104503 (22 pages) (May 2007). ("Sun-2007")
1525	D. James, "2004 – The Year of 90-nm: A Review of 90 nm Devices," 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 72-77 (2005). ("James")
1526	U.S. Patent Application Publication No. 2006/0148151 A1 to Murthy et al. ("Murthy151")
1527	U.S. Patent Application Publication No. 2004/0262683 A1 to Bohr et al. ("Bohr")
1528	P. Morin et al., "Extensive Study of the Correlation between Contact Etch Stop Nitride Material Properties and Negative Bias Temperature Instabilities Measured in pMOSFETS," ECS Transactions, vol. 6, no. 3, pp. 355-69 (2007). ("Morin-2007")
1529	U.S. Patent Application Publication No. 2005/0170104 A1 to Jung et al. ("Jung")
1530	RESERVED
1531	U.S. Patent Application Publication No. 2008/0145984 A1 to Ke et al. ("Ke")
1532	P. Bai et al., "A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm2 SRAM Cell," Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 657-60 (Dec. 2004). ("Bai-2004")

Under 35 U.S.C. §§ 311, 312 and 37 C.F.R. § 42.104, United Microelectronics Corporation and UMC Group (USA) (collectively, "Petitioner") request *inter partes* review ("IPR") of claims 1, 2, 3, 6, 7, 8, 10, 11, 12, and 13 ("Challenged Claims") of U.S. Patent No. 8,587,076 (Ex.1001, "the '076 patent").

I. Introduction

The '076 patent relates "to techniques for improving the driving power and reliability of a MISFET [metal insulator semiconductor field-effect transistor]" by (1) extending a high-k gate insulating film from under the gate electrode to under a sidewall and (2) making the high-k film thicker under the gate electrode than under the sidewall. Ex.1001, 1:17-24, 2:9-19, 2:39-46. These basic concepts were known before the '076 patent, a fact corroborated by the Examiner and acquiesced to by the Applicant during Japanese prosecution. Petitioner, supported by the Declaration of Dr. Sanjay Banerjee (Ex.1101), demonstrates the Challenged Claims are unpatentable.

II. Certification of Grounds for Standing

Petitioner certifies under 37 C.F.R. §42.104(a) that the '076 patent is available for IPR and Petitioner is not barred or estopped from requesting IPR of the Challenged Claims on the Grounds identified in this Petition.

III. Identification of Challenge and Requested Relief

A. Prior Art

The ’076 patent was filed on July 12, 2012 and claims priority to Japan Patent Application No. JP2005- 227457 (“JP application”), filed August 5, 2005. Petitioner does not acquiesce the ’076 patent is entitled to priority of the JP application. Regardless, each applied reference identified below was filed or published before August 5, 2005 and is prior art to the ’076 patent.

1. U.S. Patent Application Publication No. 2002/0063299 to Kamata, et al. (“Kamata”; Ex.1027), published May 20, 2002, is prior art under 35 U.S.C. §102(b).[1]

2. “Effects of ALD HfO_2 thickness on charge trapping and mobility” to Sim, et al. (“Sim”; Ex.1024), published June 17, 2005, is prior art under 35 U.S.C. §102(b). Ex.1326, ¶¶14-17.

3. U.S. Patent Application Publication No. 2006/0091432 to Guha, et al. (“Guha”; Ex.1028), filed November 2, 2004, is prior art under 35 U.S.C. §102(e).

4. U.S. Patent Application Publication No. 2003/0025135 A1 to Matsumoto, et al. (“Matsumoto”; Ex.1009), published February 6, 2003, is prior art under 35 U.S.C. §102(b).

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[1] Pre-AIA 35 U.S.C. §102 applies.

5. U.S. Patent 6,504,214 to Yu, et al. ("Yu"; Ex.1048), issued January 7, 2003, is prior art under 35 U.S.C. §102(b).

6. "Effects of Nitrogen in HfSiON Gate Dielectric on the Electrical and Thermal Characteristics" to Koyama, et al. ("Koyama"; Ex.1029), published in 2002, is prior art under 35 U.S.C. §102(b). Ex.1326, ¶¶18-21.

7. U.S. Patent Application Publication No. 2005/0051856 A1 to Ono, et al. ("Ono"; Ex.1013), published March 10, 2005, is prior art under 35 U.S.C. §102(b).

B. Grounds for Challenge

The specific Grounds of the challenge are set forth below and are supported by the Declaration of Sanjay Banerjee, Ph.D. (Ex.1101).

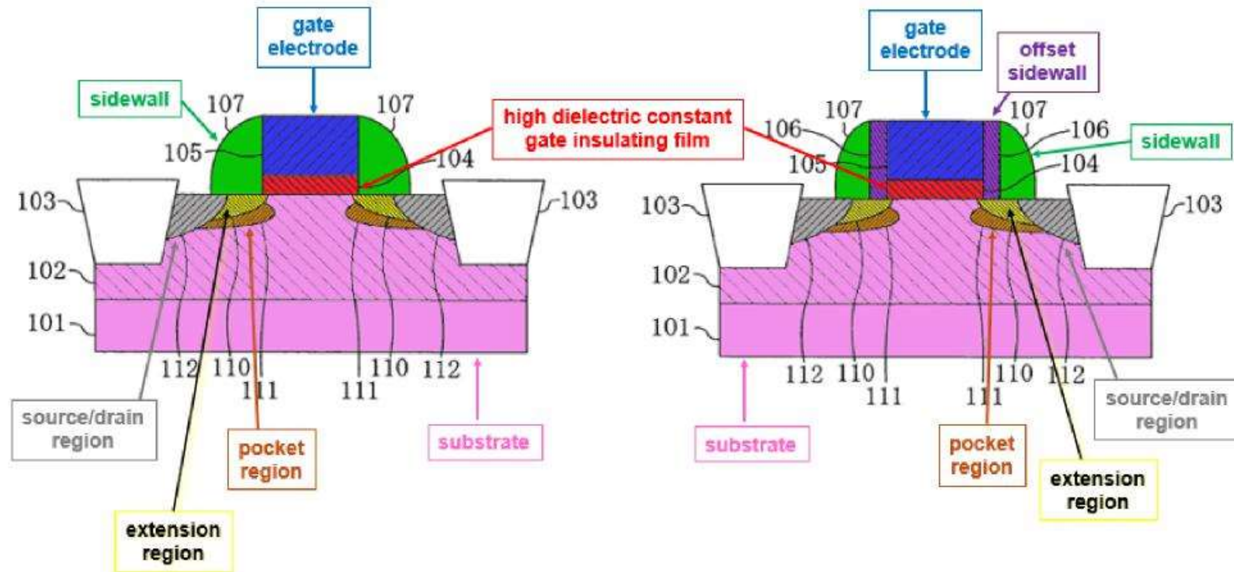
Ground	Basis	Challenged Claims	Prior Art Reference(s)
I	§103	1-3, 7-8, 10-13	Kamata (Ex.1027)
II	§103	6	Kamata (Ex.1027)-Sim (Ex.1024)
III	§103	1-3, 7-8, 10-13	Guha (Ex.1028)
IV	§103	6	Guha (Ex.1028)-Sim (Ex.1024)
V	§103	1-3, 7-8, 10, 13	Matsumoto (Ex.1009)-Yu (Ex. 1048)
VI	§103	6	Matsumoto (Ex.1009)-Yu (Ex.1048)-Sim (Ex.1024)
VII	§103	1	Matsumoto (Ex.1009)-Koyama (Ex.1029)
VIII	§103	1, 11, 12	Matsumoto (Ex.1009)-Ono (Ex.1013)

IV. THE ’076 PATENT

A. Applicant Admitted Prior Art

The ’076 patent recognized that, prior to August 2005, semiconductor devices had used “a high dielectric constant film formed of a Hf based oxide, Al based oxide or the like” as a gate insulating film. (Ex.1001, 1:26-34.) It describes two prior art metal insulator semiconductor field-effect transistors (MISFETs), depicted in Figures 16A-16B, each including a high dielectric constant gate insulating film[2] 104 (shaded red) interposed between gate electrode 105 (shaded blue) and the substrate. In the Figure 16A device, sidewall 107 (shaded green) is formed on each side of gate electrode 105. (Ex.1001, 1:46-47.) In the Figure 16B device, an additional offset sidewall 106 (shaded purple) is interposed between sidewall 107 and gate electrode 105. (Ex.1001, 1:55-58.)

[2] The terms “gate dielectric” and “gate insulating film” are used interchangeably. The term “high dielectric constant” is also referred to as “high-k” in this Petition and the prior art documents.



’076 Patent, Figure 16A[3] **’076 Patent, Figure 16B**

In these prior art devices, the “side end portions” of the high-k gate insulating film “are in direct contact with sidewalls.” (Ex.1001, 1:66-69.) The ’076 patent purports to address issues with this arrangement by extending the high-k film under the “sidewalls to prevent end portions of the [high-k] film from being in contact with the sidewalls.” (Ex.1001, 2:13-22.)

The basic concept of extending a high-k gate insulating film from under the gate electrode to beneath sidewalls was well-known. (*E.g.*, §§IV.B.2.b, IV.D.2, V, VII, IX.)

[3] All shading and annotations in figures added, unless otherwise noted.

B. Technical Background

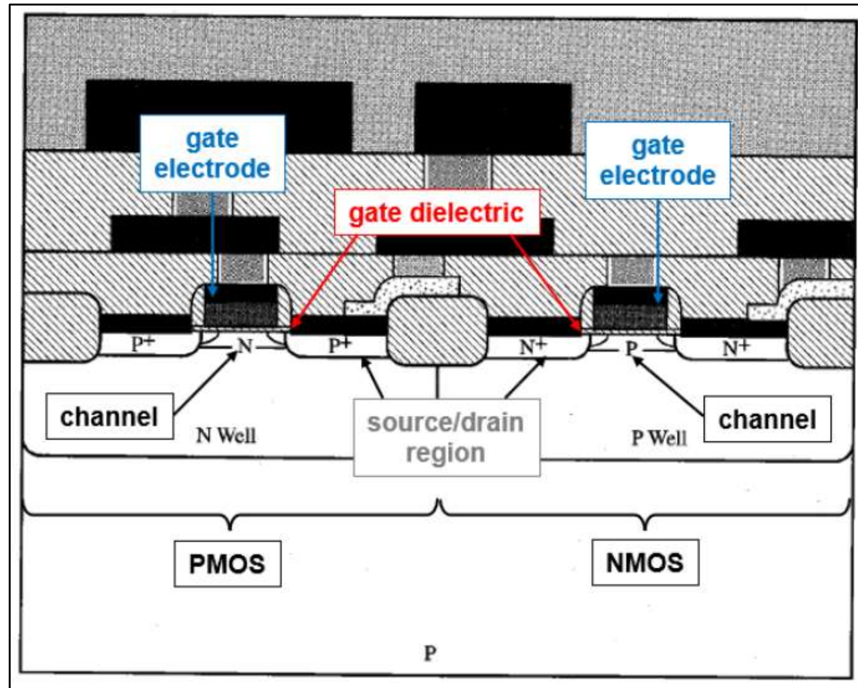
A semiconductor device, at its most basic, exploits the properties of semiconductor materials such as silicon or geranium. Ex.1101, ¶39. Many types of semiconductor devices exist including, *e.g.*, diodes and metal oxide semiconductor (MOS) transistors (*e.g.*, field effect transistors (FETs)). *See e.g.*, *id.*; Plummer, Ex.1215, 33-41. For ease of discussion, Petitioner describes FET devices in further detail below. A POSITA would understand the basic concepts in §IV.B also apply to other types of semiconductor devices.

1. MISFET/MOSFET

MISFETs[4] have a **source/drain** for current input/output. Ex.1101, ¶40; Plummer, Ex.1215, 76-82. MISFETs like the ones at issue here also have a **gate** above a **channel** region between the source and drain. Ex.1101, ¶40; Plummer, Ex.1215, 71-76. The **gate** includes a **gate electrode** and **gate dielectric** (also referred to as a gate insulating film) separating the gate electrode from the channel region. *Id.* Applying voltage to the gate electrode controls the channel region to connect (ON state) or disconnect (OFF state) the source and drain. Ex.1101, ¶40; Ex.1341, 8-9. Generally, source/drain regions are **doped** with either a **p-type** or **n-**

[4] The terms "MISFET" and "MOSFET" ("Metal-***Oxide***-Semiconductor Field-Effect Transistor") are interchangeable. Ex.1101, ¶40)

type impurity. Ex.1101, ¶44; Plummer, Ex.1215, 76-82. MISFETs with n-type source/drain regions are called **NMOS**, and MISFETs with p-type source/drain regions are called **PMOS**, as illustrated below. Ex.1101, ¶44; Plummer, Ex.1215, 13, Fig. 1-11 (below).



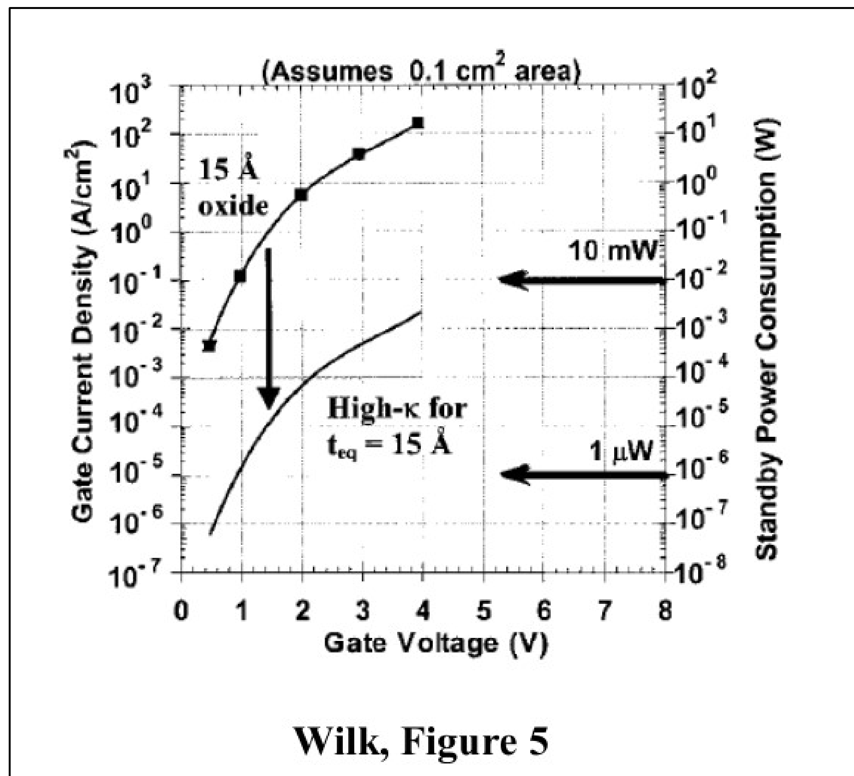
2. Gate Insulating Film

a. Materials

A common feature of a FET is the gate dielectric. Plummer, Ex.1215, 288. For decades prior to the '076 patent, silicon dioxide (SiO_2) was the primary material used for gate dielectrics in MOSFETs. Ex.1101, ¶52; Plummer, Ex.1215, 53 ("SiO_2 is essentially a perfect insulator and provides the needed [electrical] isolation."); Houssa, Ex.1213, 3-4. As gate dielectric layers continued to shrink in thickness (*e.g.*,

below 1.5 nm), use of SiO_2 became untenable, because the amount of gate-to-channel tunneling leakage-current passing through the gate dielectric prevents the gate electrode from effectively controlling the ON/OFF states of the FET. Ex.1101, ¶¶52-63; Wolf-4, Ex.1214, 4-5.

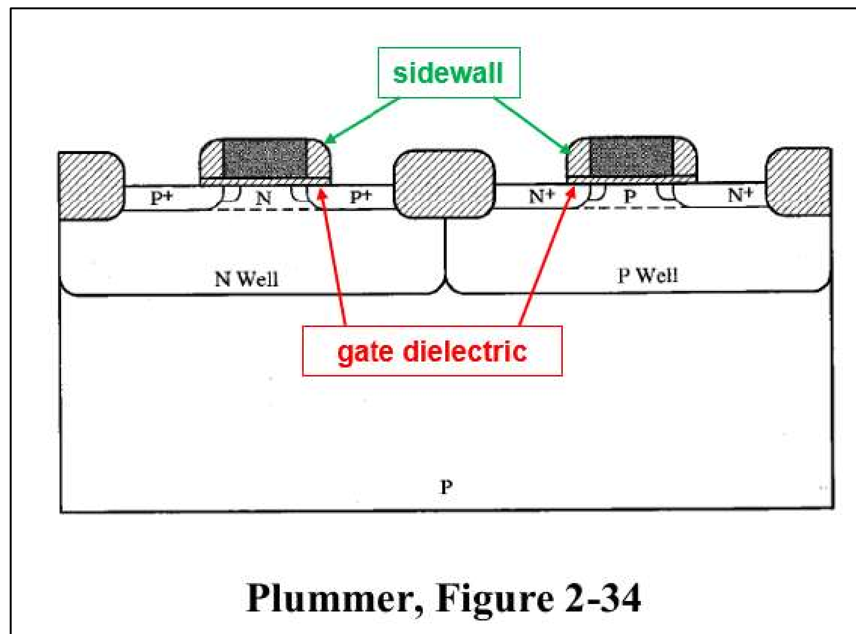
High-k dielectrics, like Hf-based oxides, Ta_2O_5, or ZrO_2, replaced SiO_2 to address these challenges. Ex.1101, ¶¶58-63; Wolf-4, Ex.1214, 146. For example, it was known by 2005 that, as compared to SiO_2, high-k materials significantly reduce the amount of leakage current and, thus, improve energy efficiency. Ex.1101, ¶¶58-63; Wilk, Ex.1018, 5250, Fig. 5 (below); Wolf-4, Ex.1214, 146-47.



Wilk, Figure 5

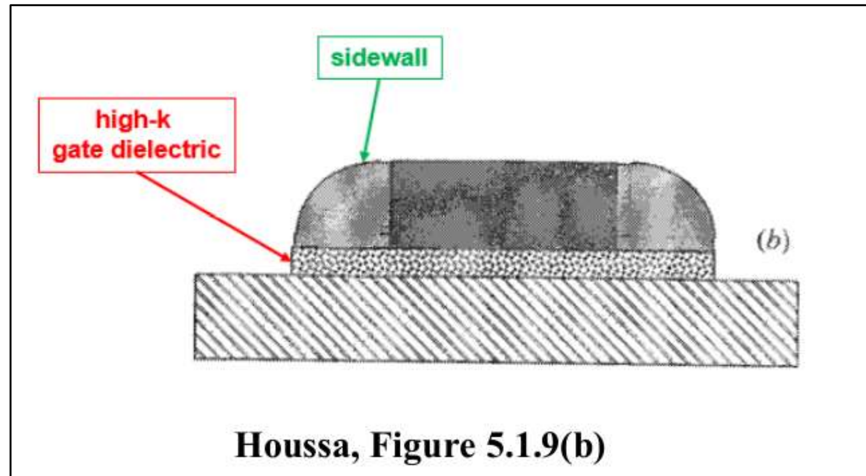
b. Extended Gate Insulating Films

Prior to 2005, it was common practice to extend the gate dielectric from under the gate electrode to under the gate sidewalls. For example, Plummer depicts a CMOS device having an extended gate dielectric in the NMOS and PMOS transistors. Ex.1101, ¶64; Plummer, Ex.1215, Fig. 2-34 (below), 82-83.



Plummer, Figure 2-34

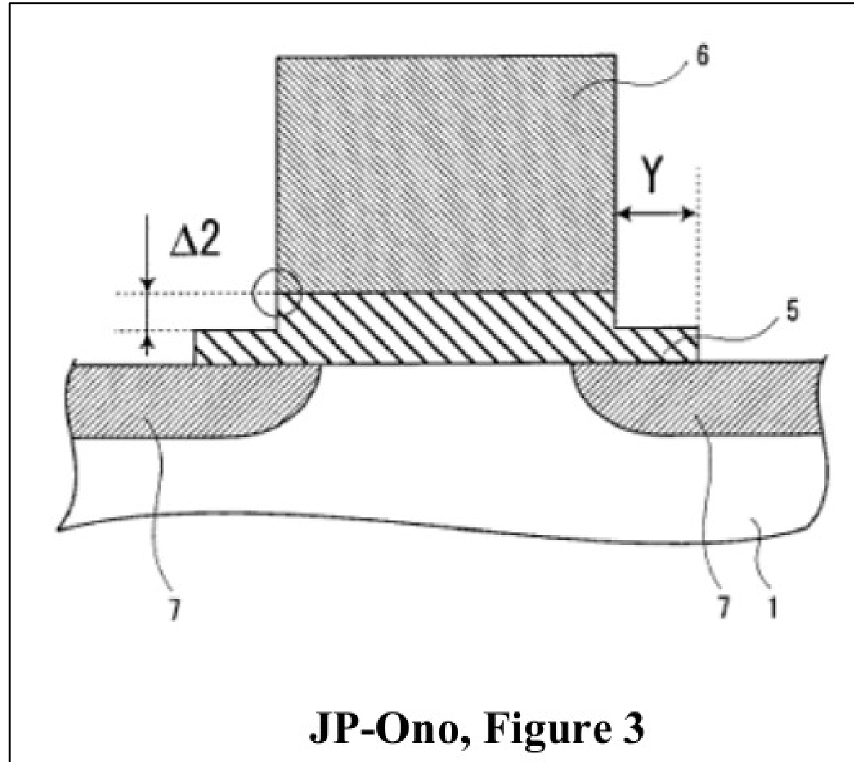
Houssa discloses another example using a high-k material as the gate insulating film that extends from under the gate electrode to under the sidewalls. Ex.1101, ¶65; Houssa, Ex.1213, 510, Fig. 5.1.9(b) (below).



Houssa, Figure 5.1.9(b)

JP Publication No. 2005-064190 ("JP-Ono"[5]; Ex.1340), filed two years before the earliest priority date of the '076 patent, also describes extending the gate dielectric and varying its thickness. Specifically, JP-Ono adjusts both the reduction in thickness of the gate dielectric (Δ2) outside the gate electrode and the length of the gate dielectric from the outer edge of the gate electrode (Y) (*i.e.*, how far the gate dielectric protrudes from under the gate electrode). Ex.1340, ¶35, Fig. 3 (below); Ex.1101, ¶¶66-70.

[5] A certified translation of JP-Ono is included with Ex.1340.

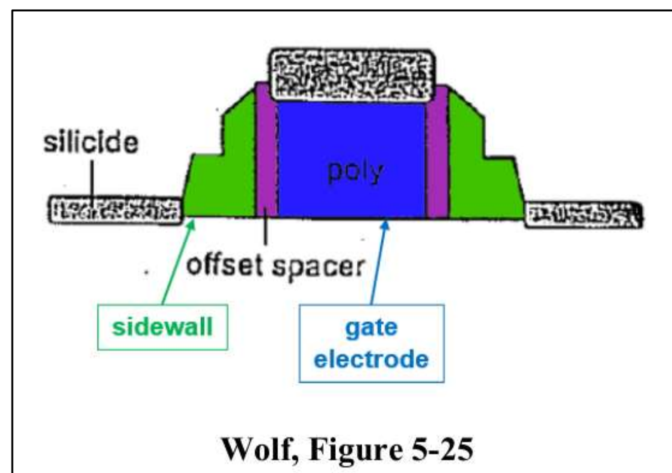


JP-Ono, Figure 3

3. Sidewall Structures

Another common feature of a semiconductor device is sidewalls, vertical insulating structures formed on or proximate to the side surfaces of a gate electrode. Sometimes, the terms "sidewall," "spacer," and "sidewall spacer" are used interchangeably. Ex.1101, ¶71. Sidewalls serve a variety of purposes and functions in a semiconductor device such as defining the source/drain region, providing isolation, protecting the gate during subsequent fabrication, and controlling the width of the gate in the gate length direction. *Id.*

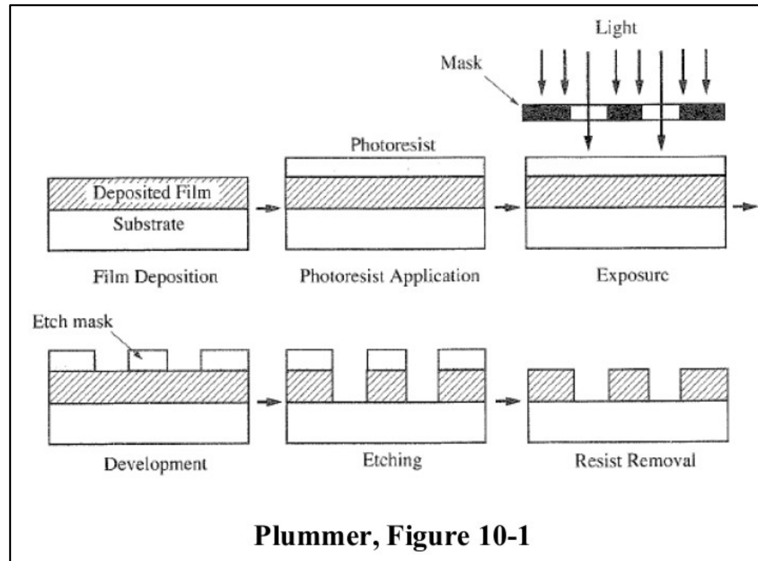
As an example, sidewalls may be used for "[c]ontrolling the position of the edge of the SDE [source/drain extension] region with respect to the gate edge" so as to achieve optimal amount of overlap between the SDE and the gate edge. Wolf-4, Ex.1214, 217. As shown below, "an offset-spacer is fabricated on the side of the gate after the gate-poly is etched (but before the SDE implant step is carried out ...," with offset-spacer width "varied from zero (no-spacer) to some upper-bound (e.g., 50-nm)" to achieve optimum device characteristics. *Id.*, 217, Fig. 5-25 (below); Ex.1101, ¶72.



Wolf, Figure 5-25

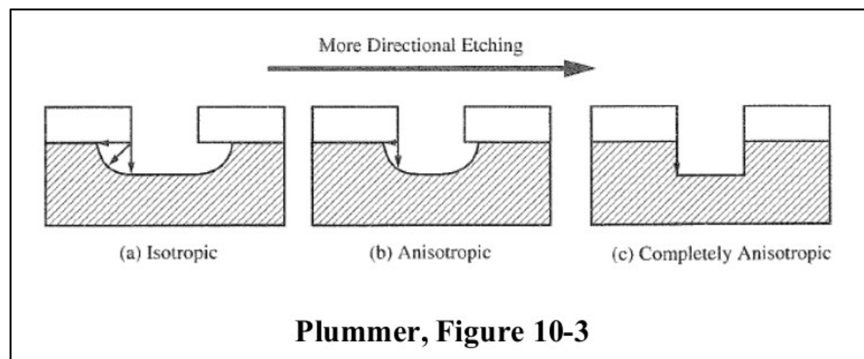
4. Etching Properties

In semiconductor devices, thin films are often first deposited on the wafer surface and then selectively removed by etching to leave the desired pattern of the film. Ex.1101, ¶73; Plummer, Ex.1215, 609-11. The desired pattern is often defined by placing a mask on the surface before etching; the mask is removed after etching. Ex.1101, ¶73; Plummer, Ex.1215, 609-10, Fig. 10-1 (below).



Plummer, Figure 10-1

Etching is performed in a "wet" or "dry" environment. Ex.1101, ¶75; Plummer, Ex.1215, 609, 612-37. Wet etching involves the use of liquid etchants (*e.g.*, hydrofluoric acid), whereas dry etching involves the use of gas-phase etchants in a plasma. Ex.1101, ¶75; Plummer, Ex.1215, 609. Etching processes are also described based on the relative etch rates in different directions. Ex.1101, ¶76; Plummer, Ex.1215, 610-11. Isotropic etching occurs when the etch rate is the same in all directions, resulting in a semicircular etch profile as shown in Figure 10-3(a) below.

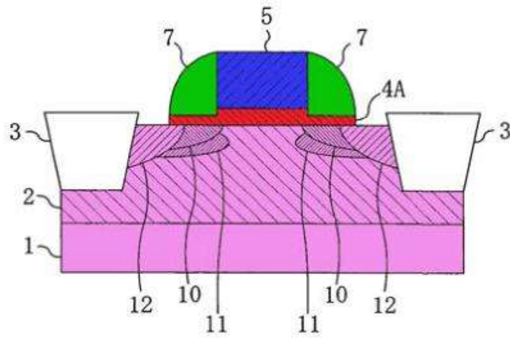


Plummer, Figure 10-3

Plummer, Ex.1215, Fig. 10-3. Most wet chemical etchants etch isotropically. *Id.*, 610-13. Anisotropic etching occurs where there is little or no etching in the lateral direction. *Id.*, 611, Figure 10-3(b), (c) (above). For anisotropic etching, the amount of lateral etching may vary, such that the etched surface may be curved or sloped (*see id.*, Fig. 10-3(b) (above)) to completely vertical (*see id.*, Fig. 10-3(c) (above)). Ex.1101, ¶76.

C. ’076 Patent Overview

The ’076 patent presents four semiconductor device embodiments (first-fourth embodiments) and their associated fabrication methods (fifth-eighth embodiments). In each embodiment, the high-k gate insulating film (shaded red) extends beyond the gate electrode to under the sidewall(s). (Ex.1001, Figures 1-2, 5, 9 (below).) The embodiments differ in the number of sidewalls (one/two) and the presence of a buffer layer under the gate insulating film (fourth embodiment). The embodiments also vary in the relative thickness of the gate insulating film under the gate electrode and sidewalls, though this difference is not relevant to most of ’076 patent claims.



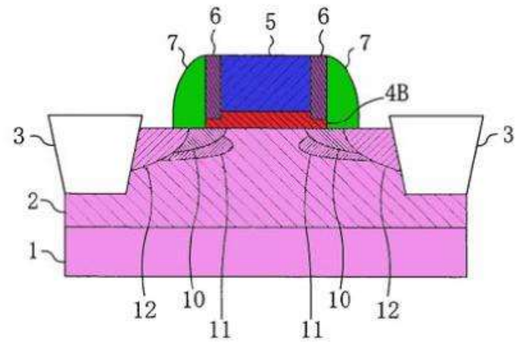
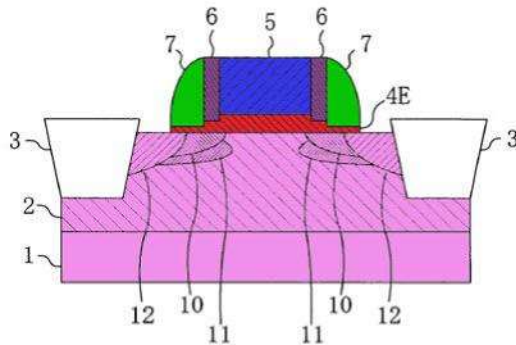


Figure 1—First Embodiment **Figure 2—Second Embodiment**



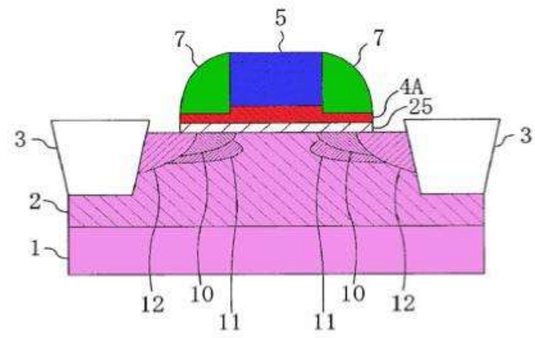
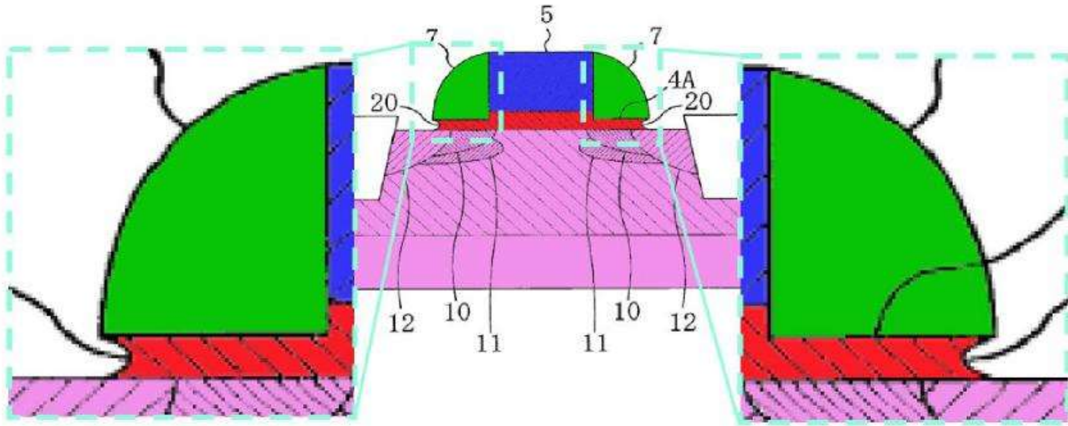


Figure 5—Third Embodiment **Figure 9—Fourth Embodiment**

Each embodiment includes a modification in which "a side portion of the high dielectric constant gate insulating film ... is removed in a notch shape, so that a notch 20 is provided", illustrated in Figure 6 below for the first embodiment modification. (Ex.1001, 7:10-15, 14:49-56, Figure 6, 8:41-46, 16:14-21, Figure 7, 11:53-58, 18:22-28, Figure 8, 13:8-21, Figure 10.)



Annotated Figure 6 with enlargements

The concept of changing the shape and/or location of the end of a dielectric was known, long before the ’076 patent. (*E.g.*, §§IV.D.2, V, VII, IX, XII.)

D. Prosecution History

1. ’076 Patent

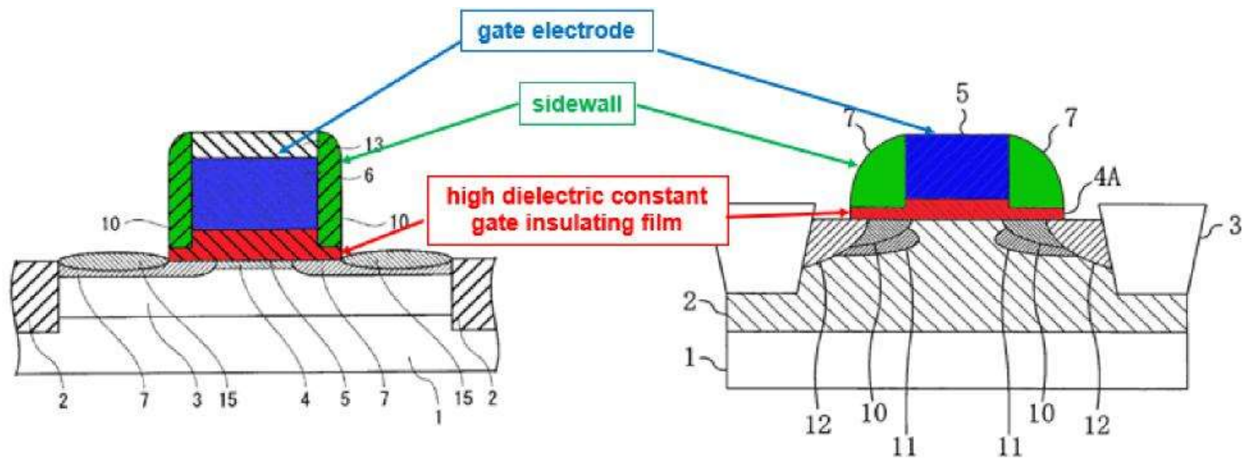
The ’076 patent application was filed with 13 claims including a single independent claim corresponding to issued claim 1. The Examiner rejected the claims based on nonstatutory obviousness-type double patenting over claims 1-22 of the ’180 patent (Ex.1002, 133-34.) The Examiner also rejected the claims as unpatentable over U.S. Patent 6,992,358 to Hieda (“Hieda”). (Ex.1002, 12933.) Applicant submitted a terminal disclaimer and traversed the Hieda rejection. (Ex.1002, 157-159.) The Examiner allowed the claims. (Ex.1002, 173-74.)

2. ’180 Patent

Like in the ’076 prosecution, the filed ’180 patent application claims were rejected as unpatentable over Hieda. (Ex.1308, 123-27.) Applicant traversed, arguing Hieda did not disclose the “predetermined distance” limitation. (Ex.1308, 151-52.) According to Applicant, this limitation was not met because “the high dielectric constant insulating [film] recited by claim 21 [issued claim 1] does not extend so far such that it is disposed beneath the outer end of the insulating sidewall .... It is disposed inwardly of the outer end of the insulating sidewall.” (Ex.1308, 151-52.) The claims were allowed.

3. JP Application

The JP Application was filed with the same device claim originally filed with the U.S. application for the ’076 patent. (Ex.1305, 1.) On September 16, 2011 (before filing of the ’076 patent), the JP-Examiner found this claim scope unpatentable, citing the JP-Ono publication discussed in §IV.B.2 (Figure 23-left) and WO2004/017418 to Sakai, et al. (“Sakai”) which both teach a high-k gate insulating film extending from under the gate electrode to under the sidewalls. (Ex.1305, 4-6.)



JP-Ono, Figure 23 **’076 Patent, Figure 1**

For the claim reciting a “notch” at the end of the high-k gate insulating film, the JP-Examiner determined JP-Ono taught this limitation at ¶84 which states:

> In this embodiment, the side surface of the gate insulating film 5 is aligned with the outer surface of the gate sidewall 10, but this is not essential, and the side surface of the gate insulating film 5 is inside the outer surface of the gate side wall 10. Or even if it exists outside, the effect similar to this Embodiment is acquired.

(Ex.1340, ¶84; Ex.1305, 5.) This disclosure from JP-Ono is also relevant to the ’076 patent because it discloses the end of the extended gate dielectric is retracted from the outer end of the sidewall.

In response, Applicant narrowed the independent claim. (Ex.1305, 8.) The JP-Examiner rejected the amended claim based on both JP2003-258241 to Kajiyama (“Kajiyama”) and JP2004-241755 to Matsumoto (“JP-Matsumoto”) which both have

extended gate insulating films. (Ex.1305, 14-16.) The JP- Examiner maintained the rejection of the notch claim over JP-Ono combined with either Kajiyama or JP-Matsumoto. (Ex.1305, 15.) Applicant further narrowed the claim to obtain allowance. (Ex.1305, 18.)

Despite the materiality of the JP notices of refusal, Applicant did not inform the U.S. Examiner of the rejections by the JP-Examiner during pendency of the ’076 patent.

E. Claim Construction

Claims in an IPR are construed under *Phillips v. AWH Corp*., 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). *See* 37 C.F.R. §42.100(b).

Petitioner does not believe any terms need be construed to resolve the issues presented in this Petition, and Petitioner takes no position regarding claim construction at this time. The Challenged Claims are unpatentable under their plain and ordinary meaning. Ex.1101, ¶¶21-22. Petitioner reserves the right to respond to any purported claim constructions that Patent Owner raises.

F. Level of Ordinary Skill in the Art

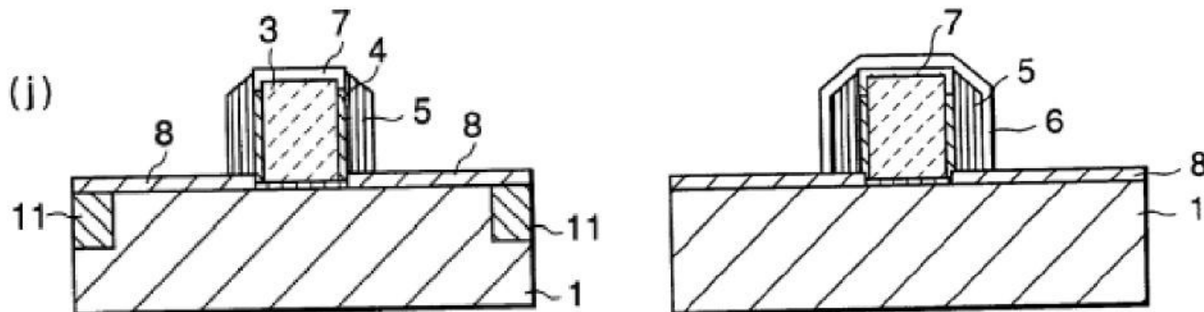
A POSITA would have had at least a Master’s degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. Ex.1101, ¶¶119-22. Additional

graduate education could substitute for work experience, and additional work experience/training could substitute for formal education. *Id.*

V. Ground I: Kamata Renders Claims 1-3, 5-6, 13, 14, 16-19, and 21-22 Obvious[6]

A. Overview

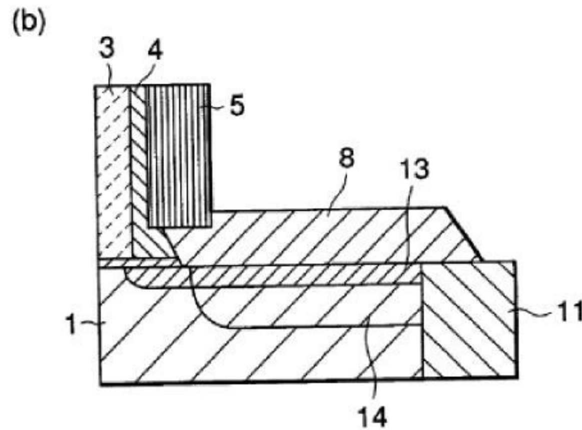
While numerous embodiments are relevant and invalidating, this Petition focuses on Kamata's first (Figure 1B(j)), fourth (Figure 5(c)), and ninth (Figure 10(b)) embodiments. Each embodiment's device includes a gate electrode, a gate insulating film, and a sidewall structure having first sidewall film 4 and second sidewall film 5. (Kamata, Ex.1027, ¶¶50-61 (first embodiment), 68 (fourth embodiment), 93-94 (ninth embodiment).) In each embodiment, the gate insulating film extends from under the gate electrode to under only a portion of the sidewall structure.



Kamata, Figure 1B(j) (First Embodiment)

Kamata, Figure 5(c) (Fourth Embodiment)

[6] Challenged claims listing is provided in the Appendix.



Kamata, Figure 10(b)
(Ninth Embodiment)

B. Independent Claim 1

1. Preamble

Kamata's first, fourth, and ninth embodiments each discloses a "*semiconductor device*"[7]: "invention relates to a **semiconductor device**."[8] (Kamata, Ex.1027, ¶¶3, 8; *see also* Kamata, Ex.1027, ¶¶32, 50 (first embodiment), 36, 68 (fourth embodiment), 93-94 (ninth embodiment).)

2. Limitation 1[a]

Kamata's first, fourth, and ninth embodiment each discloses "*a gate insulating film formed on an active region in a substrate and including Hf*" (Limitation 1[a]). (Ex.1101, ¶149-53.)

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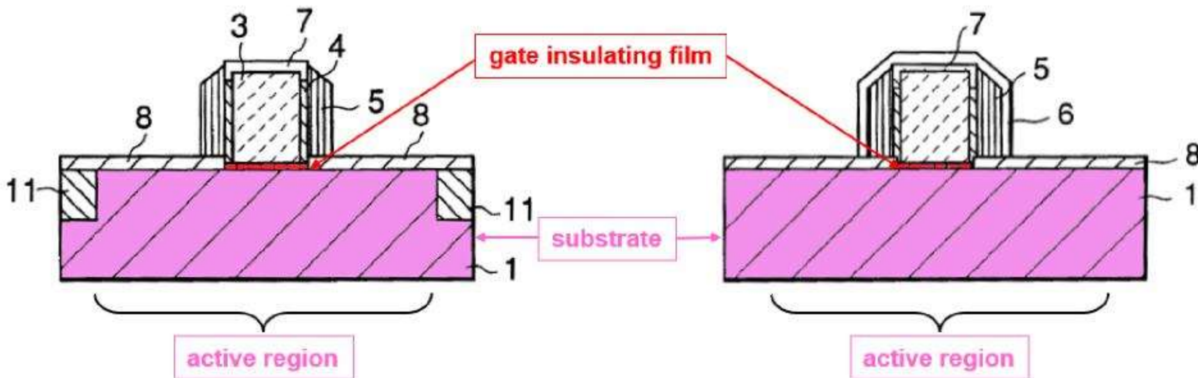
[7] Claim language is indicated by italics throughout.

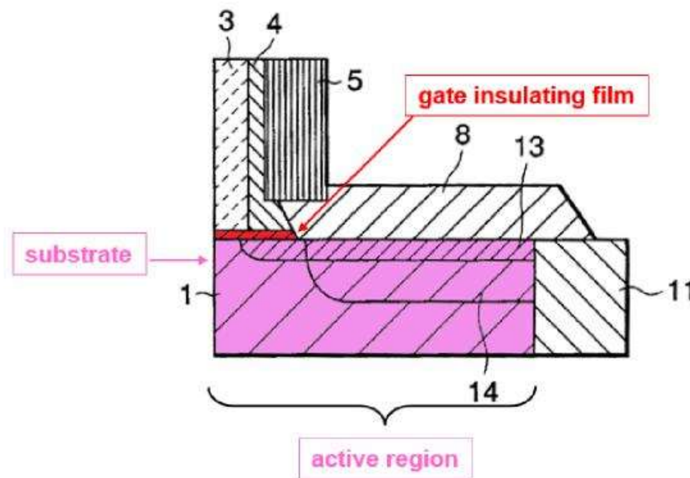
[8] Unless otherwise noted, all emphasis added.

The device of each embodiment has "a semiconductor **substrate** 1 made of silicon" (shaded pink). (Kamata, Ex.1027, ¶¶50, 68 ("parts [of fourth embodiment] that are same as or similar to those of the first embodiment are denoted respectively by the same reference symbols"), 94 ("portions [of ninth embodiment] that are same as or similar to those FIGS. 1A through 2C are denoted respectively by the same reference symbols").) Kamata explains "shallow trench isolation zones (STI) 11" are formed on the substrate "to define an element region 1a" and refers to element 1a as an "active region." (Kamata, Ex.1027, ¶¶50, 68, 94, 99-100 (referring to element 1a of Figure 1A(a) as "active region" and indicating same parts are "denoted ... by the same reference symbols"); *Google LLC v. Jenam Tech, LLC*, IPR2021-00630, 2022 WL 4287797, *9 n.9 (P.T.A.B. Sept. 16, 2022) (applying same disclosures where "figures refer to corresponding features using the same reference numbers"); Ex.1001, 1:42-43 ("region of the well 102 surrounded by the STI serves as an active region of a substrate 101"); Ex.1101, ¶150). A POSITA would have therefore understood element region 1a, identified by STI, is an "active region in a substrate." (Ex.1101, ¶150.)



Kamata, Figures 1B(j)
(First Embodiment)

Kamata, Figure 5(c)
(Fourth Embodiment)



Kamata, Figure 10(b)
(Ninth Embodiment)

The device of each embodiment includes film 2 (shaded red) formed on the active region under the gate electrode extending beneath the sidewall structure. (*E.g.*, Kamata, Ex.1027, ¶¶56, 68, 94; §§V.B.3-5; *Unified Pats., LLC v. Oceana Innovations LLC*, No. IPR2020-01463, 2022 WL 500391, *17 (P.T.A.B. Feb. 14, 2022) ("patent drawing may serve as prior art 'without referring to the surrounding description' if

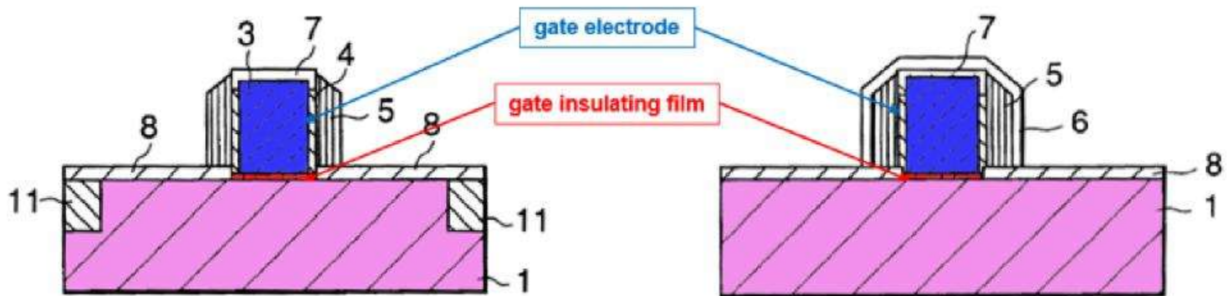
'the prior art features are clearly disclosed by the drawing.'") (citations omitted).) Gate insulating film 2 is disclosed as "**a high dielectric constant film** such as an oxide film with higher dielectric constant than the silicon oxide, containing at least an element selected from a group of Ti, Zr, **<u>Hf</u>**, Ta, La, Al Ba, Sr, Y, Pr and Gd, and a silicate film containing such an element." (Kamata, Ex.1027, ¶52; *see also* Kamata, Ex.1027, ¶53 (listing exemplary high-k films including HfO_2).) By 2005, a POSITA would have been motivated to select HfO_2 given its known benefits, including, for example, "its superior thermal stability with poly-Si and reasonable band alignment." (Lee-2000, Ex.1337, 2.4.1; *see also* Houssa, Ex.1213, 207 (HfO_2 "combines a high k (15–26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ..."); Lee-1999, Ex.1349, 134 ("Excellent dielectric properties ... suggest that HfO_2 is a promising material for the future gate dielectric application."); Ex.1101, ¶¶151-52.) HfO_2 also could be scaled down to a smaller EOT. (Houssa, Ex.1213, 207.)

Kamata therefore discloses "*a gate insulating film* [film 2] *formed on an active region in a substrate and including Hf.*" (E.g., Kamata, Ex.1027, ¶73 (referring to "gate insulating film 2"), ¶¶8-10 ("present invention" device includes "a gate insulating film formed on a surface of the silicon substrate"), claim 1; Ex.1101, ¶153.)

3. Limitation 1[b]

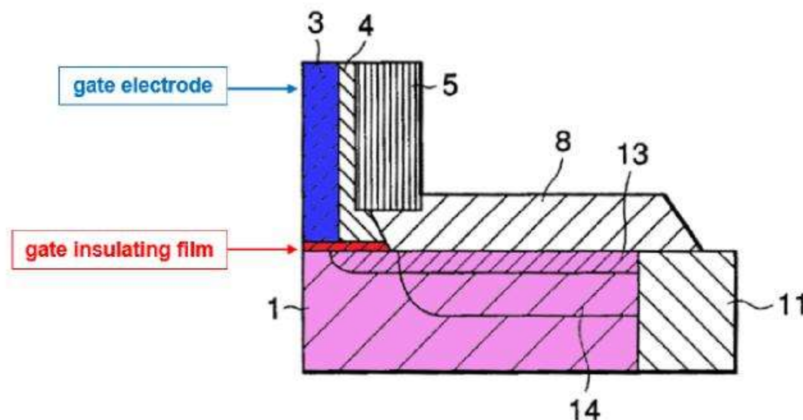
Kamata's first, fourth, and ninth embodiment each discloses "*a gate electrode formed on the gate insulating film*" (Limitation 1[b]). (Ex.1101, ¶¶154-55.)

As shown below, each embodiment's device has a gate electrode (shaded blue) formed on film 2 ("*gate insulating film*"). (Ex.1101, ¶155; Kamata, Ex.1027, ¶50 (explaining gate electrode 3 is "formed by depositing polycrystalline silicon" and performing a subsequent anisotropic etch), ¶¶68, 94, Figures 1A(a)-(c); *see also, e.g.*, Kamata, Ex.1027, claim 1 (reciting device with "gate electrode formed on the gate insulating film").)



Kamata, Figures 1B(j) (First Embodiment)

Kamata, Figure 5(c) (Fourth Embodiment)



Kamata, Figure 10(b)
(Ninth Embodiment)

4. Limitation 1[c]

Kamata's first, fourth, and ninth embodiment each discloses "*a insulating sidewall formed on each side surface of the gate electrode*" (Limitation 1[c]). (Ex.1101, ¶¶156-59.)

As shown in Figures 1B(j) and 5(c) below, the first and fourth embodiment devices each includes sidewall film 4 (shaded purple) and sidewall film 5 (shaded green) formed on the gate electrode's side surfaces (shaded blue). (Kamata, Ex.1027, ¶¶8-16 ("first aspect of the present invention [provides] a semiconductor device comprising ... multilayer type sidewall films [] formed on the respective side surface of the gate electrode"), 57 (referring to film 5 as "sidewall film 5"), 74 (referring to film 4 as "sidewall film 4").) Sidewall film 4 is a silicon oxide film, and sidewall film 5 is a silicon nitride film—both are insulating films. (Kamata, Ex.1027, ¶¶50 (referring to "silicon nitride film (Si3N4) 5"), 58 (referring to "silicon oxide film 4"), 68.) Sidewall 4 and sidewall 5 are collectively an "insulating sidewall," consistent with the '076 patent's disclosure.[9] (Ex.1101, ¶158.)

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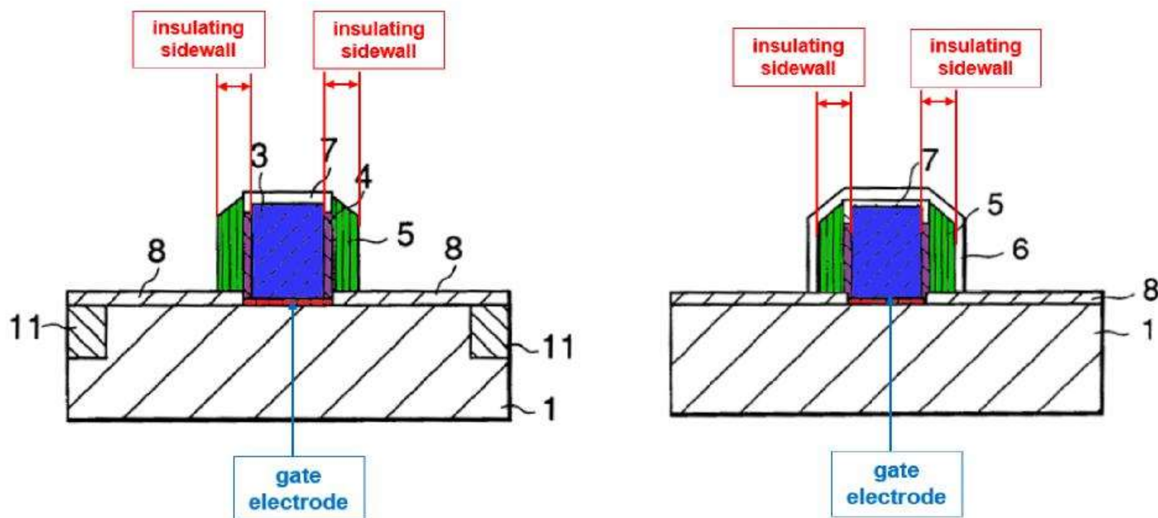
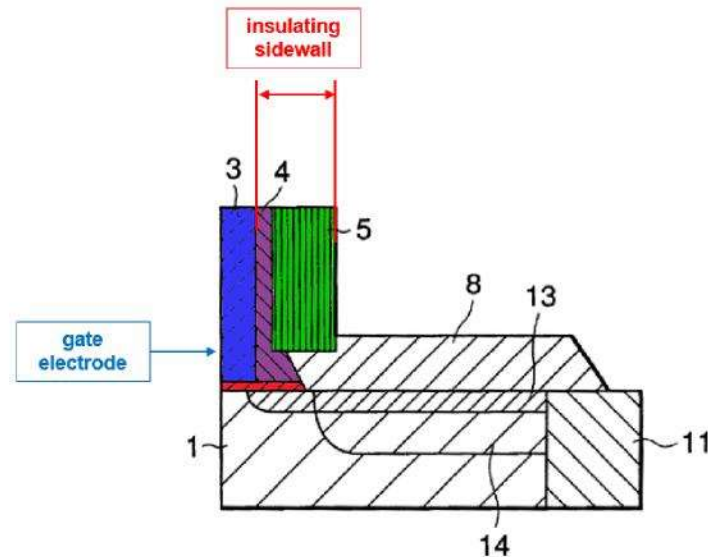
[9] The '076 patent uses the term "insulating sidewall" to refer to a single component (6:9), a collective structure of two components (2:60-65), and as a component having multiple layers (21:6-15)



Kamata, Figures 1B(j) (First Embodiment)

Kamata, Figure 5(c) (Fourth Embodiment)

Figure 10(b) below depicts a portion of the ninth embodiment device. As shown, the device includes sidewall film 4 (shaded purple) and sidewall film 5 (shaded green) formed on the right side surface of the gate electrode. (Kamata, Ex.1027, ¶¶8-16, 57, 74; *see also* Kamata, Ex.1027, ¶¶50, 58, 94.) A POSITA would have understood this device includes corresponding sidewalls on the left side surface of the gate electrode. (Ex.1101, ¶159 n.1.) Like the first/fourth embodiments, sidewall film 4 and sidewall film 5 are collectively an "*insulating sidewall.*" (Ex.1101, ¶158.)



Kamata, Figure 10(b)
(Ninth Embodiment)

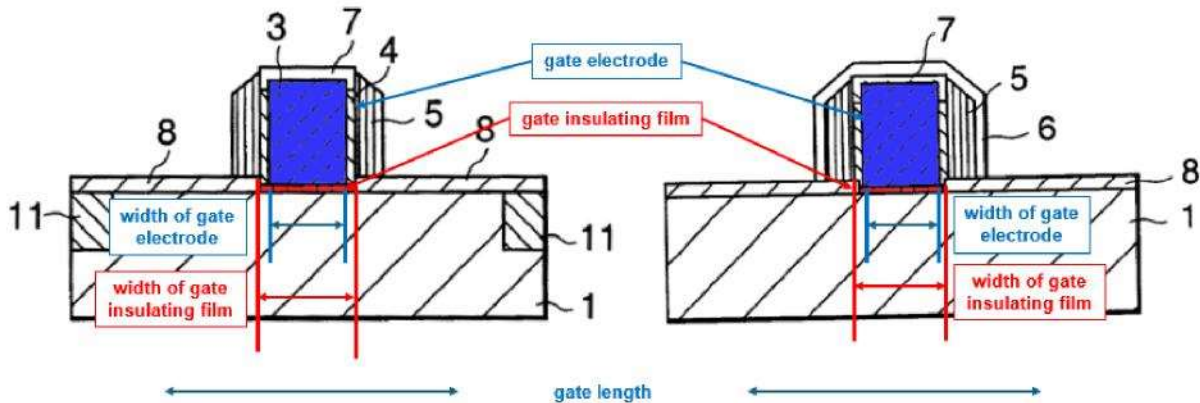
5. Limitation 1[d]

Kamata's first, fourth, and ninth embodiments each discloses "*a width of the gate insulating film along a gate length*[10] *is larger than a width of the gate electrode along the gate length*" (Limitation 1[d]). (Ex.1101, ¶¶160-63.)

As shown in Figures 1B(j) and 5(c) below for the first and fourth embodiments, the width along the gate length of high-k film 2 (shaded red) is larger than the width along the gate length of gate electrode 3 (shaded blue). (Ex.1101, ¶161 *Unified*, 2022 WL 500391, *17.) This is confirmed by Kamata's manufacturing process, in which

[10] The '076 patent uses the term "gate length" to refer to a direction, specifically from source to drain regions. (Ex.1101, ¶161 n.2.)

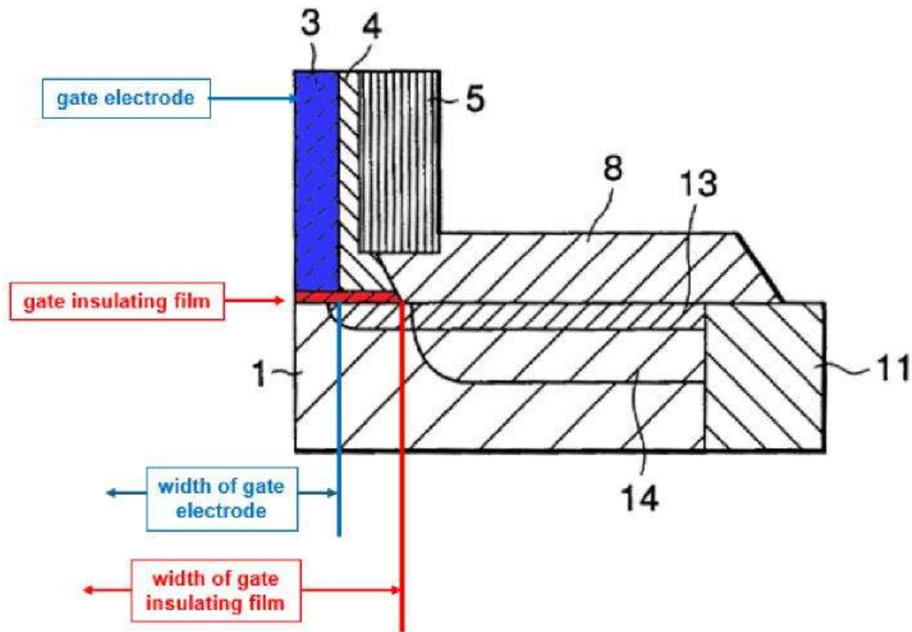
gate insulating film 2 and sidewall film 4 are etched together, with gate insulating film 2 extending beyond gate electrode 3 to under sidewall film 4. (Kamata, Ex.1027, Figures 1A(f), 1B(g), ¶¶50, 56, 68 (fourth embodiment); Ex.1101, ¶162.).)



Kamata, Figures 1B(j) (First Embodiment)

Kamata, Figure 5(c) (Fourth Embodiment)

In the ninth embodiment, high-k film 2 (shaded red) extends beyond (protrudes from) under the gate electrode to under sidewall films 4 and 5. (Ex.1101, ¶163; *see also* Kamata, Ex.1027, ¶50 (formation of gate electrode 3), 93 (describing deep diffusion region 14 after formation of sidewalls), 94, Figure 10(b) (below).) Although Figure 10(b) shows only a right portion of the device, a POSITA would have understood the left portion has a similar structure and therefore the width of high-k film 2 (shaded red) is larger than the width of the gate electrode (shaded blue). (Ex.1101, ¶163.)



Kamata, Figure 10(b)
(Ninth Embodiment)

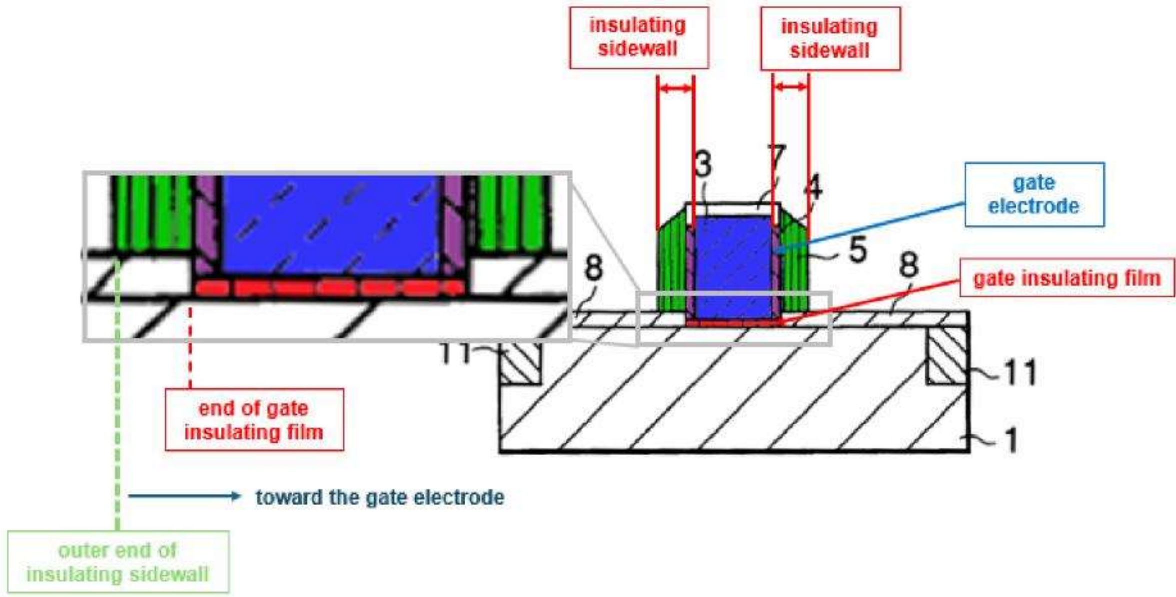
6. Limitation 1[e]

Kamata's first, fourth, and ninth embodiments each discloses "*an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode*" (Limitation 1[e]). (Ex.1101, ¶¶164-69.)

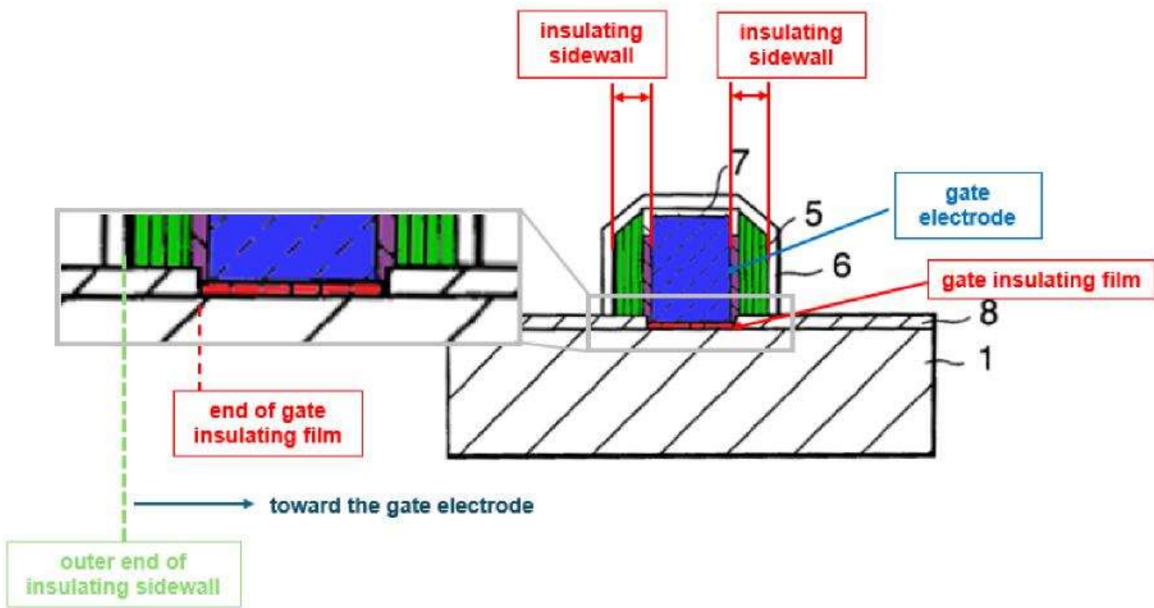
The term "retract" first appeared in claim 21 of the application leading to the '076 patent (issued claim 1). The term "retract" does not appear anywhere in the '076 patent specification or any other patent in the same family. In the co-pending district court litigation against TSMC, PO contends limitation 1[e] is satisfied by a gate insulating film whose end is disposed inward at a distance from the outer end

of the insulating sidewall and does not require any portion of the end of the gate insulating film to be in contact with the outer end of the insulating sidewall. Kamata meets this limitation at least under PO's litigation allegation.

As discussed in §V.B.5, Kamata's gate insulating film 2 extends from under gate electrode 3 to under the "*insulating sidewall*" (collectively films 4 and 5). In Kamata's first and fourth embodiments, the end of the gate insulating film is perpendicular to the substrate surface. As shown in Figures 1B(j) and 5(c) below, the end of the gate insulating film is disposed inward from the outer end of sidewall film 5 (the outer end of the "*insulating sidewall*") toward the gate electrode. Accordingly, Kamata's first and fourth embodiments each discloses "*an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode*" (Limitation 1[e]). (Ex.1101, ¶¶167; *Unified*, 2022 WL 500391, at *17.)

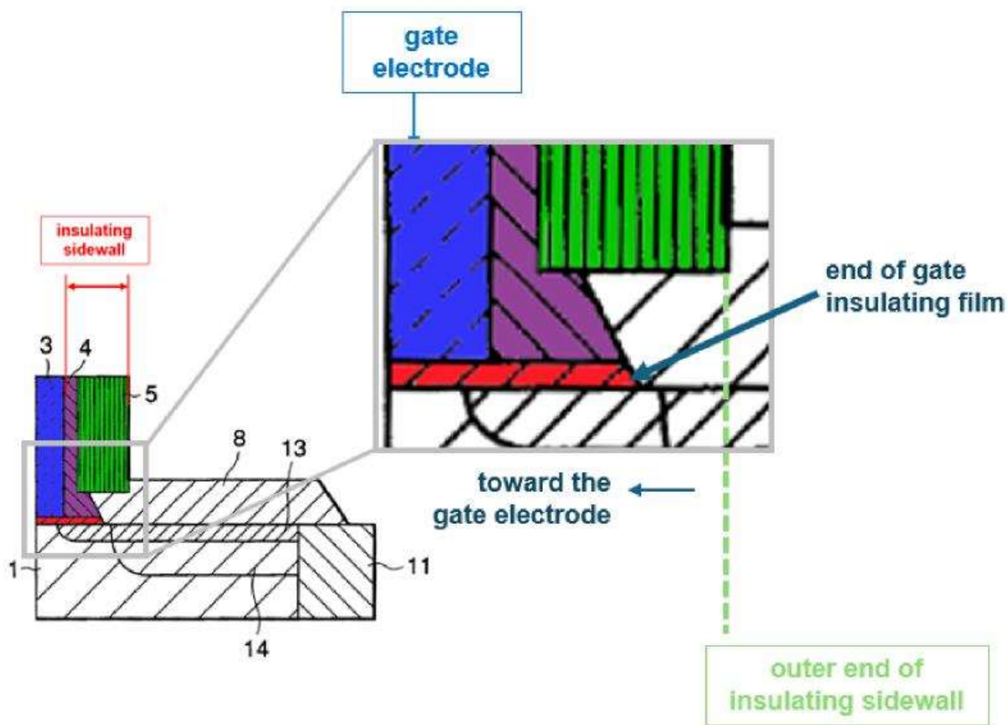


Kamata, Figure 1B(j) with enlargement (First Embodiment)



Kamata, Figure 5(c) with enlargement (Fourth Embodiment)

In Kamata's ninth embodiment, the end of the gate insulating film 2 (shaded red) slants upward and is not flush with the outer end of sidewall film 5; it is drawn inward from the outer end of sidewall 5 toward the gate electrode. Accordingly, Kamata's ninth embodiment discloses limitation (Limitation 1[e]). (Ex.1101, ¶¶169; *Unified*, 2022 WL 500391, *17.)



Kamata, Figure 10(b) with enlargement

C. Claim 2

Kamata's first, fourth, and ninth embodiments each discloses "*a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film*" [2]. (Ex.1101, ¶¶170-71.)

Kamata discloses "[i]t is desired that a SiOx ($0<x\leqq 2$) layer ... is interposed between the gate insulating film and the silicon substrate." (Kamata, Ex.1027, ¶¶54, 68 (relating fourth embodiment to first), 94 (relating ninth embodiment to first).) Therefore, in each embodiment, the SiOx layer is a "buffer insulating layer" formed of "a silicon oxide film" disposed between the substrate and gate insulating film 2. (Ex.1101, ¶171.)

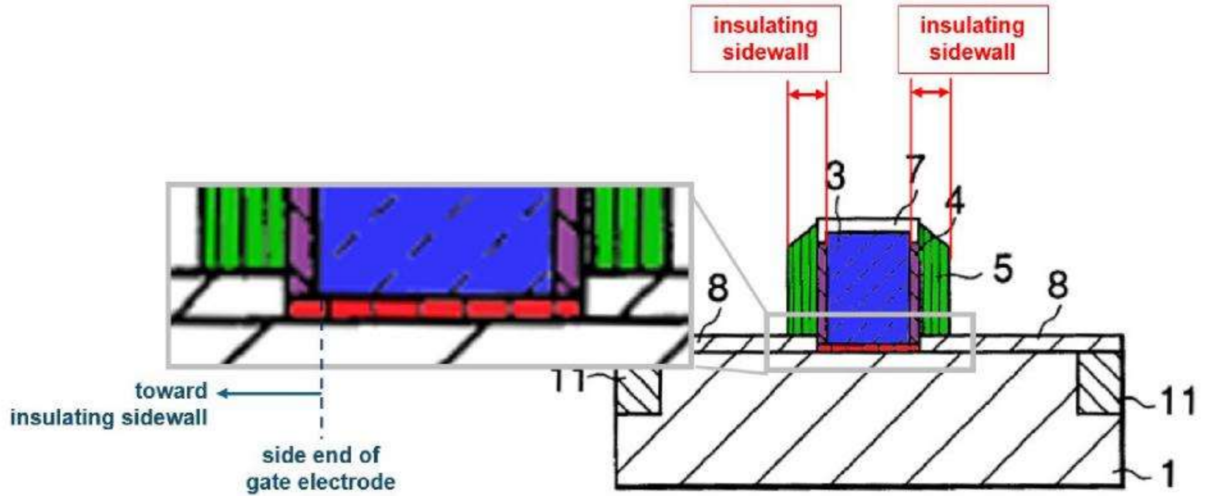
D. Claim 3

Kamata's first, fourth, and ninth embodiments each discloses "*the gate insulating film is formed of a Hf based oxide*" [3]. (Ex.1101, ¶¶172-74.) As discussed in §V.B.2, HfO_2 is used as Kamata's gate insulating film 2. (Kamata, Ex.1027, ¶52; §V.B.2.) HfO_2 is a "*Hf based oxide*." (Ex.1101, ¶174; Houssa, Ex.1213, 207.)

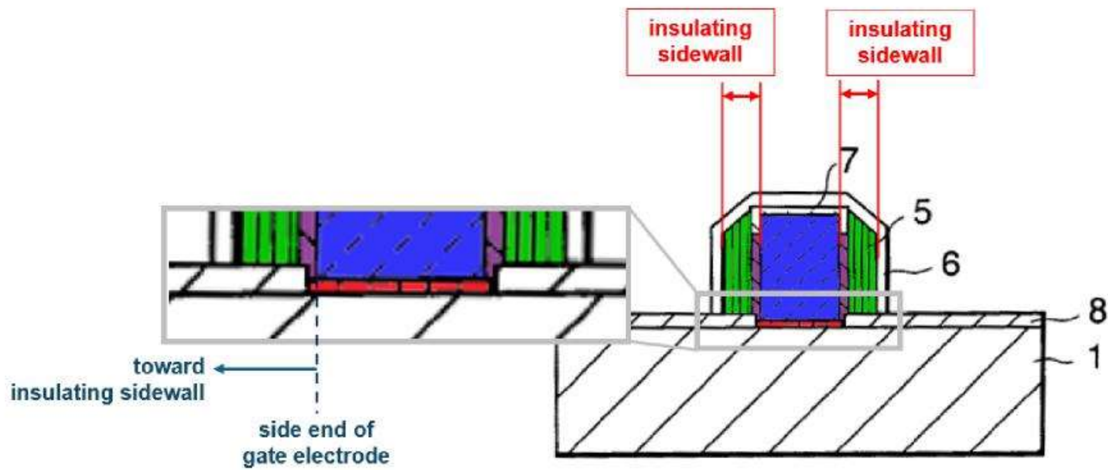
E. Claim 7

Kamata's first, fourth, and ninth embodiments each discloses "*an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall*" [7]. (Ex.1101, ¶¶175-178.)

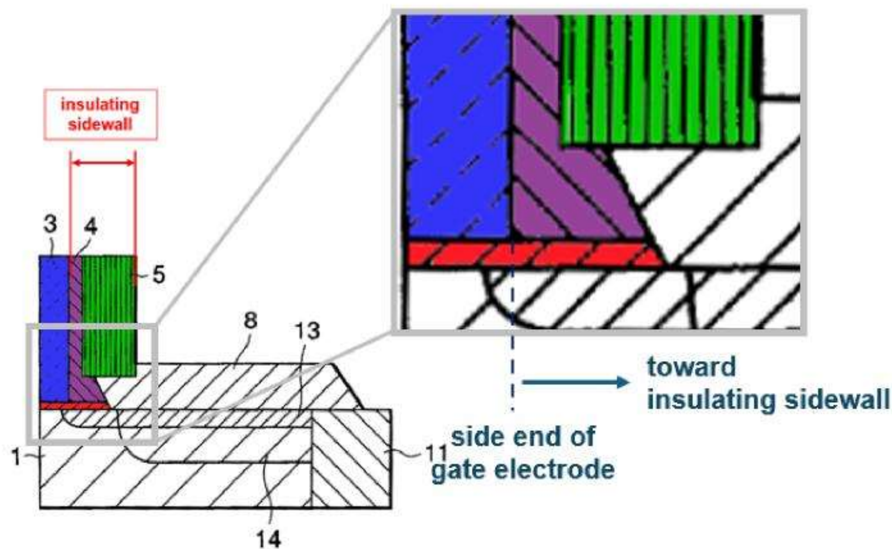
In Kamata's devices, high-k dielectric film 2 extends (protrudes outward) from under the gate electrode to under at least first sidewall 4 which is part of the "*insulating sidewall*." (*See* §V.B.5; Kamata, Ex.1027, Figures 1B(j), 5(c), 10(b)(below).)



Kamata, Figure 1B(j) with enlargement



Kamata, Figure 5(c) with enlargement



Kamata, Figure 10(b) with enlargement

F. Claim 8

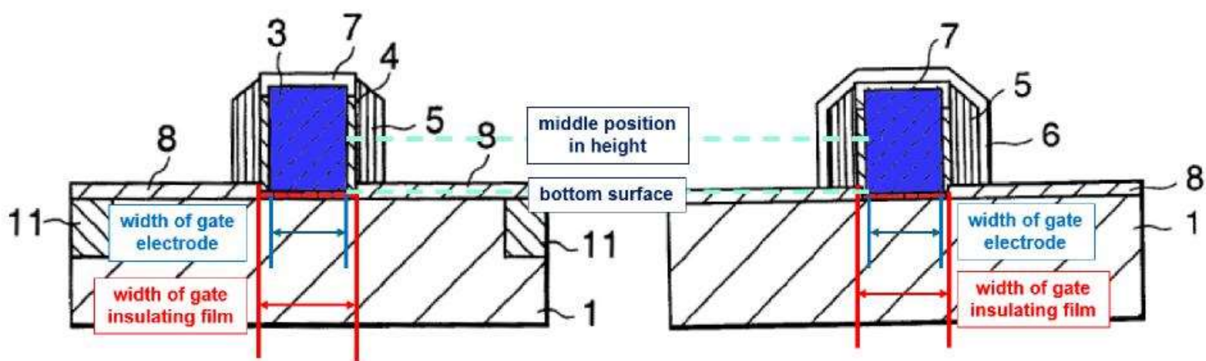
Kamata's first, fourth, and ninth embodiments each discloses "*the insulating sidewall has a double layer structure including an oxide film and a nitride film*" [8]. (Ex.1101, ¶179.)

The "*insulating sidewall*" of each embodiment includes first sidewall film 4 and second sidewall film 5. (§V.B.4.) Film 4 is an **oxide** film and film 5 is a **nitride** film. (Kamata, Ex.1027, ¶¶50, 58.) A POSITA would have understood films 4 and 5 to each be a "layer" of the collective sidewall, consistent with the '076 patent's disclosure. (Kamata, Ex.1027, ¶¶16 (referring to "multilayer type sidewall films"), 50, 58; Ex.1001, 21:6-15; Ex.1101, ¶179.)

G. Claims 10 and 13

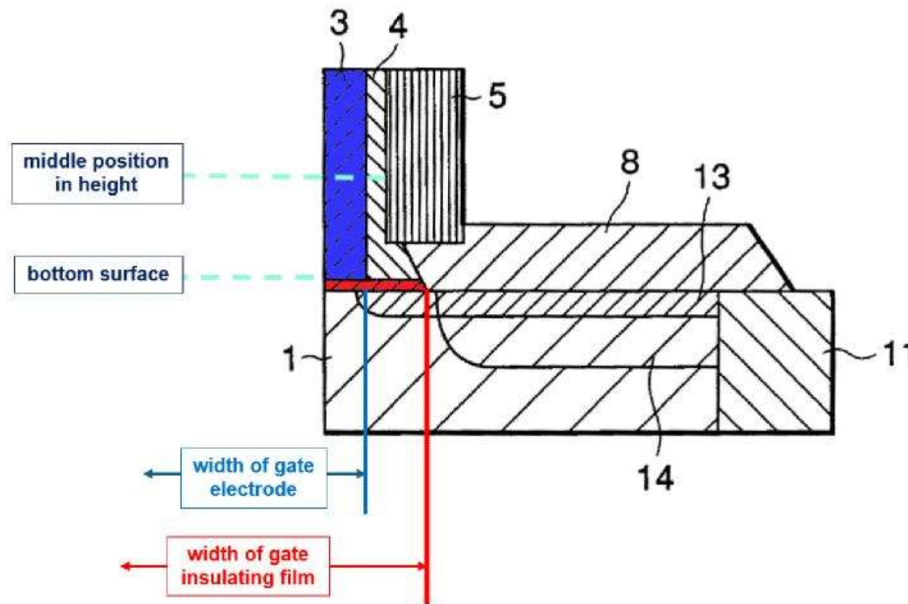
Kamata's first, fourth, and ninth embodiments each discloses "*a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length*" [10], and "*width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length*" [13]. (Ex.1101, ¶¶180-83.)

The width of Kamata's gate electrode is consistent across its entire height in each embodiment. Therefore, for the reasons discussed in §V.B.5, the width of the gate insulating film 2 (shaded red), including at film 2's bottom surface, is larger than the width of gate electrode 7 (shaded blue) at both the bottom surface and a middle position in height of the gate electrode. (Ex.1101, ¶181; *Unified*, 2022 WL 500391, *17.)



Kamata, Figures 1B(j) (First Embodiment)

Kamata, Figure 5(c) (Fourth Embodiment)



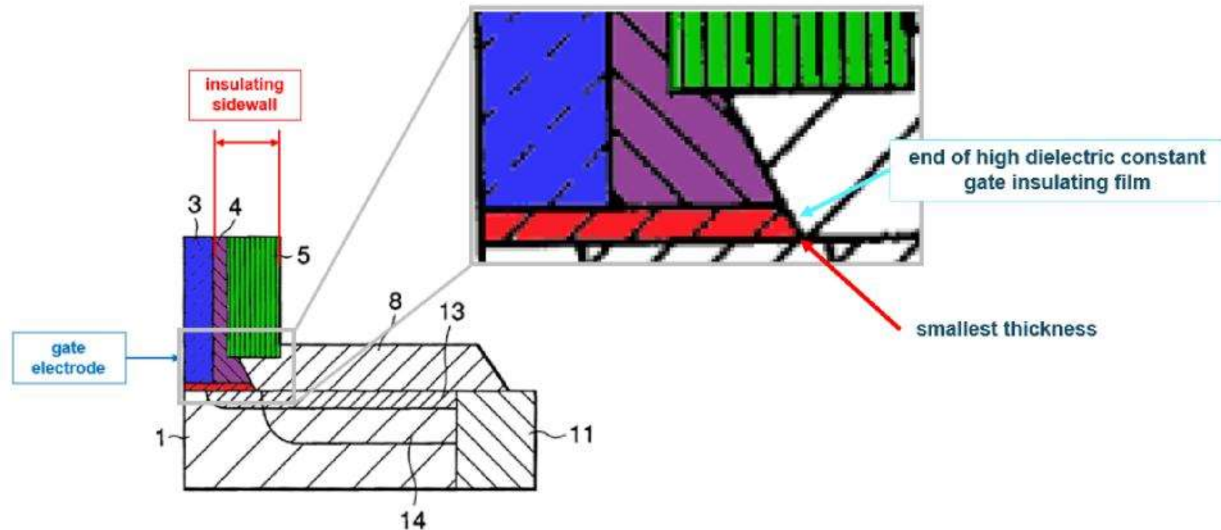
Kamata, Figure 10(b)
(Ninth Embodiment)

H. Claims 11-12

Kamata's ninth embodiment discloses "*the end of the gate insulating film located under the insulating sidewall has a tapered surface*" [11] and "*the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof*" [12]. (Ex.1101, ¶¶184-86.)

Gate insulating film 2 extends from under gate electrode 3 to under sidewall films 4 and 5 (collectively the "*insulating sidewall*"). (§V.B.5.) As shown in Figure 10(b) below, the end surface of gate insulating film 2, located under the "*insulating sidewall*," diminishes in thickness from its maximum (which is equivalent to its thickness under the gate electrode) to its smallest at its far end—it is "*tapered.*" (Kamata, Ex.1027, ¶93; *see also* Kamata, Ex.1027, ¶¶18, 85 (describing formation

of slanted surfaces in embodiment having same slanted gate dielectric and slanted epitaxially grown film 8) ; *Unified*, 2022 WL 500391, *17.)



Kamata, Figure 10(b) with enlargement
(Ninth Embodiment)

VI. Ground II: Kamata-Sim Combination Renders Claim 6 Obvious

Kamata discloses using HfO_2 as a high-k gate insulating film (Kamata, Ex.1027, ¶53) but does not expressly disclose the high-k gate dielectric "*has a thickness of 2 nm or less*" [6]. Sim, which "systematically evaluated the effects of high-k film thickness on charge trapping and channel carrier mobility," discloses this teaching. (Sim, Ex.1024, 218-19, 221.) Sim and Kamata are in the same field as the '076 patent, "a semiconductor device and a method for fabricating the semiconductor device." (Ex.1001, 1:18-19; Kamata, Ex.1027, ¶3; Sim, Ex.1024, Abstract; Ex.1101, ¶189) The devices of the combination of Kamata (first/fourth/ninth embodiments)

and Sim disclose "*a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less*" [6]. (Ex.1101, ¶¶188-93.)

A POSITA would have been motivated to adopt Sim's solution of forming a gate insulating film with a thickness of 20Å (2 nm) or less in Kamata's first/fourth/ninth embodiments. Sim expressly motivates the combination, finding that reducing the thickness of HfO_2 to below 20Å (2 nm) enhances mobility and reduces charge trapping, key issues in ensuring the performance and scalability of semiconductor devices. (Sim, Ex.1024, 221 ("Scaling the physical thickness of the HfO_2 dielectric to below 20Å [2 nm] causes less charge trapping and higher mobility."), 219 ("Even within 100μs, a 33Å HfO_2 sample shows significant current reduction while a 18Å HfO_2 sample is free from transient charging within the detection limits.").) A POSITA would further have understood this improvement aligns with the continued miniaturization of devices, which both Kamata and Sim emphasize is crucial to advancing CMOS technology. (Kamata, Ex.1027, ¶5; Sim, Ex.1024, 218; Ex.1101, ¶192.)

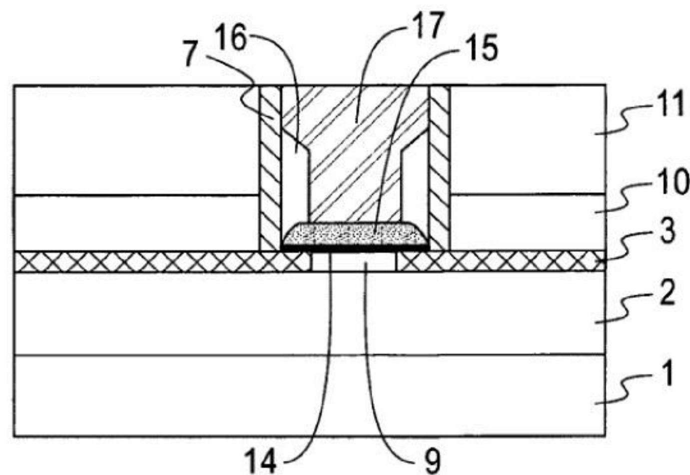
Additionally, the combination is nothing more than use of a known technique (Sim's HfO_2 dielectric layer with less than 20Å thickness) to improve similar devices in the same way for the reasons above. *KSR*, 550 U.S. at 416-417; Ex.1101, ¶¶192-93. A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable because Sim uses a well-known

process, atomic layer deposition (ALD), for fabricating high-k films. (Sim, Ex.1024, 218; Houssa, Ex.1213, 17-19; Ex.1101, ¶193.)

VII. Ground III: Guha Renders Claims 1-3, 7-8, 10-13 Obvious

A. Overview

Guha's Figure 12 device includes gate 17 with gate spacer structure 16 and isolating spacer 7. (Guha, Ex.1028, ¶¶43-45.) Dielectric layer 15, formed on gate-isolating layer 14, extends from under gate 17 to under gate spacer 16. (Guha, Ex.1028, ¶¶38, 43-44.)



Guha, Figure 12

B. Independent Claim 1

1. Preamble

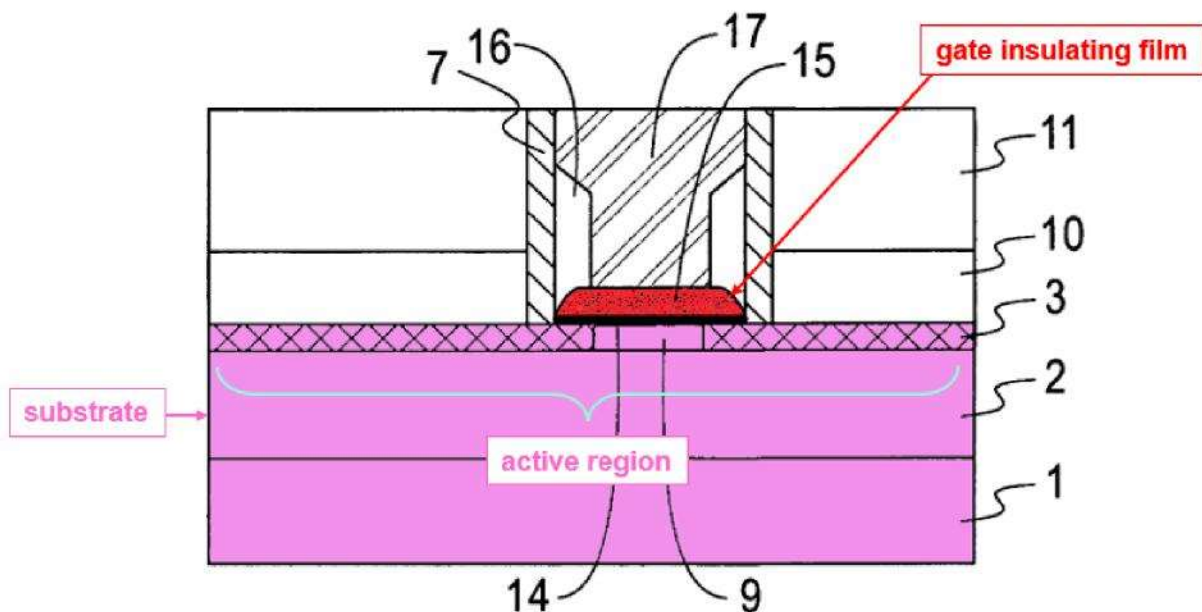
Guha's Figure 12 device includes substrate 1 and channel layer 3 each "compris[ing] any **semiconducting material**." (Guha, Ex.1028, ¶¶22-23, ¶¶43-45 (relating Figure 9's first embodiment device to Figure 12 device); *see Google*, 2022

WL 4287797, *9 n.9). Guha's Figure 12 device is a "*semiconductor device*." (Ex.1101, ¶195.)

2. Limitation 1[a]

Guha discloses "*a gate insulating film formed on an active region in a substrate and including Hf*" (Limitation 1[a]). (Ex.1101, ¶¶196-200.)

Guha's Figure 12 device, below, includes substrate 1, which "may be of the **n or p-type** depending on the desired device to be fabricated." (Guha, Ex.1028, ¶¶22, 43.) Channel layer 3 is further provided over buried oxide layer 2 which "can be omitted." (*Id*.) Substrate 1, channel layer 3, and buried oxide layer 2 (if present) are collectively "*a substrate*" (shaded pink). (Ex.1101, ¶196.)



Guha, Figure 12

Guha's substrate contains "active device regions." (Guha, Ex.1028, ¶¶22, 43.) Source/drain extensions "are formed by implanting dopants ... into the channel layer 3," further indicating presence of an active region in Guha's Figure 12 device. (Guha, Ex.1028, ¶¶26, 43.) A POSITA would have understood Guha's device has "*an active region in a substrate*." (Guha, Ex.1028, ¶22; Ex.1101, ¶197.)

Guha's Figure 12 device includes gate-isolating layer 14 (shaded black) formed on a portion of channel layer 3 which is part of the "*active region in a substrate.*" (Guha, Ex.1028, ¶¶37, 43.) Dielectric layer 15 (shaded red), "comprising a high-k dielectric material," is "formed only on the gate-isolating layer 14." (Guha, Ex.1028, ¶¶38, 43.) Dielectric layer 15 is therefore "*a gate insulating film formed on*[11] *an active region in a substrate*." (Ex.1101, ¶¶198; *see also* Guha, Ex.1028, ¶37 (gate-isolating layer 14 "acts as a buffering layer between channel 9 and the" high-k dielectric).)

Guha discloses that high-k dielectric layer is a material such as "hafnium oxide, hafnium silicate, aluminum oxide or zirconium oxide." (Guha, Ex.1028, ¶38.) A POSITA would have been motivated to select hafnium oxide or hafnium silicate

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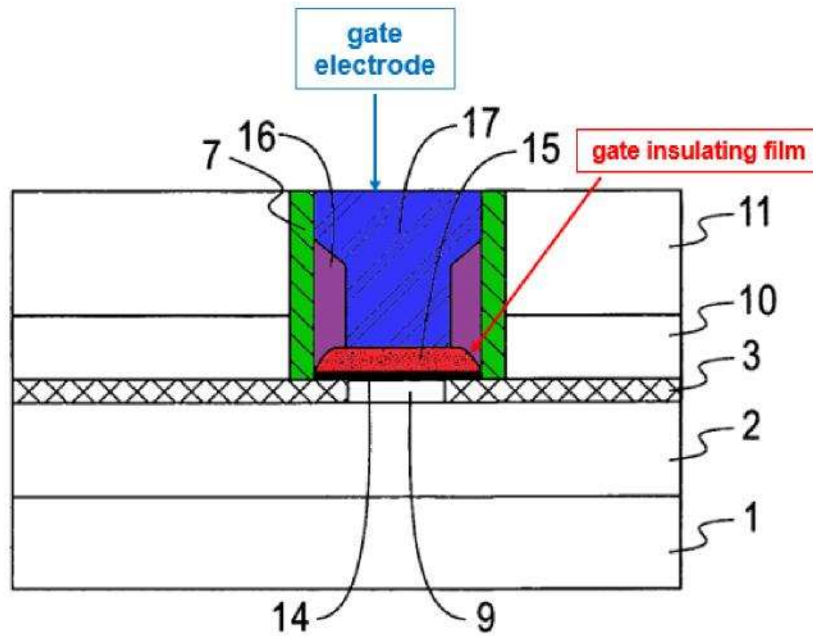
[11] The '076 patent uses the term "formed on" to indicate relative position and does not require direct contact. (E.g., 7:42-44 ("insulating sidewall 7 is formed on each side surface of the gate electrode 5 with an offset sidewall 6 interposed therebetween").)

because of their known benefits, e.g., HfO_2's "superior thermal stability with poly-Si and reasonable band alignment," and HfSiON's "improved thermal stability and electrical characteristics." (Lee-2000, Ex.1337, 2.4.1; Koyama, Ex.1029, 849; *see also* Houssa, Ex.1213, 207 (HfO_2 "combines a high k (15–26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ..."; HfO_2 can be scaled down to a smaller EOT); Ex.1101, ¶199.) Guha therefore discloses a "*gate insulating film* [film 2] ... *including Hf*."

3. Limitation 1[b]

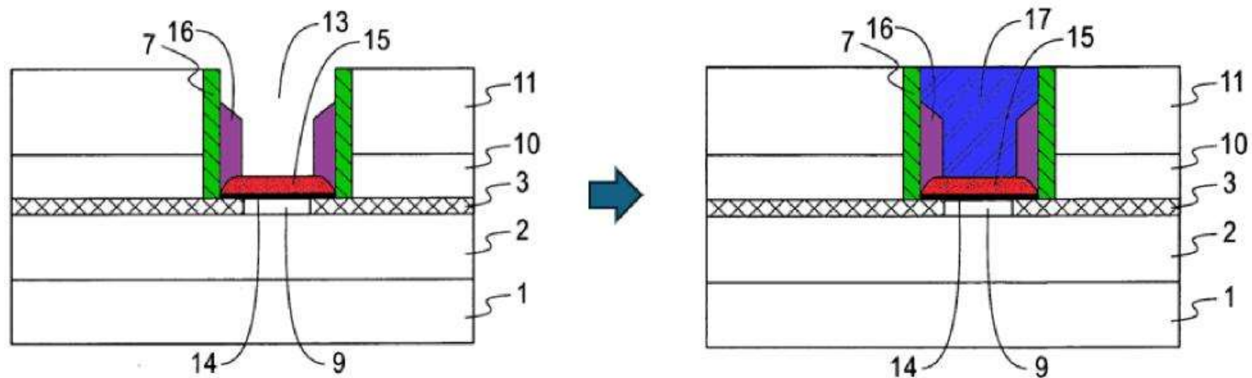
Guha discloses "*a gate electrode formed on the gate insulating film*" (Limitation 1[b]). (Ex.1101, ¶¶201-203.)

In Guha's Figure 12 below, gate 17 (shaded blue) is formed on high-k dielectric layer 15 (shaded red). Gate 17 is formed of a "conductive material" and therefore is "*a gate electrode formed on the gate insulating film*." (Guha, Ex.1028, ¶¶41, 45; Ex.1101, ¶¶202-03; *Unified*, 2022 WL 500391, *17.)



Guha, Figure 12

Guha's fabrication process confirms the Figure 12 structure. For example, Guha describes cavity 13 (Figure 11 (left)) is "filled with a conductive material to form the **gate 17**" by "depositing the material ... **onto the dielectric layer 15**", resulting in formation of the gate electrode over dielectric layer 15. (Guha, Ex.1028, ¶¶41, 44 (associating gate formation in Figure 12 (right) with first embodiment process), 45; Ex.1101, ¶203.)



Guha, Figure 11 (left), Figure 12 (right)

4. Limitation 1[c]

Guha discloses "*a insulating sidewall formed on each side surface of the gate electrode*" (Limitation 1[c]). (Ex.1101, ¶¶204-12.)

Guha's device includes gate spacers 16 (shaded purple) and isolating spacers 7 (shaded green) on gate electrode 17's side surfaces (shaded blue). (Guha, Ex.1028, ¶¶28 (formation of spacers 7), 44 (formation of spacers 16 in Figure 12 device), 43 (associating Figure 12 device to process steps associated with Figures 1-7).) Although Guha refers to each as a "spacer," as noted above, "spacer" and "sidewall" are often used interchangeably. (Ex.1101, ¶207; §IV.B.3.) Further, a POSITA would thus have understood them to be "sidewalls." (*E.g.*, Guha, Ex.1028, ¶¶40, 44-45; Ex.1101, ¶204.)

Guha, Figure 12

Gate spacers 16 are made of "e.g. an oxide or other suitable material." (Guha, Ex.1028, ¶¶40, 43.) Through use of gate spacers 16, "the interface between the bottom of the gate 17 and the dielectric layer 15 is better defined and offers a better control over the channel 9." (Guha, Ex.1028, ¶45.) To provide such benefits, a POSITA would have understood gate spacers 16 to be formed of an insulating oxide material. (Ex.1101, ¶¶208-09; Wolf-4, Ex.1214, 9, 75; Plummer, Ex.1215, 79-80.) Isolating spacers 7 are "composed of any insulating material including, for example,

an oxide, nitride, oxynitride or any combination thereof" with the "preferred material [being] silicon nitride." (Guha, Ex.1028, ¶¶28, 43.)

Gate spacers 16 and isolating spacers 7 are collectively an "*insulating sidewall formed on each side surface of the gate electrode*" (Limitation 1[c]), consistent with the '076 patent's disclosure. (Ex.1101, ¶210; Ex.1001, 2:60-65 ("insulating sidewall" includes two sidewalls).) Petitioner refers to this as the first "*insulating sidewall*" configuration.

Alternatively, gate spacers 16 alone disclose an "*insulating sidewall formed on each side surface of the gate electrode*" (Limitation 1[c]), consistent with the '076 patent's disclosure. (Ex.1101, ¶211; Ex.1001, 6:9 ("insulating sidewall" has a single component).) Petitioner refers to this as the second "*insulating sidewall*" configuration.

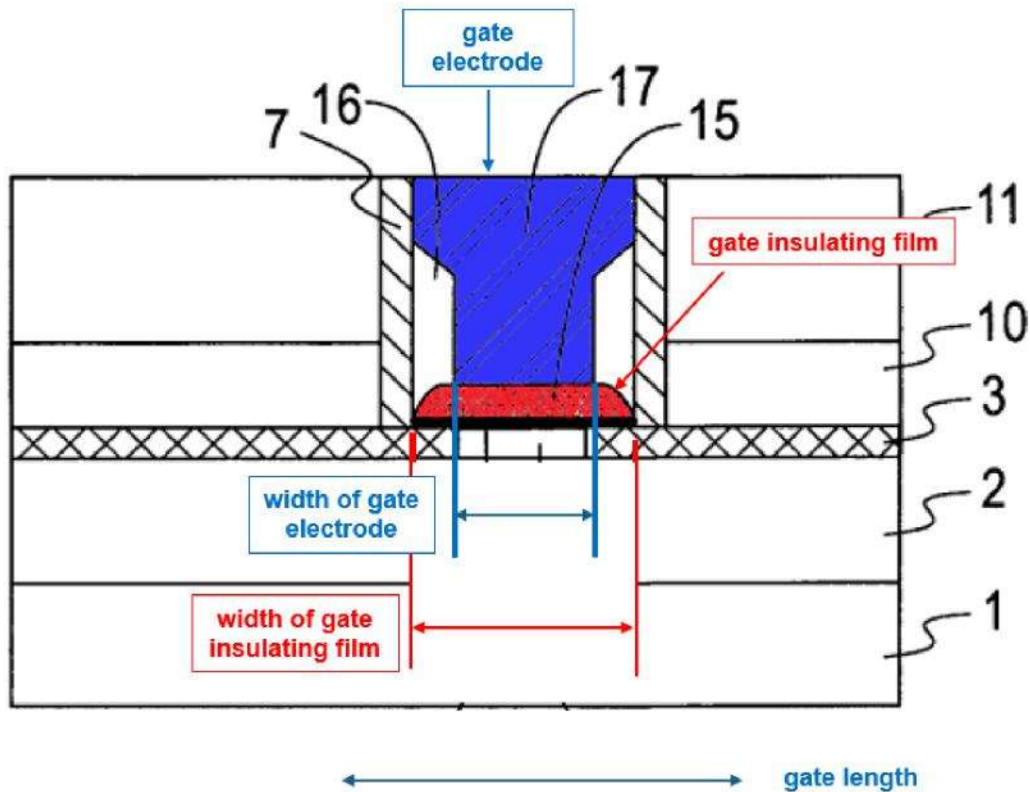
Both the first and second "*insulating sidewall*" configurations teach limitation (Limitation 1[c]). (Ex.1101, ¶212.)

5. Limitation 1[d]

Guha discloses "*a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length*" (Limitation 1[d]). (Ex.1101, ¶¶213-15.)

As shown in Figure 12 below, the width of dielectric layer 15 (shaded red) is larger than the width of the bottom portion of the gate electrode (shaded blue).

(Ex.1101, ¶213; *see also* Guha, Ex.1028, ¶¶41, 43-45 (describing formation of spacers 16 in the cavity followed by deposition of the gate electrode).)

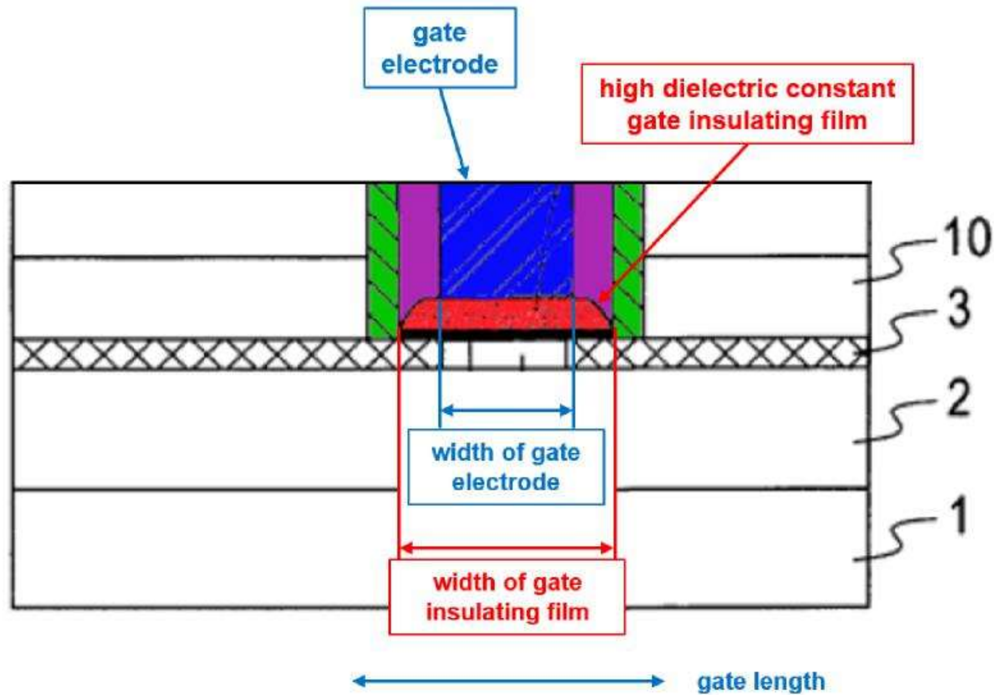


Guha, Figure 12

Should an argument be made the width of the gate electrode at its upper portion is equal to the width of dielectric layer 15 and therefore Guha fails to disclose this limitation, such an argument is improper. First, nothing in this limitation requires the gate electrode width at all heights to be smaller than the width of the gate insulating film. The limitation recites broadly "*a width of the gate electrode.*" Claim 10 narrows this limitation, reciting that "*a width of a bottom surface of the gate insulating film along a gate length is larger than* ***a width of a <u>bottom surface</u> of the***

gate electrode** along the gate length*," and claim 13 also narrows this limitation, reciting "*the width of the gate insulating film along a gate length is larger than* ***a width of part of the gate electrode in a <u>middle position</u> in height along the gate length." (Ex.1101, ¶214.)

Second, Guha discloses "internal spacer 16a and 16b may also have a rectangular cross-section, e.g., by polishing or removing the upper curved region to form a horizontal portion of the internal surface." (Guha, Ex.1028, ¶47.) A POSITA would have understood, with this teaching, the expanded upper portion of the gate electrode is removed along with the slanted upper portion of spacers 16 to obtain a rectangular cross-section. (Ex.1101, ¶215.) In this embodiment, shown in modified Figure 12 below, the gate electrode width is the same at the bottom and the top, meeting limitation 1[d], even under an impermissibly narrow interpretation. *See Boston Sci. Scimed, Inc. v. Cordis Corp.*, 554 F. 3d 982, 991 (Fed. Cir. 2009) ("[c]ombining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness").



Guha, Modified Figure 12

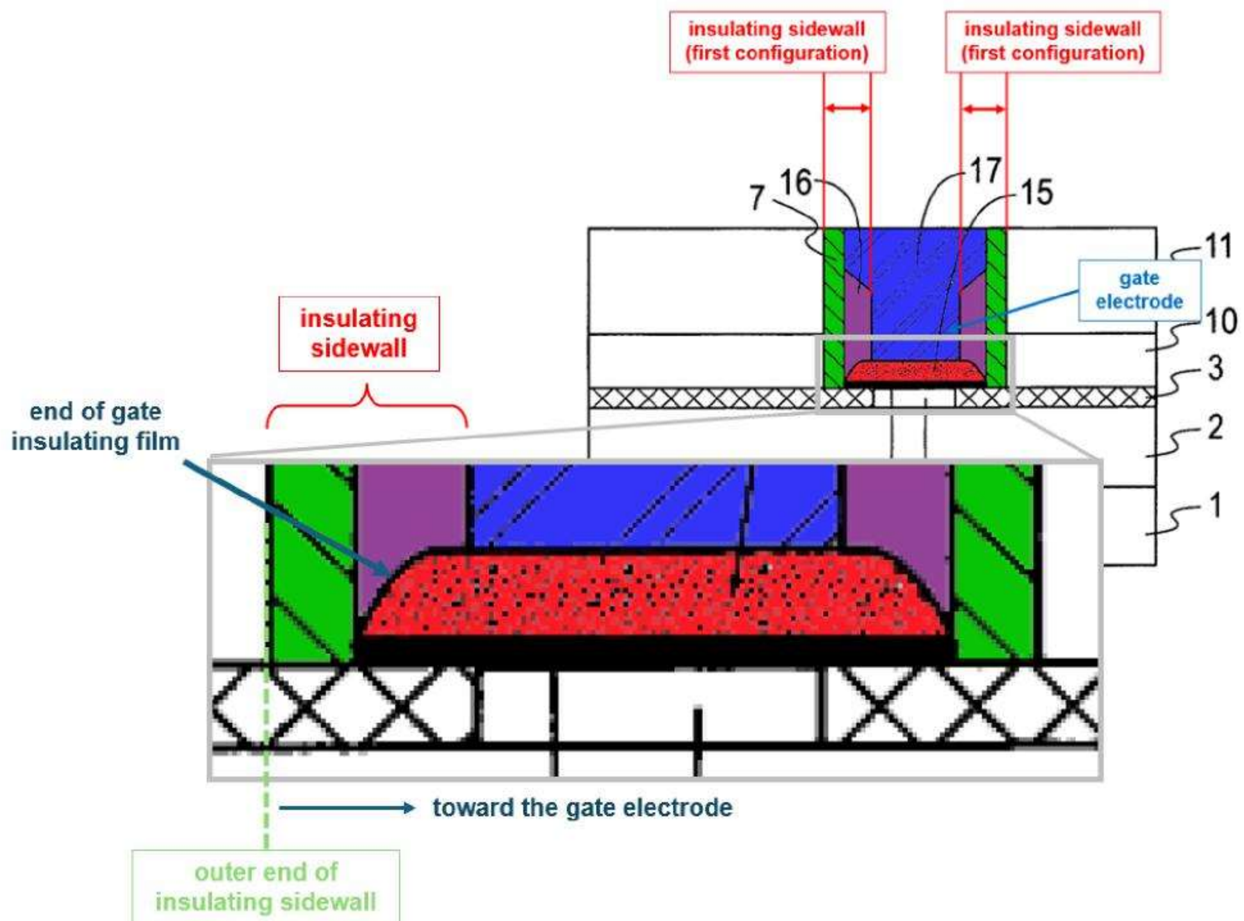
6. Limitation 1[e]

Guha discloses "*an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode*" (Limitation 1[e]) under both the first and second "*insulating sidewall*" configurations. (Ex.1101, ¶¶216-21.)

a. First Configuration (Spacer 16 and Spacer 7)

As shown below, the rounded end of dielectric layer 15 (shaded red) is under spacer 16 (shaded purple), but not under spacer 7 (shaded green). Therefore, the end of dielectric layer 15 is disposed inward at a distance from the outer end of the "*insulating sidewall*" (outer end of spacer 7) toward the gate electrode. (Ex.1101,

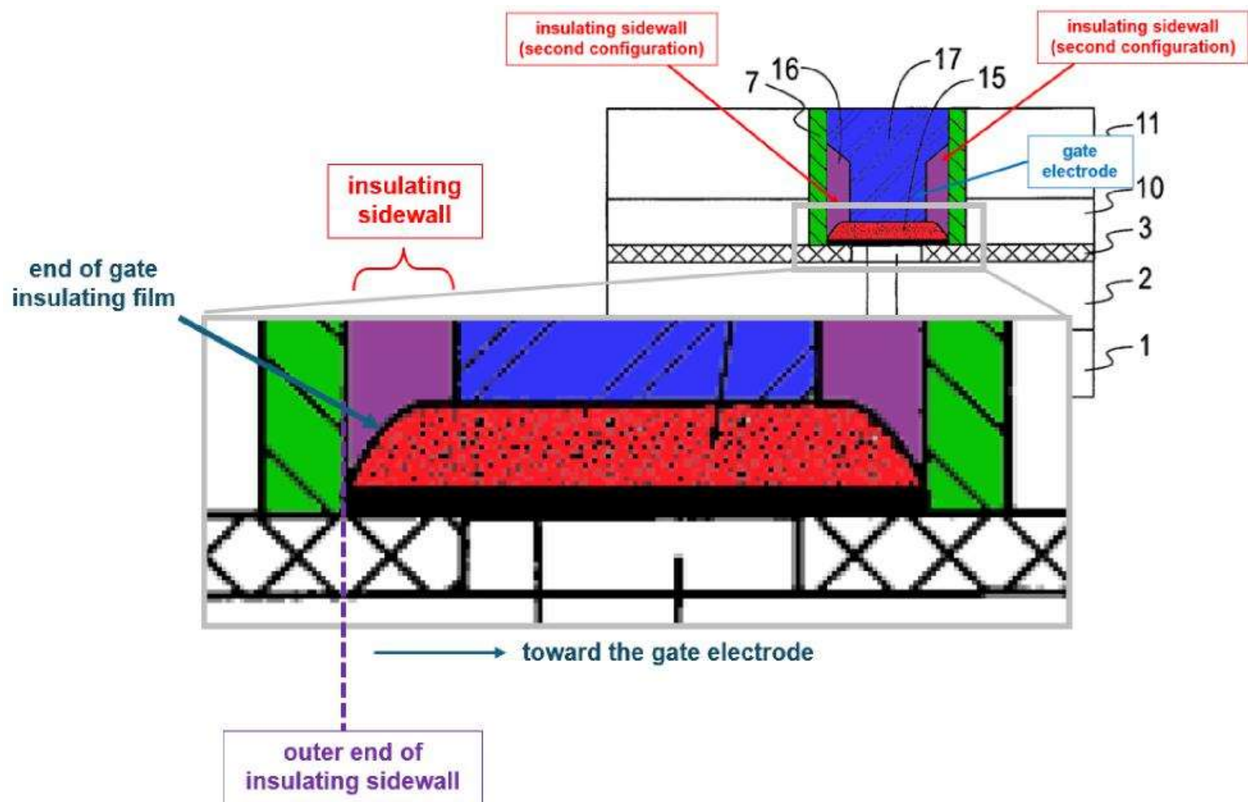
¶217.) This is confirmed by Guha's manufacturing process, in which dielectric layer 15 is formed in cavity 13 after formation of isolating spacers 7 but before gate spacers 16. (Guha, Ex.1028, ¶¶43-45; Ex.1101, ¶219.) Accordingly, Guha discloses "*an end of the gate insulating film under the insulating sidewall* [spacer 16 and spacer 7] *is retracted from an outer end of the insulating sidewall* [outer end of spacer 7] *toward the gate electrode*" (Limitation 1[e]). *Unified*, 2022 WL 500391, *17.



Guha, Figure 12 with enlargement

b. Second Configuration (Gate Spacer 16)

As shown below, the point at which the gate insulating film is the thinnest contacts the outer end of the insulating sidewall (outer end of spacer 16). (Guha, Ex.1028, Figure 12.) Due to its rounded shape, the end of gate insulating film 2 curves inward from the outer edge of spacer 16 towards the gate electrode, as shown below. Accordingly, Guha discloses an "*end of the gate insulating film under the insulating sidewall* [spacer 16] *is retracted from an outer end of the insulating sidewall toward the gate electrode*" (Limitation 1[e]). (Ex.1101, ¶¶220-21; *Unified*, 2022 WL 500391, at *17.)



Guha, Figure 12 with enlargement

C. Claim 2

Guha discloses "*a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film*" [2]. (Ex.1101, ¶¶222-24.)

Gate-isolating layer 14 (shaded black) "**acts as a buffering layer** between channel 9 and the dielectric material to be deposited thereon" (i.e., high-k dielectric 15). (Guha, Ex.1028, ¶¶37, 43, Figure 12 (below).) Channel 9 is part of the substrate. (§VII.B.2.) Gate-isolating layer 14 is therefore "*a buffer insulating film ... provided between the substrate and the gate insulating film.*" (Ex.1101, ¶¶222-24) The "preferred material for the gate-isolating layer 14 is silicon oxide" and therefore Guha's gate isolating layer is "*formed of a silicon oxide film*." (Guha, Ex.1028, ¶¶37, 43; Ex.1101, ¶¶223-24.)

Guha, Figure 12

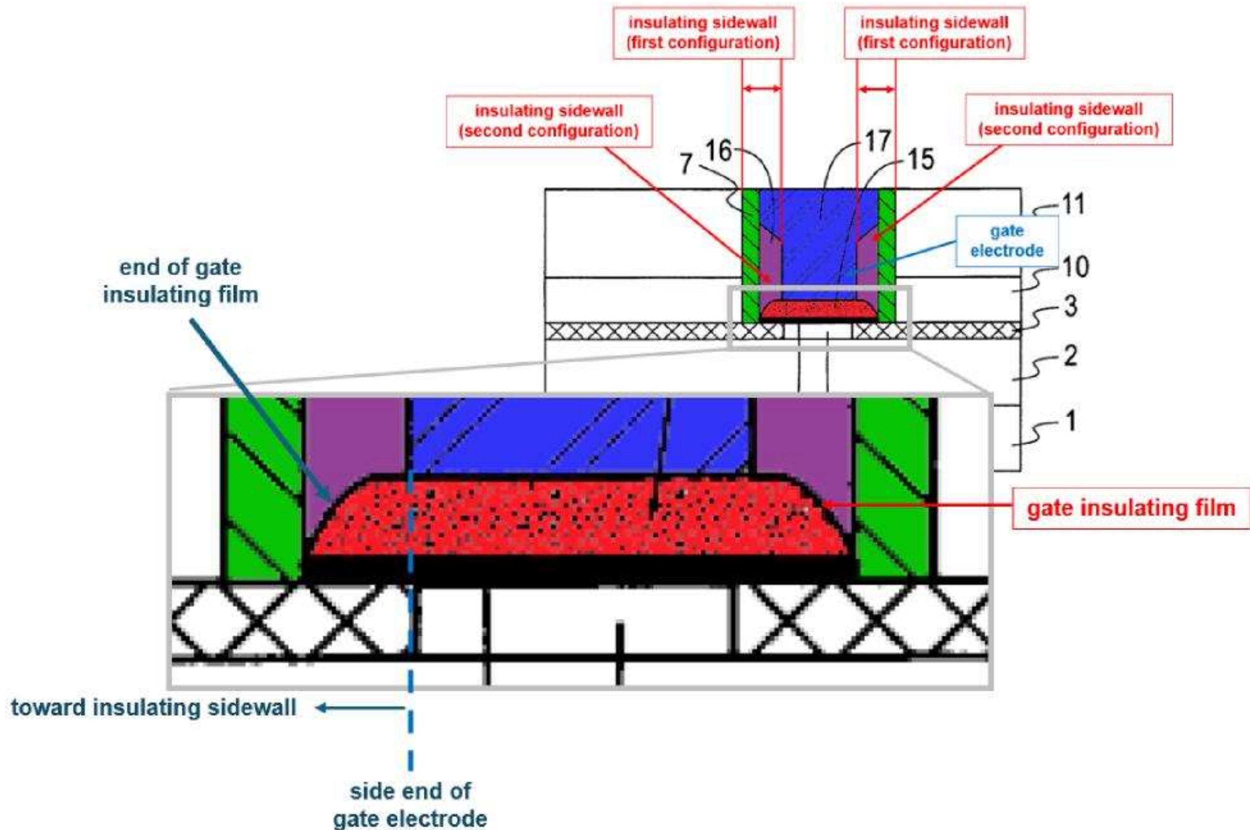
D. Claim 3

Guha discloses "*the gate insulating film is formed of a Hf based oxide*" [3]. (Ex.1101, ¶225.) Guha's dielectric layer 15 ("*gate insulating film*") "preferably compris[es] a high-K dielectric material" such as "**hafnium oxide**," which is "*a Hf based oxide*." (Guha, Ex.1028, ¶¶38, 43.) A POSITA would have been motivated to select HfO_2 in light of its known benefits, including thermal stability, band alignment, and ability to scale. (Lee-2000, Ex.1337, 2.4.1; Houssa, Ex.1213, 207; Ex.1101, ¶225; §VII.B.2.)

E. Claim 7

Guha discloses "*an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall*" [7], under both the first and second "*insulating sidewall*" configurations. (Ex.1101, ¶¶226-27.)

As discussed in §§VII.B.5-6, dielectric layer 15 in Guha's Figure 12 device extends from under the gate electrode to under spacer 16 (i.e., it protrudes from the side end of the gate electrode). Spacer 16 alone is the recited "*insulating sidewall*" (second configuration) or alternatively spacer 16 and spacer 7 are collectively the "*insulating sidewall*" (first configuration). Therefore, in Guha's Figure 12 device, the end of dielectric layer 15 ("*gate insulating film*") "*protrudes from a side end of the gate electrode toward the insulating sidewall*" [7]. (Ex.1101, ¶¶226-27.)



Guha, Figure 12 with enlargement

F. Claim 8

Guha discloses "*the insulating sidewall has a double layer structure including an oxide film and a nitride film*" [8], under the first "*insulating sidewall*" configuration (spacer 16 and spacer 7). (Ex.1101, ¶¶228-31.)

Gate spacer 16 is a "material, e.g. an **oxide** or other suitable material" and is thus "*an oxide film*." (Guha, Ex.1028, ¶40; Ex.1101, ¶229.) Isolating spacer structure 7 "can be composed of any insulating material including, for example, an oxide, **nitride**, oxynitride or any combination thereof" with "**silicon nitride**" as the "preferred material." (Guha, Ex.1028, ¶28.) A POSITA would have considered gate

spacer 16 and isolating spacer 7 to each be a "layer" of the collective sidewall, consistent with the '076 patent's disclosure. (*E.g.*, Guha, Ex.1028, ¶¶28 (formation of spacers 7), 44 (formation of spacers 16); §VII.B.4; Ex.1001, 21:6-15; Ex.1101, ¶231.)

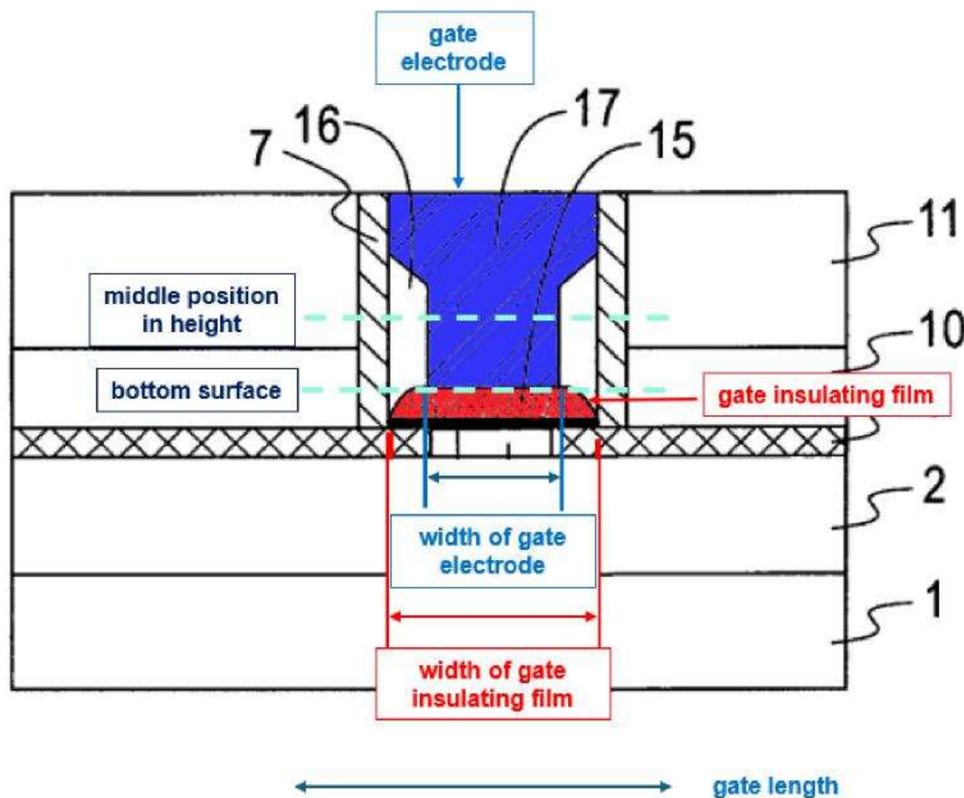
Guha, Figure 12

G. Claims 10 and 13

Guha discloses "*a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length*" [10] and "*the width of the gate insulating film along a gate length*

is larger than a width of part of the gate electrode in a middle position in height along the gate length" [13]. (Ex.1101, ¶¶232-33.)

As shown in Figure 12 below, the width of the bottom surface of dielectric layer 15 (shaded red) is larger than the width of the bottom portion of the gate electrode (shaded blue). (Ex.1101, ¶2323.) The width of the gate electrode is the same at its middle position as at its bottom. Therefore, the width of the dielectric layer 15 is also larger than the width of the gate electrode at its middle. (Ex.1101, ¶233; *Unified*, 2022 WL 500391, *17.)

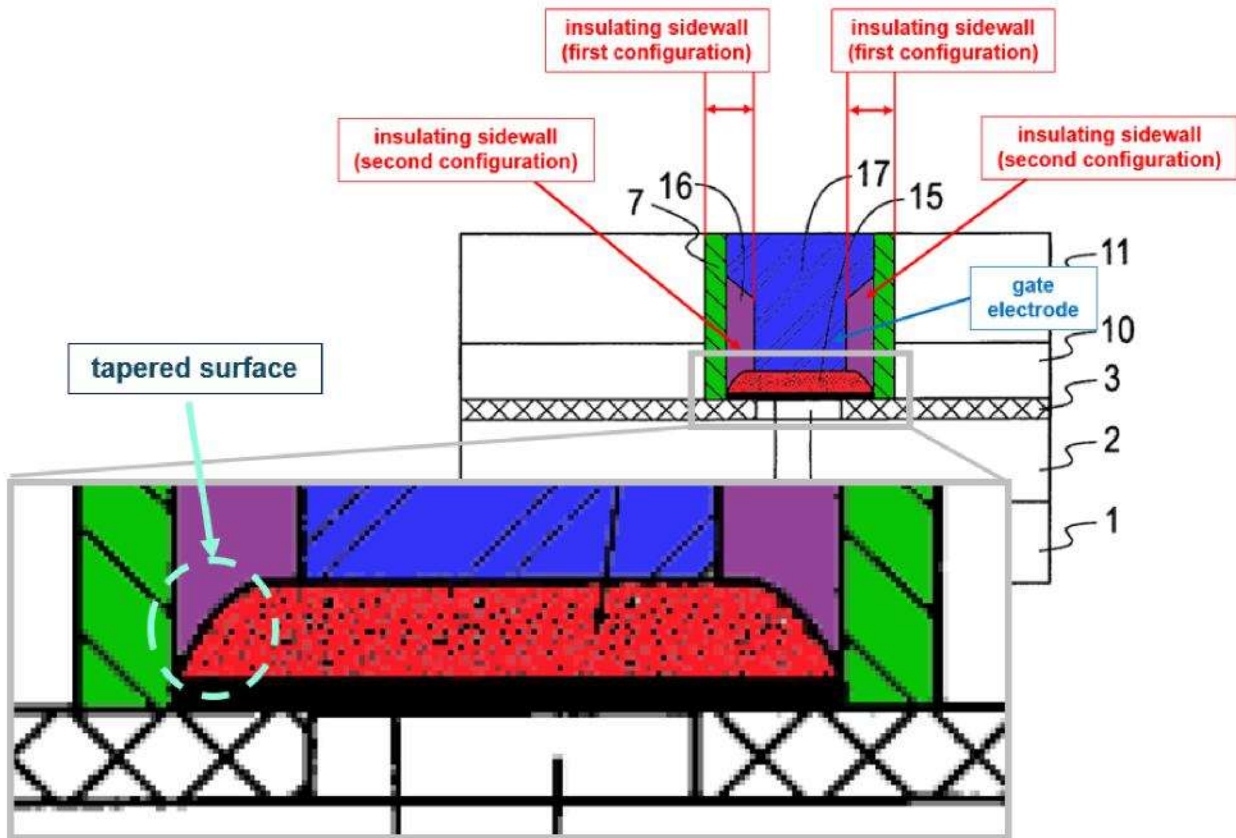


Guha, Figure 12

H. Claims 11-12

Guha discloses "*the end of the gate insulating film located under the insulating sidewall has a tapered surface*" [11] and "*the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof*" [12], under both the first and second "*insulating sidewall*" configurations. (Ex.1101, ¶¶234-35.)

In Guha's device, "the edge where the dielectric layer 15 meets the isolating spacer structure 7 ... is **rounded** either upwards or **downwards** (e.g., similar to a cusp)." (Guha, Ex.1028, ¶43.) That is, the dielectric layer reduces in thickness at its end such that its smallest thickness is under spacer 16—i.e., it tapers. (Ex.1101, ¶235; *see* Guha, Ex.1028, ¶44 (spacer 16 is formed after and on dielectric layer 15).) Accordingly, the tapered end portion of dielectric layer 15 is "*located under the insulating sidewall*" in the first configuration (**spacers 16** and spacers 7) and second configuration (**spacers 16**). (Ex.1101, ¶235.)



Guha, Figure 12

VIII. Ground IV: Guha-Sim Combination Renders Claim 6 Obvious

Guha does not expressly disclose "*a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less*" [6]. Sim discloses this teaching, as discussed in §VI. Accordingly, the Guha-Sim combination discloses claim 6. (Ex.1101, ¶¶237.) Sim and Guha are in the same field as he '076 patent, "a semiconductor device and a method for fabricating the semiconductor device." (Ex.1001, 1:18-19; Guha, Ex.1028, ¶1; Sim, Ex.1024, Abstract; Ex.1101, ¶238.)

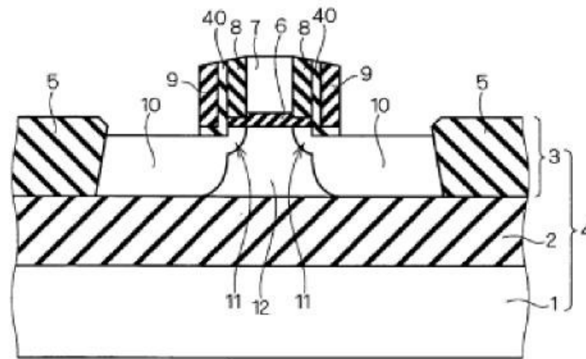
A POSITA would have been motivated to adopt Sim's solution of forming a gate insulating film with a thickness of 20Å (2 nm) or less in Guha's Figure 12 device. Sim discloses reducing the thickness of HfO_2 to below 20Å enhances mobility and reduces charge trapping, which ensures the performance and scalability of semiconductor devices. (Sim, Ex.1024, 219, 221; §VI.) Such improvements align with the continued miniaturization of devices, which both Guha and Sim emphasize is crucial to advancing CMOS technology. (Guha, Ex.1028, ¶2; Sim, Ex.1024, 218; Ex.1101, ¶¶239-42)

Additionally, the combination is nothing more than use of a known technique (Sim's HfO_2 dielectric layer with less than 20Å thickness) to improve similar devices in the same way. *KSR,* 550 U.S. at 416-417; Ex.1101, ¶242.) A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable because Sim uses a well-known process, atomic layer deposition (ALD), for fabricating high-k films. (Sim, Ex.1024, 218; Houssa, Ex.1213, 17-19; Ex.1101, ¶242.)

IX. Ground V: Matsumoto-Yu Combination Renders Claims 1-3, 7-8, 10, & 13 Obvious

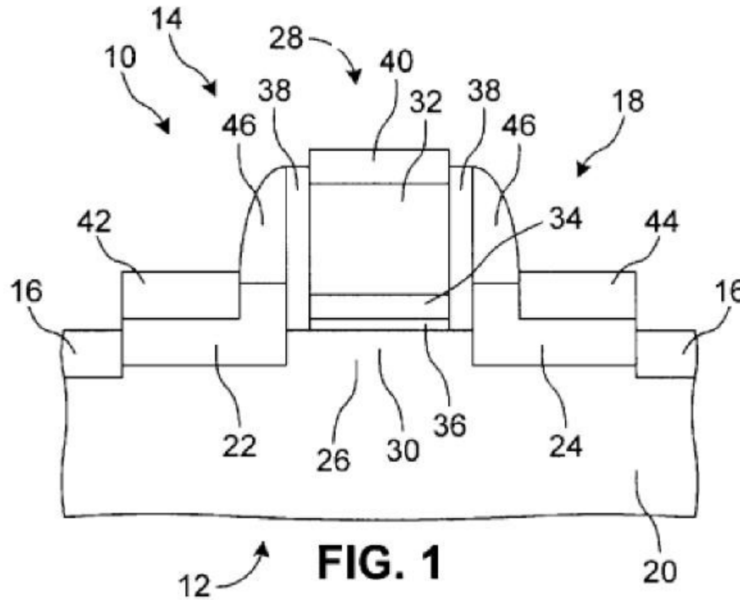
A. Overview

Matsumoto's fourth embodiment MOSFET includes a gate insulating film extending from under gate electrode 7 to under only film 8 formed on the gate electrode's sidewalls. (Matsumoto, Ex.1009, ¶¶137-140, Figure 22 (below).)



Matsumoto, Figure 22

Yu's MOSFET device includes buffer interface 36 between semiconductor substrate 20 and high-k gate dielectric 34. (Yu, Ex.1048, 3:59-62; Figure 1 (below).) Yu's gate dielectric 34 "is made from a high-K material"; examples of such high-k materials include "hafnium oxide (e.g., HfO_2), zirconium oxide (e.g., ZrO_2), cerium oxide (e.g., CeO_2), aluminum oxide (e.g., Al_2O_3), titanium oxide (e.g., TiO_2), yttrium oxide (e.g., Y_2O_3) and barium strontium titanate (BST) ...." (Yu, Ex.1048, 3:15-30.) Buffer interface 36 "can be a thin layer of oxide," e.g., "a layer of silicon oxide that is about 0.5 nm to about 0.7 nm thick." (Yu, Ex.1048, 4:58-61; *see also* Yu, Ex.1048, 3:62-63.)



Yu, Figure 1

B. Motivation to Combine

A POSITA would have been motivated to make the following two combinations of the teachings of Yu with Matsumoto. Yu and Matsumoto are in the same field as the ’076 patent, “a semiconductor device and a method for fabricating the semiconductor device.” (Ex.1001, 1:18-19; Matsumoto, Ex.1009, ¶2; Yu, Ex.1048, Abstract; Ex.1101, ¶244.)

1. First Combination

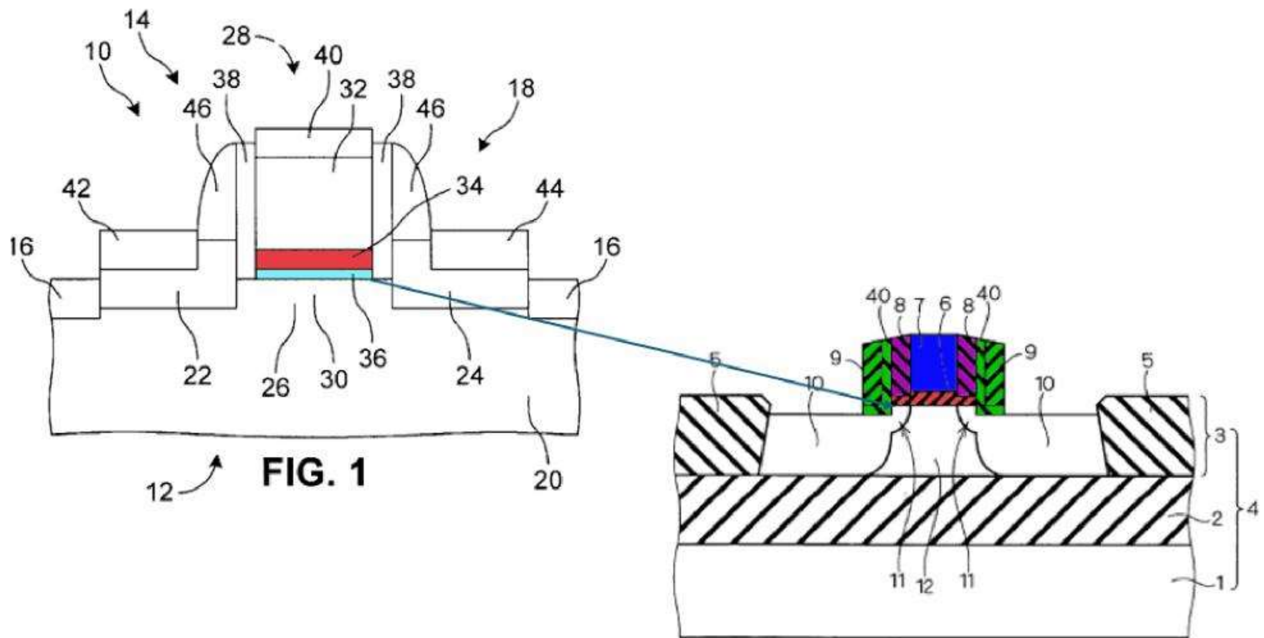
A POSITA would have been motivated to select a Hf-based oxide as the gate insulating film in Matsumoto's fourth embodiment device, as taught by Yu. (Ex.1101, ¶245)

Matsumoto discloses a list of exemplary films, including "a metal oxide film **such as** Al_2O_3 or a ferroelectric film such as Ta_2O_5 and BST," to use as its gate insulating film. (Matsumoto, Ex.1009, ¶107.) A POSITA would have understood these films to be high-k dielectrics. (*E.g.*, Wilk, Ex.1018, Table 1; Campbell, Ex.1338, 88-89.) In addition to "aluminum oxide (e.g., Al_2O_3)" and "barium strontium titanate (BST)" as identified in Matsumoto, Yu discloses a gate dielectric 34 comprising "hafnium oxide (e.g., HfO_2)," which is also a high-k film. (Yu, Ex.1048, 3:15-30; *see also* Wilk, Ex.1018, Table 1.) By 2005, a POSITA would have been motivated to select HfO_2 given its known benefits, discussed in §V.B.2. (Lee-2000, Ex.1337, 2.4.1; Houssa, Ex.1213, 207; Lee-1999, Ex.1349, 134; Ex.1101, ¶¶246-47)

2. Second Combination

A POSITA would have also been motivated to apply Yu's teaching of a buffer interface layer between a high-k gate dielectric and a substrate with Matsumoto's fourth embodiment device. (Ex.1101, ¶248.) For example, a POSITA would have been motivated to integrate Yu's buffer interface 36 (shaded aqua) between the

substrate and Matsumoto's high-k dielectric (shaded red) in the combined device, as illustrated below. (Ex.1101, ¶249.)



Yu, Figure 1 (left); Matsumoto, Figure 22 (right)

Yu motivates the combination, teaching buffer interface (a) "acts to reduce diffusion and/or penetration of atoms from the high-K dielectric material into the layer of semiconductor material 20 that could lead to a degradation in channel mobility" and (b) "retard[s] reaction of the high-K material with the layer of semiconductor material 20." (Yu, Ex.1048, 3:64-4:2; *see also* Yu, Ex.1048, 4:6567 ("buffer interface material layer 62 assists in reducing integration issues that may arise when attempting form a layer of high-K material on a semiconductor layer."); Ex.1101, ¶250.) Based on these explicit disclosures, a POSITA would have been motivated to use Yu's buffer interface to improve channel mobility and performance of the

combined device. (Ex.1101, ¶¶251-53; Matsumoto, Ex.1009, ¶13 (describing objective of Matsumoto to reduce malfunctions and operating characteristic variations).)

Moreover, the combination is nothing more than use of a known technique (Yu's buffer interface) to improve similar devices in the same way for the above reasons. *KSR*, 550 U.S. at 416-417; Ex.1101, ¶¶252-53. A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable because Yu discloses instructions on conventional techniques to create buffer layers between the high-k gate dielectric film and substrate. (Yu, Ex.1048, 4:61-65; Ex.1101, ¶¶252-53.)

C. Independent Claim 1

1. Preamble

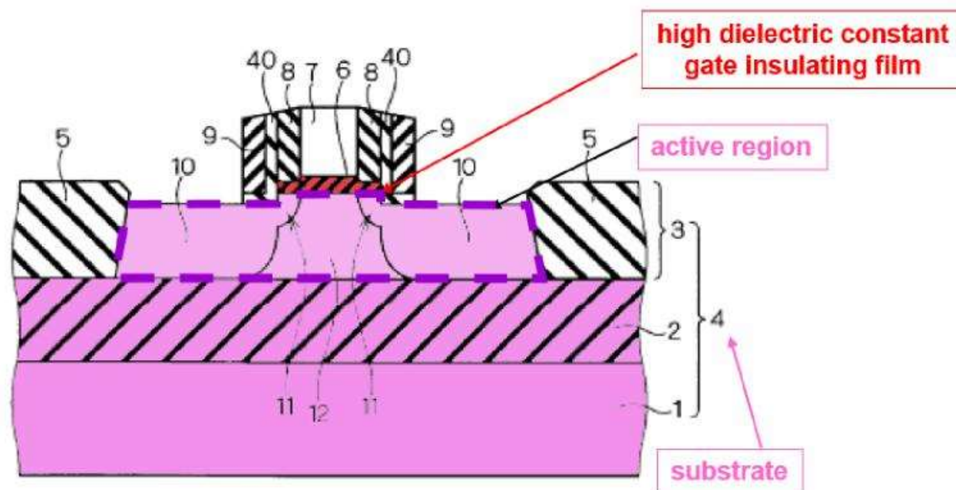
The Matsumoto-Yu combination discloses a "*semiconductor device*": "present invention relates to **a semiconductor device**." (Matsumoto, Ex.1009, ¶¶2, 137; *see also* Yu, Ex.1048, 1:7-11.)

2. Limitation 1[a]

The Matsumoto-Yu combination discloses "*a gate insulating film formed on an active region in a substrate and including Hf*" (Limitation 1[a]). (Ex.1101. ¶¶255-61.)

Matsumoto's fourth embodiment device includes "*a substrate*." (Ex.1101, ¶256.) The device has a multi-layer SOI **substrate** 4 (shaded pink) with silicon

substrate 1, BOX layer 2 and single-crystalline silicon layer 3. (Matsumoto, Ex.1009, ¶102, ¶¶137, 140 (relating fourth embodiment to first embodiment), Figure 22 (below)); *Google*, 2022 WL 4287797, *9 n.9 (applying same disclosure where "figures refer to corresponding features using the same reference numbers").[12])



Matsumoto, Figure 22

Isolating insulation film structures 5, "extend[ing] from the upper surface of the silicon layer 3 to the upper surface of the BOX layer 2," define a "**device region**." (Matsumoto, Ex.1009, ¶¶102-103, ¶¶137, 140.) The device region, identified by isolation regions, is an "*active region in a substrate*" and includes source/drain

[12] Although Matsumoto discloses several embodiments, many of the fabrication steps are discussed in relation to the first embodiment. (Ex.1101, ¶256; Matsumoto, ¶137.) Thus, Petitioner at times relies on disclosures from Matsumoto's first embodiment when discussing the fourth embodiment.

regions 10. (Matsumoto, Ex.1009, ¶139; Ex.1101, ¶257; *see* Ex.1001, 1:41-42 ("region of the well 102 surrounded by the STI serves as an active region of a substrate 101"), 7:28-45.)

Film 6 (shaded red) "is formed partially on the upper surface of the silicon layer 3" in the device region with gate electrode 7 "formed partially" thereon. (Matsumoto, Ex.1009, ¶¶103 (first embodiment), 137 (fourth embodiment "gate electrode 7 is formed by the process described in the first embodiment").) Film 6 is therefore a "*gate insulating film formed on an active region in a substrate*" (Limitation 1[a]). (Ex.1101, ¶¶259-60; *see* Matsumoto, Ex.1009, ¶103 (referring to film 6 as a "gate insulation film").)

The Matsumoto-Yu combination uses HfO_2 as the gate insulting film 6 in Matsumoto's device, as taught by Yu. (§IX.B.1; *see also* Matsumoto, Ex.1009, ¶107 (film 6 is a high-k film); Yu, Ex.1048, 3:15-30.) Accordingly, the Matsumoto-Yu combination discloses "*a gate insulating film ... including Hf*" (Limitation 1[a]). (Ex.1101, ¶261.)

3. Limitation 1[b]

The Matsumoto-Yu combination discloses "a gate electrode formed on the gate insulating film" (Limitation 1[b]). (Ex.1101, ¶¶262-63.) In Matsumoto's device, "gate electrode 7 [shaded blue] made of polysilicon is formed partially" on

film 6, which in the combination is HfO_2. (Matsumoto, Ex.1009, ¶¶103, 107 (describing formation of film 6 and gate electrode 7), 137-138, Figure 22 (below).)

Matsumoto, Figure 22

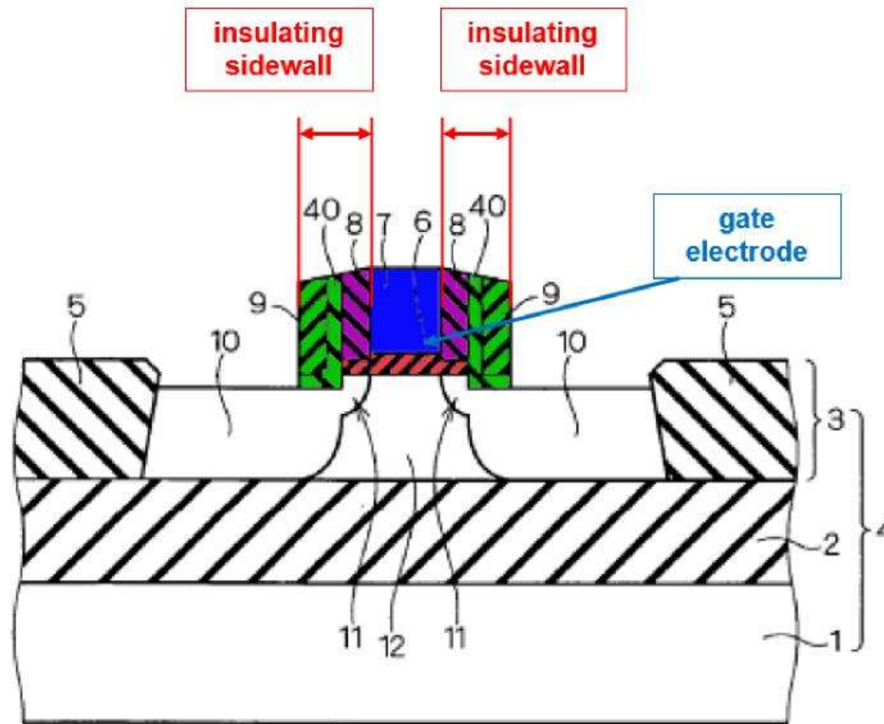
4. Limitation 1[c]

The Matsumoto-Yu combination discloses "*a insulating sidewall formed on each side surface of the gate electrode*" (Limitation 1[c]). (Ex.1101, ¶¶264-67.)

In Matsumoto's device, silicon oxide film 40 and silicon nitride film 9 are formed "on the outer side surfaces of" silicon oxide film 8. (Matsumoto, Ex.1009, ¶139, Figure 22 (below).) Matsumoto refers to film 9 as a "sidewall insulation film" but does not expressly refer to films 40 or 8 as a "sidewall." (Matsumoto, Ex.1009, ¶114 (describing nitride films 9a/9b "serving as **sidewall** insulation films").) A POSITA would have understood films 40 and 8 also to be sidewalls. (Matsumoto,

Ex.1009, ¶¶104, 110, 138 ("This forms the silicon oxide films 8 on the side surfaces of the gate electrode 7."), 139 ("This forms silicon oxide films 40 and the silicon nitride films 9 on the outer side surfaces of the silicon oxide films 8."), 40 ("the semiconductor device further includes a second sidewall formed on the side surface of the gate electrode, with the first sidewall therebetween"); Ex.1101, ¶¶266-67)

Because silicon oxide and silicon nitride are both insulators, film 8, film 40, and film 9 are collectively "*a insulating sidewall formed on each side surface of the gate electrode*" (Limitation 1[c]). (Matsumoto, Ex.1009, ¶¶110 (describing formation of silicon oxide films 8a/8b on the side surfaces of the gate electrodes), 114; Matsumoto, Ex.1009, claim 1 (referring to "insulation films" formed on side surfaces of gate electrode); Ex.1001, 2:60-65 (referring to multiple components collectively as an "insulating sidewall"); Ex.1101, ¶267.) Alternatively, film 8 alone is the claimed "*insulating sidewall*." (Ex.1101, ¶267; Ex.1001, 6:9.)

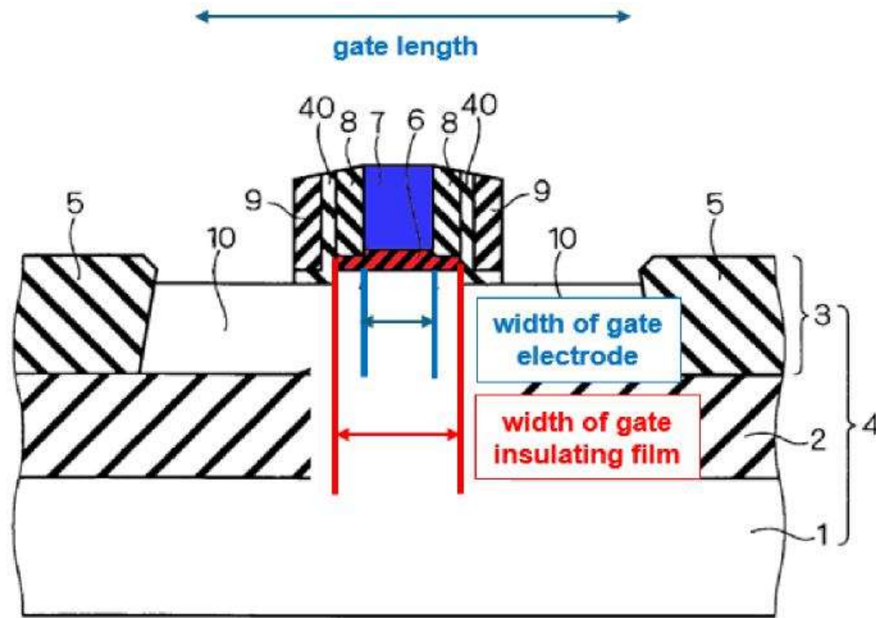


Matsumoto, Figure 22

5. Limitation 1[d]

The Matsumoto-Yu combination discloses "*a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length*" (Limitation 1[d]). (Ex.1101, ¶¶268-72.)

As illustrated in Matsumoto's Figure 22 below, the width of gate insulating film 6 (shaded red) along the gate length is larger than the width of gate electrode 7 (shaded blue). (Ex.1101, ¶269; *Unified*, 2022 WL 500391, *17.)



Matsumoto, Figure 22

Matsumoto's fabrication process confirms this arrangement of the gate electrode and gate insulating film. After formation of gate electrode 7, high-k dielectric film 13 extends beyond the gate electrode with a larger thickness under the gate electrode. (Matsumoto, Ex.1009, ¶¶137, 107-08, Figure 18 (top-left); Ex.1101, ¶269.) The etching process forming sidewall 8 (shaded purple) "overetch[es] the upper surface of the silicon layer 3" thereby leaving high-k dielectric film (shaded red) under the gate electrode and film 8. (Ex.1101, ¶271; Matsumoto, Ex.1009, ¶138, Figure 19 (top-right).) Film 40 and film 9 (shaded green) are then formed on the outer side surfaces of film 8 and in contact with the substrate. (Matsumoto, Ex.1009, ¶139; Figure 21 (bottom).)

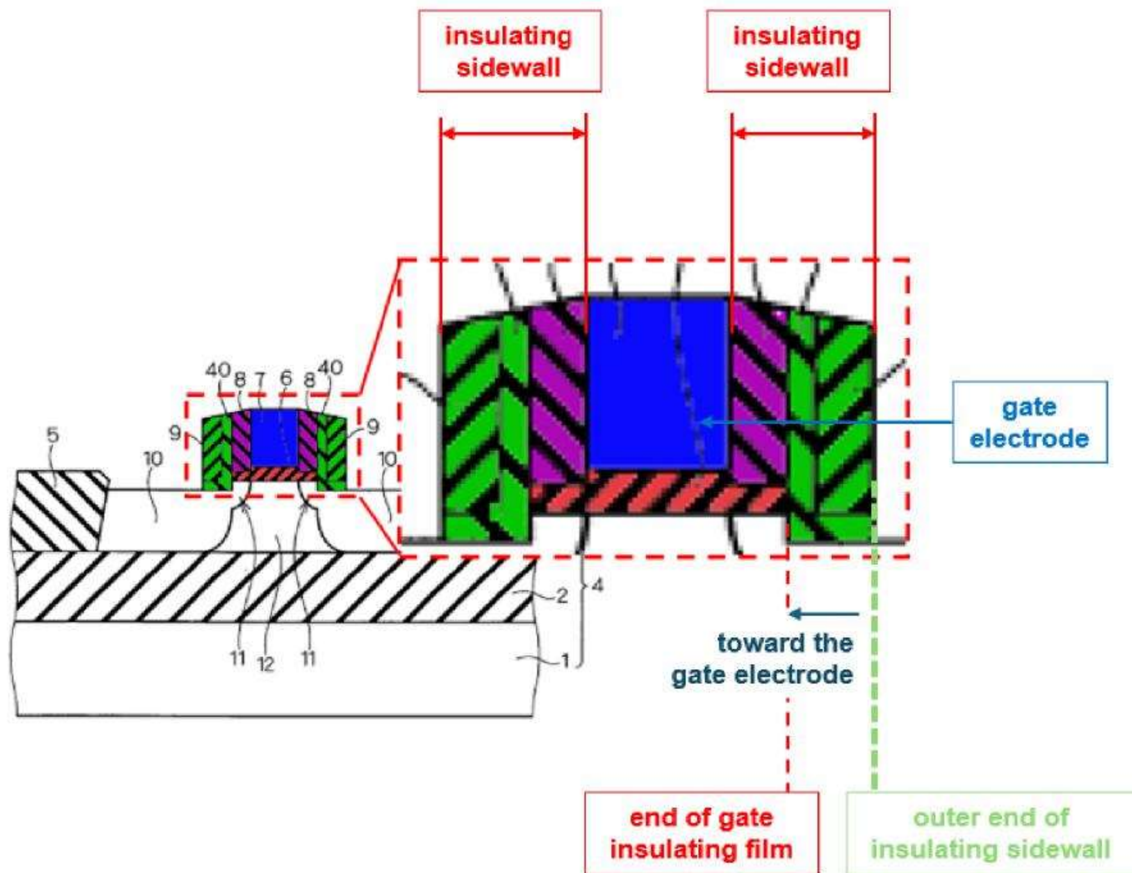
Matsumoto, Figures 18 (top-left), 19 (top-right), 21 (bottom)

6. Limitation 1[e]

The Matsumoto-Yu combination includes "*an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode*" (Limitation 1[e]). (Ex.1101, ¶¶273-74.)

Matsumoto's gate insulating film 6 (shaded red) is an uninterrupted layer that extends from under the gate electrode to under only film 8, which is part of the collective "*insulating sidewall*" (collectively films 8, 40, 9). (§IX.C.2.) The end of high-k gate insulating film 6 is perpendicular to the substrate's surface. As shown below, the end of gate insulating film 6 is disposed at a distance inward from the outer

end of sidewall 9 (outer end of the "*insulating sidewall*") toward the gate electrode. (Ex.1101, ¶274.) Thus, the end of the gate insulating film is "*retracted from an outer end of the insulating sidewall toward the gate electrode*" (Limitation 1[e]). (Ex.1101, ¶274; *Unified*, 2022 WL 500391, *17.)



Matsumoto, Figure 22 with enlargement

D. Claim 2

As discussed in § IX.B.2, the Matsumoto-Yu device includes Yu's buffer interface 36, which "can be a layer of **silicon oxide** ... ," between the high-k dielectric ("gate insulating film") and the substrate. (Yu, Ex.1048, 4:58-61, 3:62¬63; Ex.1101,

¶275.) The Matsumoto-Yu combination discloses "a buffer insulating film [buffer interface 36] formed of a silicon oxide film and provided between the substrate and the gate insulating film [high-k dielectric]" [2].

E. Claim 3

The Matsumoto-Yu combination discloses "*the gate insulating film is formed of a Hf based oxide*" [3]. (Ex.1101, ¶276.) As discussed in §IX.C.2, the Matsumoto-Yu combination uses a Hf-based oxide as the gate insulating film in Matsumoto's device, as taught by Yu. (Yu, Ex.1048, 3:15-30 (identifying "hafnium oxide (e.g., HfO_2)" as example material for gate dielectric 34).)

F. Claim 7

The Matsumoto-Yu combination discloses "*an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall*" [7]. (Ex.1101, ¶277.) As discussed in §IX.C.5, film 6 (shaded red) extends (protrudes) from under the gate electrode 7 to under sidewall 8 (part of the collective "*insulating sidewall*" comprising films 8, 40, and 9). (Ex.1101, ¶277.)

Matsumoto, Figure 22 with enlargement

G. Claim 8

Matsumoto discloses a modification of the fourth embodiment that omits layer 40. In this modification, illustrated in Figure 23 below, "silicon nitride films 9 are formed directly on the upper surface of the silicon layer 3." (Matsumoto, Ex.1009, ¶141.) Matsumoto motivates this modification stating it "is applicable to any one of the first to fourth preferred embodiments" and therefore the analysis of the fourth embodiment in §§ IX.C.1-6 applies equally. *See Boston Sci.*, 554 F. 3d at 991. Thus, Matsumoto's fourth embodiment modification meets each limitation of claim 1 and the combination further discloses "*the insulating sidewall* [collective structure of

silicon oxide film 8 and silicon nitride film 9] *has a double layer structure including an oxide film and a nitride film*" [8]. (Ex.1101, ¶¶278-80.)

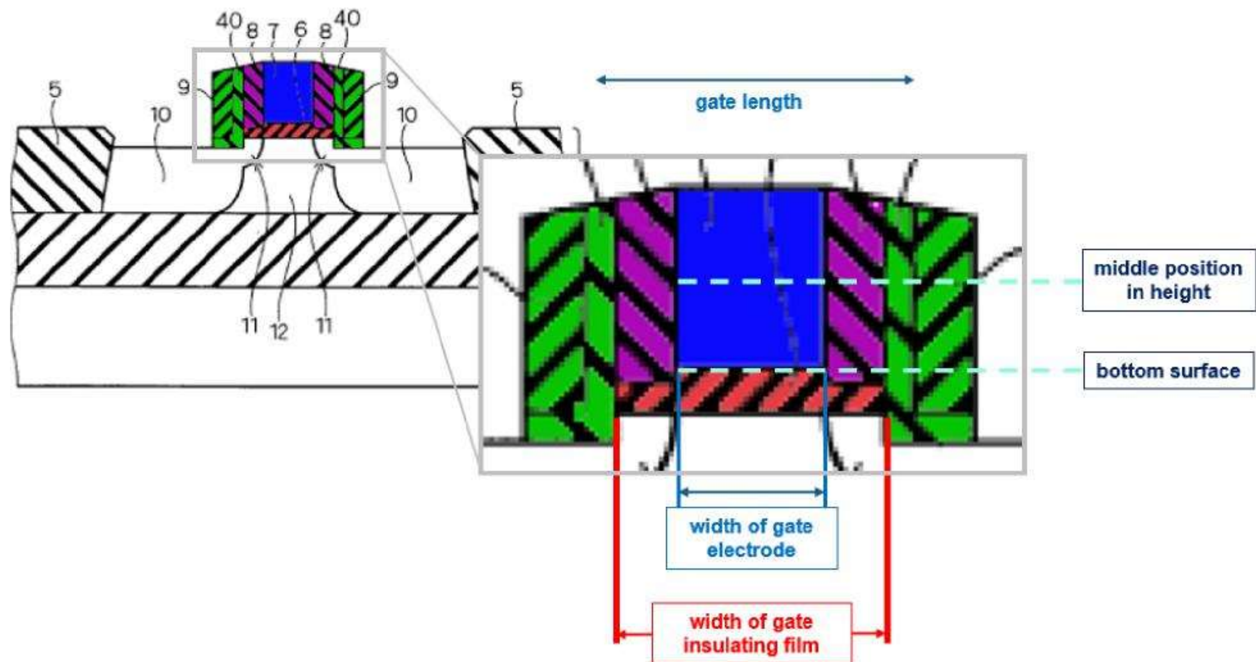
Matsumoto, Figure 23 with enlargement

H. Claims 10 and 13

The Matsumoto-Yu combination discloses "*a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length*" [10] and "*the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length*" [13]. (Ex.1101, ¶¶281-83.)

As illustrated below, the width of Matsumoto's gate electrode 7 is constant across its entire height. Therefore, for the reasons discussed in § IX.C.5, the width of the gate insulating film 6 (shaded red), including at film 6's bottom surface, is larger than the width of gate electrode 7 (shaded blue) at both the bottom surface and

a middle position in height of the gate electrode. (Ex.1101, ¶¶281-83; *Unified*, 2022 WL 500391, *17.)



Matsumoto, Figure 22 with enlargement

X. Ground VI: Matsumoto-Yu-Sim Combination Renders Claim 6 Obvious

The Matsumoto-Yu combination discloses every limitation of claim 1 but does not explicitly disclose "a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less" [6]. As discussed in §VI, Sim discloses this teaching, such that the combined device of Matsumoto, Yu, and Sim renders claim 6 obvious. (Ex.1101, ¶¶284-89.) Sim, Matsumoto, and Yu are in the same field as the '076 patent, "a semiconductor device and a method for fabricating

the semiconductor device." (Ex.1001, 1:18-19; Matsumoto, Ex.1009, ¶2; Sim, Ex.1024, Abstract; Yu, Ex.1048, Abstract; Ex.1101, ¶285.)

Although neither Matsumoto nor Yu specifically discloses a HfO_2 film that is less than 2 nm thick, a POSITA would have been motivated to use a thickness of 2 nm or less in the combined device, as taught by Sim. The resulting device of the combination includes a high-k gate dielectric having "*a thickness of 2 nm or less.*" (Ex.1101, ¶286.)

A POSITA would have been motivated to make the above combination because Sim expressly motivates the combination, as discussed in §VI. (Ex.1101, ¶¶287-89.) A POSITA would understand the improvements described by Sim align with Matsumoto's goal of providing "a semiconductor device which achieves reductions in malfunctions and operating characteristic variations." (Matsumoto, Ex.1009, ¶13.)

Additionally, the combination is nothing more than use of a known technique (Sim's HfO_2 dielectric layer with less than 20Å thickness) to improve similar devices (combined device of Matsumoto and Yu with HfO_2 gate insulating film) in the same way (forming a high-k gate insulating film, with a smaller thickness) for the above reasons. *KSR*, 550 U.S. at 416-417; Ex.1101, ¶289. A POSITA would have had a reasonable expectation of success in the combination and the results of the

combination would have been predictable because Sim uses a well-known process (ALD) for fabricating high-k films. (Sim, Ex.1024, 218; Ex.1101, ¶289.)

XI. Ground VII: Matsumoto-Koyama Combination Renders Claim 1 Obvious

As discussed in §IX.C, Matsumoto discloses each limitation of claim 1, but does not expressly disclose "*a gate insulating film ... including Hf*" (Limitation 1[a]). (Ex.1101, ¶291.) This limitation is disclosed by Koyama. Koyama and Matsumoto are in the same field as the '076 patent, "a semiconductor device and a method for fabricating the semiconductor device." (Ex.1001, 1:18-19; Matsumoto, Ex.1009, ¶2; Sim, Ex.1024, Abstract; Koyama, Ex.1029, Title; Ex.1101, ¶291.)

A. Motivation to Combine

A POSITA would have been motivated to combine Koyama's use of HfSiON as a gate insulating film with Matsumoto's fourth embodiment device. (Ex.1101, ¶¶293-95.) As discussed in §IX.B.2, Matsumoto discloses a list of exemplary high-k films which can be used as a gate dielectric. (Matsumoto, Ex.1009, ¶107.) A POSITA would have been motivated to investigate other high-k options, including hafnium-based materials, and would have been led to Koyama's study of HfSiON. (Ex.1101, ¶293) A POSITA would have been motivated to make the above combination to achieve the enhanced benefits of HfSiON high-k film, e.g., improved thermal stability and electrical characteristics, described by Koyama. (Ex.1101, ¶295.)

Moreover, the combination is nothing more than use of a known technique (Koyama's use of HfSiON as a gate insulating film) to improve similar devices in the same way. *KSR*, 550 U.S. at 416-417; Ex.1101, ¶295. A POSITA would have had a reasonable expectation of success and the combination would have yielded predictable results. (Ex.1101, ¶295.)

B. Independent Claim 1

In the combination of Matsumoto's fourth embodiment and Koyama, Matsumoto's gate insulating film 6 comprises HfSiON, as taught by Koyama. (Ex.1101, ¶294.) Koyama described that as early as 2002, "Hf(Zr) silicates are considered to be prospective high-K materials due to their modest dielectric constants and good interface properties." (Koyama, Ex.1029, 849.) Proposing to use a "HfSiON gate dielectric with excellent thermal stability," Koyama compared "the effects of nitrogen on the improved thermal stability and electrical characteristics of this dielectric." (Koyama, Ex.1029, 849.) Koyama concluded that "nitrogen [in HfSiON] enhances the dielectric constant of silicates" and "boron penetration is substantially suppressed in the HfSiON during high temperature annealing." (Koyama, Ex.1029, 849.) These results "strongly suggest that HfSiON is the most probable material for first generation high-K gate dielectrics." (Koyama, Ex.1029, 850.) Thus, the combination discloses "*a gate insulating film ... including Hf*"

(Limitation 1[a]). For this reason and the reasons discussed in §§IX.C, XI.A, the combination of Matsumoto-Koyama renders obvious claim 1. (*Id.*)

XII. Ground VIII: Matsumoto-Ono Combination Renders Claims 1 and 11-12 Obvious

A. Overview

Ono's[13] second embodiment FET includes a gate stack comprising gate insulator film 5 "made of a metal oxide" and gate insulator film 11 "made of a metal

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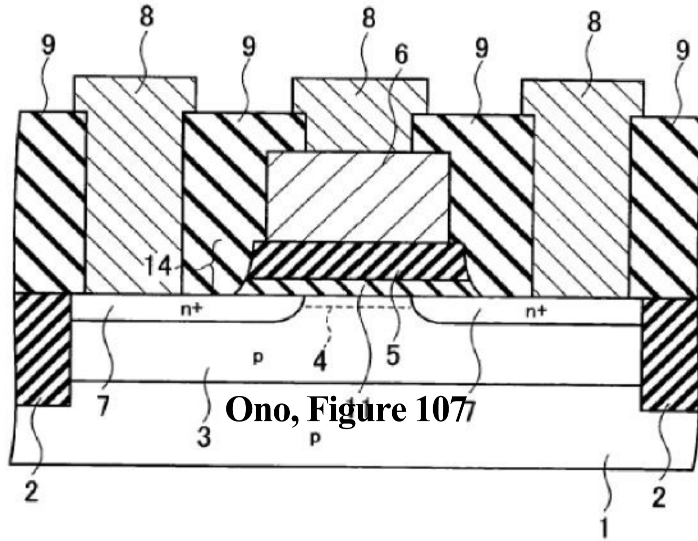
[13] None of the ground references was applied by the Examiner during prosecution of the '764 patent. Applicant cited JP-Ono on an information disclosure statement ("IDS"). However, JP-Ono has no familial relationship to Ono, is not a foreign counterpart to JP-Ono, does not have the same specification as Ono, and was filed by different inventors than Ono. *See* Ex.1340, cover ("Ono Tamashiro"); *compare* Ono, Ex.1013, cover ("Mizuki Ono"). JP-Ono was not applied by the Examiner and thus was not evaluated during examination. Significantly, Applicant supplied JP-Ono with its IDS in the Japanese language with only an English language abstract. *See* Ex.1112. Even assuming JP-Ono was evaluated by the Examiner, which the record does not support, the Examiner erred in allowing the claims over JP-Ono and by failing to recognize its teachings relating to the side end of the gate insulating film, which is understandable in view of the limited English language content of JP-Ono submitted by the Applicant.

oxide with a higher dielectric constant than the gate insulator film 5." (Ono, Ex.1013, ¶207, Figure 77.) Gate insulator film 5 is made of a "HfO_2 film." (Ono, Ex.1013, ¶209.) Gate electrode 6 is formed on gate insulator film 5 and can have gate sidewalls. (Ono, Ex.1013, ¶¶207, 181, 210, Figure 77.) Ono and Matsumoto are in the same field as the '076 patent, "a semiconductor device and a method for fabricating the semiconductor device." (Ex.1001, 1:18-19; Matsumoto, Ex.1009, ¶2; Ono, Ex.1013, Abstract, ¶¶3-7; Ex.1101, ¶298.)

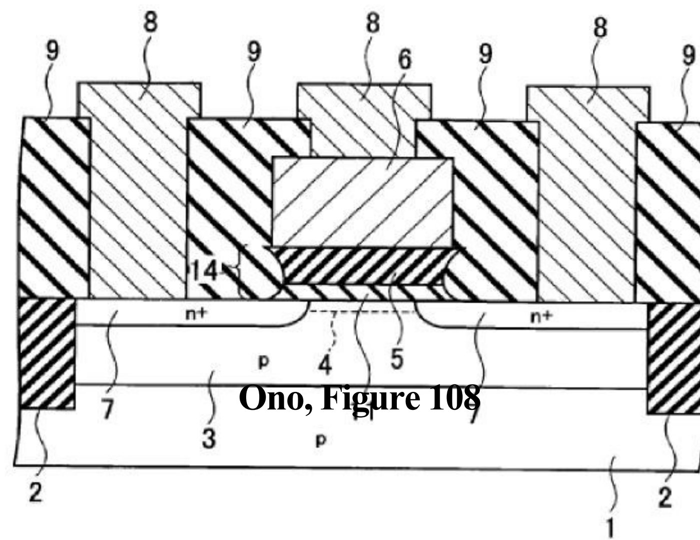
Ono, Figure 77

Ono discloses a modification of its second embodiment devices where the sidewalls of this two-layered structure "may curve." (Ono, Ex.1013, ¶216.) Ono discloses numerous examples of such curved end portions (Figures 104-123). (Ono,

Ex.1013, ¶200.) Petitioner focuses its analysis on the structure depicted in Figures 107 and 108 (reproduced below), although other structures are equally applicable.



Ono, Figure 107

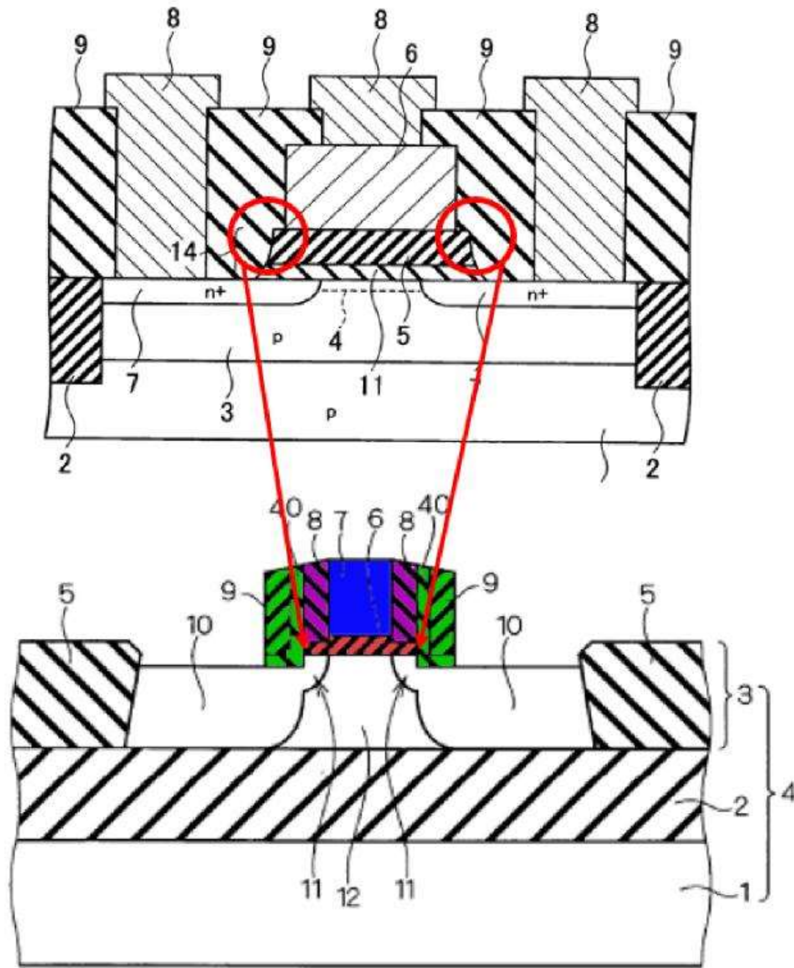


Ono, Figure 108

B. Motivation to Combine

A POSITA would have been motivated to combine the teachings of Matsumoto and Ono. First, a POSITA would have been motivated to select a Hf-based oxide as the gate insulating film in Matsumoto's device, as taught by Ono. (Ex.1101, ¶298; Ono, Ex.1013, ¶209 (describing use of a "HfO_2 film").) As discussed in §V.B.2, a POSITA would have been motivated to select HfO_2 given its known benefits. (Lee-2000, Ex.1337, 2.4.1; Houssa, Ex.1213, 207; Lee-1999, Ex.1349, 134; Ex.1101, ¶298.)

Second, a POSITA would have also been motivated to apply Ono's teaching of curving the end portion of a gate insulating film to Matsumoto's device, as illustrated below. (Ex.1101, ¶299.)



Ono, Figure 107 (top); Matsumoto, Figure 22 (bottom)

Ono expressly suggests the combination, teaching that using its curved side surfaces provides "an advantage of possible optimization ... by reducing the scattering of carriers as well as enhancing the controllability of the gate electrode with respect to the potential of the channel region." (Ono, Ex.1013, ¶216; *see also* Ono, Ex.1013, ¶200 (noting, for another embodiment, by using curved side surfaces, "the electrical capacitance between the gate electrode 6 and the source/drain regions 7 may be adjusted," resulting in "an advantage of optimization"). Ono's curved

sidewall approach therefore provides optimization—reducing carrier scattering while enhancing control of the gate electrode over the channel. (Ex.1101, ¶¶300-04; Ono, Ex.1013, ¶206.) A POSITA would have been further motivated to curve the end of Matsumoto's gate insulating film to optimize parasitic resistance and parasitic capacitance, improving device performance. (Ex.1101, ¶300 Ex.1340, ¶108; §IV.B.2.)

The Matsumoto-Ono combination is merely the application of a known technique (Ono's curved film ends) to improve similar devices in the same way (modifying the dielectric layer to control capacitance) for the above reasons. *KSR*, 550 U.S. at 416-17; Ex.1101, ¶304. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable. (Ex.1101, ¶304) Matsumoto and Ono both use high-k gate insulating films that extend under the gate electrode and the insulating sidewall, a concept well-known before the '076 patent. (§§IV.B.2.b, IV.D.2, IX.A, XII.A.) And both form their high-k dielectrics using conventional techniques. (Matsumoto, Ex.1009, ¶114; Ono, Ex.1013, ¶167; Ex.1101, ¶304.)

C. Independent Claim 1

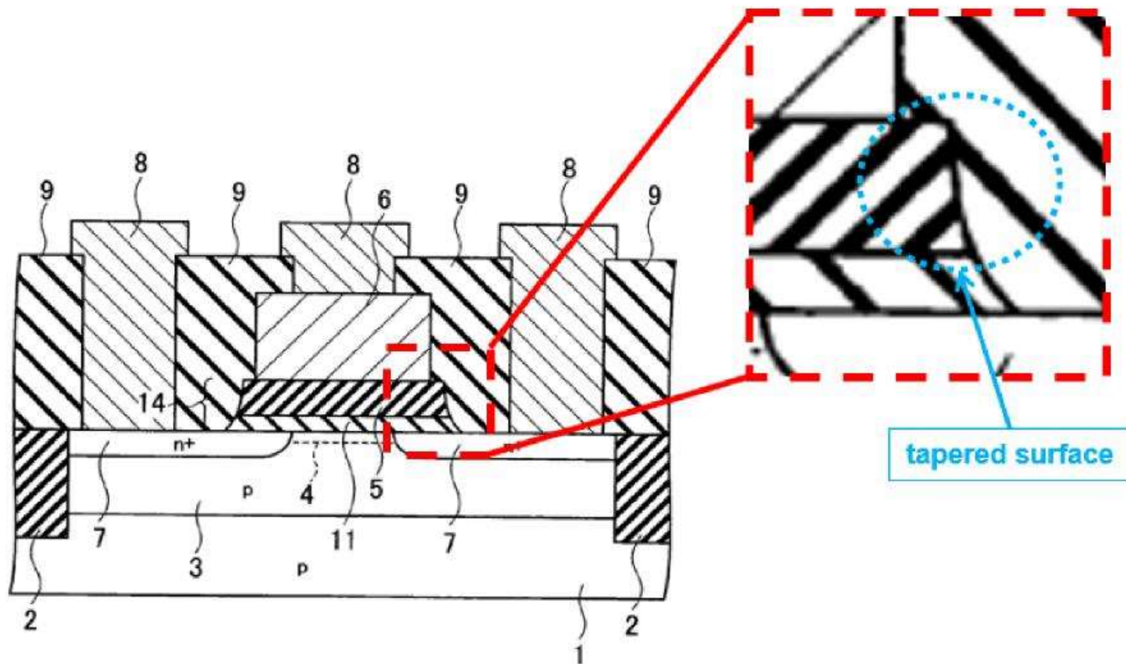
For the reasons discussed in §IX.C, Matsumoto discloses each limitation of claim 1, except it does not expressly disclose "*a gate insulating film ... including Hf*" (Limitation 1[a]). (Ex.1101, ¶305.) In the combination, Matsumoto's gate insulating

film 6 comprises HfO_2, as taught by Ono. (Ex.1101, ¶305; Ono, Ex.1013, ¶200.) Accordingly, the Matsumoto-Ono combination renders obvious claim 1. (Ex.1101, ¶305.)

D. Claims 11-12

The Matsumoto-Ono combination discloses "*the end of the gate insulating film located under the insulating sidewall has a tapered surface*" [11] and "*the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof*" [12]. (Ex.1101, ¶¶306-08.)

As discussed above, the Matsumoto-Ono combination includes a gate insulating film with curved ends under the "insulating sidewall." As shown below in the exemplary shape of Ono Figure 107, the curved shape, when used with Matsumoto's gate insulating film, has a thickness that decreases toward the end of the gate insulating film—i.e., it tapers like the end surface of the gate insulating film in the '076 patent's Figure 7. (Ex.1101, ¶308; §IV.C.)



Ono, Figure 107 with enlargement

XIII. MANDATORY NOTICES

A. Real Party-in-Interest (37 C.F.R. §42.8(b)(1))

United Microelectronics Corporation and UMC Group (USA) are the real parties-in-interest.

B. Related Matters (37 C.F.R. §42.8(b)(2))

The ’076 patent is the subject of the following active proceedings:

- *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation*, Civil Action No. 2:24-cv-00730 in the Eastern District of Texas (Lead Case), filed September 6, 2024;
- *Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Manufacturing Company Limited*, Civil Action No. 2:24-cv-00623 in the

Eastern District of Texas (Consolidated Member Case), filed August 1, 2024; and

- *Taiwan Semiconductor Manufacturing Company, Ltd. v. Advanced Integrated Circuit Process LLC*, IPR2025-00831 in the U.S. Patent and Trademark Office, Patent Trial and Appeal Board, filed April 15, 2025.

C. Lead and Back-up Counsel (37 C.F.R. §42.8(b)(3))

Lead Counsel	Back-up Counsel
Tim Tingkang Xia (No. 45,242) Tim.Xia@troutman.com TROUTMAN PEPPER LOCKE LLP 600 Peachtree Street, NE, Suite 3000 Atlanta, GA 30308 Telephone: (404) 870-4698	Emma A. Bennett (No. 80,631) Emma.Bennett@troutman.com TROUTMAN PEPPER LOCKE LLP 600 Travis Street, Suite 2800 Houston, TX 77002 Telephone: (713) 226-1549

D. Service Information (37 C.F.R. §42.8(b)(4))

Service information is provided in the designation of counsel above. Petitioner consents to electronic service by email to Tim.Xia@troutman.com and Emma.Bennett@troutman.com.

E. Payment of Fees (37 C.F.R. §42.103)

The Office is authorized to charge the fee set forth in 37 C.F.R. §42.15(a)(1) for this Petition to Deposit Account No. DA201507. Review of ten claims is requested. The undersigned further authorizes payment for any additional fees that may be due in connection with this Petition.

XIV. CONCLUSION

For the reasons set forth above, *Inter Partes* Review of the Challenged Claims of the ’076 patent is respectfully requested.

Respectfully submitted,

Date: June 6, 2025

/s/Tim Tingkang Xia
Tim Tingkang Xia (Lead Counsel)
Registration No. 45,242

Counsel for Petitioner

CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that this Petition complies with the type-volume limits of 37 C.F.R. § 42.24(a)(1)(i) because it contains 11,865 words, according to the word-processing system used to prepare this Petition, excluding the parts of this Petition that are exempted by 37 C.F.R. § 42.24(a)(1) (table of contents, table of authorities, mandatory notices under § 42.8, certificate of service, certificate of word count, or appendix of exhibits or claim listing).

Date: June 6, 2025

/s/Tim Tingkang Xia
Tim Tingkang Xia (Lead Counsel)
Registration No. 45,242
Counsel for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), this is to certify that on this 6th day of June 2025, I caused to be served on a USB thumb drive a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,587,076 Under 35 U.S.C. §§ 311, 312 and 37 C.F.R. § 42.104 (with Exhibits 1001-1002, 1009, 1013, 1018, 1024, 1027-1029, 1048, 1101-1112, 1211-1216, 1223, 1226-1227, 1229, 1305, 1308, 1323, 1326, 1337-1338, 1340, 1349, 1406, 1413, 1419, 1429-1435, 1506, 1512, 1515-1529, & 1531-1532) via Federal Express Priority Overnight at the Correspondence Address for Patent Owner:

27197 - MICHAEL J. CHERSKOV
SZYMON M. GURDA
903 COMMERCE DR
SUITE 310
OAK BROOK, IL 60523
UNITED STATES

Courtesy copies of the same have been concurrently served via email on Patent Owner's litigation counsel at:

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Tim Tingkang Xia (Lead Counsel)
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Counsel for Petitioner

Appendix: Challenged Claims Listing

1. **Preamble:** A semiconductor device comprising:

1[a]: a gate insulating film formed on an active region in a substrate and including Hf;

1[b]: a gate electrode formed on the gate insulating film;

1[c]: a insulating sidewall formed on each side surface of the gate electrode; and

1[d]: wherein a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length, and

1[e]: an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode.

2: The semiconductor device of claim 1, further comprising a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film.

3. The semiconductor device of claim 1, wherein the gate insulating film is formed of a Hf based oxide.

6. The semiconductor device of claim 1, wherein a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.

7. The semiconductor device of claim 1, wherein an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall.

8. The semiconductor device of claim 1, wherein the insulating sidewall has a double layer structure including an oxide film and a nitride film.

10. The semiconductor device of claim 1, wherein a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length.

11. The semiconductor device of claim 1, wherein the end of the gate insulating film located under the insulating sidewall has a tapered surface.

12. The semiconductor device of claim 1, wherein the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof

13. The semiconductor device of claim 1, wherein the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length.