A 90-nm Logic Technology Featuring Strained-Silicon

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***Abstract*—A leading-edge 90-nm technology with 1.2-nm physical gate oxide, 45-nm gate length, strained silicon, NiSi, seven layers of Cu interconnects, and low-κ CDO for high-performance dense logic is presented. Strained silicon is used to increase saturated n-type and p-type metal–oxide–semiconductor field-effect transistors (MOSFETs) drive currents by 10% and 25%, respectively. Using selective epitaxial $Si_{1-x}Ge_x$ in the source and drain regions, longitudinal *uniaxial* compressive stress is introduced into the p-type MOSEFT to increase hole mobility by $> 50\%$. A tensile silicon nitride-capping layer is used to introduce tensile strain into the n-type MOSFET and enhance electron mobility by 20%. Unlike all past strained-Si work, the hole mobility enhancement in this paper is present at large vertical electric fields in nanoscale transistors making this strain technique useful for advanced logic technologies. Furthermore, using piezoresistance coefficients it is shown that significantly less strain $(\sim 5\ \times)$ is needed for a given PMOS mobility enhancement when applied via longitudinal uniaxial compression versus in-plane biaxial tension using the conventional $Si_{1-x}Ge_x$ substrate approach.**

***Index Terms*—CMOS, metal–oxide–semiconductor field-effect transistors (MOSFETs), strained-silicon, very large scale integration (VLSI).**

I. Introduction

RAPID SCALING of MOSFETs drives increasing microprocessors performance and rapid growth of the information technology revolution. The underlying principle behind the revolution is Moore's law. In 1965, Gordon Moore observed that the number of transistors in a chip increased exponentially over time [1]–[3]. Moore's law is possible because the transistor size decreases exponentially over time. When Moore made his prediction in 1965, transistor size was 100 μm. During the last three decades, Moore's prediction has held as transistor size exponentially decreased from micrometers to submicrometers and then to deep submicrometers. Presently, with the introduction of 90-nm CMOS logic technologies and 45-nm transistors in 2003 [4]–[6], Moore's law is found to still be valid in the nanotechnology era. Fig. 1 shows the historical feature size reduction during the past three decades and the start of the nanotechnology era for the microelectronic industry as feature size moves from deep submicrometer to nanometer scale.

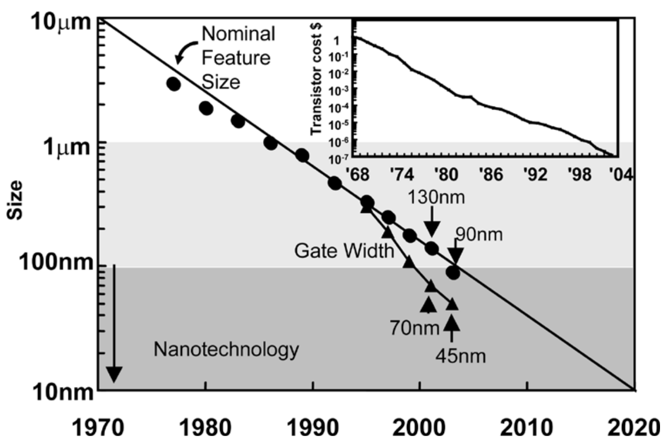

Fig. 1. Technology and transistor features size and transistor cost versus year.

Moore pointed out that reduced cost per function is the driving force behind the exponential increase in transistor density. It is this exponential reduction in cost per function that drives microprocessor performance and growth of the information technology and semiconductor industry. Fig. 1 shows the dramatic decrease in cost per transistor during the last three decades. In 1965 when Moore made his prediction, a transistor cost \$1. In 2003, with the start of the nanotechnology era, transistors are basically free costing less than $\$10^{-6}$. According to Moore, "no exponential is for ever" [3], but Moore's law will continue well into the next decade as long as the net cost per function continues to drop.

In this paper, we describe the transistor structure used in a 90-nm generation CMOS logic technology designed for high speed and low power operation. Section II describes the uniaxial stressed Si process flow used in this work. Section III presents transistor electrical data and reviews the current strained Si literature to understand why longitudinal uniaxial compressive stress offers large hole mobility enhancement at low strain and large vertical electric fields.

II. Strained-Silicon Process Flow

Strained-Si using a novel low-cost flow is introduced for the first time. Unlike the traditional approach where strain is applied into the channel from the bottom using strained-Si on relaxed $Si_{1-x}Ge_x$ [8]–[24], in this paper, strain is introduced from

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the side using $Si_{1-x}Ge_x$ in the pMOSFETs and a silicon nitride-capping film for the nMOSFET. Transmission electron microscopy (TEM) micrographs of 45-nm p- and nMOSFET are shown in Fig. 2 which are patterned with 193-nm lithography.

Only slight modifications to a standard CMOS logic technology process flow are needed to insert the compressive stress into the p-type and a combined longitudinal tensile and out-of-plane compressive stress into the nMOSFETs. An Si recess etch is inserted post spacer formation and followed by selective epitaxial chemical vapor deposition (CVD) of $Si_{1-x}Ge_x$. The process flow steps are shown in Fig. 3. In this paper 17% germanium concentration is used which has a lattice spacing $\sim 1\%$ larger than Si. The mismatch in the $Si_{1-x}Ge_x$ to Si lattice causes the smaller lattice constant Si channel to be under compressive stress. Longitudinal uniaxial tensile and out-of-plane compressive stress is introduced into the nMOSFET by engineering the stress and thickness of the Si nitride-capping layer [25], [26]. There are several techniques to nearly completely neutralize the capping layer strain on the p-type MOSFETs, one is the use of a Ge implant and masking layer [26]. Another technique to relax the strain is to selectively remove the capping from the p-type transistors which is not implemented here. All device data shown to date on this flow [4]–[6] and in this paper is for a fully integrated process flow (i.e., includes the capping layer on the p-type MOSFETs with negligible performance degradation). Thus, for the first time, a process flow has been developed that allows the strain to be targeted independently for n and p-type MOSFETs (by adjusting capping films stress for n-type and Ge source/drain concentration for p-type). The unique advantage of this uniaxial stress Si process flow is that on the same wafer compressive stress is introduced into the p-type and tensile stress in the nMOSFETs to improve *both* the electron and hole mobility. Since the nitride capping layer is already present to support unlanded contacts, only a few new process steps are introduced at less than a 2% wafer cost increase. Furthermore, by confining the $Si_{1-x}Ge_x$ to the source and drain and introducing it late in the process flow, integration challenges are reduced.

Typical integration issues for strained-Si are misfit dislocations, yield and increased self heating due to the low thermal conductivity of $Si_{1-x}Ge_x$. Since the $Si_{1-x}Ge_x$ is confined to the neutral part of the junction, no additional device leakage is observed even in the presence of misfit dislocations. With the selective $Si_{1-x}Ge_x$ process step, equivalent defect density to past technologies at mature yield levels has been obtained [6]. Lastly, since the $Si_{1-x}Ge_x$ is located only in the source/drain versus the entire substrate, the MOSFET self-heating for this structure (unlike biaxial strain) [18] is unchanged.

The use of $Si_{1-x}Ge_x$ in the source and drain area for the purpose of higher boron activation and abrupt profile was first proposed by Gannavaram *et al.* [27], however, for small devices the near completely biaxial strained-SiGe in the source and drain (if not completely strained due to the lack of misfits in Fig. 2) creates significant uniaxial compression in the channel as confirmed by three–dimensional (3-D) finite element analysis and shown in Fig. 4. The magnitude of stress in the <110> direction is plotted in MPa and the resulting stress as confirmed by finite element simulations is dominantly along the <110> direction.

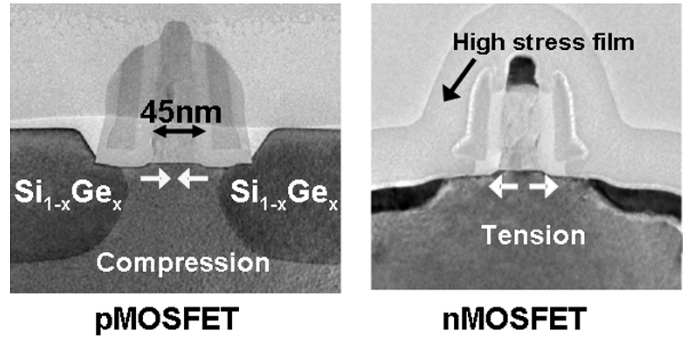

Fig. 2. TEM micrographs of 45-nm p-type and n-channel transistors [4].

For the 45-nm gate length transistor the channel longitudinal stress is ~ 600MPa. Strain can be engineered at other process steps like shallow trench isolation and silicide [28]. In this paper, the strain from other process steps is intentionally maintained to be small compared to the $Si_{1-x}Ge_x$ and tensile capping layer stress.

III. Strained Silicon Transistors

A. History

For more than 30 years, CMOS device technologies have been improving at a dramatic rate. A large part of the success of the MOSFET is due to the fact that it can be scaled to increasingly smaller dimensions, which results in higher performance. In the past 30 years, the MOSFET gate length has scaled from 10 μm to 45 nm. The ability to consistently improve performance while decreasing power consumption has made CMOS architecture the dominant technology for integrated circuits. Surprisingly, the MOSFET has undergone relatively few structure changes in the past 30 years. Fig. 5 shows the evolution of the MOSFET structure for Intel's logic technologies. Key structural changes during the last 30 years were the following: 1) Al metal to poly-Si gate in the 1970s; 2) addition of spacer, lightly doped drain (LDD) and self-aligned Ti or Co silicide in 1980s; and 3) Nickel silicide and uniaxial stressed Si at the 90-nm technology node in 2003 [4]–[6] Going forward, uniaxial stress is expected to be present for several technology generations.

B. Biaxial and Uniaxial Strained-Silicon

Mechanical stress to strain a semiconductor lattice is a well known effect that has found many applications in sensors. Two types of mechanical stress have received much focus for integration into a CMOS technology: uniaxial [25], [26], [29] and biaxial [8]–[24]. However, until now [4], neither approach has been widely adopted into a CMOS flow for improved net transistor performance. In this paper, we 1) review the history of biaxial and uniaxial stressed Si MOSFETs and 2) describe the uniaxial stressed Si incorporated into a 90-nm logic technology.

The majority of the strained-Si work to date in the literature has focused on biaxial tensile stress introduced using a thick relaxed $Si_{1-x}Ge_x$ substrate since this approach can potentially introduce advantageous strain for both n- and pMOSFETs [19], [21]. Biaxial strain using $Si_{1-x}Ge_x$ has received much focus in recent years [18], [23] but has yet to be introduced into a

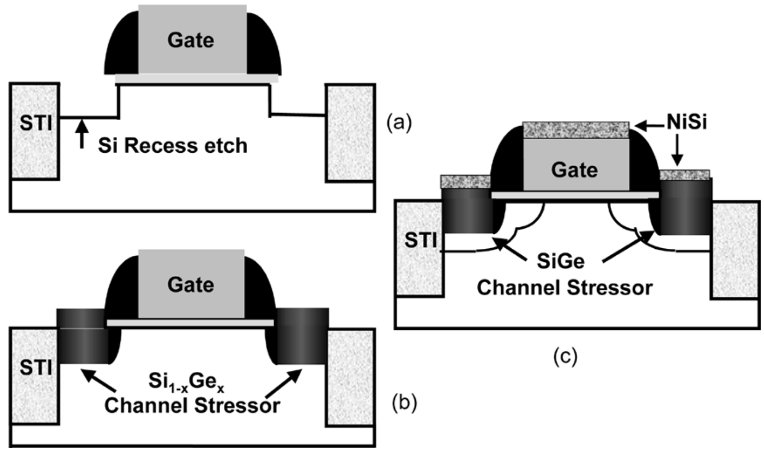

Fig. 3. Novel uniaxial strained-Si process flow use in this paper.

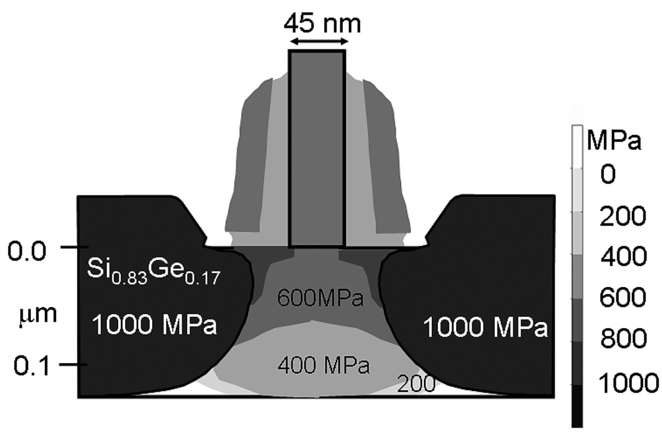

Fig. 4. Stress simulations for SiGe source/drain structure and gate length of 45 nm. Dominate stress is uniaxial along the direction of current flow. Contours of stress in MPa.

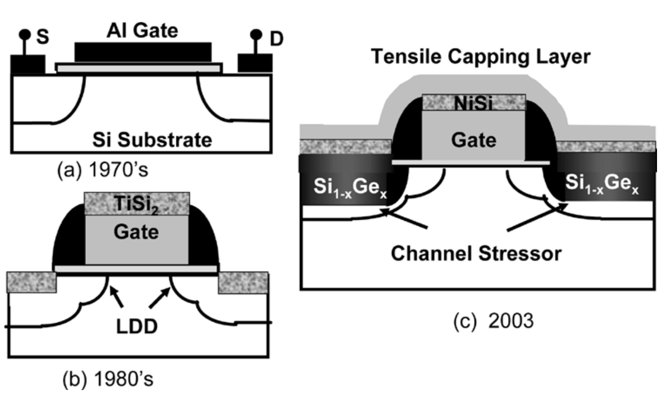

Fig. 5. Key MOSFET structure changes in the past 30 years.

CMOS logic technology for microprocessors due to 1) process integration challenges; and 2) most work showing near zero hole mobility improvement at large vertical electric fields [17], [18], [21], [22] (typical operating region for high-performance nanoscale MOSFETs). The near zero hole enhancement at large vertical fields causes the 1) net logic technology advantage to be small; and 2) further degrades the n- to pMOSFET ratio beyond the typical range of 2–2.4, which is highly undesirable since p-type transistors are already drawn at twice the n-type transistor width.

The strong enhancement of hole and electron mobility via uniaxial stress has been known for 50 years [30]. In fact, due to the large change in hole mobility in uniaxial stressed p-type Si, it is the dominant diaphragm type pressure sensors [31]. The difficulty in using uniaxial stress to improve the performance of complementary MOSFETs arises since it is difficult to improve both n- and pMOSFETs simultaneously [25], [26], [29]. As a result, uniaxial stress (unlike biaxial) was relatively neglected with little theoretical work developed for MOSFETs during the last decade.

As a consequence, the best quantitative predictor for uniaxial stress mobility enhancement at the time of this work which started in 1999 was the piezoresistance coefficients in Si. Piezoresistance coefficients are valid under small and moderate stress (less than approximately 250-500 MPa), where the piezoresistance varies linearly with stress. Yamada *et al.* found the nonlinearity in the piezoresistance to be small ($\sim$1% for longitudinal compression) up to 250 MPa [32]. Under small stress, the linearly varying mobility enhancement results primarily from changes in the conductivity effective mass through strain induced band/subband energy shifts, band warping and repopulation. At much higher strain levels, large energy band shifts alter mobility through changes in intervalley or interband scattering which invalidate the linear piezoresistance assumption. In this paper, we investigate large mobility enhancement in the small and moderate strain regime where the piezoresistance coefficients are valid since the integration of low strain into a CMOS logic technology create less defects and require less alteration of the technology midsection thermal cycles to avoid strain relaxation.

We now use the piezoresistance coefficients to quantify which types of stresses are more advantageous for mobility enhancement. For this discussion, we assume industry standard Si wafers with a (001) surface and wafer notch on the [110] axis (Fig. 6). Thus, the direction of current flow for transistors with 0 and 90 orientation is along the [110] axis. Transistors with a 45 orientation conduct along the [100] axis. Since uniaxial process-induced stress is generally applied either parallel (longitudinal) or perpendicular (transverse) to the direction

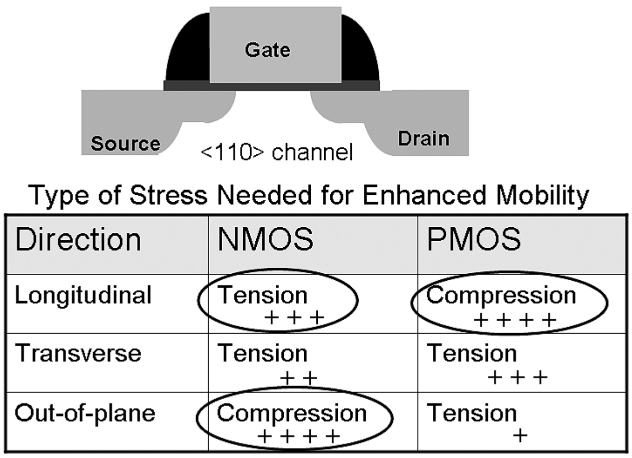

Fig. 6. From piezoresistance, the effect of various stress on electron and hole mobility (adapted from [28]).

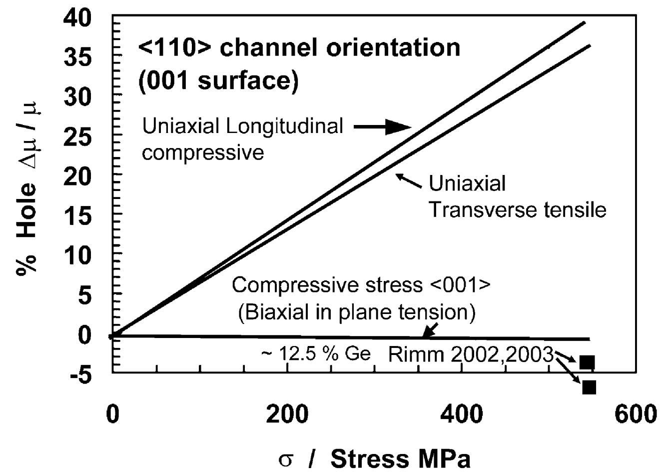

Fig. 7. Hole mobility enhancement versus stress as calculated from piezoresistance coefficients.

TABLE I
LONGITUDINAL AND TRANSVERSE PIEZORESISTANCE COEFFICIENTS EVALUATED FOR STANDARD LAYOUT AND WAFER ORIENTATION (UNITS OF 10^{-12} $\mathrm{cm^2 dyne^{-1}}$)

	<100>		<110>	
Polarity	$\pi_{\parallel}$	$\pi_{\perp}$	$\pi_{\parallel}$	$\pi_{\perp}$
N or P	π_{11}	π_{12}	$(\pi_{11}+\pi_{12}+\pi_{44})/2$	$(\pi_{11}+\pi_{12}-\pi_{44})/2$
N-type	-102	53.4	-31.6	-17.6
P-type	6.6	-1.1	71.8	-66.3

Biaxial Stress   Uniaxial Stress

of MOSFET current flow, we choose this coordinate system versus one aligned to the $\langle 100\rangle$ axes. The effect of mechanical stress on the mobility can then be expressed as follows:

$$\frac{\Delta\mu}{\mu} \approx \left|\pi_{\|}\sigma_{\|} + \pi_{\perp}\sigma_{\perp}\right|$$

where the subscripts $\|$ and $\perp$ refer to the directions parallel and transverse to the current flow in the plane of the MOSFETs. $\sigma_{\|}$ and $\sigma_{\perp}$ are the longitudinal and transverse stresses, and $\pi_{\|}$ and $\pi_{\perp}$ are the piezoresistance coefficients expressed in Pa^{-1}. $\pi_{\|}$ and $\pi_{\perp}$ can be expressed in terms of the three fundamental cubic piezoresistance coefficients π_{11}, π_{12}, and π_{44}.

In the case of the technologically important (001) wafer, the longitudinal and transverse piezoresistance coefficients for the standard layouts are given in Table I [4]. For simplicity we use the bulk values for π_{11}, π_{12}, and π_{44} first measured 50 years ago by Smith [30], though technically piezoresistance coefficients should take into account the two-dimensional nature of transport in the MOSFET and depend on temperature, gate voltage, and doping [29], [33]. Using the bulk coefficients, $\pi_{\|}$ and $\pi_{\perp}$ are calculated in Table I. Consistent with other work [29], we find the bulk coefficients, as measured by Smith, quantitatively predict the strained-Si experimental data in this work. Using the values in Table I, Fig. 6 summarizes how various stresses in sign and magnitude enhance or degrade the mobility. For the <110> channel direction, the most effective stresses to implement are longitudinal compressive stress for pMOSFETs and longitudinal tensile and out-of-plane compressive stress for nMOSFETs. These are the three dominate stresses that result from SiGe in the pMOSFET source/drain and a tensile capping layer on the nMOSFET and why the current strain integration scheme in this paper was chosen. For hole mobility enhancement, another key takeaway from Table I is how much more effective longitudinal compressive stress is over biaxial tensile stress.

Using the piezoresistance coefficients in Table I, Fig. 7 plots the hole mobility improvement versus stress for both cases. At 500 MPa of stress, the piezoresistance coefficients predicts 40% and -5% hole mobility enhancement for longitudinal uniaxial compressive and biaxial tensile, respectively, which is consistent with the MOSFET data [4], [19]. The piezoresistance coefficient π_{12} is used to model biaxial mobility enhancement since biaxial stress band splitting can be identically modeled by a compressive uniaxial stress in the $\langle 001\rangle$ direction. Thus π_{12} is the piezoresistance coefficient for biaxial stress. For low to moderate biaxial stress, the piezoresistance coefficient predicts a slight mobility degradation which is consistent with the biaxial stress experimental data [19], [20] (see Fig. 7). This analysis again is only valid for biaxial substrates with low germanium concentration (~ 5%-10%) when the mobility enhancement results from changes in the conductivity effective mass as opposed to scattering but is relevant since large strain is difficult to integrate due to strain relaxation. At present, it is not clear biaxial substrates with the 25%-30% Ge needed for hole mobility enhancement can be integrated.

C. *Mobility Enhancement With Strained-Si*

A key scaling problem in nanoscale transistors is the mobility degradation caused by the large vertical electric fields. Fig. 8 shows the mobility versus technology scaling trend for various Intel process technologies. In Fig. 8, the mobility has decreased from 400 to 120 $\mathrm{cm^2/Vs}$ during the last decade. To counteract this undesirable mobility trend, it is becoming increasingly important to incorporate mobility enhancing process features in nanometer logic technology.

1) Strained-Si Hole Mobility Enhancement: In this paper, longitudinal uniaxial strain introduced by the $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ in

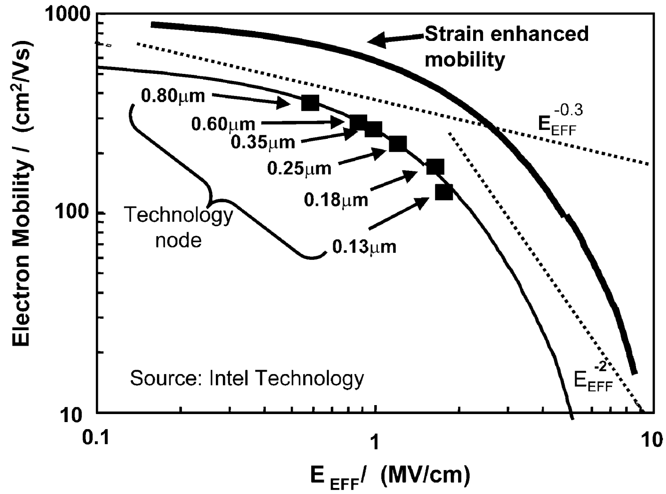

Fig. 8. Mobility versus technology scaling trend for Intel process technologies.

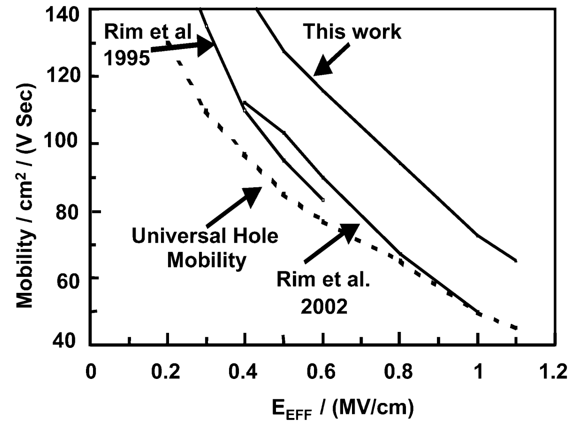

Fig. 9. Hole mobility for uniaxial strained-Si introduced $Si_{1-x}Ge_x$ in the source and drain [5].

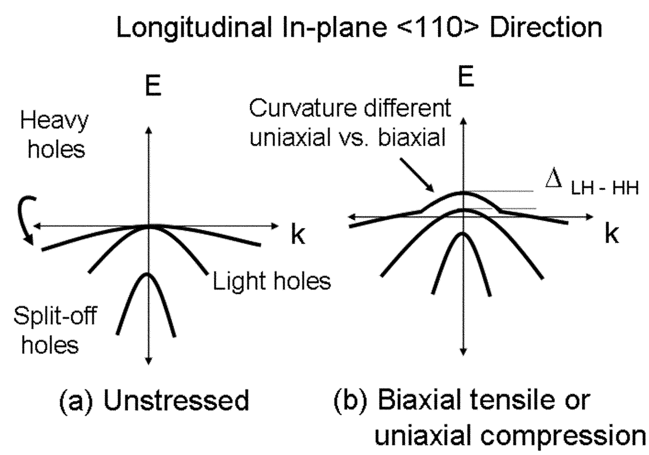

Fig. 10. Simplified hole valence band structure for longitudinal in-plane direction (a) unstrained and (b) strained-Si (adapted from [17]).

the source and drain of the p-type MOSFET increases the hole mobility for the 45-nm gate length transistor by 50% as shown in Fig. 9. The mobility for the short channel device is extracted from the improvement in the linear current using $I_D = k(V_{\mathrm{GS}}–V_T)(V_{\mathrm{DS}}–I_D R_{\mathrm{SD}})(V_{\mathrm{DS}} = 50\ \mathrm{mV})$ where R_{SD} is measured independently. The field dependence of the mobility is also extracted using conventional techniques on a long channel transistor [4] where R_{SD} is negligible to validate the field dependence is correct. Two important observations are made from Fig. 9. First and consistent with the piezoresistance coefficients, large hole mobility enhancement is present at low longitudinal uniaxial compressive stress. Second, for longitudinal uniaxial stress (unlike biaxial) the hole mobility enhancement is maintained at large vertical fields. Why the hole mobility enhancement is present at low stress and large vertical fields are major advantages of this strained Si technology. The physical mechanism for the large hole mobility enhancement at low stress and large vertical field has not been highlighted previously but can be inferred from the data using previous experimental and theoretical work [34]–[40].

Summarizing references [34]–[40], the strain enhanced hole mobility understanding has lagged behind electron [38], [41] and much of the understanding, as in this paper, has first been driven by experimental data. There have been few theoretical hole mobility studies due to the complicated nature of the valence bands not amenable to a simple analytic description [41] From [34], [35], and [38] Fig. 10 summarizes what is known about the hole band structure for unstrained and strained-Si. The valence bands are plotted for the in-plane direction of the MOSFET. Both uniaxial and biaxial stress lifts the degeneracy in the valence band and causes shift and warping of the bands as shown in Fig. 10. For both types of stresses, holes populate the lowest energy band which is light-hole like. Considering the mobility enhancement at low strain results from in-plane conductivity effective mass changes, the biaxial tensile and longitudinal uniaxial compressive stress mobility data suggest the uniaxial stress band warping and repopulation creates a significantly lower in-plane mass. Evidence of a low in-plane effective mass (high mobility) for uniaxial stress exists in the literature and was first calculated by Bir and Pikus in 1958 in which a "dimple" at $k = 0$ is formed by the light-hole band dropping in energy [34], [35].

Next, we summarize what is known about the field dependence of the hole mobility. For biaxial stress, Fischetti showed the loss in enhanced hole mobility results from reduced separation between the light and heavy-hole like bands ($\Delta_{\mathrm{lh-hh}}$ see Fig. 10) with increased vertical field [38]. Based on the experimental hole mobility enhancement in this work, the confining surface potential does not reduce the strain induced band separation for uniaxial compressive stress. The reason the separation is not lost for uniaxial stress must again be caused by band warping creating an advantageous (large) out-of-plane effective mass for the top energy band [42]. The band warping for biaxial and uniaxial stress must look like as shown in Fig. 11, which is consistent with the published data in references [17], [38], [40] for biaxial tensile and [34], [35] for uniaxial compressive stress. Experimentally for uniaxial stressed Si, the mobility enhancement at high fields is observed for all work to date where the stress was introduced using a number of different techniques: mechanical wafer bending [43], nitride capping layer [25], [26], and the $Si_{1-x}Ge_x$ adjacent to the channel [4]–[6] and it is this data that suggested to us longitudinal compressive uniaxial stress should be pursued.

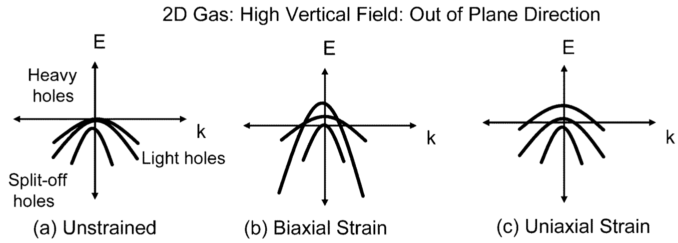

Fig. 11. Simplified hole valance band structure for out-of-plane direction (a) unstrained, (b) biaxial tension, and (c) uniaxial compression strained-Si.

2) Strained-Si Electron Mobility Enhancement: The electron mobility enhancement in this paper is significant but less than the hole mobility gain since the stress applied via a silicon nitride-capping layer is less than the SiGe in the source and drain. Using finite element simulations, the tensile capping layer causes both longitudinal tensile and out-of-plane compressive stress in the channel both of which from the piezoresistance coefficients improves the electron mobility. Fig. 12 plots the improvement in the n-type saturation drive current obtained at a constant off-state leakage of 40 nAμm versus increasing capping layer strain. In this 90-nm technology, greater than 10% improvement in drive current is obtained with the use a 75-nm silicon nitride film.

Contrary to hole mobility enhancement with stress, the theoretical understanding for electron mobility enhancement for biaxial and uniaxial tensile stress is well developed. Experimental and theoretical work to provide insight into the field dependence of the electron mobility enhancement started with the 1970 work by Dorda [33]. The vast experimental data on the biaxial and uniaxial strained-Si suggest the strain enhanced electron mobility [12], [39] is present at large vertical fields. Since the electron enhancement for uniaxial and biaxial tensile stress arise from the same mechanisms (namely sixfold degenerate conduction band valleys split into two groups: 1) lower energy two fold degenerate valleys having low in-plane transverse effective mass $m_t = 0.19m_o$, and 2) higher energy four-fold degenerate valleys), the field dependence and the maximum electron mobility enhancement will be identical.

Yamada *et al.* [44], Takagi, *et al.* [12], and Fischetti *et al.* [39] have published recent theoretical work on strain enhanced electron mobility which demonstrates qualitative agreement with most of the experimental data. One area of discrepancy is with the electron mobility enhancement at high fields which is slightly larger than expected from theory since the addition of strain to a MOSFET under large vertical fields should cause negligible additional electron repopulation into the lower two fold valleys (bands with lighter conductivity mass) and only small additional reduction in intervalley scattering [39]. This is because the carrier confinement in the two–dimensional gas lifts the six-conduction band degeneracy identically for the biaxial and uniaxial stressed Si cases. Furthermore, due to the continued large gain seen experimentally at large stresses, Fischetti *et al.* has proposed an ad hoc assumption of an increasingly smoother interfaces with increasing strain as a possible explanation to the electron mobility improvement. Interestingly, the stress-induced increase in the out-of-plane effective mass for electrons (biaxial and uniaxial tensile stress)

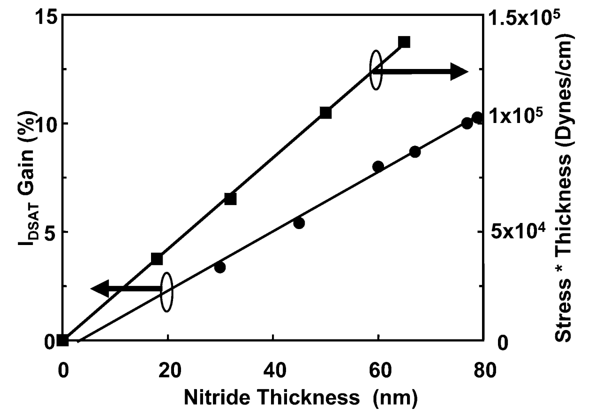

Fig. 12. Electron saturated drive current improvement versus nitride thickness [6].

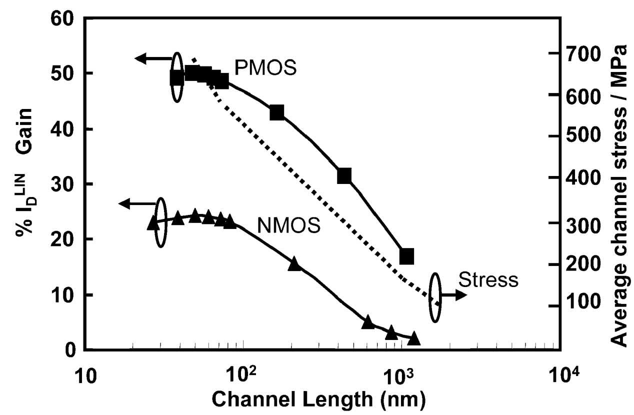

Fig. 13. Linear current and p-channel average channel stress improvement versus channel length.

and holes (uniaxial compression) will reduce surface roughness scattering and make the interface look smoother but the effect does not appear large enough to explain the majority of the mobility enhancement at high fields. Another explanation for this electron phenomenon is the relative strength of the f-type phonon. While the scattering used by Fischetti assumes that the g-type phonon is dominant, that used by Formicone *et al.* [45] suggest that it is the f-type phonon which is dominant. As the valley shifting in n-type Si suppresses this f-type phonon, the more dominant this phonon is in relaxed Si, the more there is to gain from its suppression in stressed Si. This concept of a dominant f-type phonon being required to reproduce experimentally measured gain in Si has also been shown by the calculation performed by Takagi [12].

3) Mobility Enhancement Versus Channel Length: There is one last major difference for the side stress enhanced mobility in this paper versus the bottom biaxial tensile stress. Stress applied to the side of a device causes the strain and mobility to increase with channel length. The p-type Si channel strain depends on the volume of $Si_{1-x}Ge_x$ and pMOSFET channel length. As the gate length decreases, the volume of $Si_{1-x}Ge_x$ increases while the Si channel volume decreases. This enlarges the amount of strain in the channel. Fig. 13 shows 1) the n and p-type MOSFET linear current improvement; and 2) p-type MOSFET average channel uniaxial stress calculated by finite element simulations versus channel length. For the side-induced stressed silicon technique, as short channel effects are improved and smaller channel length MOSFETs are targeted, the mobility for the target channel length device will increase, thus, further enhancing the benefit of this strained-Si approach.

IV. Conclusion

In this paper, we described a 90-nm generation logic technology designed for high speed and low power operation. In the nanotechnology era, strained-Si channel transistors are added to continue Moore's law. Strained-Si is added using a novel process flow for significant mobility enhancement. The process flow is scalable for several generations. The strain to first-order is constant with pitch providing the channel length and source/drain width with are scaled equally.

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