55nm high mobility SiGe(:C) pMOSFETs with HfO_2 gate dielectric and TiN metal gate for advanced CMOS

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Abstract

For the first time, MOS transistors with compressively strained SiGe(:C) channel, metal gate and high-k dielectric are demonstrated down to 55nm gate length. SiGe(:C) surface channel pMOSFETs with HfO_2 gate dielectric exhibit a 10^4 gate leakage reduction and a 65% mobility enhancement at high transverse effective field (1MV/cm) when compared to the universal SiO_2/Si reference. With such a thin Equivalent Oxide Thickness (EOT=16-18Å), this represents the best gate leakage/mobility trade-off ever published.

Keywords : pMOSFET, High-k, SiGe(:C) and Metal Gate.

Introduction

HfO_2 is a leading high-k gate dielectric candidate to replace SiON in future CMOS technology generations [1]. However, the most serious drawback in integrating HfO_2 is the carrier mobility degradation. In this context, tensile strained Si channel is a promising solution [2]. The drive current enhancement is then larger for nMOSFETs than for pMOSFETs, inducing even more unbalanced CMOS layout and performances [3]. Today, the compressively strained SiGe (or pure Ge [4]) channel is the best candidate for hole mobility enhancement. Using a SiGe channel with an appropriate high-k gate dielectric makes it possible to get rid of a thick Si cap and thus take advantage of a surface channel operation [5]. In this paper, the benefits of an optimised HfO_2/SiGe interfacial layer are discussed. We demonstrate an excellent gate leakage/mobility trade-off for pMOSFETs with HfO_2 gate dielectric and well controlled 55nm gate length transistors using strained SiGe channels. Another advantage of using a SiGe surface channel in terms of CMOS threshold voltage (V_{th}) adjustment with a TiN gate is demonstrated.

Device fabrication

After isolation and well implants, the $Si_{0.72}Ge_{0.28}$ (or $Si_{0.715}Ge_{0.28}C_{0.005}$) epitaxial channel was selectively grown on Si(001) at 650°C by Reduced Pressure - Chemical Vapour Deposition (RPCVD). 0.5% of carbon was added in some of the SiGe layers to improve their thermal stability. A damascene replacement gate process (described in details in [6]) was used to make the TiN/HfO_2 gate stack (Fig.1). The crucial step was the surface preparation just before the high-k dielectric deposition. On samples A ($SiGe_A$), HfO_2 was directly deposited on the HF cleaned SiGe surface. On samples B ($SiGe_B$), the ozone cleaning was the same as for our silicon references and resulted in a native chemical oxide growth. This oxide is thicker on SiGe surfaces (≈10Å) than on Si ones (≈7Å) and exhibits high interface state densities (D_{it}). In order to avoid those degradations in our $SiGe_B$ samples, a sacrificial silicon layer (3nm) was grown just after the epitaxy of SiGe. A Ge retrograde profile is then obtained due to the chemically non abrupt Si on SiGe interface. Thin films of HfO_2 were deposited using an Atomic Layer Deposition PULSAR 2000™ with a {$HfCl_4$,H_2O} chemistry. Post deposition annealing (PDA) was performed at 600°C or 800°C in N_2 followed by a CVD TiN metal gate deposition. Both processes (A and B) are summarized in Table 1.

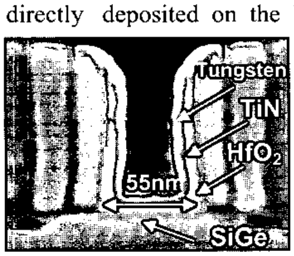

Fig.1: SEM cross section of a 55nm gate length SiGe pMOSFET with a TiN/HfO_2 gate stack.

Table1: process description

A	B
- SiGe epitaxy (RPCVD)	- SiGe + Si (3nm) epitaxy (RPCVD)
- Replacement gate process	- Replacement gate process
- Clean A (HF-Last)	- Clean B (ozone)
- HfO_2 and TiN deposition	- HfO_2 and TiN deposition

HfO_2 gate dielectric characterization

The Equivalent Oxide Thickness (EOT) was calculated accurately by using capacitance measurements and a quantum mechanical simulator. Clean A (HF-Last) exhibits lower EOT than clean B due to a thinner thickness of the interfacial layer (10Å and 14Å, respectively) for the same PDA (800°C) (Fig.2-Left). For lower temperature PDA (600°C), the EOT of $SiGe_B$ samples can be reduced to 16.5Å (insert). Process quality for $SiGe_B$ devices is demonstrated by the perfect interface structural quality analysed by High Resolution Transmission Electron Microscopy (HRTEM) (Fig.2-Right). An interfacial layer physical thickness of 15Å is measured on $SiGe_B$ devices. In $SiGe_A$ devices, even if the interface roughness is worse, a thinner interfacial layer thickness is confirmed (average=12Å). The high interface quality observed for $SiGe_B$ is confirmed by the lack of C-V curve stretching (Fig.3-Left). A D_{it} as low as $3\text{-}4.10^{11}cm^{-2}.eV^{-1}$ is obtained (Fig.3-Right). For the same flatband voltage (Vfb), a

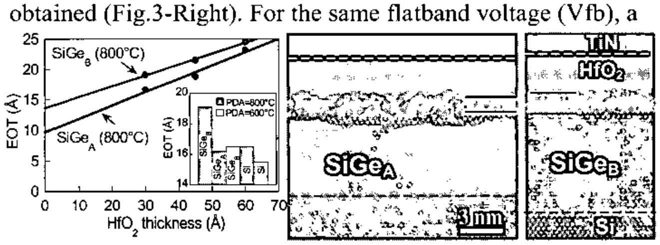

Fig.2: Left-Interface layer EOT determination for clean A and B. EOTs for 30Å deposited HfO_2 are summarized in the insert. Right-HRTEM comparison of the interfacial layers after the 800°C PDA.

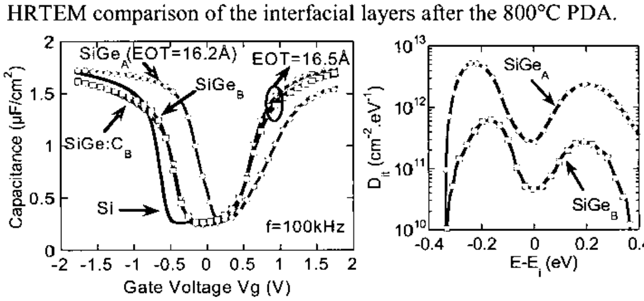

Fig.3: Left-Gate capacitance versus gate voltage for $SiGe_A$ and $SiGe(:C)_B$ samples. Right-D_{it} energy distribution in the band-gap.

V_{th} shift (0.25V) is obtained in $SiGe_B$ devices compared to Si ones due to the valence band offset. The V_{th} is therefore adjusted by the channel material, so the advantages of a mid-gap metal gate are reinforced by a strained SiGe channel. For EOT=16.5Å, gate leakage current is reduced by 4 orders of magnitude compared to SiO_2/Si devices (Fig.4).

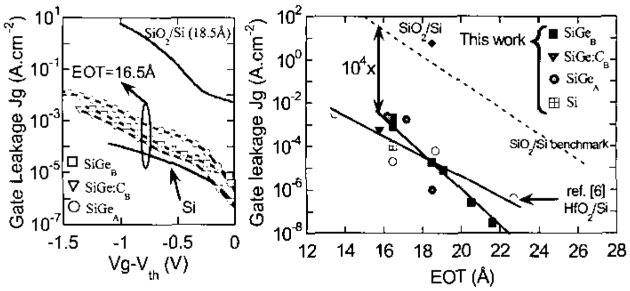

Fig.4: Left-Gate leakage (Jg) versus (V_g-V_{th}) for 3nm deposited HfO_2 pMOSFETs in inversion regime. Right-Jg (EOT) @ |V_g-V_{th}|=1V

Mobility results

In $SiGe_B$, a small capacitance loss (EOT=1Å) is observed in inversion due to the retrograde Ge profile at the interface (Fig.3-Left and Fig.5-Left). Mobility curves (extracted by split C-V measurements, Fig.5-Right) show this loss is not associated with Si parasitic channel conduction, even at high effective field. The 15% mobility degradation with the HfO_2/Si stack compared to universal mobility is consistent with previously reported results [6]. At 1MV/cm, the $HfO_2/SiGe_B$ (HfO_2/SiGe:C_B) device exhibits a 58% (65%) higher mobility than the universal mobility and a 90% (100%) higher mobility than our HfO_2/Si references. The corresponding measured drain current enhancement is shown in Fig.6-Left. The lower mobility in $SiGe_A$ devices is explained by the high interface state density (Fig.6-Right). The SiGe strain induced mobility enhancement is higher with HfO_2 than with SiO_2 [7-10] (Fig.7-Left). This represents the best gate leakage/mobility trade-off in pMOSFETs for such a thin EOT [5],[11-12] (Fig.7-Right).

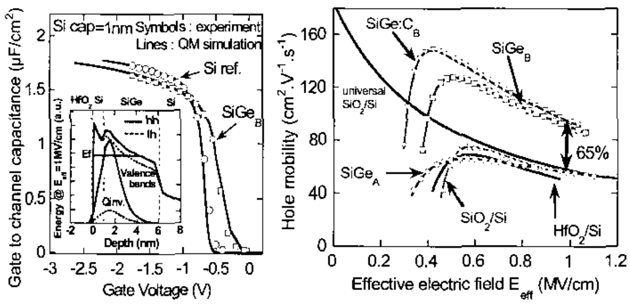

Fig.5: Left-quantum mechanical simulation of the gate to channel capacitance (Cgc) in $SiGe_B$. Right-Effective hole mobility versus effective field for the various channel-gate dielectric stacks.

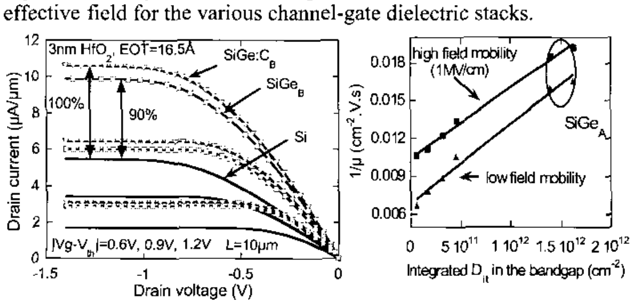

Fig.6: Left-Drain current enhancement on long channel pMOSFETs. Right-Coulomb scattering impact on effective hole mobility.

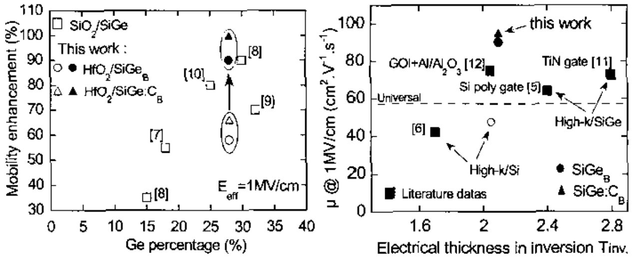

Fig.7: Left-Mobility enhancement at 1MV/cm compared to the SiO_2/Si universal mobility (open symbols) and to the HfO_2/Si reference (full symbols). Right-Mobility at 1MV/cm versus T_{inv} compared to literature results.

55nm gate length devices characteristics

Well controlled 55nm gate length transistors with reduced Drain Induced Barrier Lowering (DIBL) are obtained (Fig.8 and Table 2). An adjusted V_{th} (V_{th}=-0.3V) is achieved thanks to the SiGe channel which allows an improved I_{on}(260µA/µm)/I_{off}(40nA/µm) ratio @ Vdd=1.5V for high-performance applications. The V_{th} shift induced by the band offset of the channel material is of great interest since it is well established that dual metal gates with work-functions within about 0.2eV of the band edges will be required for sub-50nm high-performance CMOSFETs [13]. In this context a strained Si/strained SiGe (or Ge) for N/P dual channel [14] is a promising CMOS architecture to solve both the mobility and the metal work-function issues in mid-gap metal/high-k gate stacks.

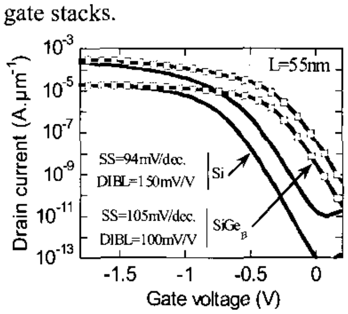

Fig.8: Drain current versus gate voltage for Vd=-0.05V and Vd=-1.2V

Table 2 : Summary of $SiGe_B$ versus Si pMOSFETs results.

55nm pMOSFETs	**Si**	**$SiGe_B$**
EOT	16.5Å	18.5Å
DIBL	140mV/V	100mV/V
SS (10µm) SS (55nm)	75mV/dec. 94mV/dec.	78mV/dec. 105mV/dec
Vth (10µm)	-0.65V	-0.4V
Vth (55nm)	-0.7V	-0.3V
I_{on} @ Vg-V_{th}=-1V	201uA/um	192uA/um
I_{off} @ Vg-V_{th}=0.3V	245nA/um	40nA/um
I_{on}/I_{off} @Vdd=-1.5V	156uA/um-19pA/um	260uA/um-40nA/um

Conclusion

An excellent gate leakage/mobility trade-off is achieved by optimising the HfO_2/SiGe(:C) interface. The advantage of the SiGe(:C) surface channel in advanced CMOS concerning the hole mobility enhancement and the threshold voltage adjustment in mid-gap metal/High-k gate stacks is clearly demonstrated.

References

[1] H. Iwai et *al.*, IEDM Tech. Dig, pp.625-628, 2002
[2] S. Datta et *al.*, IEDM Tech. Dig, pp.653-656, 2003
[3] K. Rim et *al.*, Symp. VLSI Tech., pp.98-99, 2002
[4] M. L. Lee et *al.*, IEDM Tech. Dig, pp.429-432, 2003
[5] Z. Shi et *al.*, IEEE EDL, 24 (1), pp.34-36, 2003
[6] B. Guillaumot et *al.*, IEDM Tech. Dig, pp.355-358, 2002
[7] F. Andrieu et *al.*, ESSDERC, pp.267-270, 2003
[8] P. Bouillon et *al.*, IEDM tech. Dig, pp.559-562, 1996
[9] N. Collaert et *al.*, Si. Nano. Workshop, pp.15-16, 2002
[10] Y. C. Yeo et *al.*, IEDM Tech. Dig, pp.753-756, 2000
[11] D. Wu et *al.*, IEEE EDL, 24 (3), pp.171-173, 2003
[12] C. H. Huang et *al.*, Symp. VLSI Tech., pp.119-120, 2003
[13] I. De et *al.*, Solid State Elec., (44), pp.1077-1080, 2000
[14] Q. Xiang, US Patent #6,600,170 B1, published Jul. 2003.