

Filed on behalf of:

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Petitioner

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE PATENT TRIAL AND APPEAL BOARD

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UNITED MICROELECTRONICS CORPORATION,  
AND  
UMC GROUP (USA),  
Petitioners,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,  
Patent Owner.

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Case No. IPR2025-01053  
Patent No. 8,796,779

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**PETITION FOR *INTER PARTES* REVIEW OF  
U.S. PATENT NO. 8,796,779  
UNDER 35 U.S.C. §§ 311, 312 AND 37 C.F.R. § 42.104**

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1001	U.S. Patent No. 8,796,779 to Ito (the “’779 patent”)
1002	Prosecution History of the ’779 patent (“the Prosecution History”)
1003-1004	RESERVED
1005	U.S. Patent No. 6,881,657 B2 to Torii et al. (“Torii”)
1006	U.S. Patent Application Publication No. 2010/0258878 to Mise, et al. (“Mise”)
1007	U.S. Patent No. 8,114,739 to Chowdhury, et al. (“Chowdhury”)
1008	U.S. Patent No. 6,693,333 to Yu (“Yu”)
1009	U.S. Patent No. 6,787,421 B2 to Gilmer et al. (“Gilmer”)
1010	U.S. Patent No. 7,382,023 B2 to Chen et al. (“Chen”)
1101	Declaration of Sanjay Banerjee, PhD
1102	Curriculum Vitae of Sanjay Banerjee, PhD
1103	“Stress Memorization Technique (SMT) by Selectively Strained-Nitride Capping for Sub-65nm High- Performance Strained-Si Device Application,” Chen et al., 2004 Symposium on VLSI Technology Digest of Technical Papers (2004) (“Chen-2004”)
1104	“35% Drive Current Improvement from Recessed-SiGe Drain Extensions on 37 nm Gate Length PMOS,” Chidambaram et al., 2004 Symposium on VLSI Technology Digest of Technical Papers (2004) (“Chidambaram-2004”)

Exhibit No.	Description
1105	<p>“Self-Aligned Ultra Thin HfO<sub>2</sub> CMOS Transistors with High Quality CVD TaN Gate Electrode,” Lee et al., 2002 Symposium On VLSI Technology Digest of Technical Papers (2002)                      (“Lee-2002”)</p>
1106	<p>“Delaying Forever: Uniaxial Strained Silicon Transistors in a 90nm CMOS Technology,” Mistry et al., 2004 Symposium on VLSI Technology Digest of Technical Papers (2004)                      (“Mistry-2004”)</p>
1107	<p>“Effects of High-Temperature Forming Gas Anneal on HfO<sub>2</sub> MOSFET Performance,” Onishi et al., 2002 Symposium On VLSI Technology Digest of Technical Papers (2002)                      (“Onishi-2002”)</p>
1108	<p>“Low Standby Power CMOS with HfO<sub>2</sub> Gate Oxide for 100-nm Generation,” 2002 Symposium On VLSI Technology Digest of Technical Papers (2002)                      (“Pidin-2002”)</p>
1109	<p>“Mobility Enhancement in Strained Si NMOSFETs with HfO<sub>2</sub> Gate Dielectrics,” Rim et. al., 2002 Symposium On VLSI Technology Digest of Technical Papers (2002)                      (“Rim-2002”)</p>
1110	<p>“Metal Gate MOSFETs with HfO<sub>2</sub> Gate Dielectric,” Samavedam et al., 2002 Symposium On VLSI Technology Digest of Technical Papers (2002)                      (“Samavedam-2002”)</p>
1111	<p>“55nm high mobility SiGe(:C) pMOSFETs with HfO<sub>2</sub> gate dielectric and TiN metal gate for advanced CMOS,” Weber et al., 2004 Symposium on VLSI Technology Digest of Technical Papers (2004)                      (“Weber-2004”)</p>
1112-1210	RESERVED
1211	<p>Van Zant, “Microchip Fabrication” (Fifth Ed. 2004)                      (“Van Zant”)</p>

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Exhibit No.	Description
1212	Weste, “CMOS VLSI Design: A Circuits and Systems Perspective” (Third Edition, 2005) (“Weste”)
1213	Houssa, M., “High-k Dielectrics” to Houssa (IOP Publishing Ltd. 2004) (“Houssa”)
1214	Wolf, S., “Silicon Processing for the VLSI Era, Volume 4 – Deep-Submicron Process Technology” (“Wolf-4”)
1215	Plummer, J. et al., “Silicon VLSI Technology: Fundamentals, Practice and Modeling” (Prentice Hall 2000) (“Plummer”)
1216	“International Technology Roadmap for Semiconductors: Process Integration, Devices, and Structures” (2007 Edition) (“ITRS-PIDS”)
1217-1222	RESERVED
1223	“Semiconductor Devices: Physics and Technology” by Sze (Second Edition, 2002) (“Sze-2002”)
1224-1225	RESERVED
1226	U.S. Patent No. 7,709,331 to Karve, et al. (“Karve”)
1227	U.S. Patent No. 8,017,469 to Luo, et al. (“Luo”)
1228	RESERVED
1229	Wolf, “Silicon Processing for the VLSI Era, Volume 3 – The Submicron MOSFET” (1995) (“Wolf-3”)
1230	RESERVED
1231	U.S. Patent No. 8,384,160 to Onishi, et al. (“Onishi160”)

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Exhibit No.	Description
1232	“An Adjustable Work Function Technology Using Mo Gate for CMOS Devices”, Lin, et al., IEEE Electron Device Letters, Vol. 23, No. 1, January 2002 (“Lin-2002”)
1233	“Dual Work Function Metal Gate CMOS Transistors by Ni-Ti Interdiffusion”, Polishchuk, et al., IEEE Electron Device Letters, Vol. 23, No. 4, April 2002 (“Polishchuk”)
1234-1318	RESERVED
1318	Wilk, G. D., et al., “High-k gate dielectrics: Current status and materials properties considerations,” Journal of Applied Physics, Vol. 89, No. 10, pp. 5243-75, May 15, 2001 (“Wilk”)
1319-1322	RESERVED
1323	U.S. Patent No. 6,306,712 to Rodder, et al. (“Rodder”)
1324-1339	RESERVED
1340	Japanese Patent Publication JP2005-064190 to Ono with certified translation (“JP-Ono”)
1341-1405	RESERVED
1406	U.S. Patent Application Publication No. 2007/0249069 A1 to Alvarez et al. (“Alvarez”).
1407-1412	RESERVED
1413	S.M. Sze, Physics of Semiconductor Devices (2d ed. 1981) (excerpted). (“Sze-1981”)
1414-1418	RESERVED
1419	U.S. Patent Application Publication No. 2006/0286729 A1 to Kavalieros et al. (“Kavalieros729”)

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Exhibit No.	Description
1420-1428	RESERVED
1429	U.S. Patent Application Publication 2004/0262784 A1 to Doris et al. (“Doris”)
1430	U.S. Patent No. 6,797,556 B2 to Murthy et al. (“Murthy556”)
1431	U.S. Patent Application Publication No. 2007/0134870 A1 to Lee et al. (“Lee870”)
1432	U.S. Patent Application Publication No. 2005/0260810 A1 to Cheng et al. (“Cheng810”)
1433	U.S. Patent Application Publication No. 2009/0020820 A1 to Baik et al. (“Baik”)
1434	U.S. Patent Application Publication No. 2008/0293207 A1 to Koutny et al. (“Koutny”)
1435	U.S. Patent Application Publication No. 2010/0075476 A1 to Miyashita. (“Miyashita”)
1436-1505	RESERVED
1506	U.S. Patent Application Publication 2007/0235823 A1 to Hsu et al. (“Hsu823”).
1507-1511	RESERVED
1512	International Technology Roadmap for Semiconductors: Front End Processes (2007 ed.). (“ITRS_FEP”)
1513-1514	RESERVED
1515	U.S. Patent Application Publication No. 2006/0022277 A1 to Kavalieros et al. (“Kavalieros277”)

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Exhibit No.	Description
1516	K. Mistry, et al., “A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging,” Technical Digest of the of the 2007 IEEE International Electron Devices Meeting (IEDM), pp. 247-50 (Dec. 2007) (“Mistry2007”)
1517	K. Mistry, et al., “A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging,” presented at 2007 IEEE International Electron Devices Meeting (IEDM), pp. 1-37 (Dec. 2007) (“Mistry_Presentation”)
1518	U.S. Patent No. 6,881,631 B2 to Saito et al. (“Saito631”)
1519	U.S. Patent No. 7,812,414 B2 to Hou et al. (“Hou”)
1520	U.S. Patent Application Publication No. 2005/0258468 A1 to Colombo et al. (“Colombo”)
1521	U.S. Patent No. 6,849,511 B2 to Iriyama et al. (“Iriyama”)
1522	U.S. Patent Application Publication No. 2002/0037615 A1 to Matsuo. (“Matsuo”)
1523	S.E. Thompson et al., “A 90-nm Logic Technology Featuring Strained Silicon,” IEEE Transactions on Electron Devices, vol. 51. No. 11, pp. 1790-97 (Nov. 2004). (“Thompson-2004”)

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Exhibit No.	Description
1524	Y. Sun et al., “Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors,” <i>Journal of Applied Physics</i> , vol. 101, Art. No. 104503 (22 pages) (May 2007). (“Sun-2007”)
1525	D. James, “2004 – The Year of 90-nm: A Review of 90 nm Devices,” 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 72-77 (2005). (“James”)
1526	U.S. Patent Application Publication No. 2006/0148151 A1 to Murthy et al. (“Murthy151”)
1527	U.S. Patent Application Publication No. 2004/0262683 A1 to Bohr et al. (“Bohr”)
1528	P. Morin et al., “Extensive Study of the Correlation between Contact Etch Stop Nitride Material Properties and Negative Bias Temperature Instabilities Measured in pMOSFETS,” <i>ECS Transactions</i> , vol. 6, no. 3, pp. 355-69 (2007). (“Morin-2007”)
1529	U.S. Patent Application Publication No. 2005/0170104 A1 to Jung et al. (“Jung”)
1530	RESERVED
1531	U.S. Patent Application Publication No. 2008/0145984 A1 to Ke et al. (“Ke”)
1532	P. Bai et al., “A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 $\mu\text{m}^2$ SRAM Cell,” <i>Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM)</i> , pp. 657-60 (Dec. 2004). (“Bai-2004”)

**CHALLENGED CLAIM LISTING FOR U.S. PATENT NO. 8,796,779**

1. **Preamble:** A semiconductor device comprising:

**Limitation 1[a]:** a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate,

**Limitation 1[b]:** wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film,

**Limitation 1[c]:** the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film,

**Limitation 1[d]:** the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer,

**Limitation 1[e]:** the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer,

**Limitation 1[f]:** the first interface layer has a thickness larger than that of the second interface layer, and

**Limitation 1[g]:** each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film.

2. **Limitation 2[a]:** The semiconductor device of claim 1, wherein the first gate electrode includes first sidewall spacers formed on side surfaces thereof and first insulating spacers interposed between the first gate electrode and the first sidewall spacers,

**Limitation 2[b]:** the second gate electrode includes second sidewall spacers formed on side surfaces thereof and second insulating spacers interposed between the second gate electrode and the second sidewall spacers, and

**Limitation 2[c]:** the first insulating spacers are thinner than the second insulating spacers.

7. **Limitation 7:** The semiconductor device of claim 2, wherein each of the first insulating spacers and the second insulating spacers is made of a silicon nitride film.

12. **Limitation 12:** The semiconductor device of claim 1, wherein each of the first and second high dielectric constant insulating films contains hafnium or zirconium.

13. **Limitation 13:** The semiconductor device of claim 1, wherein the first and second high dielectric constant insulating films are equal in thickness.

Ex.1001, 13:64-14:22, 14:23-33, 14:60-62, 15:20-22, 15:23-25.

Under 35 U.S.C. §§ 311, 312 and 37 C.F.R. § 42.104, United Microelectronics Corporation and UMC Group (USA) (collectively, “Petitioner”) request *inter partes* review (“IPR”) of claims 1, 2, 7, 12, and 13 (“Challenged Claims”) of U.S. Patent No. 8,796,779 (Ex.1001, “the ’779 patent”).

## **I. INTRODUCTION**

The ’779 patent is directed to a “semiconductor device” containing at least two separate “metal insulator semiconductor (MIS)” transistors, each with a “high dielectric constant insulating film” and an intervening “interface layer” between the substrate and the insulating film. Ex.1001, 13:64-14:22; *see also id.*, 1:17. The alleged point of novelty is forming the two MIS transistors on the same semiconductor device with differently sized structures, *e.g.* a “first interface layer has a thickness larger than that of the second interface layer.” *Id.* (claim 1). But these types of system-on-chip devices were well known long before the ’779 patent was filed in 2010. In Ground I, Torii anticipates all challenged claims, was filed in 2004, and issued as a United States Patent in 2005. This Petition demonstrates that the Challenged Claims are unpatentable as anticipated and obvious.

With respect to claims 1, 12, and 13, the Grounds presented here are the same grounds presented in IPR2025-00832. Claims 2 and 7 were not challenged in IPR2025-00832 but are challenged here in Ground I using the same prior art (Torii) used in Ground 1 of IPR2025-00832.

## II. MANDATORY NOTICES

### A. Real Party-in-Interest (37 C.F.R. §42.8(b)(1))

United Microelectronics Corporation and UMC Group (USA) are the real parties-in-interest.

### B. Related Matters (37 C.F.R. §42.8(b)(2))

The '779 patent is the subject of the following active proceedings:

- *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation*, Civil Action No. 2:24-cv-00730 in the Eastern District of Texas (Lead Case), filed September 6, 2024;
- *Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Manufacturing Company Limited*, Civil Action No. 2:24-cv-00623 in the Eastern District of Texas (Consolidated Member Case), filed August 1, 2024; and
- *Taiwan Semiconductor Manufacturing Company, Ltd. v. Advanced Integrated Circuit Process LLC*, IPR2025-00832 in the U.S. Patent and Trademark Office, Patent Trial and Appeal Board, filed April 11, 2025.

### C. Lead and Back-up Counsel (37 C.F.R. §42.8(b)(3))

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**D. Service Information (37 C.F.R. §42.8(b)(4))**

Service information is provided in the designation of counsel above. Petitioner consents to electronic service by email to Tim.Xia@troutman.com and Emma.Bennett@troutman.com.

**III. PAYMENT OF FEES UNDER 37 C.F.R. §42.103**

The Office is authorized to charge the fee set forth in 37 C.F.R. §42.15(a)(1) for this Petition to Deposit Account No. DA201507. Review of five claims is requested. The undersigned further authorizes payment for any additional fees that may be due in connection with this Petition.

**IV. CERTIFICATION OF GROUNDS FOR STANDING**

Petitioner certifies under 37 C.F.R. §42.104(a) that the '779 patent is available for IPR and Petitioner is not barred or estopped from requesting IPR of the Challenged Claims on the Grounds identified in this Petition.

**V. OVERVIEW OF CHALLENGE AND REQUESTED RELIEF**

**A. Prior Art Printed Publications**

The '779 patent claims priority to Japanese Foreign Patent Application JP 2010-205599 filed September 14, 2010. Petitioner's challenge is based on the following prior art references, none of which was before the Patent Office during prosecution of the '779 patent:

- **Torii** – U.S. Patent No. 6,881,657 B2 to Torii et al. (Ex.1005) issued on April 19, 2005, and is prior art under §102(b).<sup>1</sup>
- **Gilmer** – U.S. Patent No. 6,787,421 B2 to Gilmer et al. (Ex.1009) issued on September 7, 2004, and is prior art under §102(b).
- **Chen** – U.S. Patent No. 7,382,023 B2 to Chen et al. (Ex.1010) issued on June 3, 2008, and is prior art under §102(b).

**B. Relief Requested**

The specific Grounds of the challenge are set forth below and are supported by the Declaration of Sanjay Banerjee, Ph.D. (Ex.1101).

<b>Ground</b>	<b>Basis</b>	<b>Challenged Claims</b>	<b>Reference(s)</b>
I	§102	1, 2, 7, 12, and 13	Torii (Ex.1005)
II	§103	1, 12, and 13	Gilmer (Ex.1009)
III	§103	1, 12, and 13	Gilmer and Chen (Ex.1010)

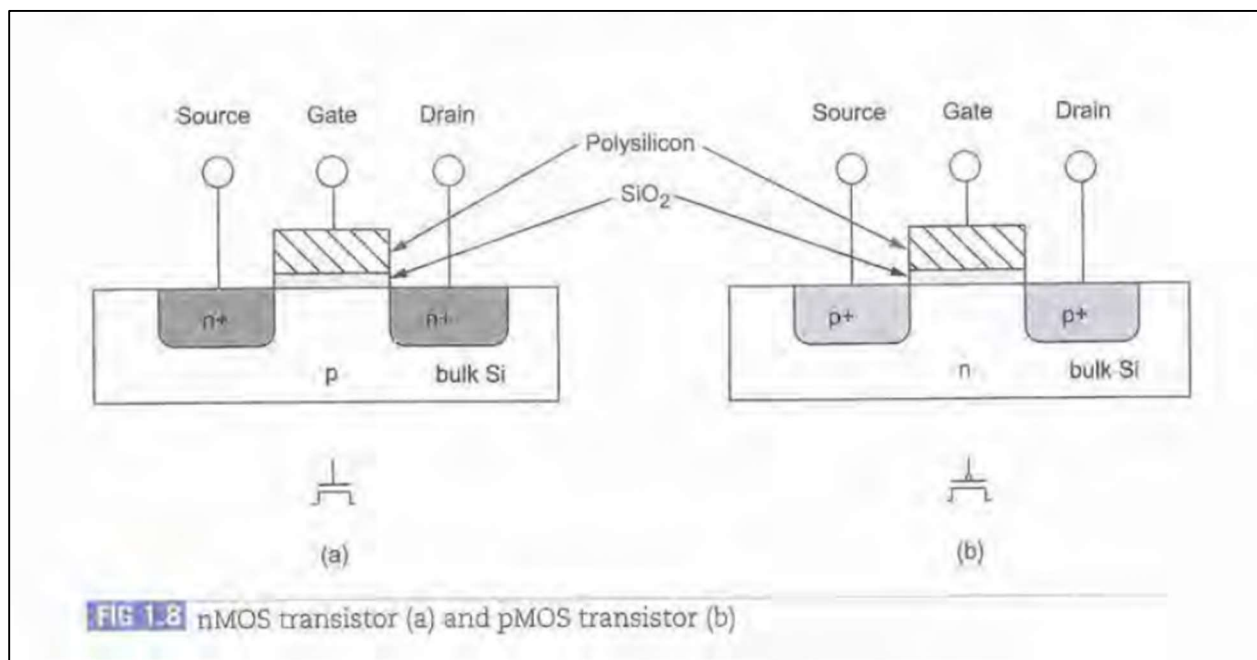
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<sup>1</sup> Cites to 35 U.S.C. §§ 102 and 103 are to the pre-America Invents Act (pre-AIA).

## VI. THE '779 PATENT

### A. Technical Background

A metal-insulating-semiconductor transistor (*e.g.*, a MISFET or MOSFET) generally includes a gate electrode, a gate insulating layer, and “the silicon wafer, also called the substrate, body or bulk.” Ex.1212, 8 (emphasis omitted). An nMOS transistor “is built with a p-type body and has regions of n-type semiconductor adjacent to the gate called the source and drain.” *Id.*, 8, FIG. 1.8(a) (emphasis omitted). A pMOS transistor “is just the opposite, consisting of p-type source and drain regions with an n-type body.” *Id.*, 8, FIG. 1.8(b); Ex.1101, ¶36.



A key device feature is the gate insulating film, commonly referred to as a “gate dielectric,” which separates the gate electrode from the semiconductor channel between the source and drain. For many years, silicon oxides were the primary

materials used for gate dielectrics due to their excellent insulating properties, thermal stability, and compatibility with silicon. However, as transistors scaled down, the silicon-based oxide layer had to become thinner, leading to increased gate leakage due to quantum tunneling. Ex.1213, 5-8. High-k dielectrics, which allow for a thicker gate insulator while maintaining the same capacitance, replaced silicon-based oxides to address these challenges. *Id.*, 8-9. Ex.1101, ¶¶47-53.

Equivalent oxide thickness (EOT) is a key concept used in assessing high-k dielectrics. The EOT ( $t_{eq}$ ) of a material “is defined as the thickness of the SiO<sub>2</sub> layer that would be required to achieve the same capacitance density as the high-k material in consideration.” Ex.1213, 9. The EOT of a gate dielectric having only a high-k layer is given by the following equation:

$$\frac{t_{eq}}{\epsilon_{r,SiO_2}} = \frac{t_{high-k}}{\epsilon_{r,high-k}} \quad (1.1.2)$$

“where  $t_{high-k}$  and  $\epsilon_{r,high-k}$  are the thickness and relative dielectric constant of the high-k material, respectively.” *Id.* For example, “using ZrO<sub>2</sub> as gate dielectric ( $\epsilon_r \approx 20$ )” allows one to “use a 5.1 nm thick layer in order to achieve a capacitance equivalent to a 1 nm thick SiO<sub>2</sub> layer; the equivalent oxide thickness of this ZrO<sub>2</sub> layer is thus 1 nm.” *Id.*; Ex.1101, ¶¶51-52.

The threshold voltage is the voltage applied at the gate that brings the onset of inversion (*i.e.*, formation of the current-carrying channel), which is referred to as the transistor’s “turn-on” voltage. Ex.1211, 526. Because pMOS and nMOS

transistors are built on different dopant type bodies, and feature different types of dopants for their respective source/drain terminals, nMOS transistors, which use electrons in a p-type body to form the channel between the source and drain terminals, have a **positive** threshold voltage and pMOS transistors, which use holes in an n-type body to form the channel between the source and drain terminals, have a **negative** threshold voltage. *See, e.g.*, Ex.1212, 74, 293-296, 302; Ex.1101, ¶¶99-100.

Consumer devices often have multiple transistors of the same conductivity types but with different threshold voltages to cope with various demands on standby power and operation speed. For example, a device may include transistors for low operating power (LOP), transistors for low stand-by power (LSTP), and/or transistors for high performance (HP). Ex.1101, ¶101; Ex.1216, 5. HP transistors have the highest operating speed, the shortest gate length, the thinnest gate oxide, and the lowest threshold voltage among the three. Ex.1216, 11, 17, 21. LSTP transistors are designed for low performance and low leakage current and therefore have thicker gate oxides and higher threshold voltage, while LOP transistors are between the HP and LSTP devices in terms of performance, leakage current, and threshold voltage. *Id.*; Ex.1101, ¶¶101.

Threshold voltage has three main components: flatband voltage ( $V_{FB}$ ), voltage drop across the gate oxide ( $V_o$ ), and semiconductor potential at the semiconductor

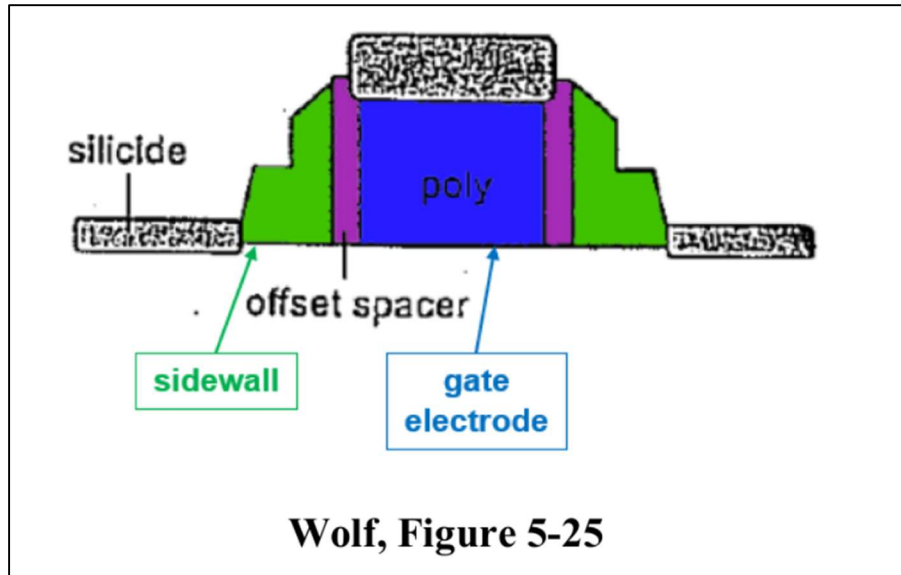
surface during strong inversion ( $\psi_s(inv)$ ). Ex.1223, 175, 178, 194. For a given semiconductor and dielectric material, substrate doping, oxide thickness  $t_{ox}$ , and the metal work function  $\Phi_m$  can be used to predictably tune a transistor's threshold voltage. Ex.1213, 535, 537. When the substrate doping and gate oxide thickness are carefully engineered to control channel mobility and the gate capacitance, respectively, the gate electrode work function can be altered to optimize or fine-tune the threshold voltage further. Ex.1101, ¶¶100-101.

A material's "work function" is "the minimum energy required to bring an electron from the Fermi level to the vacuum level." Ex.1229, 117. However, in MOS/MIS structures, the metal is in direct contact with a dielectric, not with the vacuum. Moreover, work functions of metal gates are highly dependent on material properties and interfaces. To differentiate this, an "effective work function" of the metal gate is commonly used to refer to the metal work function as measured (*e.g.*, through the threshold voltage of the device). Ex.1101, ¶75.

Metal gates are commonly used in gate stacks with high-k gate dielectrics because metal gates eliminate the polysilicon depletion effect, have very low resistance, and have better compatibility with high-k dielectrics (*e.g.*, are immune to Fermi level pinning). Because the work function of a metal is an intrinsic material property that cannot be easily tuned via doping as in the case of polysilicon gates, introducing metal gates into transistors means the threshold voltage of the MOSFET

becomes tied to the metal selection. Ex.1216, 3. Many techniques existed prior to the '779 patent to tune the work function of a metal gate including, for example, adjusting the gate electrode composition and adding metal layer(s). Ex.1101, ¶¶72-81.

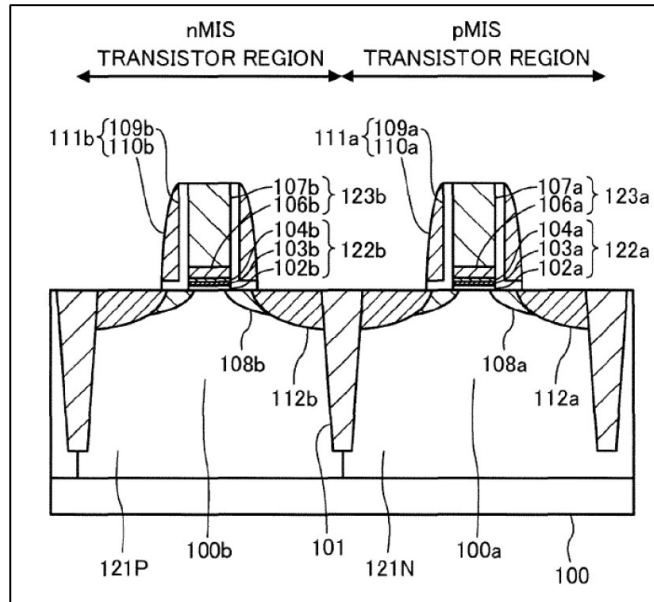
Finally, another common component of semiconductor devices is the sidewall, insulating structures formed on the side surfaces of a gate electrode. The terms “sidewall,” “spacer,” and “sidewall spacer” are often used interchangeably. Ex.1101, ¶¶66-67. Sidewalls can serve a number of purposes, such as defining the source/drain region, providing isolation, protecting the gate during subsequent fabrication, and controlling the width of the gate in the gate length direction. *Id.* For example, the prior art had long disclosed that sidewalls may be used for “[c]ontrolling the position of the edge of the SDE [source/drain extension] region with respect to the gate edge” so as to achieve optimal amount of overlap between the source/drain region and the gate edge. Ex.1214, 217. As shown below, “an offset-spacer is fabricated on the side of the gate after the gate-poly is etched (but before the SDE implant step is carried out . . .),” with offset-spacer width “varied from zero (no-spacer) to some upper-bound (e.g., 50-nm)” to achieve optimum device characteristics.



*Id.*, 217, FIG. 5-25 (annotated).

### **B. The '779 Patent's Background**

The '779 patent describes a conventional “complementary metal insulator semiconductor (CMIS) device composed of an n-type MIS transistor and a p-type MIS transistor which are provided on an identical substrate.” Ex.1001, 1:48-51. The pMIS/nMIS transistors in the conventional device include a gate insulating film having interface layer 102, high-k dielectric 103, and cap layer 104 and a gate electrode having a metal film and a polysilicon film. *See id.*, 1:61-2:31, FIG. 13 (below).



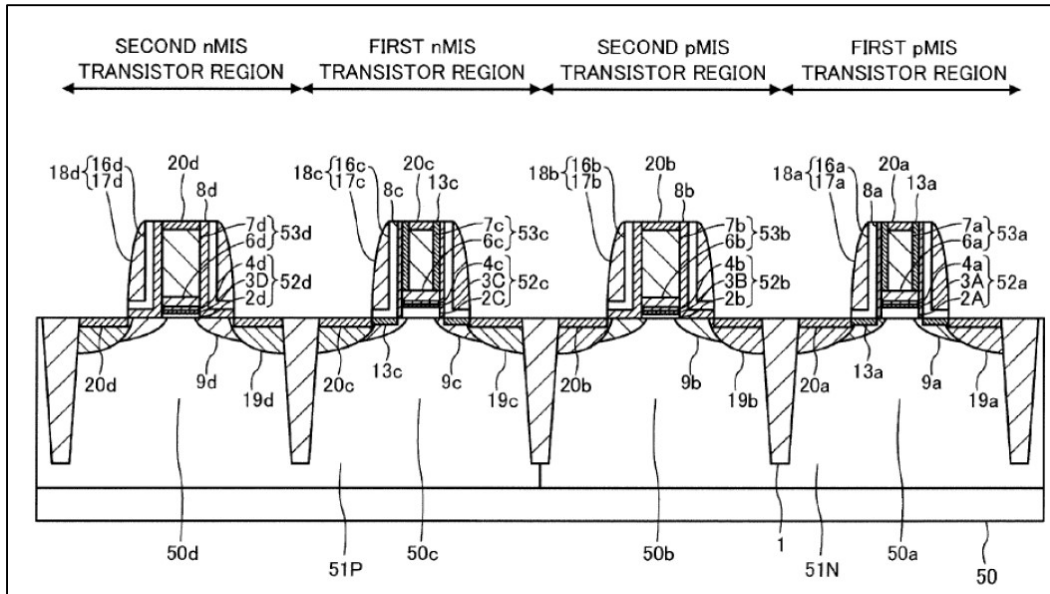
The background section of the '779 patent acknowledges pMIS cap film 104a and nMIS cap film 104b “enable control of a work function of each of the gate electrodes 123a and 123b.” Ex.1001, 2:24-27. The '779 patent also refers to an effective work function of a transistor, which it describes as “a work function obtained from electrical characteristics of a MIS transistor.” *Id.*, 3:18-19. The '779 patent contends that the transistor’s “effective work function is obtained by incorporating influence such as a level in an insulating film into a work function related to physical properties and representing a difference between a vacuum level and an energy level of a metal.” *Id.*, 3:20-24.

**C. Overview of the '779 Patent**

The '779 patent purports to enable “formation of a plurality of transistors of the same conductivity type and different from each other in work function in a semiconductor device having a MIS structure in which a high-k film is used as a gate

insulating film.” Ex.1001, 6:35-39. Thus, the ’779 patent explains that “the present disclosure is useful as a semiconductor device having a CMIS structure including a plurality of MIS transistors different in threshold voltage ( $V_{th}$ ) . . . .” *Id.*, 6:39-43.

In particular, the ’779 patent is directed to a semiconductor device including two MIS transistors of the same conductivity type (P or N) in which the interface layer of one transistor is thicker than the interface layer of the other transistor. Ex.1001, 4:4-37 (“Specifically, a semiconductor device of the present disclosure includes a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate . . . . In the semiconductor device of the present disclosure, the interface layer included in the gate insulating film of the first MIS transistor has a thickness larger than that of the interface layer included in the gate insulating film of the second MIS transistor which is of the same conductivity type as the first MIS transistor.”). Each of the transistors includes a gate electrode (53a-d) with gate insulating film (52a-52d) interposed between the gate electrode and an active region of the substrate (50a-d), as illustrated below:



*Id.*, 8:47-60; FIG. 9. Each gate insulating film includes interface layer 2a-2d, high-k film 3a-3d, and cap film 4a-4d. *Id.*, 8:61-67. The interface layers 2A and 2C in the first nMIS and pMIS regions are thicker than the interface layers 2b and 2d in the second nMIS and pMIS regions. *See id.*, 9:55-10:5.

The '779 patent concludes that the increased interface layer thickness of the first pMIS and nMIS transistors leads to an increased EOT, which results in an increased “effective work function of the transistors”: “Accordingly, the EOT of the gate insulating film 52a of the first pMIS transistor and that of the gate insulating film 52c of the first nMIS transistor increase, thereby causing the effective work functions of the first pMIS transistor and the first nMIS transistor to increase.” *Ex.1001*, 13:23-27; *see also id.*, 12:47-54, 13:19-23.

**D. Prosecution History of the '779 Patent**

During prosecution of the application that led to the '779 patent, the Examiner rejected the only independent semiconductor device claim as anticipated by U.S. Patent No. 8,492,230 to Ishikawa, et al. (“Ishikawa”). Ex.1002, 204-205. In response, the Applicant argued that Ishikawa’s gate insulating films “are formed above different base substrate[s]” and therefore Ishikawa does not anticipate claim 1. *Id.*, 300-301. Notably, the Applicant did not dispute that Ishikawa discloses two transistors with different interface layer thicknesses. *See id.* The applicant also amended claim 1 to recite “each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film.” *Id.*, 294. The Examiner subsequently allowed the claims. *Id.*, 312-313.

**VII. PERSON OF ORDINARY SKILL IN THE ART**

A person of ordinary skill in the art (“POSITA”) of the subject matter of the '779 patent would have had at least a Master’s degree in electrical engineering, physics, chemistry, materials science, or a related field, and three years of work experience in semiconductor design and manufacturing, including with respect to planar transistors, or equivalent work experience. Ex.1101, ¶¶115-117. Additional graduate education might compensate for a deficiency in experience, and vice-versa. *Id.*

## VIII. CLAIM CONSTRUCTION

Claims in an IPR are construed under *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). See 37 C.F.R. §42.100(b).

Petitioner does not believe any terms need be construed to resolve the issues presented in this Petition, and Petitioner takes no position regarding claim construction at this time. The Challenged Claims are unpatentable under their plain and ordinary meaning. Ex.1101, ¶¶119-120. Petitioner reserves the right to respond to any purported claim constructions that Patent Owner raises.

## IX. OVERVIEW OF PRIOR ART

### A. Torii (Ex.1005)

Torii discloses “a semiconductor device having a plurality of transistors comprising gate insulating films of different film thickness.” Ex.1005, 1:11-14.

As background, Torii notes that logic transistors require a lower driving voltage to reduce power consumption. *Id.*, 1:24-25. Torii further notes that to avoid lowering the driving current when the driving voltage is reduced, “the thickness of the gate insulating film . . . has been reduced.” *Id.*, 1:26-30.

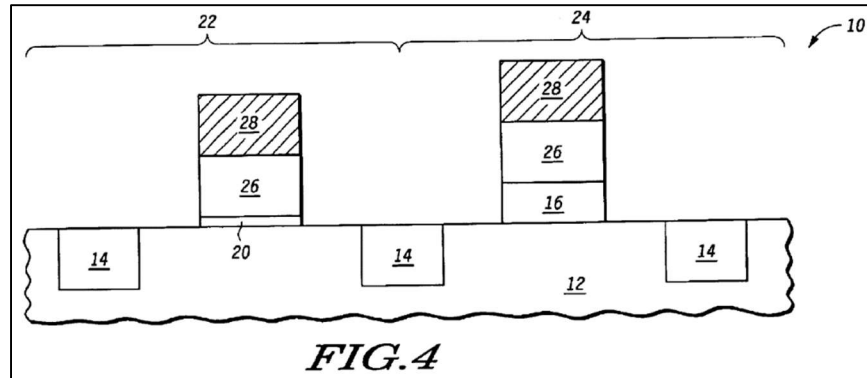
Torii further notes that a transistor “used in the peripheral circuit portions accompanying inputs and outputs must be directly driven by an external voltage,” and that therefore “a high withstand voltage is required in the MOSFET used in the peripheral circuit portions, and a gate insulating film having a large film thickness to some extent is required.” Ex.1005, 1:31-38.

Torii explains, “[w]hen a logic circuit portion and a peripheral circuit portion are formed in a semiconductor device, the gate insulating films of the different thickness require to be formed in these circuit portions on a substrate.” Ex.1005, 1:41-44. Torii goes on to describe known methods “for forming gate insulating films of different thickness.” *Id.*, 1:44-2:16.

Finding conventional methods lacking, however, Torii provides “a semiconductor device wherein gate insulating films highly controlled their thickness are formed when a plurality of transistors are formed on a chip, even if the difference between the thickness of the gate insulating films is small” (*sic*), as well as a method for making such a device. Ex.1005, 3:54-61. That is, for three transistors (LOP, LSTP, and high voltage), “gate insulating films [of] different thickness are formed.” *Id.*, 5:58-61.

**B. Gilmer (Ex.1009)**

Gilmer discloses a semiconductor device “having dual gate dielectric thicknesses and utilizing high-k gate dielectric materials such as metal oxides.” Ex.1009, 1:7-10. Gilmer’s device 10 includes transistors in core region 22 and I/O region 24. *See id.*, 4:43-47, FIG. 4 (below).



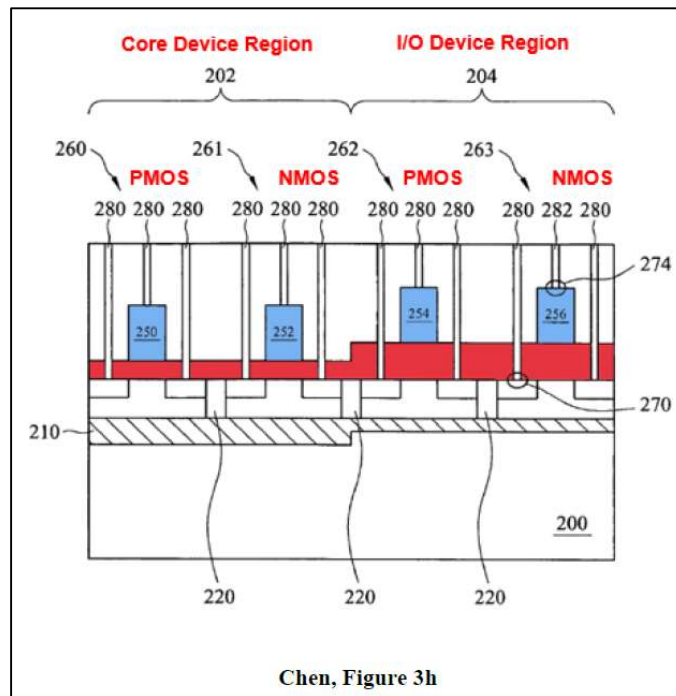
Core transistor 22 includes a gate stack having gate dielectric 20, high-k dielectric (metal oxide) 26, and gate electrode 28. *Id.*, 4:35-38. I/O transistor 24 includes gate dielectric 16, high-k dielectric (metal oxide) 26, and gate electrode 28. *Id.*, 4:35-38.

**C. Chen (Ex.1010)**

Chen explains that “to produce competitive electronic devices, it is often desired to produce semiconductor chips with several different regions (e.g., core region, low power region, I/O region) having semiconductor devices that vary according to speed and power, for example.” Ex.1010, 1:18-22. These devices have different threshold voltages, with the I/O devices having the highest threshold voltage and low operating power transistors having the lowest voltage. *Id.*, 2:25-28.

Chen’s device, illustrated below, includes a pMOS transistor with a first metal alloy gate electrode and a nMOS transistor with an n-doped first metal alloy gate electrode in a first device region and a pMOS transistor with a second metal alloy gate electrode and a nMOS transistor with an n-doped second metal alloy gate

electrode in a second device region.<sup>2</sup> Ex.1010, 8:13-18, FIG. 3h (annotated) (below). The gate electrode 252 of the first region nMOS transistor has a work function ranging between about 4.2 eV and about 4.5 eV and the gate electrode 256 of the second region nMOS transistor has a higher work function, ranging between about 4.5 eV and about 4.8 eV. *Id.*, 8:38-42.



<sup>2</sup> Chen has a typographic error referring to devices 260 and 261 as pMOS devices and devices 262 and 263 as nMOS devices. *See* Ex.1010, 8:27-29. A POSITA would have understood devices 260 and 262 to be pMOS devices and devices 261 and 263 to be nMOS devices based on discussions, *e.g.*, in columns 3, 7, and 9 and claim 31. Ex.1101, ¶152.)

Chen teaches that “[v]arying the material composition, and thereby the work function of the gate electrodes 250, 252, 254, and 256, provides a corresponding difference in voltage threshold” between devices 260, 261, 262, and 263. Ex.1010, 8:29-33. That is, the voltage thresholds of the transistors “are partially controlled by the work function of” their respective gate electrodes. *Id.*, 8:33-36.

## **X. SPECIFIC GROUNDS FOR PETITION**

### **A. Ground I (Torii)**

Torii anticipates under 35 U.S.C. § 102 claims 1, 2, 7, 12, and 13 of the ’779 patent. Ex.1101, ¶¶154-184.

#### **1. Independent Claim 1**

##### **a. Preamble: “A semiconductor device comprising:”**

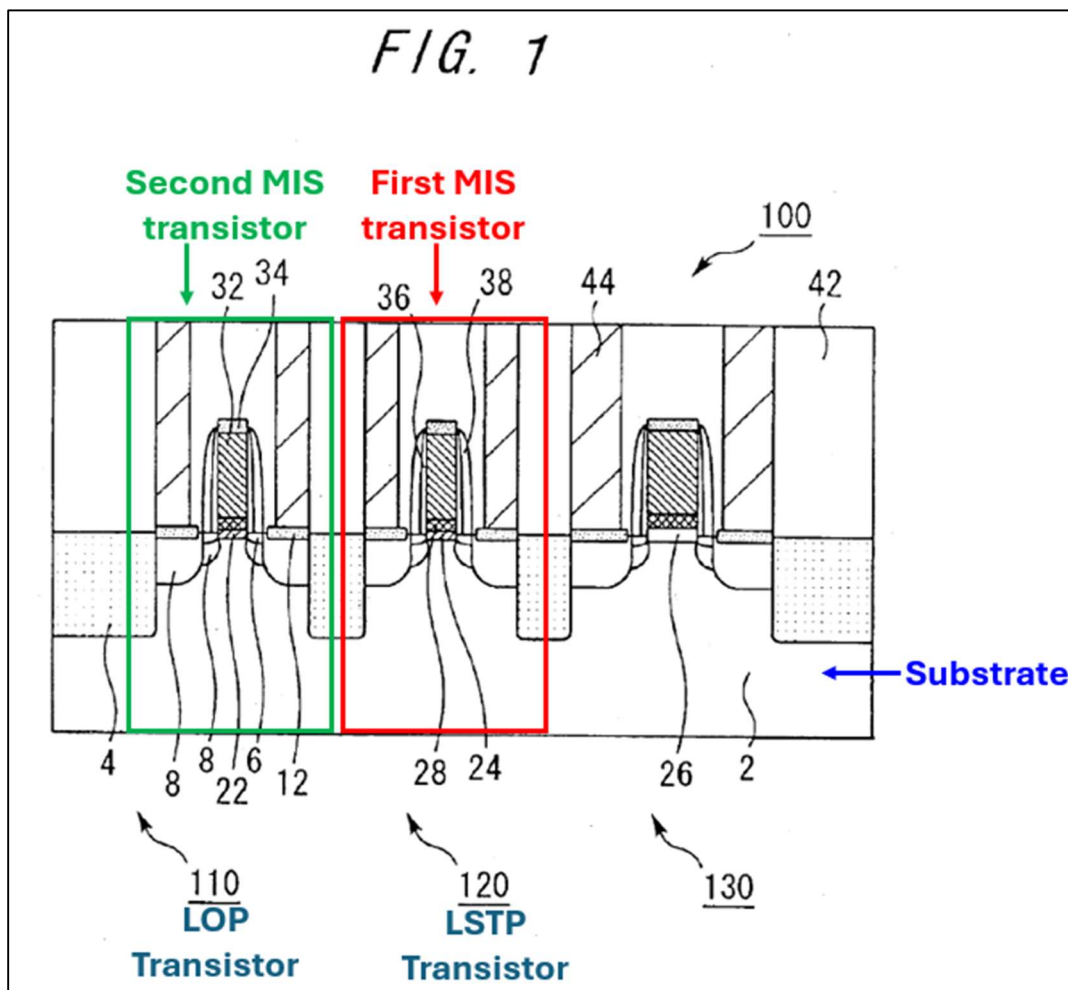
Torii discloses this limitation. Ex.1101, ¶155. Torii is directed to a semiconductor device. Ex.1005, 1:9-10 (“The present invention relates to a semiconductor device and a method for manufacturing a semiconductor device.”)

##### **b. Limitation 1[a]: “a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate,”**

Torii discloses this limitation. Ex.1101, ¶¶156-157. As can be seen in Figure 1 below, Torii teaches a semiconductor device comprising three MIS transistors: one for low operating power (LOP) (element 110), one for low stand-by power (LSTP) (element 120), and one for high withstand voltage (HWV) (element 130). Ex.1101, ¶156; Ex.1005, 4:61-67. For purposes of this Ground, Petitioner identifies the LSTP

transistor 120 as the claimed “first MIS transistor” and the LOP transistor 110 as the claimed “second MIS transistor.”

The first (LSTP) transistor 120 and the second (LOP) transistor 110 are of identical conductivity type, n-type in this embodiment. Ex.1005, 6:24-27, 10:39-45; Ex.1101, ¶157. Further, both the first transistor and the second transistor are formed on an identical semiconductor substrate, indicated by element 2 in Figures 1 and 9:

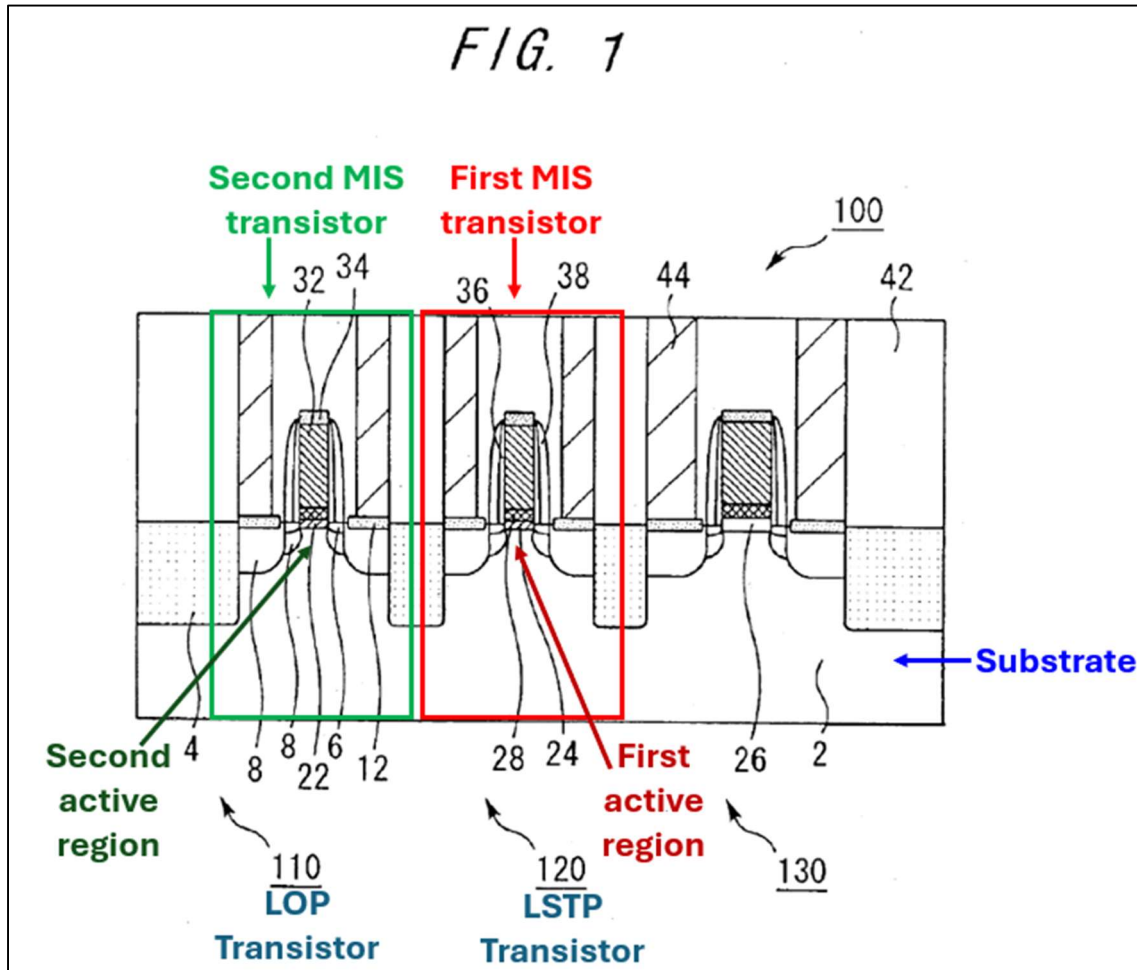


Ex.1005, Figure 1

Ex.1005, 5:1-4, FIGS. 1 (annotated), 9; Ex.1101, ¶157.

- c. **Limitation 1[b]: “wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film,”**

Torii discloses this limitation. Ex.1101, ¶¶158-161. For example, Torii teaches a first MIS transistor (LSTP transistor 120), outlined below in red.

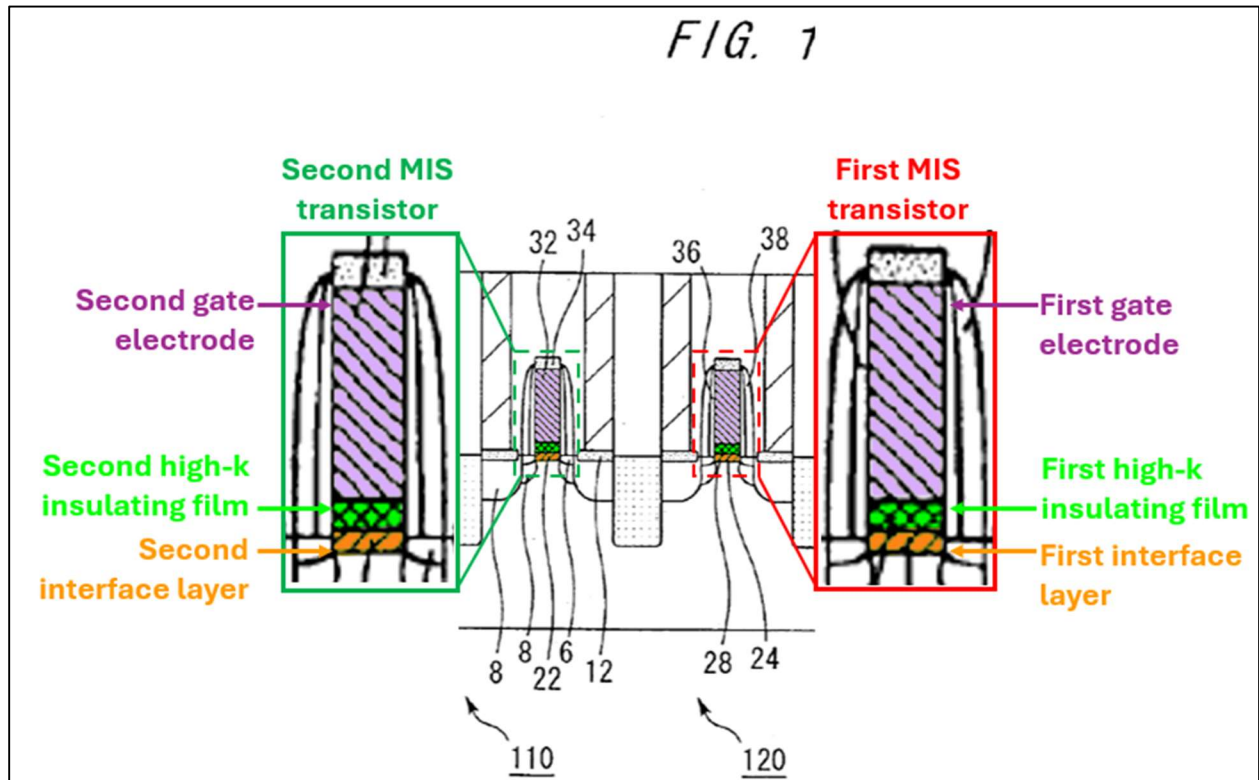


Ex.1005, Figure 1

Ex.1005, FIG. 1 (annotated).

The LSTP transistor 120 includes a first gate insulating film 24 and 28 collectively, formed on the active region in the semiconductor substrate. Ex.1101,

¶159; Ex.1005, 5:37-41 (“In each of MISFET 110, 120, and 130 for LOP, LSTP, and for high withstand voltage, respectively, a high-k film 28 is laminated on the silicon oxynitride films 22 and 24 or the thermally-oxidized film 26, thereby each gate insulating film is formed.”)



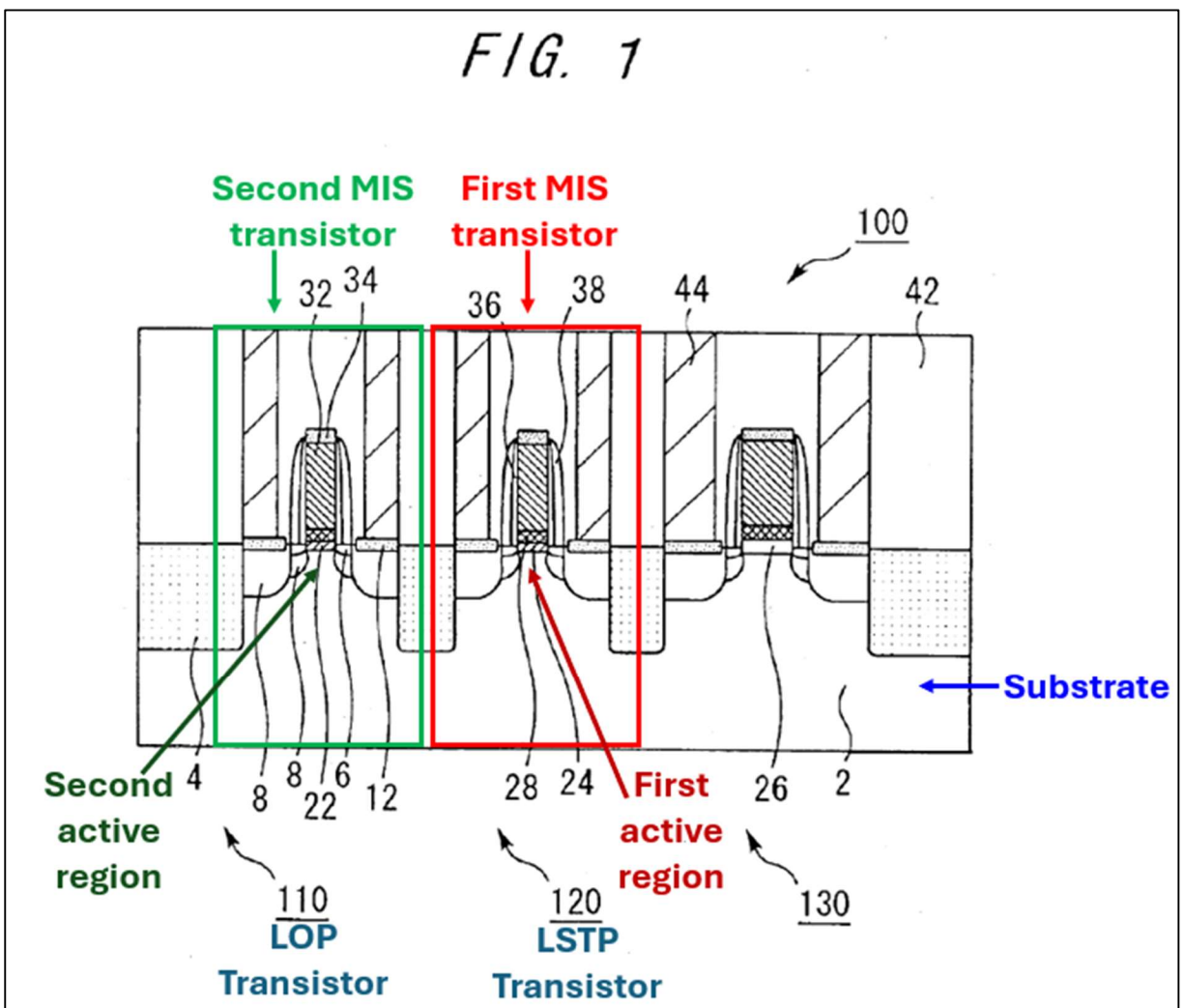
**Ex.1005, Excerpt from Figure 1 with enlargements**

Ex.1005, FIG. 1 (annotated). “The MISFET for LSTP 120 is a low-standby-power transistor using the laminated film of the silicon oxynitride film 24 and the high-k film 28 as gate insulating film . . . .” Ex.1005, 5:65-6:3.

The LSTP transistor 120 also includes a first gate electrode 32 formed on the first gate insulating film. Ex.1101, ¶160; Ex.1005, 5:42 (“On each high-k film 28, a gate electrode 32 is formed.”)

- d. **Limitation 1[c]: “the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film,”**

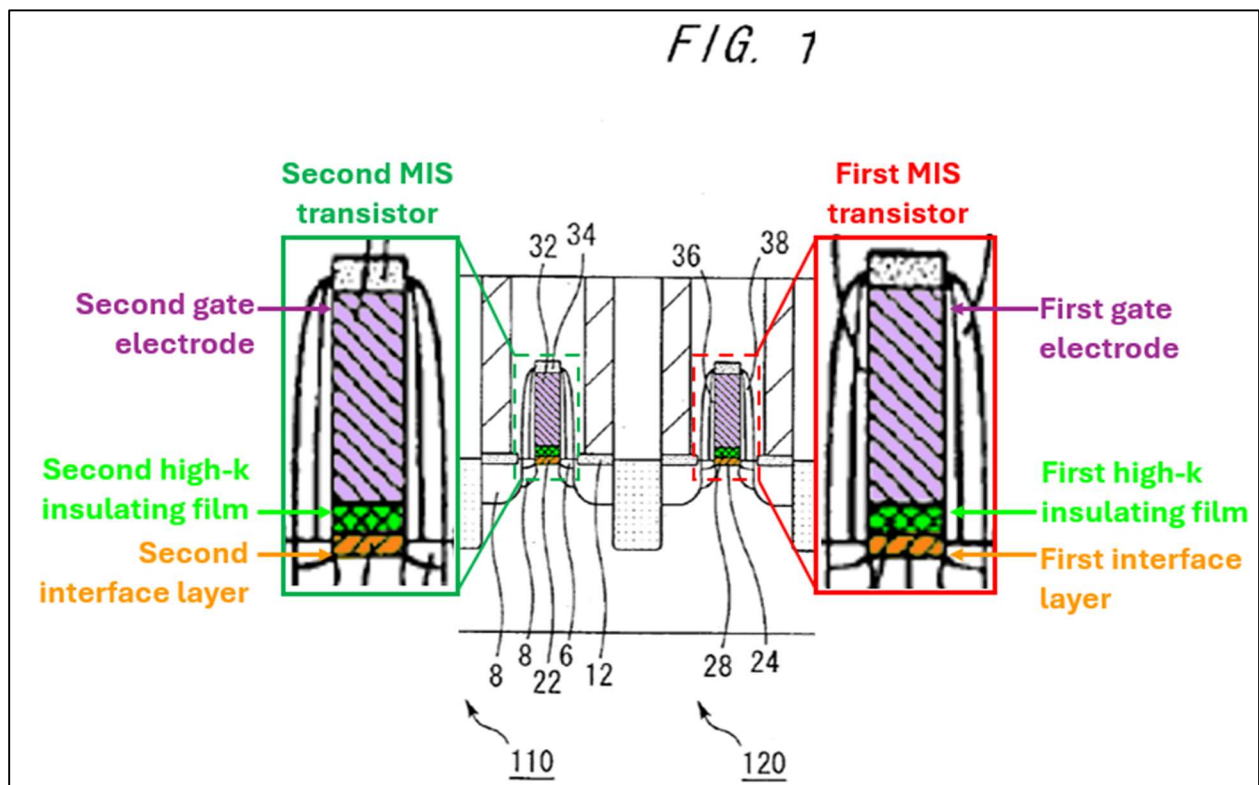
Torii discloses this limitation. Ex.1101, ¶¶162-165. For example, Torii teaches a second MIS transistor (LOP transistor 110), outlined below in green. Ex.1101, ¶162; Ex.1005, 4:61-67 (“MISFET . . . 110 for LOP”).



Ex.1005, Figure 1

Ex.1005, FIG. 1 (annotated).

The second transistor 110 includes a second gate insulating film 22 and 28, collectively, formed on the active region in the semiconductor substrate. Ex.1101, ¶163; Ex.1005, 5:37-41 (“In each of MISFET 110, 120, and 130 for LOP, LSTP, and for high withstand voltage, respectively, a high-k film 28 is laminated on the silicon oxynitride films 22 and 24 or the thermally-oxidized film 26, thereby each gate insulating film is formed.”)



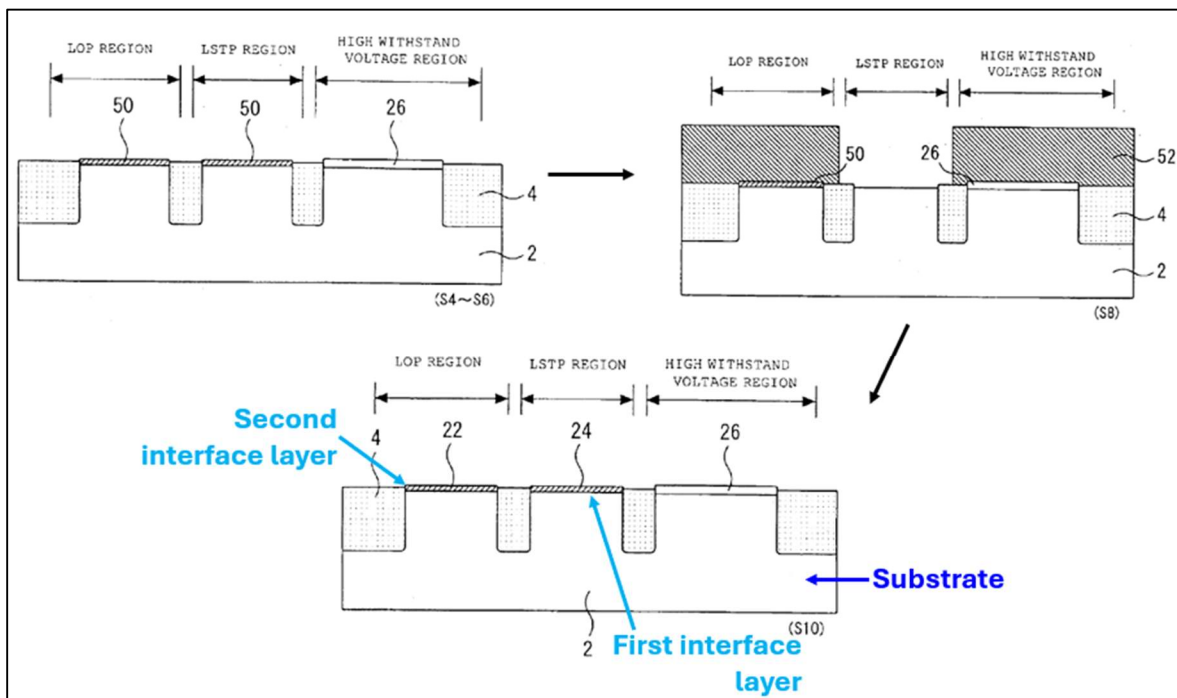
**Ex.1005, Excerpt from Figure 1 with enlargements**

Ex.1005, FIG. 1 (annotated). “[T]he MISFET for LOP 110 is a low-power-consumption transistor included (*sic*) the laminated film of the silicon oxynitride film 22 and the high-k film 28 as gate insulating film . . . .” Ex.1005, 5:62-65.

The second transistor 110 also includes a second gate electrode 32 formed on the second gate insulating film. Ex.1101, ¶164; Ex.1005, 5:42 (“On each high-k film 28, a gate electrode 32 is formed.”)

- e. **Limitation 1[d]: “the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer,”**

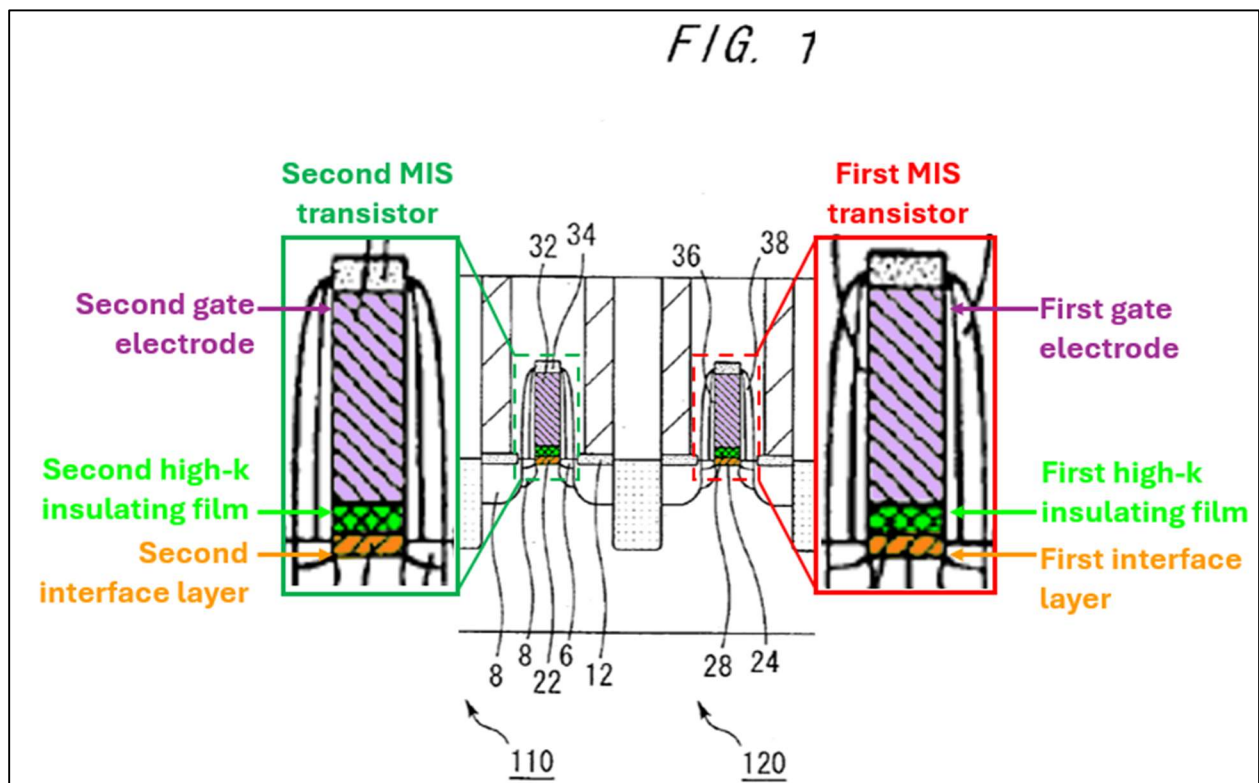
Torii discloses this limitation. Ex.1101, ¶¶166-167. In the first MIS transistor (*i.e.*, LSTP transistor 120), there is “a silicon oxynitride film 24” formed “as an interfacial gate insulating film.” Ex.1101, ¶166; Ex.1005, 5:14-18. This film is formed “on the Si substrate 2” and is the claimed first interface layer for purposes of this Ground. Ex.1005, 5:14-18.



Ex. 1005, Figures 4 (top-left), 5 (top-right), 6 (bottom)

Ex.1005, FIGS. 4-6 (annotated).

On top of the interfacial gate insulating film (*i.e.*, the first interface layer), there is a high dielectric constant (high-k) insulating film. Ex.1101, ¶167; Ex.1005, 5:33-36 (“On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia (HfO<sub>2</sub>) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed.”).

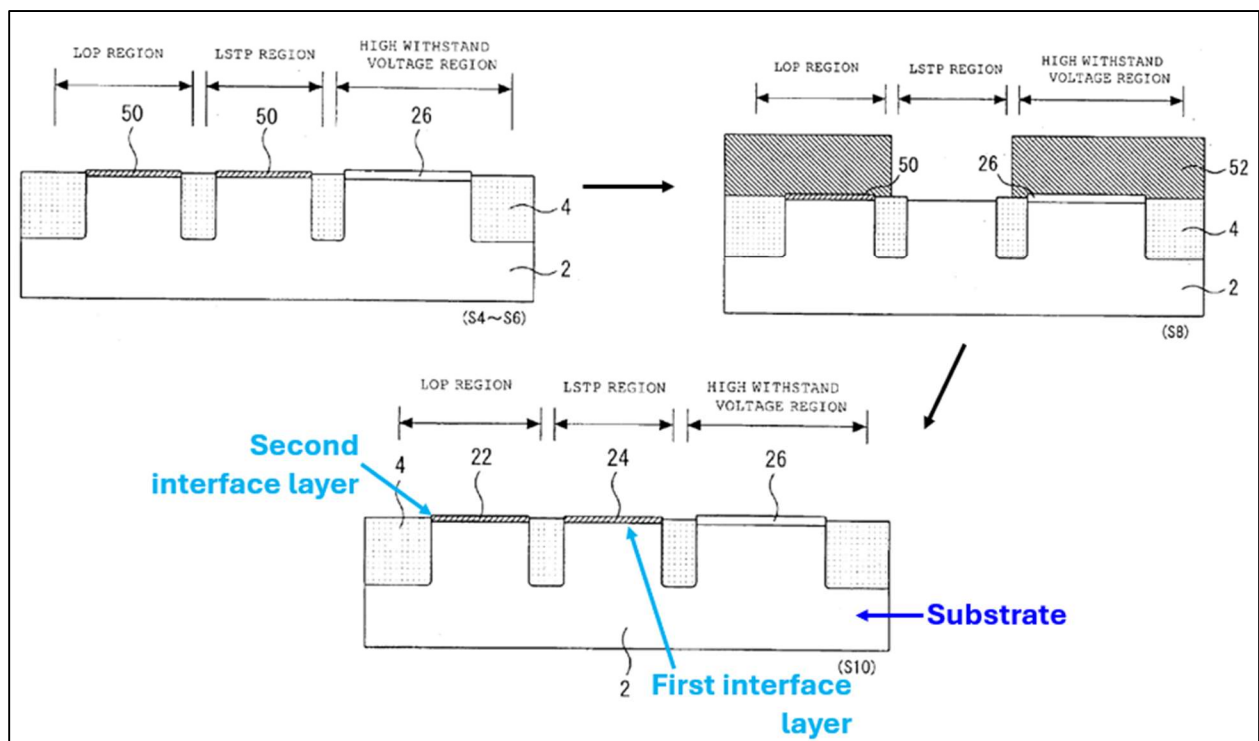


**Ex.1005, Excerpt from Figure 1 with enlargements**

Ex.1005, FIG. 1 (annotated).

- f. **Limitation 1[e]: “the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer,”**

Torii discloses this limitation. Ex.1101, ¶¶168-169. In the second MIS transistor (*i.e.*, LOP transistor 110), there is “a silicon oxynitride film 22 . . . formed as an interfacial gate insulating film.” Ex.1101, ¶168; Ex.1005, 5:14-18. This film is formed “on the Si substrate 2” and is the claimed second interface layer for purposes of this Ground. *Id.*

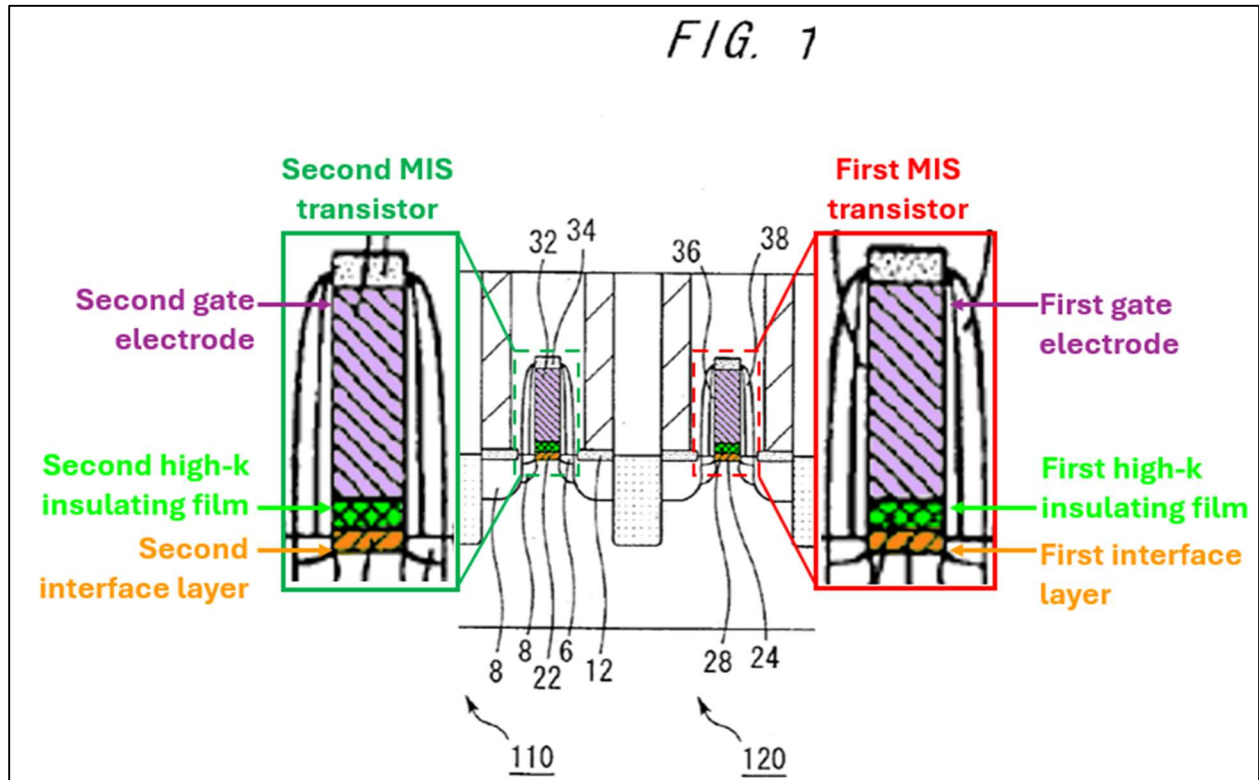


**Ex. 1005, Figures 4 (top-left), 5 (top-right), 6 (bottom)**

Ex.1005, FIGS. 4-6 (annotated).

On top of the interfacial gate insulating film, there is a high dielectric constant (high-k) insulating film. Ex.1101, ¶169; Ex.1005, 5:33-36 (“On each of the silicon

oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia ( $\text{HfO}_2$ ) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed.”).



Ex.1005, Excerpt from Figure 1 with enlargements

Ex.1005, FIG. 1 (annotated).

- g. **Limitation 1[f]: “the first interface layer has a thickness larger than that of the second interface layer, and”**

Torii discloses this limitation. Ex.1101, ¶170. In the first (LSTP) transistor 120, the first interface layer 24 is “about 1.3 nm” thick. Ex.1101, ¶170; Ex.1005, 5:23-25. In the second (LOP) transistor 110, the second interface layer 22 is “about

0.9 to 0.95 nm” thick. *Id.*, 5:20-22. The first interface layer 24 is therefore thicker than the second interface layer 22. Ex.1101, ¶170.

**h. Limitation 1[g]: “each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film.”**

Torii discloses this limitation. Ex.1101, ¶171. In the first (LSTP) transistor 120, the first interface layer 24 is “silicon oxynitride film 24.” Ex.1101, ¶171; Ex.1005, 5:23-25. In the second (LOP) transistor 110, the second interface layer 22 is “a silicon oxynitride film 22.” *Id.*, 5:14-17.

**2. Dependent Claim 2**

**a. Limitation 2[a]: “The semiconductor device of claim 1, wherein the first gate electrode includes first sidewall spacers formed on side surfaces thereof and first insulating spacers interposed between the first gate electrode and the first sidewall spacers,”**

Torii discloses this limitation. Ex.1101, ¶¶172-176. “On the sidewalls of each gate electrode 32 and the underlying gate insulating film, sidewall spacers 36 and 38 are formed.” Ex.1005, 5:49-51.

The inner spacers 36 are the first insulating spacers for purposes of this Ground. Ex.1005, 7:23-26 (“[O]n the sidewalls of each gate electrode 32 and each underlying gate insulating film of regions for LOP, LSTP, and high withstand voltage, sidewall spacers 36 are formed.”). These inner spacers are silicon nitride, which is an insulator. Ex.1101, ¶172; Ex.1005, 7:23-27 (“a silicon nitride film”). The inner spacers 36 are about 5 nm thick. Ex.1005, 7:23-28.

The outer sidewall spacers 38 in Torii comprise a triple layer structure, with an inner layer of silicon oxide about 15 nm thick (referred to hereafter as “38a”), a middle layer of silicon nitride about 25 nm thick (referred to hereafter as “38b”), and an outer layer of silicon oxide about 35 nm thick (referred to hereafter as “38c”). Ex.1101, ¶173; Ex.1005, 7:38-43 (“Next, as FIG. 9 shows, sidewall spacers 38 are further formed on the sidewall spacers 36 (Step S26). Concretely, a silicon oxide film [38a]<sup>3</sup>, a silicon nitride film [38b], and a silicon oxide film [38c] are deposited in this order on the entire surface of the substrate. At this time, the thicknesses of the films are about 15 nm, about 25 nm, and about 35 nm, respectively.”). After deposition, a series of anisotropic etching is performed to form the sidewall spacers 38, including “anisotropic dry etching . . . using the silicon nitride film of the middle layer as the etching stopper to etch the overlying silicon oxide film,” “anisotropic dry etching using the underlying silicon oxide film as the etching stopper” to remove the silicon nitride film on the surface of the substrate, and removing the remaining silicon oxide film “using wet etching.” Ex.1005, 7:44-50. Anisotropic etching is vertical etching that would remove the films from the surface of the substrate but leave the horizontal thicknesses of the different sidewall layers formed on sidewall spacer 36 relatively unchanged. *Id.*, 7:50-53 (“Thereby, sidewall spacers 38 each

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<sup>3</sup> Bracketed element callouts added.

composed of a silicon oxide film, a silicon nitride film, and a silicon oxide film are formed on the outside of each sidewall spacer 36.”); Ex.1101, ¶174.

Elements 38a, the inner silicon oxide layer of elements 38 on the LSTP transistor, are the claimed first sidewall spacers for purposes of this Ground.<sup>4</sup> Ex.1101, ¶175. Elements 38 “are further formed on the [inner] sidewall spacers 36.” Ex.1005, 7:38-39.

The inner spacers 36 are therefore interposed between the gate electrode and the first sidewall spacers 38a. Ex.1101, ¶176. The first insulating spacers (*i.e.*, inner

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<sup>4</sup> Petitioner respectfully notes that Patent Owner’s infringement contentions in the Eastern District of Texas assert infringement in exactly this way. That is, Patent Owner alleges the first and second transistors of the accused products have the same four-layered sidewall structure, an oxide-nitride-oxide-nitride (just like the sidewall structures of the LOP, LSTP, and HWV transistors in Torii). Patent Owner asserts infringement by pointing to the inner two oxide-nitride layers for one claimed transistor and the outer two oxide-nitride layers for the second claimed transistor. Patent Owner has designated the infringement contentions as confidential, and Petitioner reserves the right to seek discovery of them for this IPR if Patent Owner argues inconsistent positions.

spacers 36) and the first sidewall spacers (inner silicon oxide layer 38a) are formed on side surfaces of the first gate electrode (*i.e.*, of LSTP transistor 120).

**b. Limitation 2[b]: “the second gate electrode includes second sidewall spacers formed on side surfaces thereof and second insulating spacers interposed between the second gate electrode and the second sidewall spacers, and”**

Torii discloses this limitation. Ex.1101, ¶¶177-180. As discussed above, the outer sidewall spacers 38 in Torii comprise a triple layer structure, with an inner layer of silicon oxide about 15 nm thick, a middle layer of silicon nitride about 25 nm thick, and an outer layer of silicon oxide about 35 nm thick. Ex.1101, ¶177; Ex.1005, 7:38-43 (“Next, as FIG. 9 shows, sidewall spacers 38 are further formed on the sidewall spacers 36 (Step S26). Concretely, a silicon oxide film [38a], a silicon nitride film [38b], and a silicon oxide film [38c] are deposited in this order on the entire surface of the substrate. At this time, the thicknesses of the films are about 15 nm, about 25 nm, and about 35 nm, respectively.”). Ex.1101, ¶177.

The claimed second insulating spacers are the middle silicon nitride layers 38b of elements 38 on the LOP transistor for purposes of this Ground. Ex.1101, ¶178. These second insulating spacers are deposited about 25 nm thick and would have the same thicknesses relative to the two silicon oxide layers 38a and 38c and silicon nitride film 36 after anisotropic etching. Ex.1005, 7:38-53; Ex.1101, ¶178. The outer silicon oxide layers 38c of elements 38 of the LOP transistor are the

claimed second sidewall spacers for purposes of this Ground. Ex.1101, ¶179. The second insulating spacers (*i.e.*, middle silicon nitride layers 38b) and the second sidewall spacers (*i.e.*, outer silicon oxide layers 38c) are formed on side surfaces of the second gate electrode (*i.e.*, of LOP transistor 110). Ex.1101, ¶179.

**c. Limitation 2[c]: “the first insulating spacers are thinner than the second insulating spacers.”**

Torii discloses this limitation. Ex.1101, ¶181. As described above, the first insulating spacers are inner spacers 36 on the LSTP transistor for purposes of this Ground, which are about 5 nm thick. Ex.1005, 7:26-28. As also described above, the second insulating spacers for purposes of this Ground are element 38b (*i.e.*, middle silicon nitride layers of element 38) on the LOP transistor, which are about 25 nm thick. Ex.1005, 7:38-43.

Therefore, the first insulating spacers are thinner than the second insulating spacers. Ex.1101, ¶181.

**3. Dependent Claim 7**

**a. Limitation 7: “The semiconductor device of claim 2, wherein each of the first insulating spacers and the second insulating spacers is made of a silicon nitride film.”**

Torii discloses this limitation. Ex.1101, ¶182. Both inner spacer 36 (*i.e.*, first insulating spacer) on the LOP transistor and middle silicon nitride layers 38b (*i.e.*, second insulating spacer) on the LSTP transistor are made of a silicon nitride film. Ex.1005, 7:26-28, 7:38-43. Ex.1101, ¶182.

**4. Dependent Claim 12**

- a. Limitation 12: “The semiconductor device of claim 1, wherein each of the first and second high dielectric constant insulating films contains hafnium or zirconium.”**

Torii discloses this limitation. Ex.1101, ¶183. Both the first and the second high-k films are made of hafnia (*i.e.*, hafnium dioxide), which contains hafnium. Ex.1101, ¶183; Ex.1005, 5:33-36 (“On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia (HfO<sub>2</sub>) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed.”).

**5. Dependent Claim 13**

- a. Limitation 13: “The semiconductor device of claim 1, wherein the first and second high dielectric constant insulating films are equal in thickness.”**

Torii discloses this limitation. Ex.1101, ¶184. Both the first and the second high-k films are about 3 nm in thickness. Ex.1101, ¶184; Ex.1005, 5:33-36 (“On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia (HfO<sub>2</sub>) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed.”).

**B. Ground II (Gilmer)**

Gilmer renders obvious under 35 U.S.C. § 103 claims 1, 12, and 13 of the '779 patent. Ex.1101, ¶¶185-213.

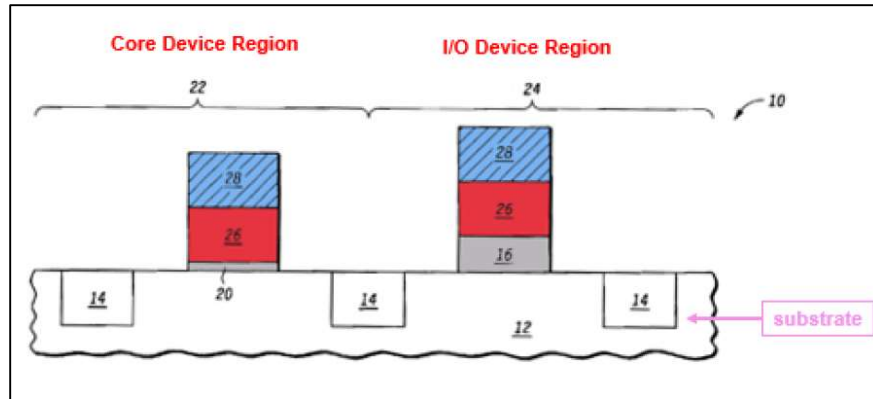
**1. Independent Claim 1**

**a. Preamble: “A semiconductor device comprising:”**

Gilmer discloses this limitation. Ex.1101, ¶¶186-209. Specifically, Gilmer discloses that “[t]he present invention relates generally to semiconductor devices, and more particularly to semiconductor devices formed having dual gate dielectric thicknesses and utilizing high-k gate dielectric materials such as metal oxides.” Ex.1009, 1:7-10; Ex.1101, ¶186.

**b. Limitation 1[a]: “a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate,”**

Gilmer teaches or at least suggests this limitation. Ex.1101, ¶¶187-196. Gilmer discloses a substrate. Ex.1009, 2:38-39 (“[S]emiconductor device 10 includes a semiconductor substrate 12.”) Gilmer also discloses two transistors provided on the same substrate. Ex.1101, ¶187; Ex.1009, FIG. 4, elements 22 and 24, and, *e.g.*, 4:35-47 (“conventional processing occurs to complete the transistor and integrated circuit formation”). In particular, core device region 22 and I/O device region 24 each includes a transistor, as illustrated below.



Ex.1009, FIG. 4 (annotated).

These two transistors (*i.e.*, I/O region transistor 24 and core region transistor 22) are MIS transistors. Ex.1101, ¶188. The gate stacks of both transistors include gate dielectric 16/20, high-k metal oxide layer 26, and gate electrode material 28. Ex.1009, 4:40-41, 2:46-48 (dielectric 16), 3:9-11 (dielectric 20), 3:44-47 (high-k layer), 4:38-40 (gate electrode), FIG. 4. Gate dielectric 16, gate dielectric 20, and high-k metal oxide 26 are each dielectrics (insulators) and gate electrode material 28 is “conductive (doped) polysilicon or a metal (e.g., titanium nitride).” Ex.1009, 2:38-40. Each transistor therefore has a metal-insulator-silicon (MIS) structure. Ex.1101, ¶188.

These two transistors are of an identical conductivity type, or at least, it would have been obvious to a POSITA to make the two transistors of the same type. Ex.1101, ¶189.

First, Gilmer provides I/O transistors (with higher voltage requirements) and logic transistors (with lower voltage requirements) having interface layers of

different thicknesses. Ex.1009, 2:60-65 (discussing voltages for core and I/O devices). Gilmer compares electrical characteristics of these I/O and core transistors. Ex.1009, 2:58-65 (discussing voltages for core and I/O devices). A POSITA would have understood such comparisons apply to transistors of an identical conductivity type. Ex.1101, ¶190.

Second, Gilmer extensively discusses the concept of Dual Gate Oxide (DGO), which relates to the formation of transistors having different gate dielectric thickness on the same semiconductor substrate or wafer. Ex.1009, 1:13-19. A POSITA would have understood the core and I/O transistors of Gilmer formed by DGO process to have the same conductivity type. Ex.1101, ¶191.

Third, a substrate typically has a conductivity type (*e.g.*, n-type or p-type). To form a transistor of a different conductivity type on the same substrate, a structure (*e.g.*, a well) having a different conductivity type must be present in the substrate. Ex.1101, ¶192. A POSITA would ascertain from Gilmer's description that both transistors share at least the same conductivity type because Gilmer does not disclose (i) the formation of any particular doped regions (*i.e.*, wells) within the substrate in either the core or I/O regions which would provide for a conductivity type separate from that of the substrate, or (ii) any indication that each of the transistors in the core or I/O regions are formed on different conductivity type regions (*i.e.*, wells) on the substrate. Ex.1101, ¶192.

Fourth, a POSITA would have further understood CMOS was the dominant processing technology in the semiconductor industry prior to the '779 patent. Ex.1101, ¶193. CMOS processing technology integrates both n- and p-type MOS devices side-by-side. *Id.* Therefore, although only one is depicted in Gilmer's figures, a POSITA would have understood the I/O device had both an n-type and a p-type transistor and the core device had both an n-type and p-type device. *Id.* That is, for every pair of DGO nMOS transistors, there is a corresponding pair of DGO pMOS transistors. *Id.*

Additionally, making both transistors the same conductivity type would have been obvious to try. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 421 (2007). A POSITA would have understood only two alternatives exist for the conductivity type of Gilmer's transistors: (1) core and I/O transistors are of an identical conductivity type or (2) core and I/O transistors are of different conductivity types. Ex.1101, ¶194.

A POSITA would have had a reasonable expectation of success in pursuing both alternatives. Ex.1101, ¶195. Forming transistors of the same conductivity type (*e.g.*, nMIS/nMOS or pMIS/pMOS transistors) in a substrate was well-known long before the '779 patent. *Id.* Additionally, CMOS processing which forms both nMIS/nMOS and pMIS/pMOS transistors was also well-known before the '779 patent. *Id.* For these reasons, trying these two alternatives would have led a POSITA

to anticipated success with either alternative. *Id.* Accordingly, having two transistors of the same conductivity type in Gilmer's semiconductor device is "the product not of innovation but of ordinary skill and common sense." See *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1331 (Fed. Cir. 2009) (internal quotation marks and citation omitted). Gilmer therefore teaches or at least suggests this limitation. Ex.1101, ¶196.

**c. Limitation 1[b]: "wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film,"**

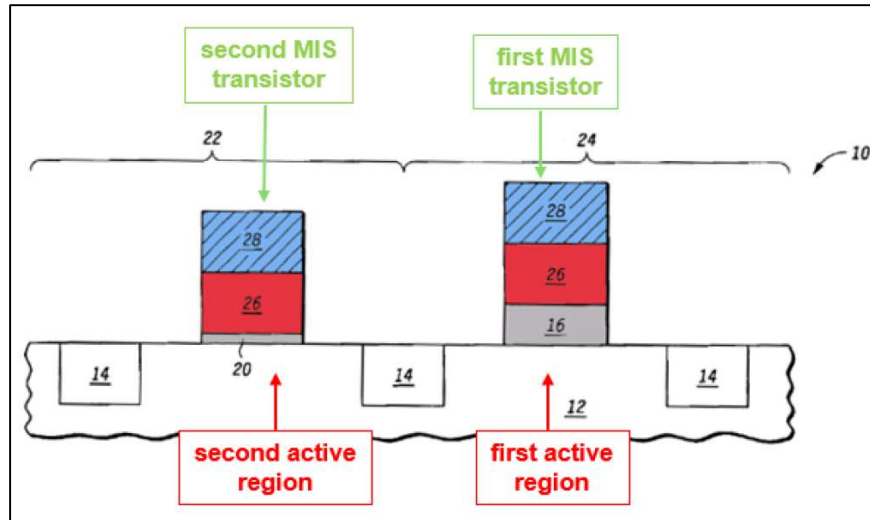
Gilmer discloses this limitation. Ex.1101, ¶¶197-198. Gilmer's I/O transistor in region 24 is the claimed first MIS transistor. Ex.1101, ¶197. The I/O transistor in region 24 includes "a first gate dielectric 16 . . . formed over substrate 12" (Ex.1009, 2:47-48), which "is preferably silicon dioxide or silicon oxynitride," (*id.*, 2:48-49), as well as a high-k dielectric layer 26 on top of the gate dielectric 16, (*id.*, 3:44-49). The gate dielectric 16 and the high-k layer 26 comprise the claimed first gate insulating film. Ex.1101, ¶197.

The I/O transistor in region 24 also includes a gate electrode formed on top of high-k layer 26. Ex.1009, 4:35-38 ("After metal oxide layer 26 has been deposited, a gate electrode material 28 is deposited over the metal oxide, and semiconductor device 10 is patterned and etched to form the gate stacks as shown in FIG. 4."). Ex.1101, ¶198.

- d. Limitation 1[c]: “the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film,”**

Gilmer discloses this limitation. Ex.1101, ¶¶199-200. Gilmer’s core transistor in region 22 is the claimed second MIS transistor. Ex.1101, ¶199. The core transistor in region 22 includes a “second gate dielectric 20 formed on” the substrate. Ex.1009, 3:9-11. “In a preferred embodiment, second gate dielectric 20 is also silicon dioxide or silicon oxynitride.” Ex.1009, 3:12-14. The core transistor in region 22 also includes as a high-k dielectric layer 26 on top of the gate dielectric 16. *Id.*, 3:44-49. The gate dielectric 16 and the high-k layer 26 comprise the claimed second gate insulating film. Ex.1101, ¶199.

The core transistor in region 22 also includes a gate electrode formed on top of high-k layer 26. Ex.1009, 4:35-38 (“After metal oxide layer 26 has been deposited, a gate electrode material 28 is deposited over the metal oxide, and semiconductor device 10 is patterned and etched to form the gate stacks as shown in FIG. 4.”) Thus, the first and second active regions in the semiconductor substrate 12, with the first and second gate insulating films of the first and second MIS transistors, respectively, formed thereon, and first and second gate electrodes formed on the first and second gate insulating films, respectively, are illustrated below. Ex.1101, ¶200.



Ex.1009, FIG. 4 (annotated).

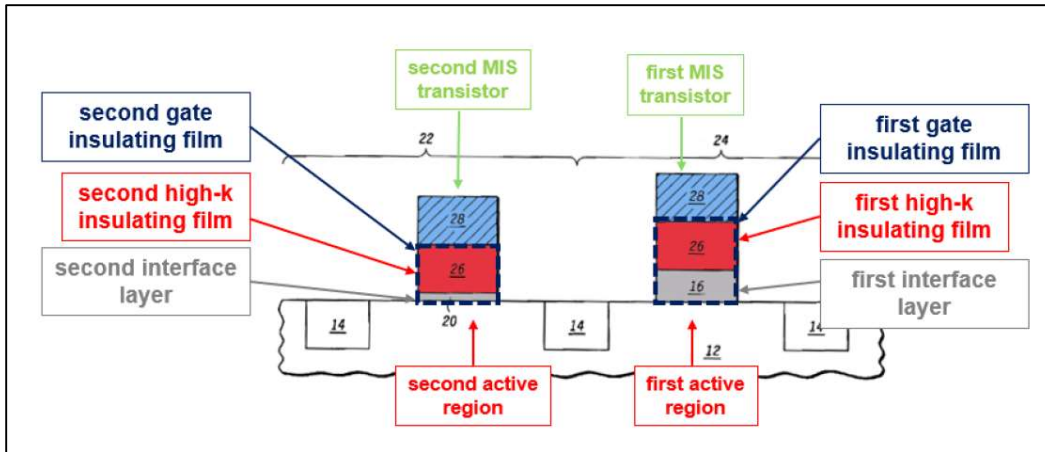
- e. **Limitation 1[d]: “the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer,”**

Gilmer discloses this limitation. Ex.1101, ¶201. The first gate insulating film, comprised of gate dielectric 16 and the high-k layer 26, includes a first interface layer (gate dielectric 16) that is in contact with the substrate. Ex.1009, 2:47-48 (“a first gate dielectric 16 is formed over substrate 12”). *Id.*, FIG. 4. The first gate insulating film also includes a high dielectric constant insulating film, the high-k dielectric layer 26, formed on top of the gate dielectric 16. *Id.*, 3:44-49; Ex.1101, ¶201.

- f. Limitation 1[e]: “the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer,”**

Gilmer discloses this limitation. Ex.1101, ¶¶202-206. The second gate insulating film, comprised of gate dielectric 20 and the high-k layer 26, includes an interface layer (gate dielectric 20) that is in contact with the substrate. Ex.1009, 3:10-12 (“a second gate dielectric 20 is formed on exposed portions of substrate 12 within the core device region 22”), FIG. 4. The second gate insulating film also includes a high dielectric constant insulating film, the high-k dielectric layer 26, formed on top of the gate dielectric 16. *Id.*, 3:44-49. Ex.1101, ¶202.

Thus, gate dielectric 16 is the claimed first interface layer being in contact with the semiconductor substrate, metal oxide 26 is the claimed first high dielectric constant insulating film formed on the first interface layer (*i.e.*, gate dielectric 16), and these dielectric layers collectively are the claimed first gate insulating film formed on a first active region in the semiconductor substrate, as illustrated below. Ex.1101, ¶203; *see* Ex.1009, 2:46-48, 3:44-47.

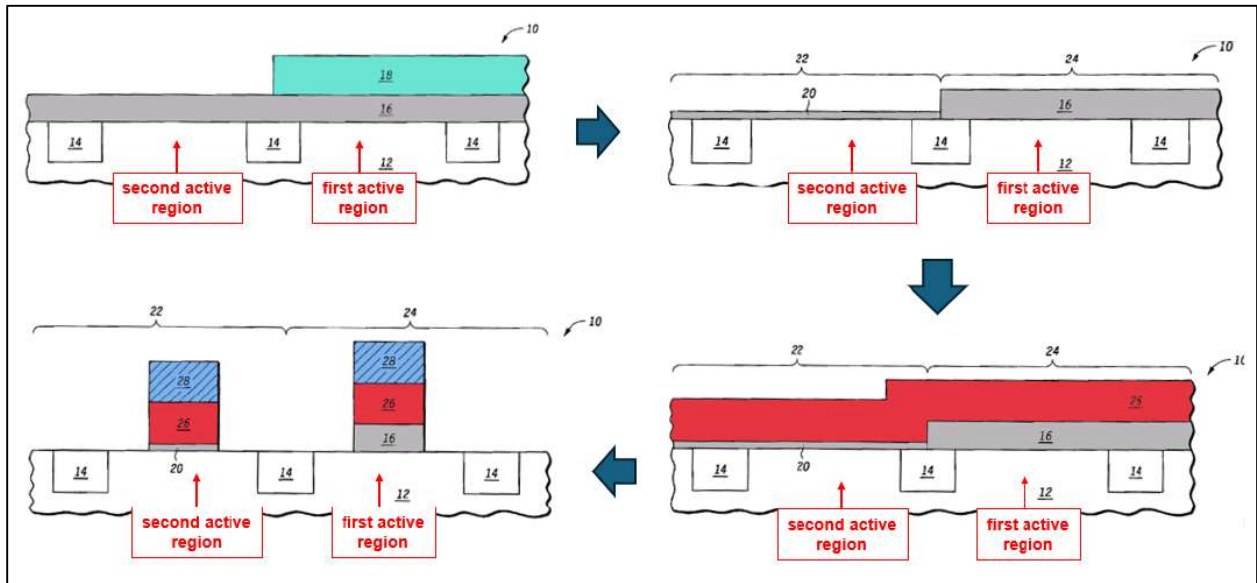


Ex.1009, FIG. 4 (annotated).

Similarly, as illustrated above, gate dielectric 20 is the claimed second interface layer being in contact with the semiconductor substrate, metal oxide 26 is the claimed second high dielectric constant insulating film formed on the second interface layer (*i.e.*, gate dielectric 20), and these dielectric layers collectively are the claimed second gate insulating film formed on a second active region in the semiconductor substrate. Ex.1101, ¶204; *see* Ex.1009, 2:46-48, 3:44-47, FIG. 4 (above).

The semiconductor fabrication process disclosed by Gilmer confirms the semiconductor device structure of Figure 4, as explained above. Ex.1101, ¶205. Gilmer teaches that “[a]fter forming trench isolation regions 14, a first gate dielectric 16 is formed over substrate 12.” Ex.1009, 2:46-48, FIG. 1 (top-left below). After masking a portion of the first gate dielectric layer, the semiconductor device 10 is then etched “to remove unprotected portions of first gate dielectric 16 in core device

region 22” and, after removal of the mask, “second gate dielectric 20 is formed on exposed portions of substrate 12 within the core device region 22.” Ex.1009, 2:25-67, 3:7-12, FIG. 2 (top-right below).



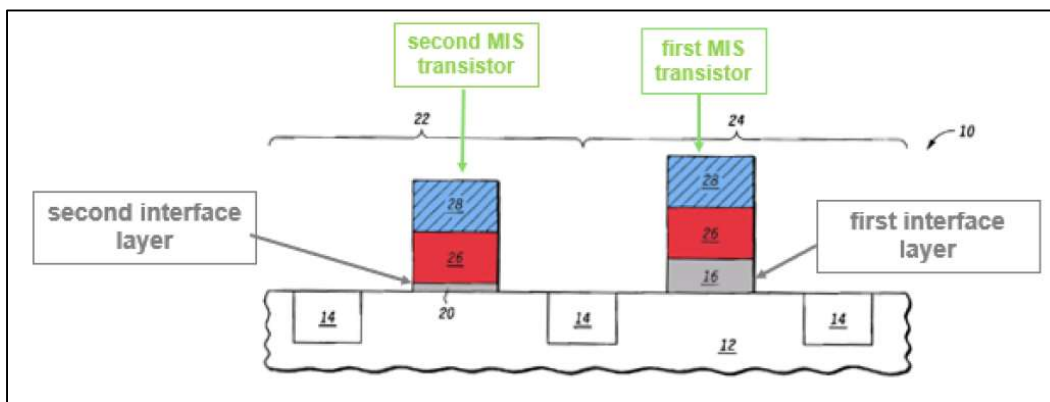
Ex.1009, FIGS. 1-4 (annotated).

After the first and second gate dielectrics with “two different thicknesses have been formed, a high-k dielectric ... is deposited over semiconductor device 10.” Ex.1009, 3:44-47, FIG. 3 (bottom-right above). Gate electrode material 28 is subsequently “deposited over the metal oxide, and semiconductor device 10 is patterned and etched to form the gate stacks.” Ex.1009, 4:35-38, FIG. 4 (bottom-left above). Ex.1101, ¶206.

**g. Limitation 1[f]: “the first interface layer has a thickness larger than that of the second interface layer, and”**

Gilmer discloses this limitation. Ex.1101, ¶¶207-208. Gilmer states that the thickness of first gate dielectric 16 “generally will be within a range of 30–50 Angstroms (3–5 nanometers),” (Ex.1009, 2:53-55), and the thickness of second gate dielectric 20 “generally will be within a range of 4–12 Angstroms (0.4–1.2 nanometers)” (*id.*, 3:17-21). Ex.1101, ¶207.

Therefore, the first interface layer in Gilmer (*i.e.*, gate dielectric 16) has a thickness greater than the second interface layer (*i.e.*, gate dielectric 20). Ex.1101, ¶207; *see also* Ex.1009, 2:60-65, Abstract, claim 1. As shown below, the gate dielectric 16, which is the claimed first interface layer, has a thickness larger than that of the gate dielectric 20, which is the claimed second interface layer. Ex.1101, ¶208.



Ex.1009, FIG. 4 (annotated).

- h. Limitation 1[g]: “each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film.”**

Gilmer discloses this limitation. Ex.1101, ¶209. Gilmer states that first and second interface layers (*i.e.*, gate dielectrics 16 and 20, respectively) are “silicon dioxide or silicon oxynitride.” Ex.1009, 2:48-49 (gate dielectric 16), 3:13 (gate dielectric 20).

## **2. Dependent Claim 12**

- a. Limitation 12: “The semiconductor device of claim 1, wherein each of the first and second high dielectric constant insulating films contains hafnium or zirconium.”**

Gilmer discloses this limitation. Ex.1101, ¶210. As discussed above, after the “gate dielectrics of two different thicknesses have been formed, a high-k dielectric ... is deposited over semiconductor device 10.” Ex.1009, 3:44-47. Preferably, the high-k dielectric is a metal oxide 26 for which “[s]uitable materials ... preferably include hafnium oxide . . . .” Ex.1009, 3:49-50; Ex.1101, ¶210.

## **3. Dependent Claim 13**

- a. Limitation 13: “The semiconductor device of claim 1, wherein the first and second high dielectric constant insulating films are equal in thickness.”**

Gilmer discloses this limitation. Ex.1101, ¶¶211-213. Metal oxide film 26 is the same thickness in both the first (I/O) and the second (core) transistors. Ex.1009,

FIG. 3, 4:8-24 (“a single metal oxide layer can be used . . . With the present invention, a single metal oxide deposition is used . . .”). Ex.1101, ¶211.

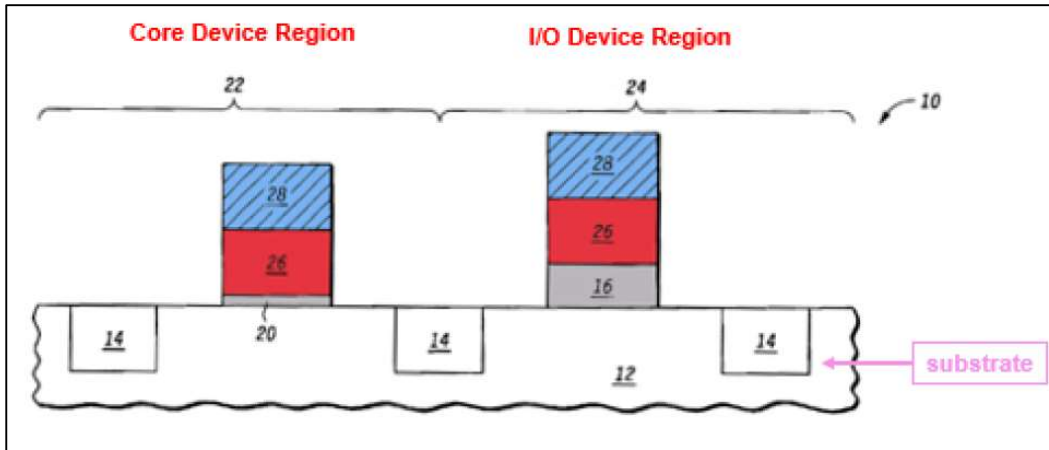
Gilmer explains that “[b]ecause metal oxide 26 is deposited as a single blanket deposition, its thickness will **not vary much** across the substrate surface.” Ex.1009, 4:2-4 (emphasis added). A POSITA would have understood that the metal oxide film 26, which is deposited as a single blanket deposition, is “equal in thickness” in both the I/O and core regions subject to very minor variations. Ex.1101, ¶212. Gilmer’s teaching is consistent with that of the ’779 patent, which only discloses the “first and second high constant dielectric insulating films may be **substantially equal** in thickness.” Ex. 1001, 5:31-33 (emphasis added).

### C. Ground III (Gilmer and Chen)

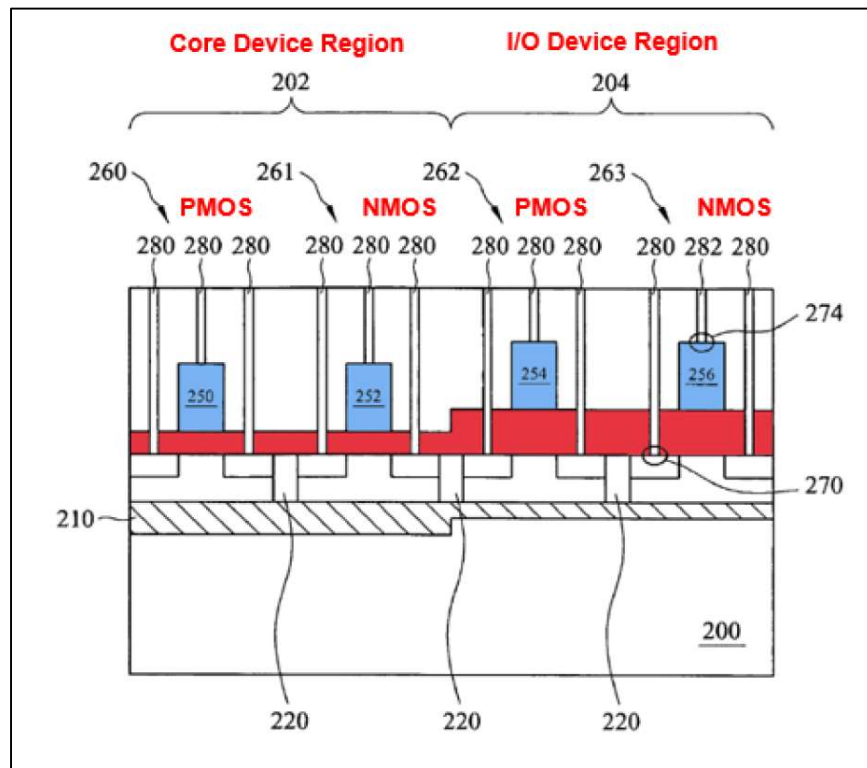
Gilmer combined with Chen renders obvious under 35 U.S.C. § 103 claims 1, 12, and 13 of the ’779 patent. Ex.1101, ¶¶214-218.

As described above, Gilmer alone explicitly teaches or at least suggests all of the limitations of claims 1, 12, and 13 of the ’779 patent. However, the Patent Owner may argue that Gilmer does not explicitly teach two transistors of the same conductivity type (a limitation of 1[a]). Chen provides this teaching.

Gilmer discloses core and I/O transistors formed on a shared substrate, as illustrated in Figure 4 (below). Ex.1101, ¶215.



Ex.1009, FIG. 4 (annotated). Chen teaches core and I/O transistors having similar structures formed in the same substrate and having “the same conductivity type,” as shown in Figure 3h (below) and as recited by limitation 1[a]. Ex.1010, 3:39-60, 8:27-42 (describing two pMOS and two nMOS transistors).



Ex.1010, FIG. 3h (annotated).

Both Gilmer and Chen are in the same field as the '779 patent, “semiconductor devices and methods for fabricating the same.” Ex.1001, 1:15-16; *see* Ex.1009, 1:7-10, 2:36-38; Ex.1010, 1:12-14, 4:14-16. A POSITA would have been motivated to combine Chen’s teachings regarding forming transistors having the same conductivity type (*e.g.*, two nMIS transistors or two pMIS transistors) with Gilmer’s semiconductor device. Ex.1101, ¶216. Gilmer suggests forming transistors of the same conductivity type, as discussed in Section X.B above. For these same reasons, Gilmer suggests the combination with Chen. Ex.1101, ¶216.

Additionally, a POSITA would have been motivated to make the combination based on his/her background knowledge in the relevant art and common sense. *See Perfect Web*, 587 F.3d at 1328-29 (“[M]otivation to combine may be found explicitly or implicitly [in] ... the background knowledge, creativity, and common sense of the person of ordinary skill.”); Ex.1101, ¶217. The '779 patent acknowledges in its background section the well-known fact that devices have conductivity types and describes use of an n-well for pMIS transistors and a p-well for nMIS transistors. Ex.1001, 1:61-2:15. Based on this background knowledge, a POSITA would have been motivated to combine Gilmer and Chen and would have had a reasonable expectation of success in forming semiconductor devices including MIS transistors of the same conductivity type in Gilmer, as taught by Chen, and as recited in limitation 1[a]. Ex.1101, ¶217.

Since Gilmer teaches every other limitation of claim 1 of the '779 patent, as discussed above with reference to Ground II, the combination of Gilmer and Chen renders claim 1 obvious. Ex.1101, ¶218. For this reason, and the reasons discussed in Section X.B above, the combination of Gilmer and Chen also renders obvious claims 12-13 of the '779 patent, which depend from claim 1.

## **XI. CONCLUSION**

For the reasons set forth above, *Inter Partes* Review of the Challenged Claims of the '779 patent is respectfully requested.

Respectfully submitted,

Date: May 23, 2025

/s/Tim Tingkang Xia

Tim Tingkang Xia (Lead Counsel)

Registration No. 45,242

*Counsel for Petitioner*

**CERTIFICATE OF COMPLIANCE WITH WORD COUNT**

Pursuant to 37 C.F.R. § 42.24(d), I certify that this Petition complies with the type-volume limits of 37 C.F.R. § 42.24(a)(1)(i) because it contains 8,296 words, according to the word-processing system used to prepare this Petition, excluding the parts of this Petition that are exempted by 37 C.F.R. § 42.24(a)(1) (table of contents, table of authorities, mandatory notices under § 42.8, certificate of service, certificate of word count, or appendix of exhibits or claim listing).

Date: May 23, 2025

/s/Tim Tingkang Xia

Tim Tingkang Xia (Lead Counsel)

Registration No. 45,242

*Counsel for Petitioner*

**CERTIFICATE OF SERVICE**

Pursuant to 37 C.F.R. § 42.6(e), this is to certify that on this 23rd day of May, 2025, I caused to be served on a USB thumb drive a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,796,779 Under 35 U.S.C. §§ 311, 312 and 37 C.F.R. § 42.104 (with Exhibits 1001-1002, 1005-1010, 1101-1111, 1211-1216, 1223, 1226-1233, 1318, 1323, 1340, 1406, 1413, 1419, 1429-1435, 1506, 1512, 1515-1529, 1531 & 1532) via Federal Express Priority Overnight at the Correspondence Address for Patent Owner:

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