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Effects of High-Temperature Forming Gas Anneal on HfO_2 MOSFET Performance

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Abstract

Effects of forming gas (FG) annealing on HfO_2 MOSFET performance have been studied. High-temperature (500-600°C) FG annealing has been shown to significantly improve carrier mobility and subthreshold slopes for both N and PMOSFET's. The improvement has been correlated to the reduction in interfacial state density. The effectiveness of FG annealing has also been examined on samples that underwent surface preparations with NH_3 or NO annealing prior to HfO_2 deposition. It was found that FG annealing did not degrade PMOS negative bias temperature instability characteristics.

Introduction

HfO_2 is considered as one of the most promising high-k gate dielectrics to replace SiO_2, due to its reasonably high dielectric constant, large band offset to Si, and thermal stability in contact with Si. MOSFET's have already been demonstrated using both TaN metal and dual-gate polysilicon gate electrodes [1, 2]. The performance of the MOSFET's, however, was generally found to be inadequate in terms of channel carrier mobility [3], and therefore further process optimization is necessary before it is introduced into the production. The degraded mobility was often observed along with poor subthreshold slopes [3], indicating high interfacial state density (D_{it}). In this paper, for the first time we have studied the effects of high-temperature FG annealing for improving HfO_2 transistor characteristics on both N and PMOS. The annealing was done at higher than typical FG annealing temperature (i.e. ≥500°C) prior to metal deposition.

Experiments

Table 1 summarizes device fabrication flow of HfO_2 MOSFET's. Prior to HfO_2 deposition, some selected wafers were annealed in NH_3 or NO ambient, in order to examine their effects on the MOSFET performance. HfO_2 was deposited using reactive dc magnetron sputtering, followed by post-deposition annealing at 500°C for 5 min in N_2. Detailed description regarding MOSFET fabrication can be found in [2]. Then high-temperature FG annealing of 4 % H_2 concentration was performed with the temperature range of 400 to 600°C, prior to Al interconnect deposition. After the interconnect patterning and Al deposition on backside, another FG annealing was employed to lower down the contact resistance at a lower temperature (400-450°C). Equivalent oxide thickness (EOT) was calculated from measured C-V curves using a simulator to deduct the quantum mechanical effect.

Results and Discussions

I_d-V_g characteristics in Fig. 1 revealed that both drive current and subthreshold slope improved significantly at the higher temperature FG annealing. The drive current enhancement was also observed in the saturation region (Fig. 2). The trend is summarized in Fig. 3. Using 600°C FG annealing, the subthreshold slope is reduced down to ~64 mV/dec, which is close to the D_{it}-free ideal value (i.e. 60 mV/dec). The steeper C-V curves at the higher temperatures confirmed the reduction in D_{it} (Fig. 4). Channel electron mobility was evaluated using the standard split C-V method (Fig. 5). As was expected from I-V characteristics, the mobility were enhanced with higher FG annealing temperatures. Since the surface morphology cannot be changed at such temperatures (≤600°C), the enhancement is attributed to the reduction of D_{it} rather than the mechanism related to surface roughness. Fig. 6 shows that gate leakage characteristics were not changed, except that slightly lower breakdown voltages were observed for the higher temperatures. In Fig. 7, mobility values at a fixed field of 1 MV/cm were compared between control, NH_3, and NO annealed samples, which have EOT's of 13, 10, and 15 Å, respectively. NO yielded the highest mobility, whereas NH_3 degraded the mobility although it is useful in reducing EOT [4]. Similar improvements of I_d-V_g characteristics (Fig. 8) and channel hole mobility (Fig. 9) were observed on PMOSFET's also, while the improvements were not as pronounced as those of NMOSFET's. Charge trapping and resulting instability in MOSFET performance are among the most serious concerns regarding hydrogen related treatments. Hysteresis on NMOS capacitors remained at ~20 mV, despite the very slight increase at the higher temperatures (Fig. 10). Hydrogen related defects are generally believed to cause NBTI. Thus, NBTI on PMOSFET's was examined. It was found that FG annealing at 600°C caused no significant degradation in V_t instability (Fig. 11).

Conclusion

High-temperature FG annealing improved channel carrier mobility as well as subthreshold slopes in both N and PMOSFET with HfO_2 gate dielectrics. These features are advantageous in achieving large on current while suppressing off current, and give more flexibility in V_t adjustment. The mobility enhancement was achieved along with D_{it} reduction. The effectiveness of the FG annealing on the NMOS electron mobility is similar for various different surface preparation techniques, whereas the highest mobility was obtained with NO surface preparation. The FG annealing did not degrade hysteresis characteristics and PMOS NBTI.

Acknowledgement: This work was partially supported by SRC/SEMATECH through FEP Research Center, and Texas Advanced Technology Program.

References

[1] B. H. Lee et al., IEDM Tech. Dig., 2000, p. 39.
[2] K. Onishi et al., IEDM Tech. Dig., 2001, p. 659.
[3] E. P. Gusev et al., IEDM Tech. Dig., 2001, p. 451.
[4] R. Choi et al., Symp. VLSI Tech., p. 15, 2001.

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- Field oxidation and active patterning
- Piranha and HF (1:100) cleaning
- **(Surface annealing in NH_3 or NO)**
- Reactive dc sputtering of HfO_2
- Post deposition annealing (PDA)
- Poly-Si deposition and patterning
- Dopant implantation
- S/D Oxidation
- Low temperature oxide deposition
- Contact patterning
- Dopant activation
- **High-temperature FG anneal**
- Metal (Al) deposition and patterning
- Sintering in FG

Table 1. Process flow of polysilicon gate HfO_2 MOSFET's.

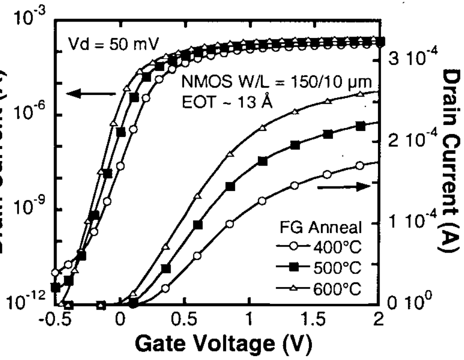

Fig. 1. Drain current and subthreshold slope were improved by high-temperature FG annealing.

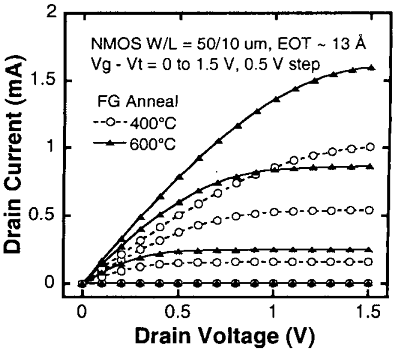

Fig. 2. I_d-V_d curves show improved I_{dsat} for 600°C FG annealing.

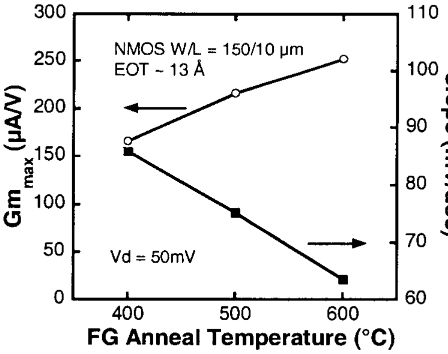

Fig. 3. Subthreshold slope of 64 mV/dec was achieved at 600°C FG annealing.

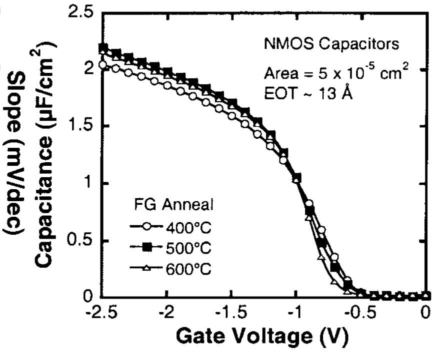

Fig. 4. Steeper C-V curves at higher FG annealing temperatures indicate reduction in D_{it}.

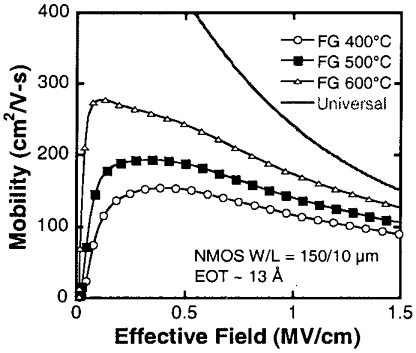

Fig. 5. Channel electron mobility in NMOSFET's was improved by high-temperature FG annealing.

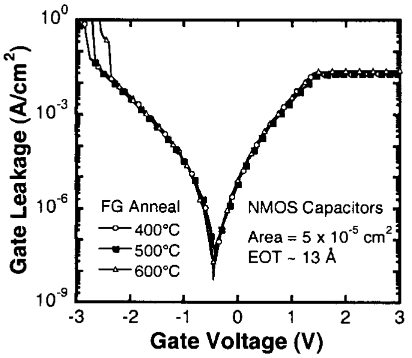

Fig. 6. Gate leakage was not changed by FG annealing, except the slightly lower breakdown voltages for higher temperatures.

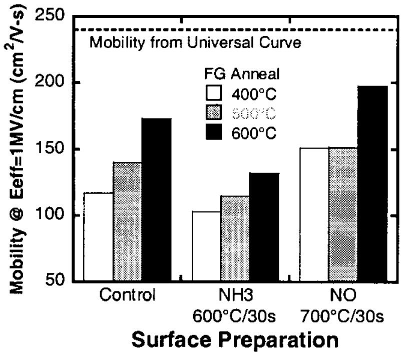

Fig. 7. Channel electron mobility comparison between different surface preparations. EOT's are ~13, 10, 15 Å for control, NH_3, and NO annealing, respectively.

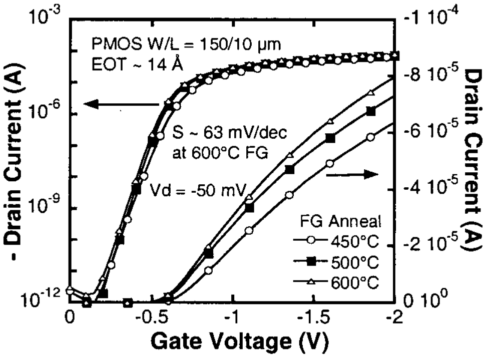

Fig. 8. I_d-V_g characteristics of HfO_2 PMOSFET's were also improved by high-temperature FG annealing.

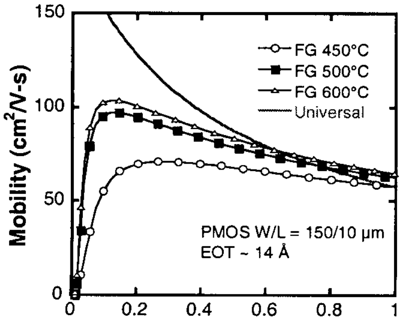

Fig. 9. Channel hole mobility in HfO_2 PMOSFET's was improved by high-temperature FG annealing.

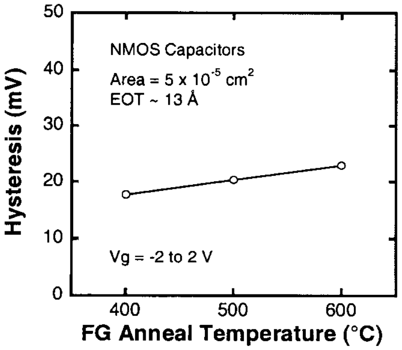

Fig. 10. Hysteresis remained at ~20 mV, despite the very slight increase at the higher FG annealing temperatures.

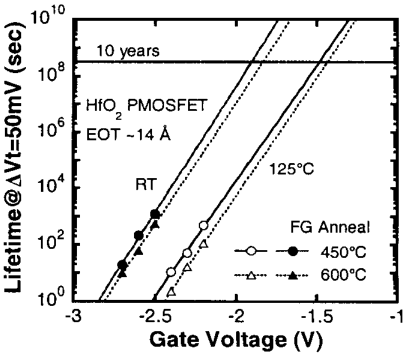

Fig. 11. Effect of FG annealing on PMOS NBTI. The lifetime was not significantly altered by the high-temperature FG annealing.