A 45nm Logic Technology with High-k + Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging

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Portland Technology Development, [*]CR, [#]QRE, [%]PTM

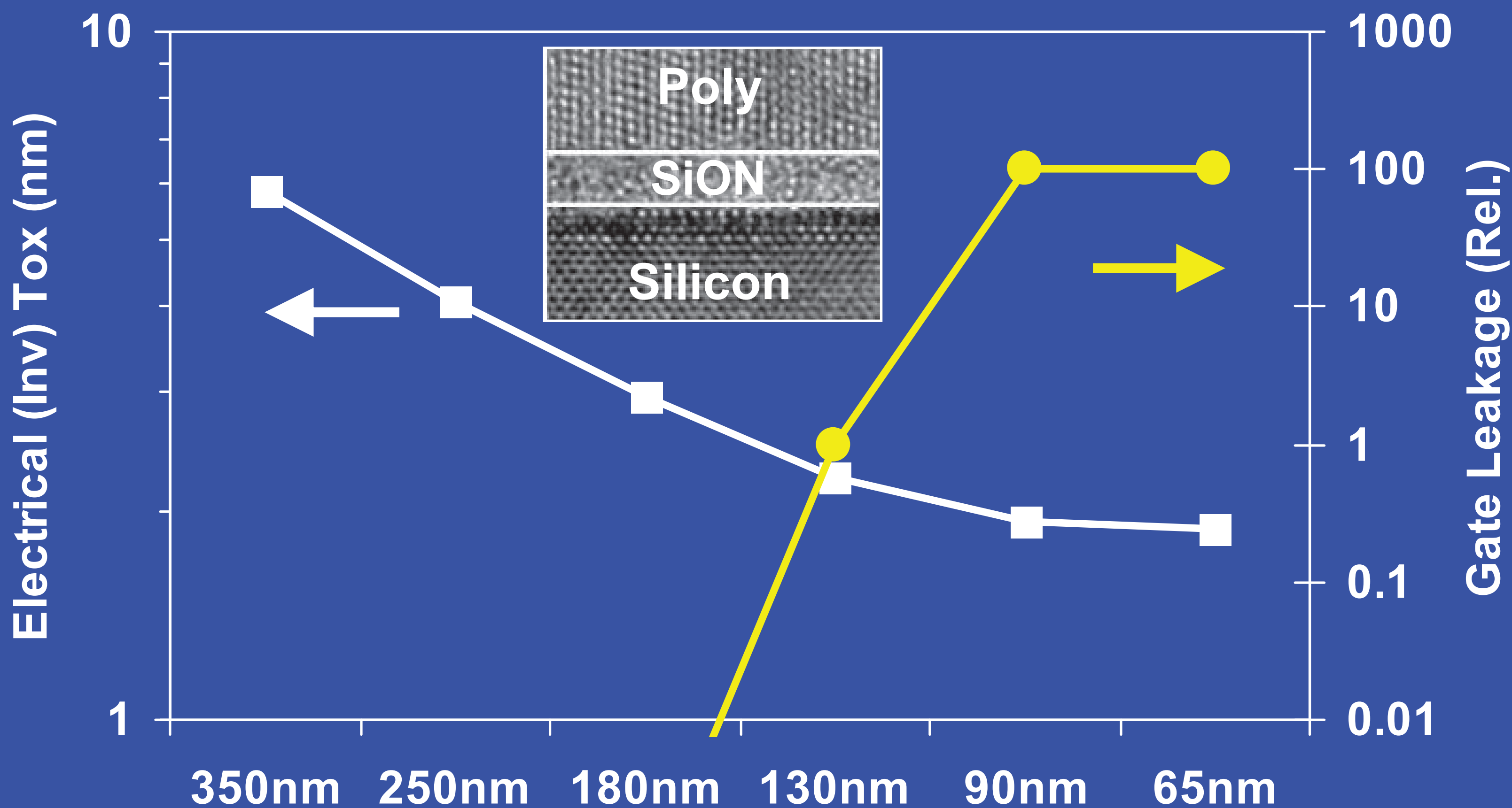
Intel Corporation

Outline

- Introduction
- Process Features
- Transistors
- Interconnects
- Manufacturing
- Conclusions

Introduction

- SiON scaling running out of atoms
- Poly depletion limits inversion T_{OX} scaling



High-k + Metal Gate Benefits

- **High-k gate dielectric**
  - Reduced gate leakage
  - T_{OX} scaling
- **Metal gates**
  - Eliminate polysilicon depletion
  - Resolves V_T pinning and poor mobility for high-k dielectrics

High-k + Metal Gate Challenges

- **High-k gate dielectric**
  - **Poor mobility, V_T pinning due to soft optical phonons**
  - **Poor reliability**
- **Metal gates**
  - **Dual bandedge workfunctions**
  - **Thermal stability**
  - **Integration scheme**

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Process Features

- 45 nm Groundrules
- 193 nm Dry Lithography
- High-K + Metal Gate Transistors
- 3^{RD} Generation Strained Silicon
- Trench Contacts with Local Routing
- 9 Cu Interconnect Layers
- 100% Lead-free Packaging

Process Features

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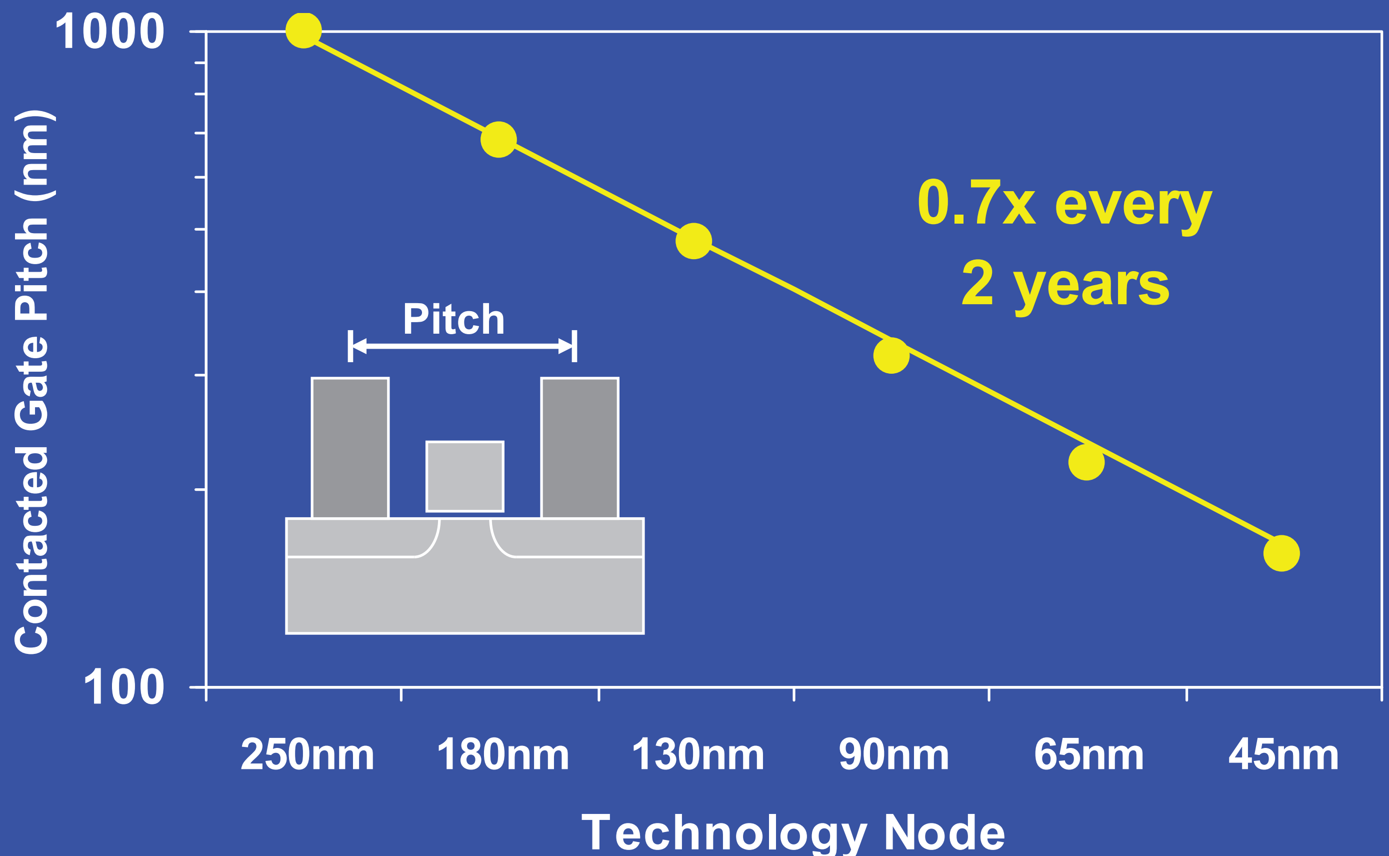
45nm Design Rules

Layer	Pitch (nm)	Thick (nm)	Aspect Ratio
Isolation	200	200	--
Contacted Gate	160	60	--
Metal 1	160	144	1.8
Metal 2	160	144	1.8
Metal 3	160	144	1.8
Metal 4	240	216	1.8
Metal 5	280	252	1.8
Metal 6	360	324	1.8
Metal 7	560	504	1.8
Metal 8	810	720	1.8
Metal 9	30.5μm	7μm	0.4

~0.7x linear scaling from 65nm

Contacted Gate Pitch

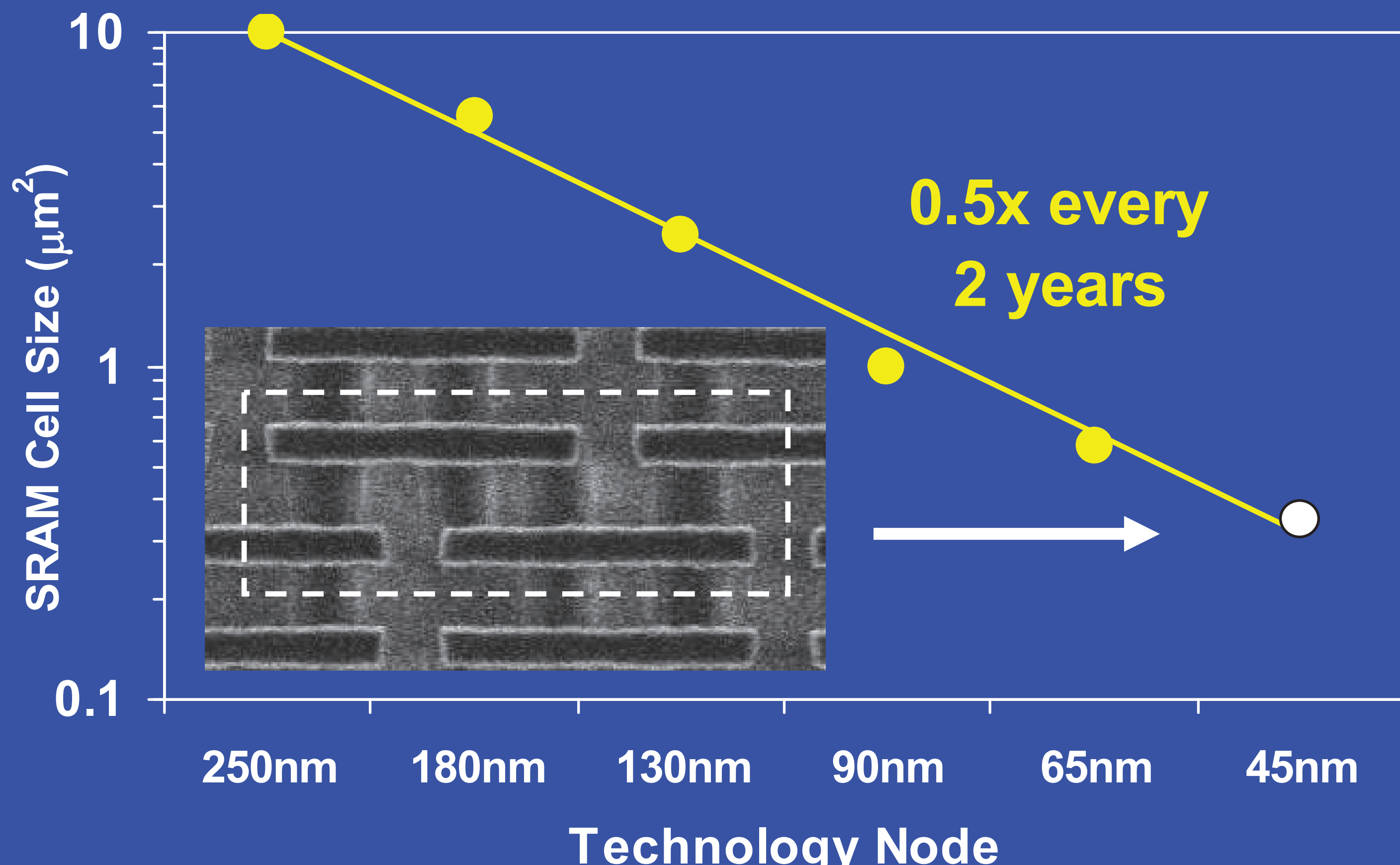
- Transistor gate pitch of 160 nm continues 0.7x per generation scaling



Tightest contacted gate pitch reported for 45 nm generation

SRAM Cells

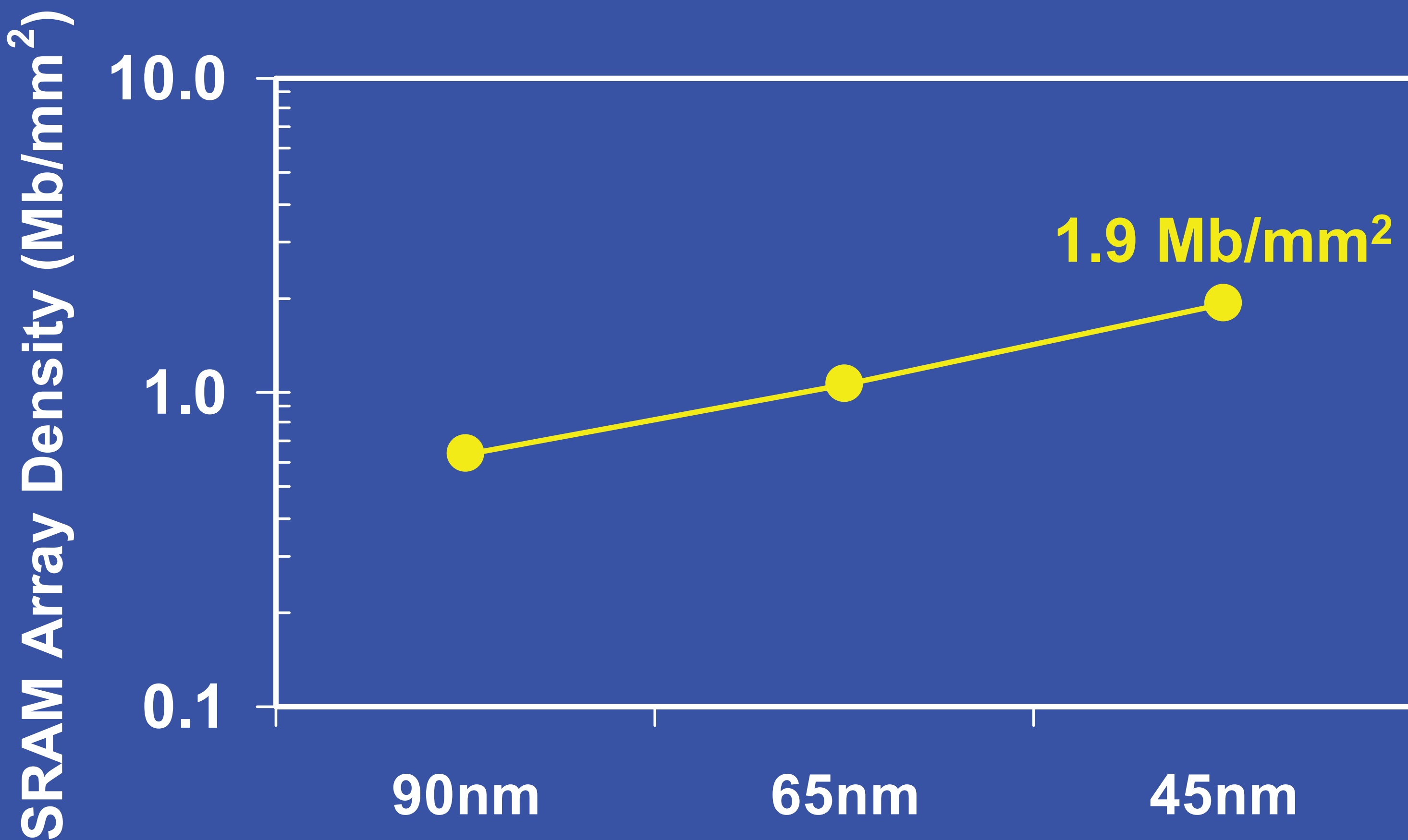
- 0.346 μm² and 0.382 μm² SRAM cells
  - Optimize density and power/performance



Transistor density doubles every two years

SRAM Array Density

- **SRAM array density achieves 1.9 Mb/mm²**
  - **Includes row/column drivers and other circuitry**



Array density scales at ~2X per generation

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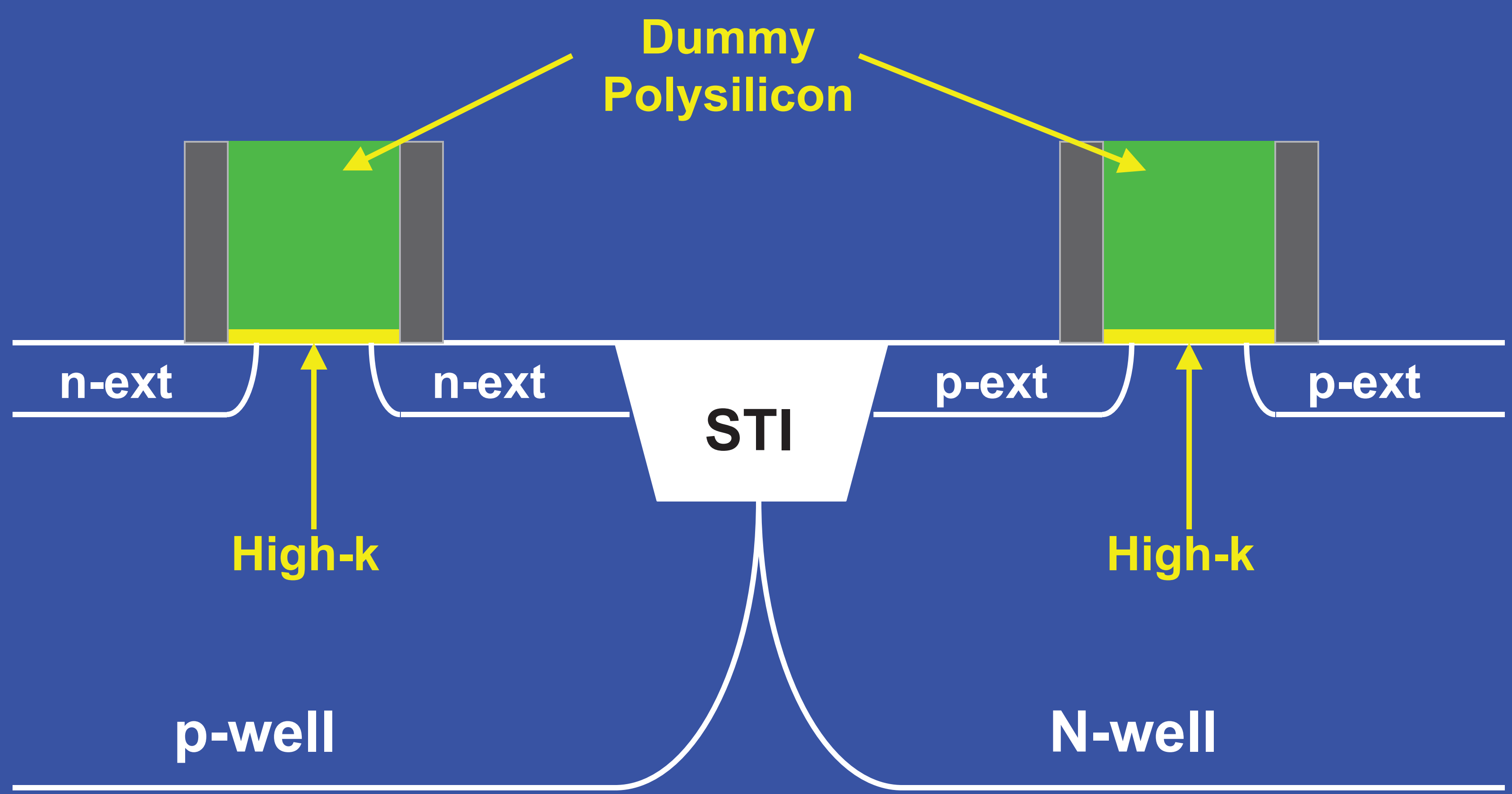
Transistor Process Flow

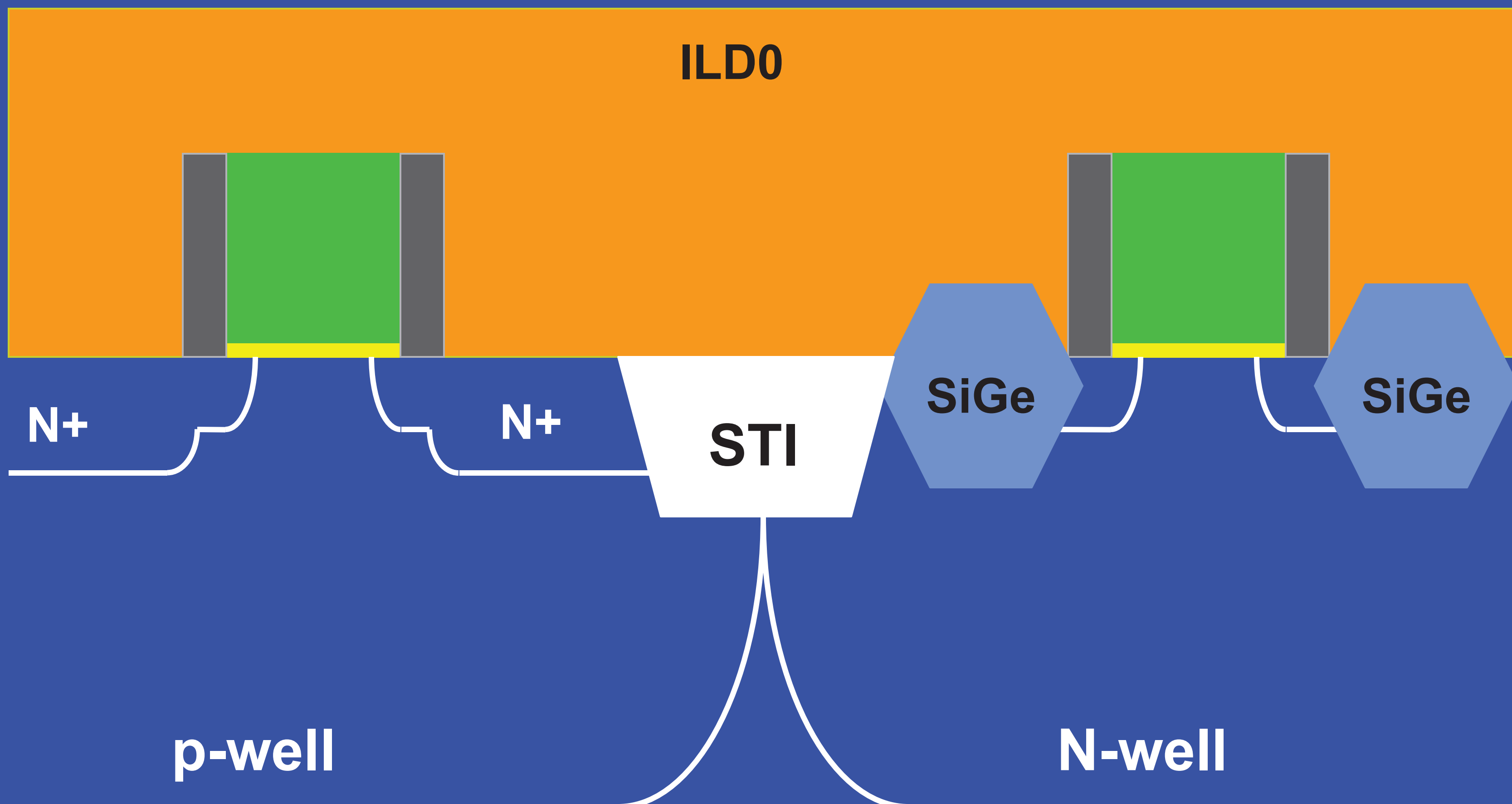
- **Key considerations**
  - Integrate hafnium-based high-k dielectric, dual metal gate electrodes, strained silicon
  - Thermal stability of metal gate electrodes
- **High-k First, Metal Gate Last**
  - Metal gate deposition after high temperature anneals
  - Integrated with strained silicon process
  - Transistor mask count same as 65nm

Transistor Process Flow



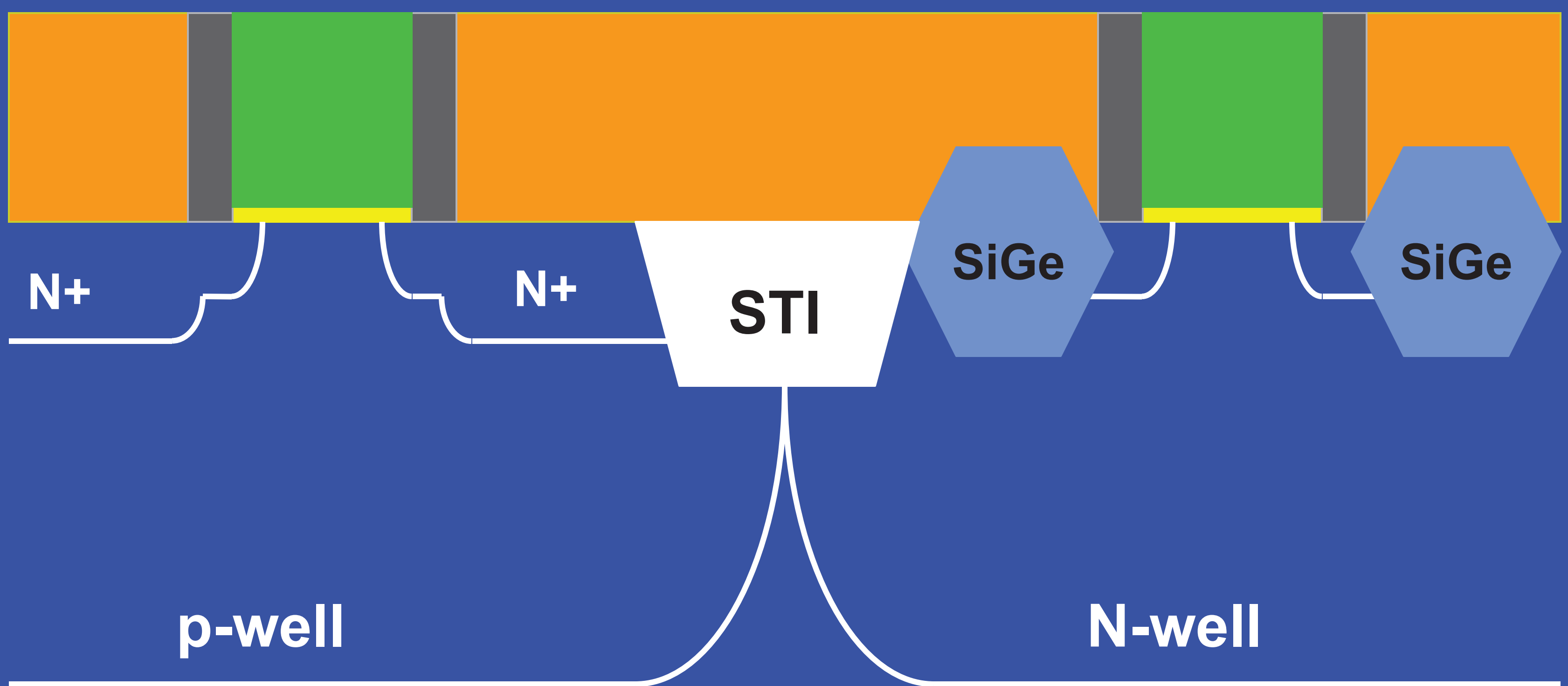
Standard process except for ALD high-k

Transistor Process Flow



e-SiGe & S/D, Thermal anneal, ILD0 deposition

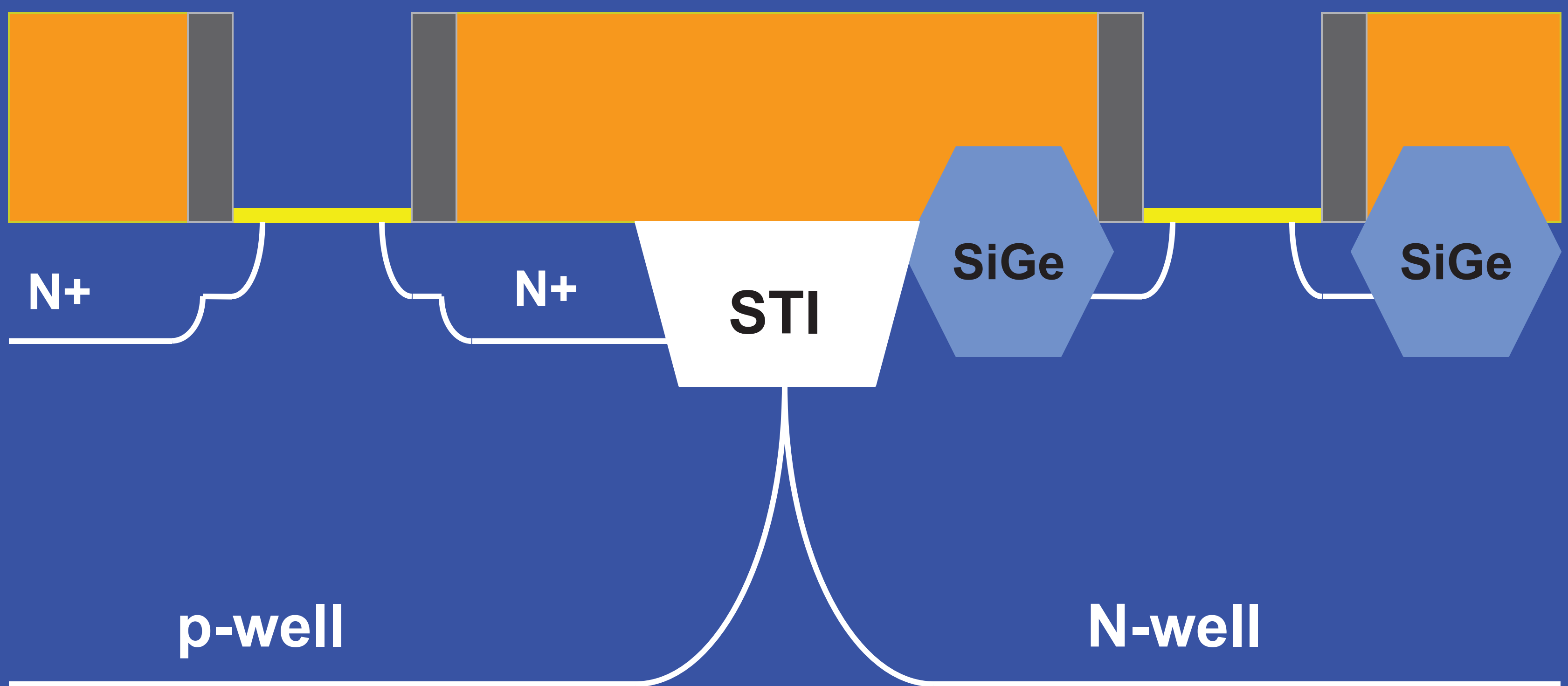
Transistor Process Flow



Poly Opening Polish

15c

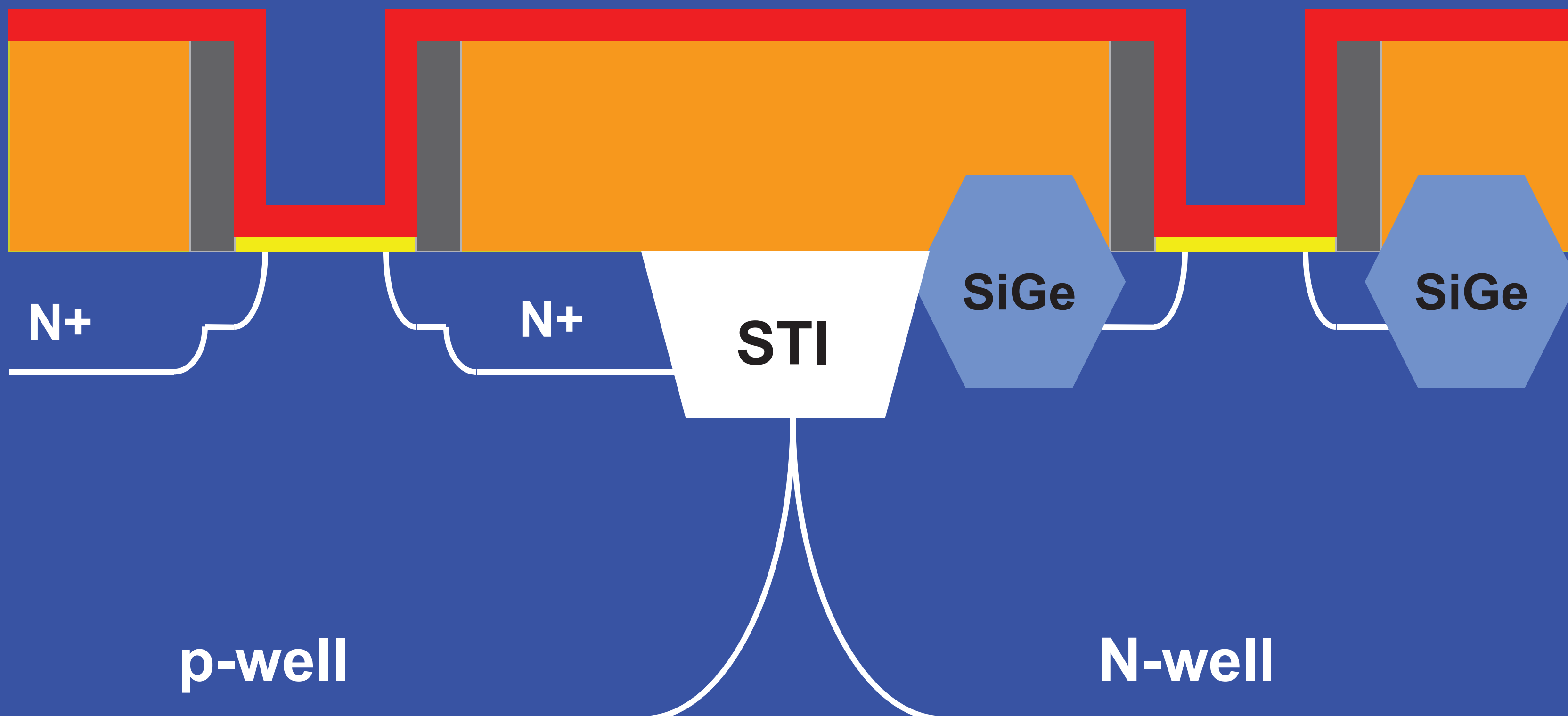
Transistor Process Flow



Dummy Poly removal

15d

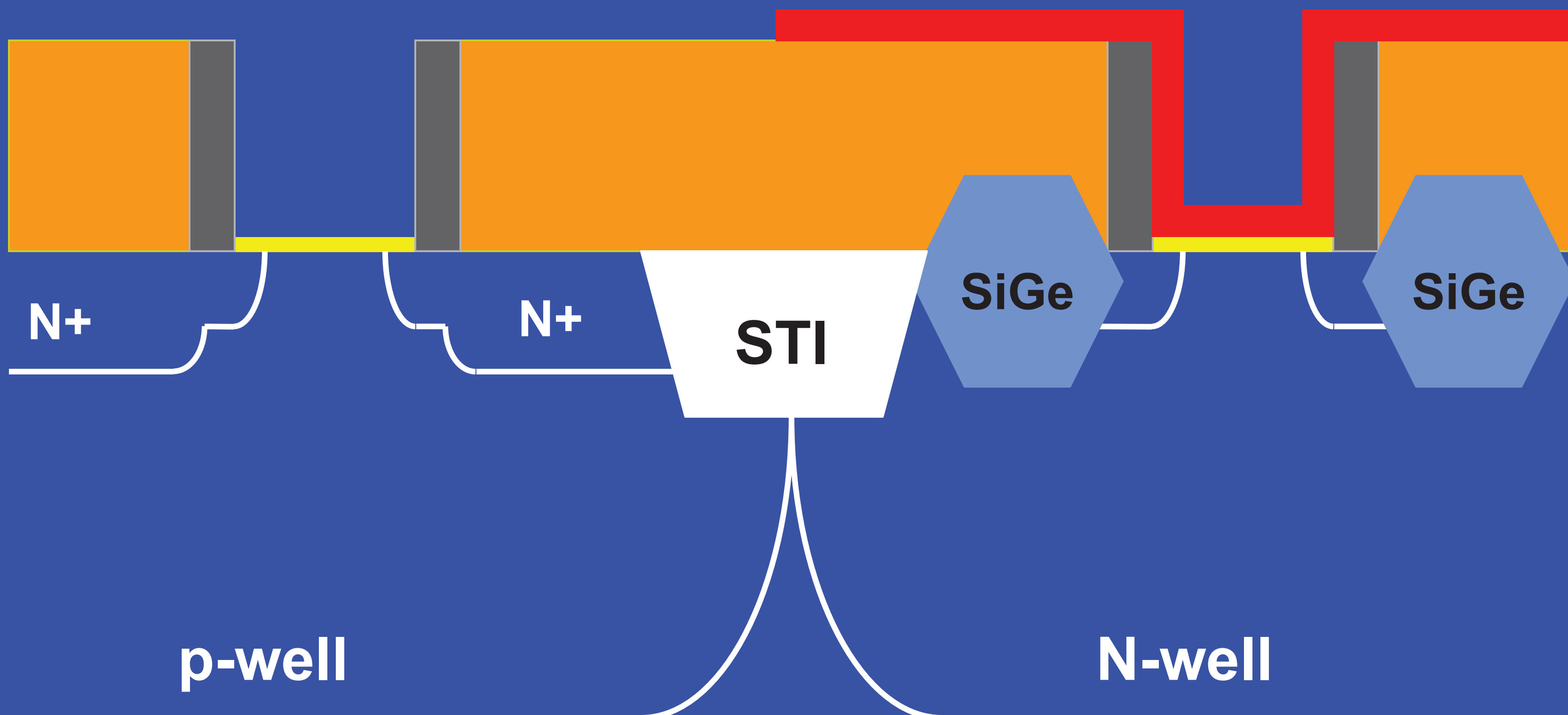
Transistor Process Flow



PMOS WF Metal deposition

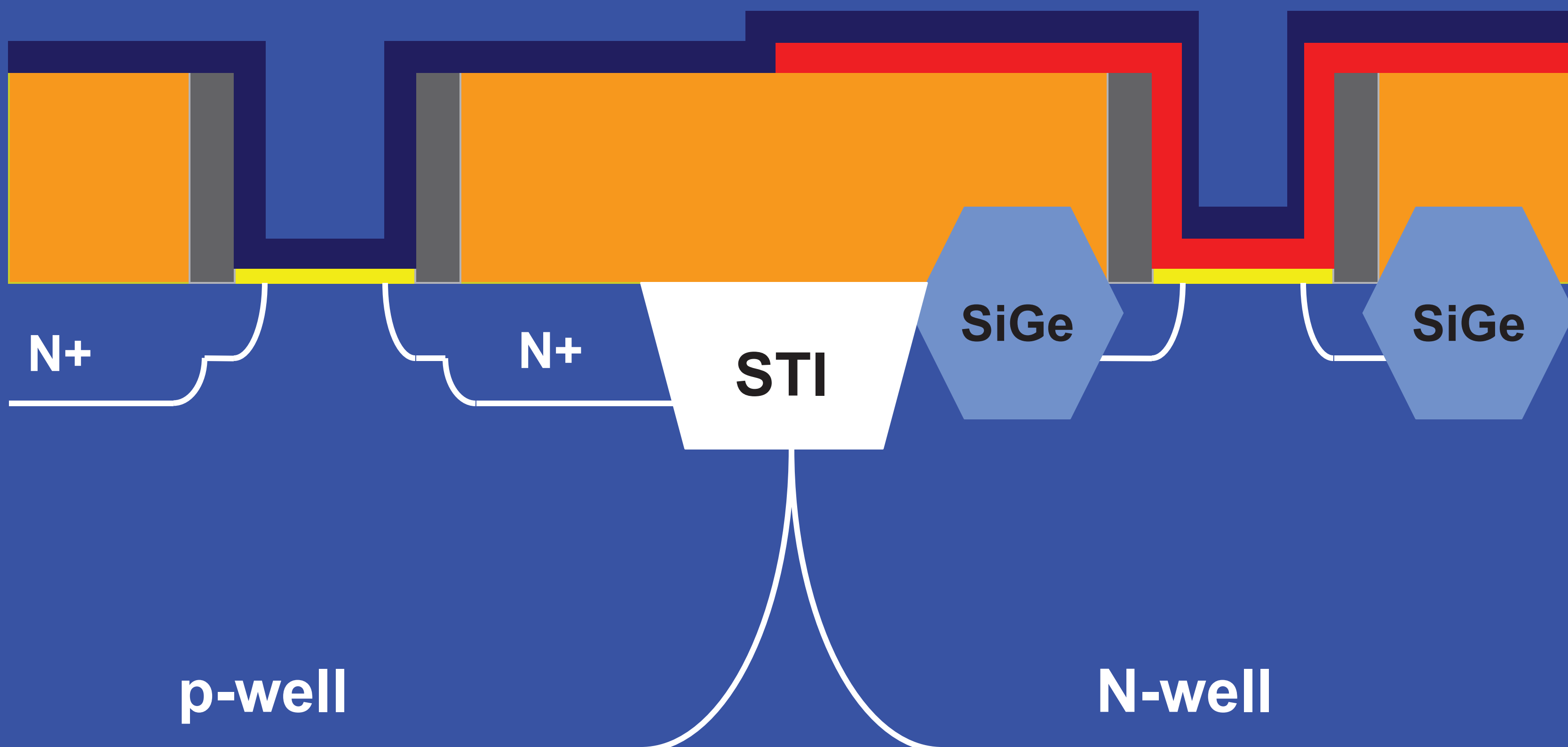
15e

Transistor Process Flow



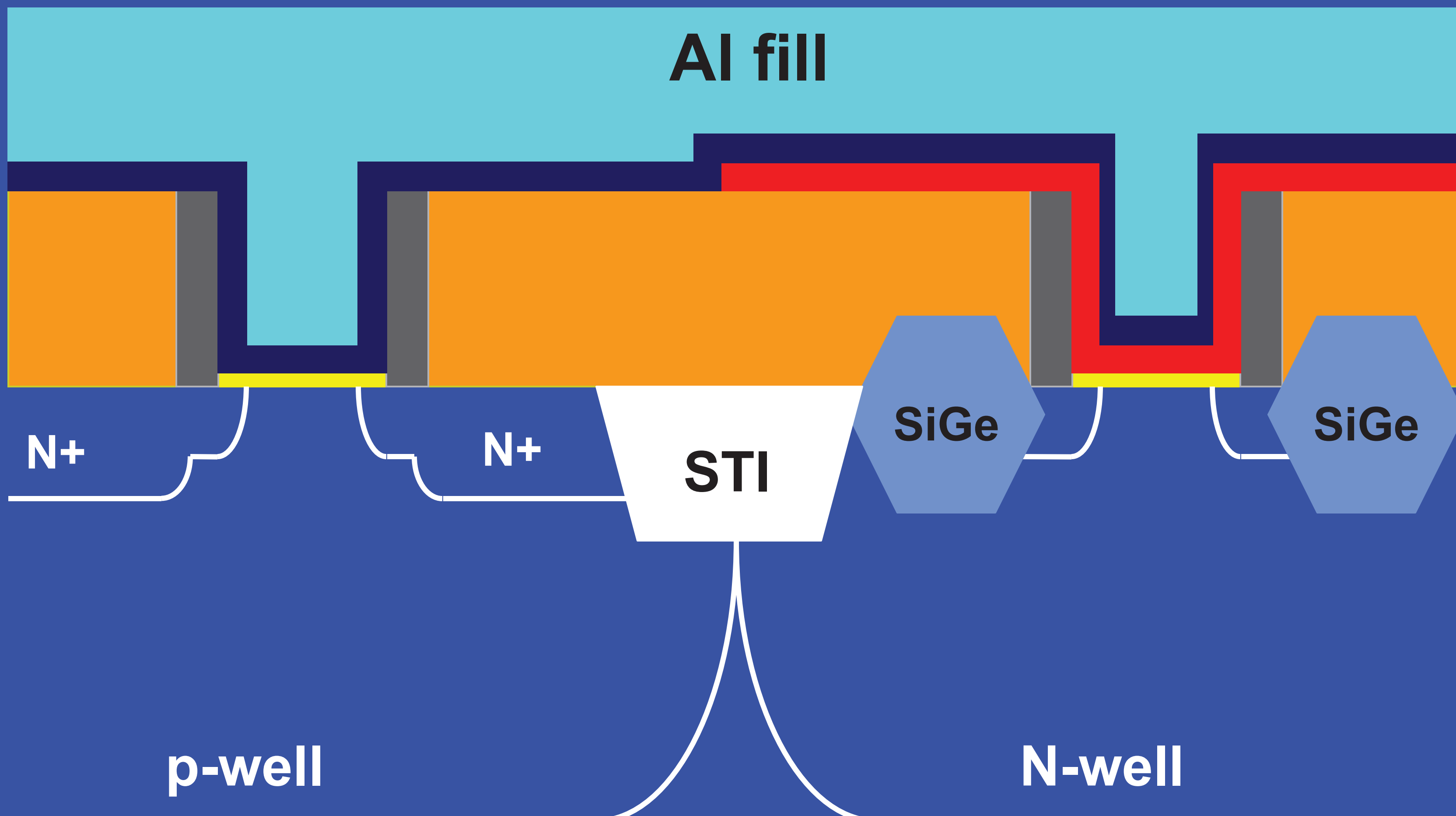
PMOS WF Metal patterning

Transistor Process Flow



NMOS WF Metal deposition

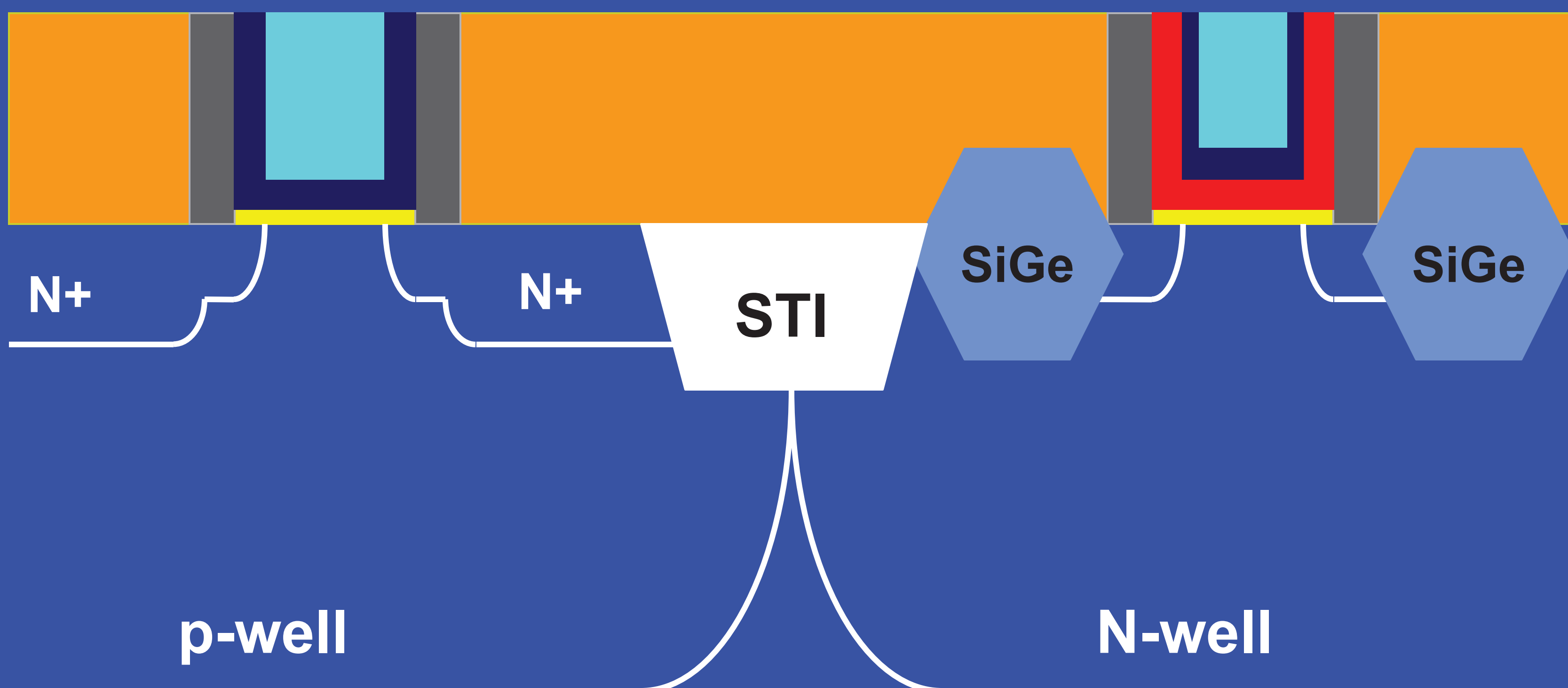
Transistor Process Flow



Metal Gate trenches filled with low resistance Al

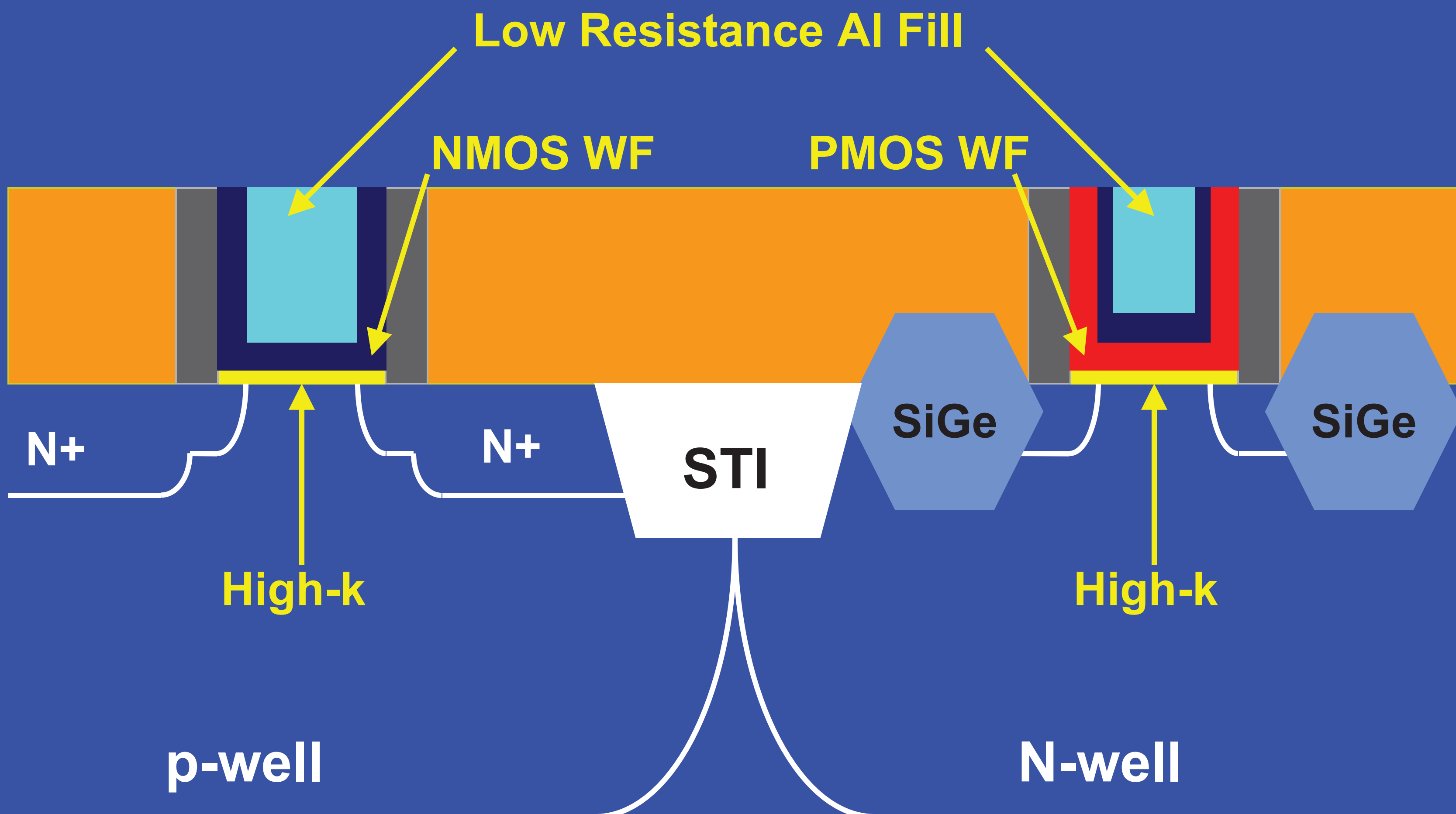
15h

Transistor Process Flow



Metal Gate Polish

Transistor Process Flow



High-k + Metal gate transistor formation complete

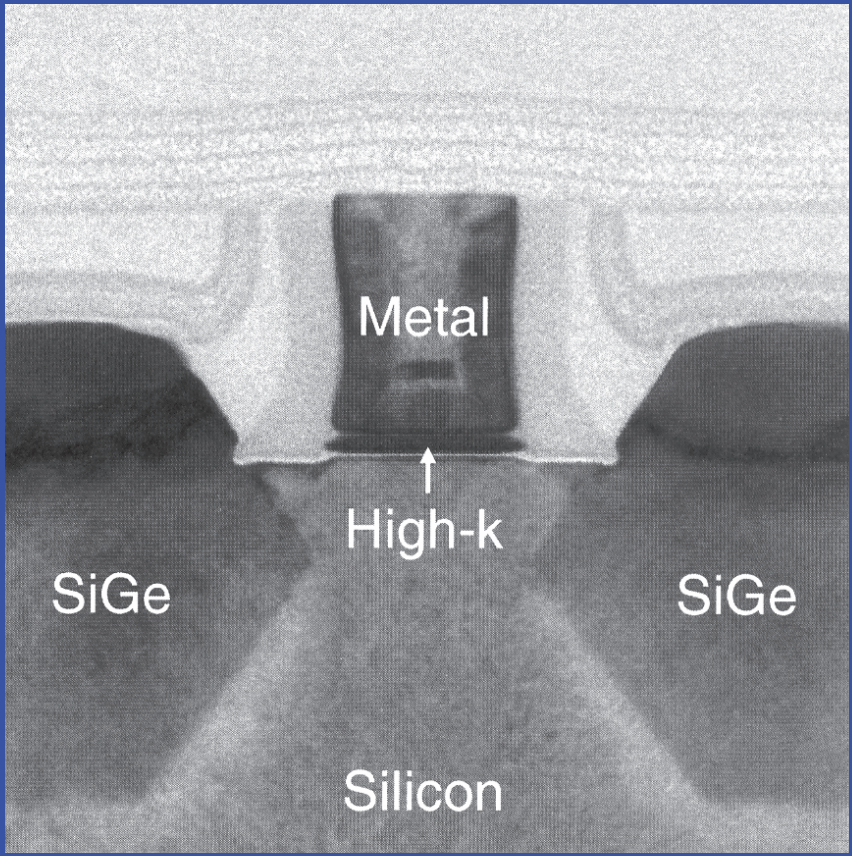
15j

Transistor Features

- 35 nm min. gate length
- 160 nm contacted gate pitch

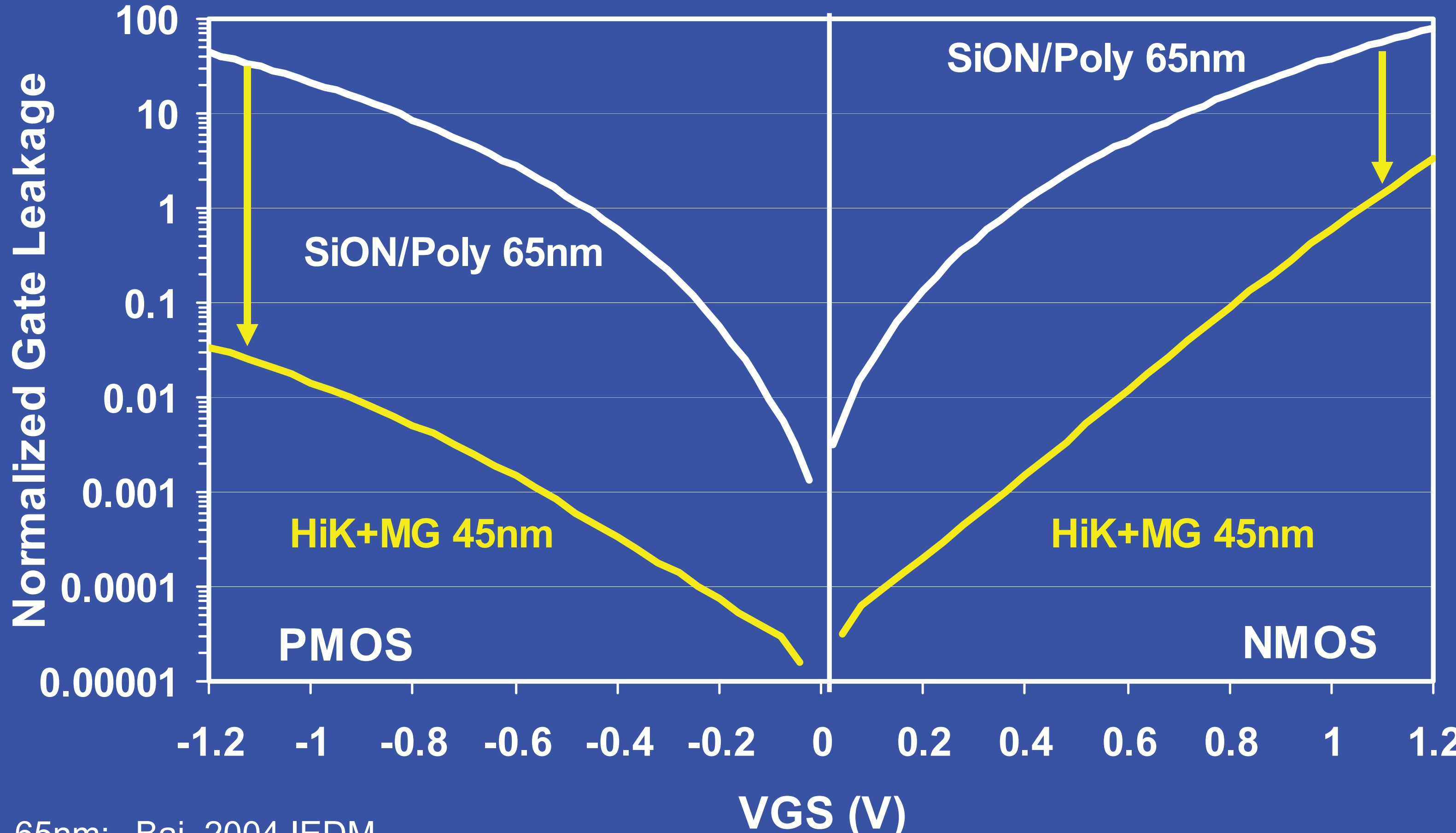
- 1.0 nm EOT Hi-K
- Dual workfunction metal gate electrodes

- 3^{RD} generation of strained silicon



Gate Leakage

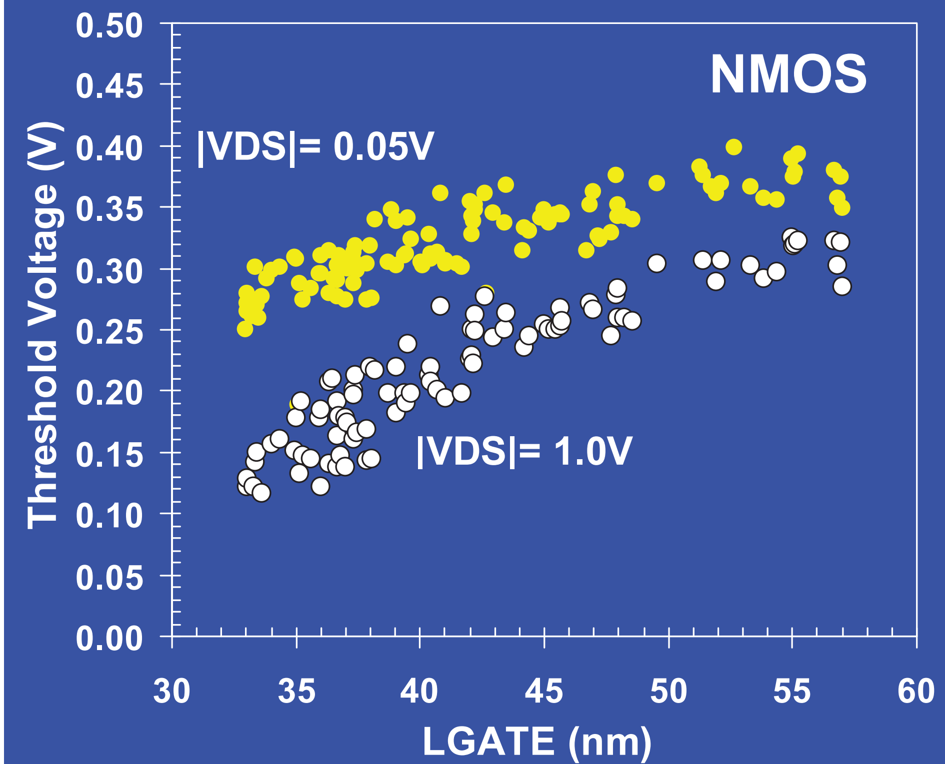
- **Gate leakage is reduced >25X for NMOS and 1000X for PMOS**

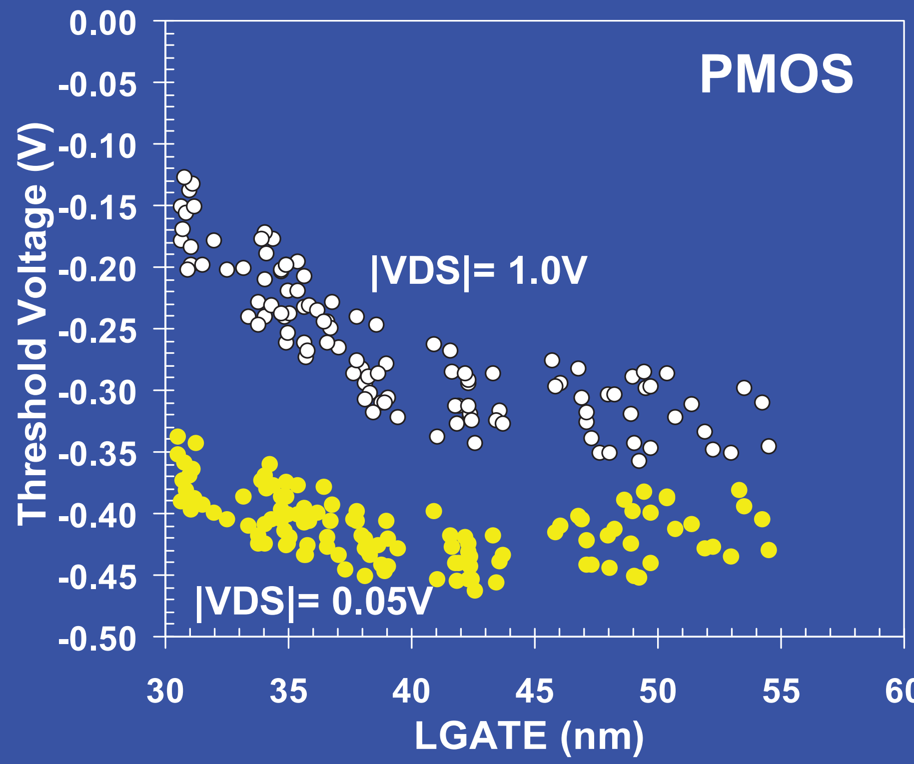


65nm: Bai, 2004 IEDM

Optimal Workfunction Metals

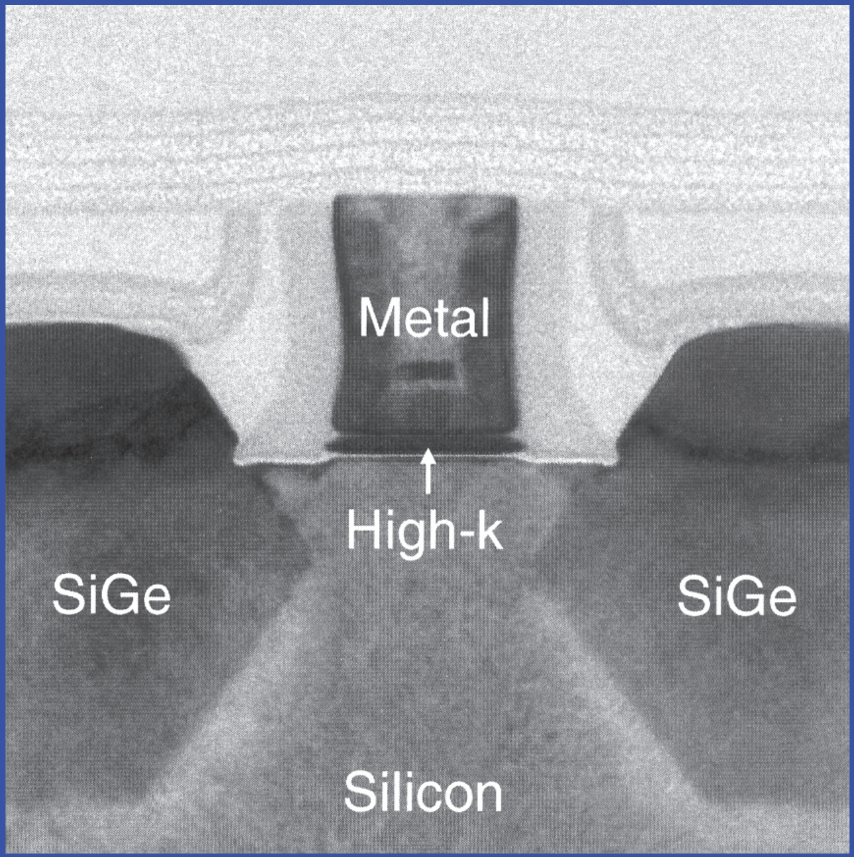
- **Excellent V_T rolloff and DIBL**





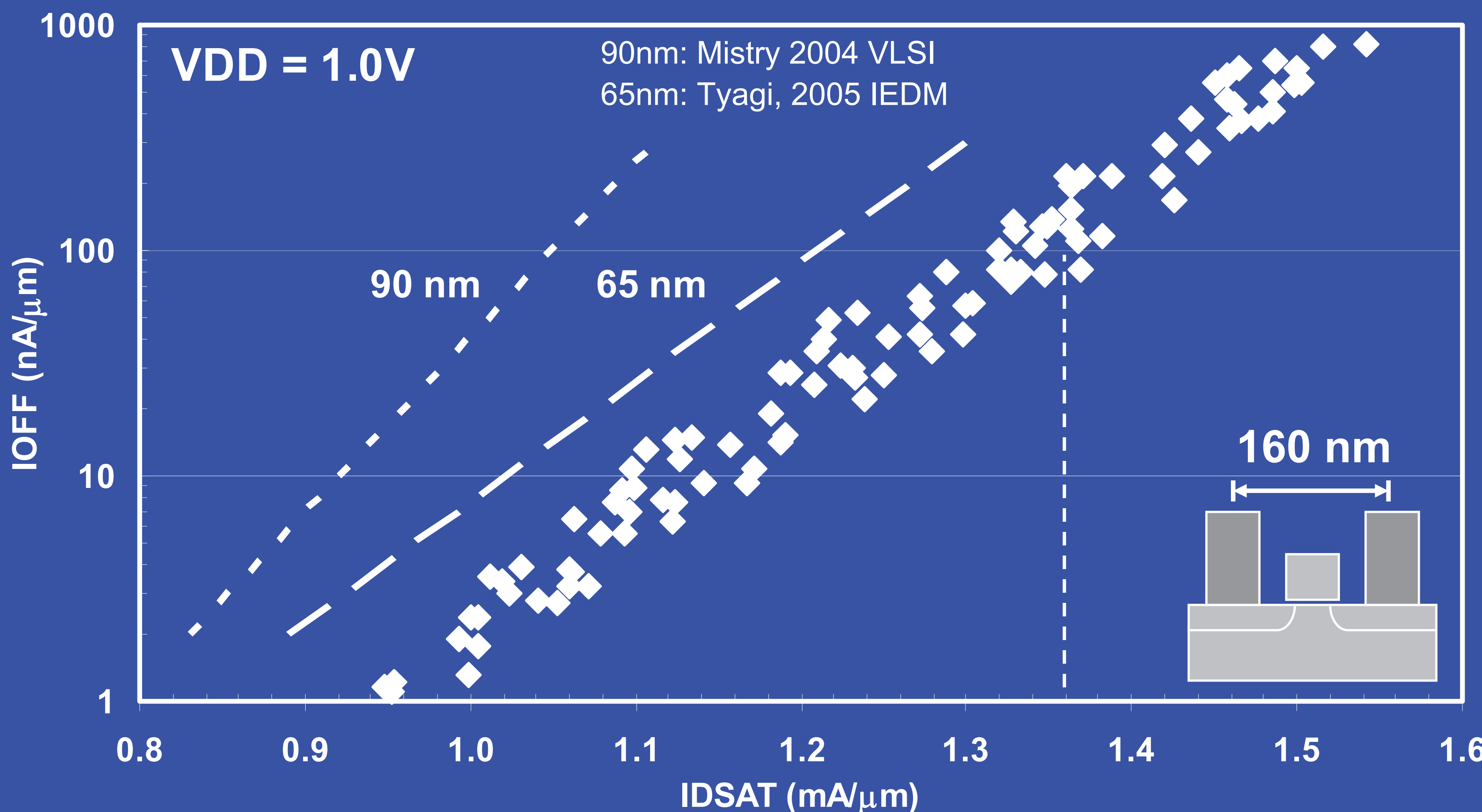
UMC 1517
UMC v. AICP

3RD Generation Strained Silicon



- **Increased Ge fraction**
  - **90 nm: 17% Ge**
  - **65 nm: 23% Ge**
  - **45 nm: 30% Ge**
- **SiGe closer to channel**

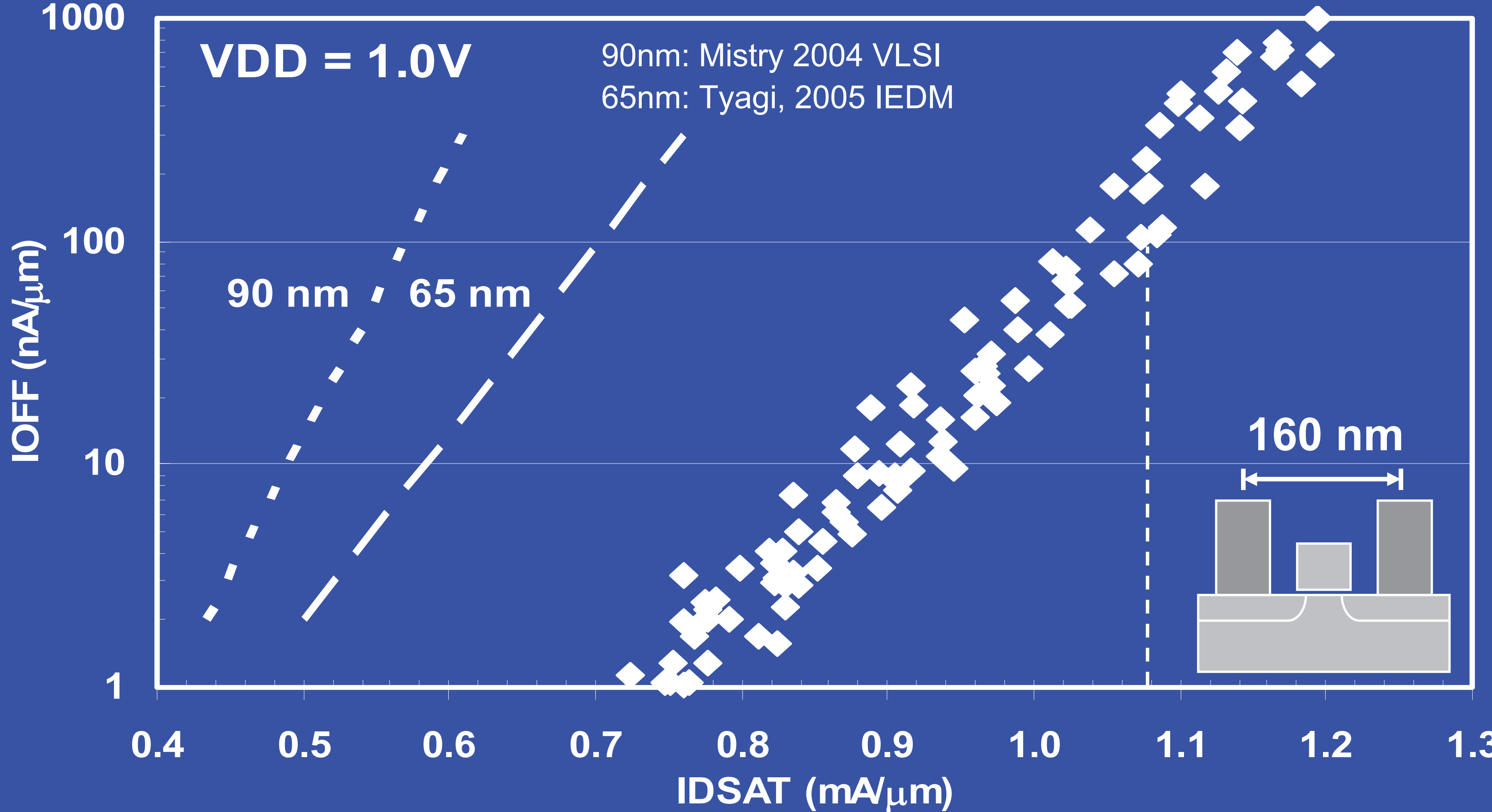
NMOS I_{DSAT} vs. I_{OFF}



1.36 mA/µm at I_{OFF} = 100 nA/µm

12% better than 65 nm

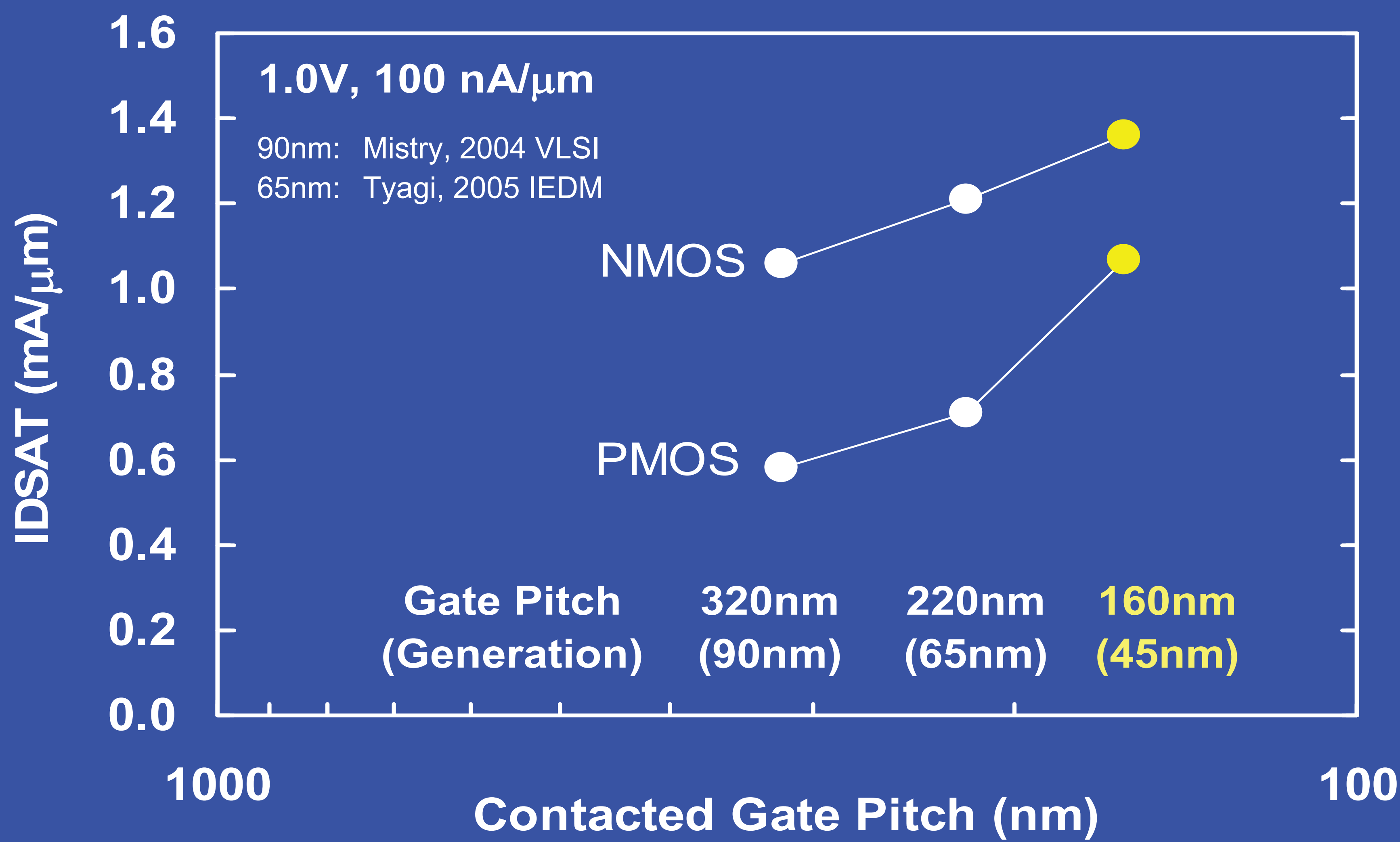
PMOS I_{DSAT} vs. I_{OFF}



1.07 mA/μm at I_{OFF} = 100 nA/μm

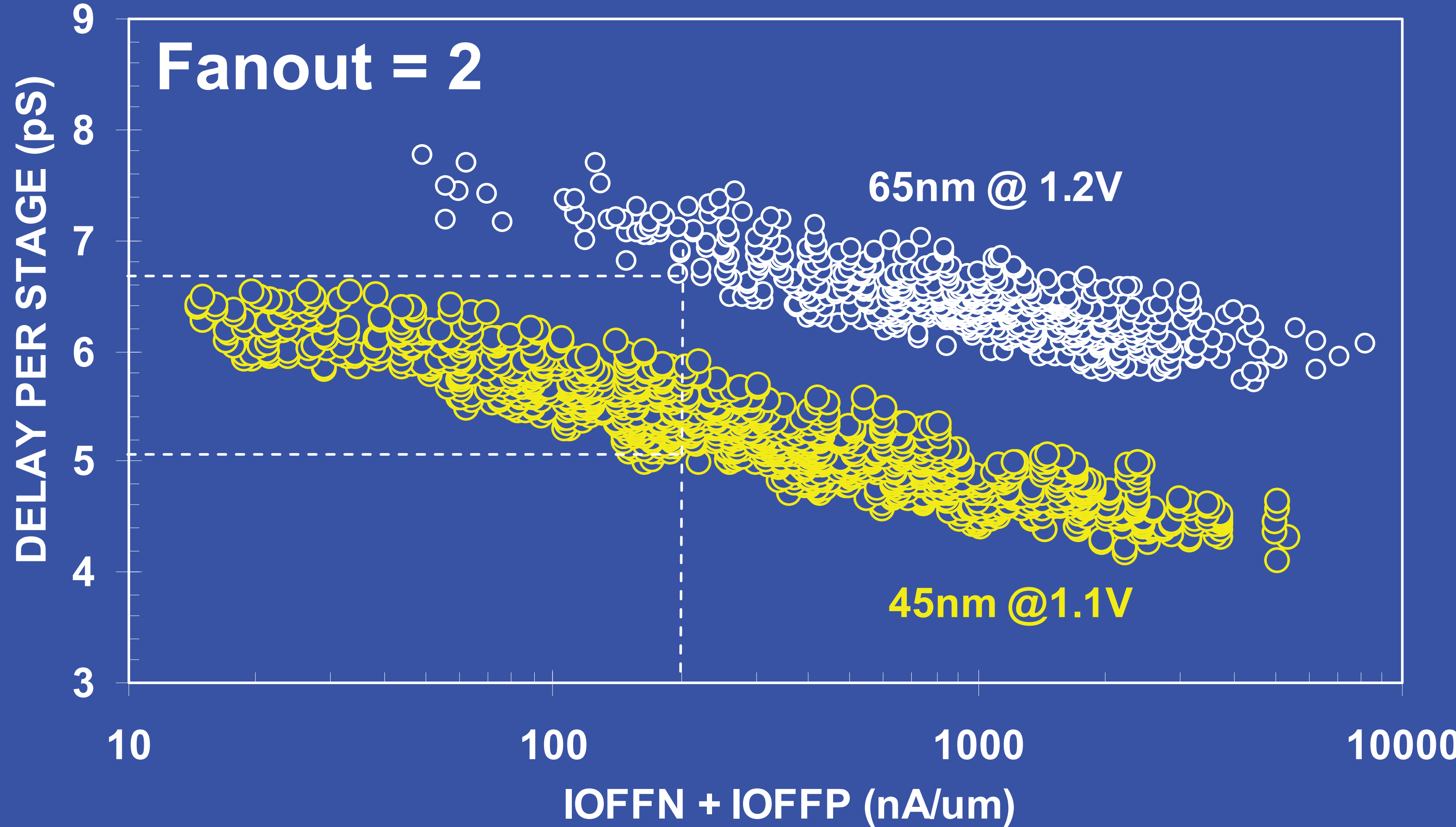
51% better than 65 nm

Transistor Performance vs. Gate Pitch



Simultaneous performance and density improvement

Ring Oscillator Performance



FO=2 delay of 5.1 ps at $I_{OFFN} = I_{OFFP}$ = 100 nA/μm

23% better than 65 nm at the same leakage

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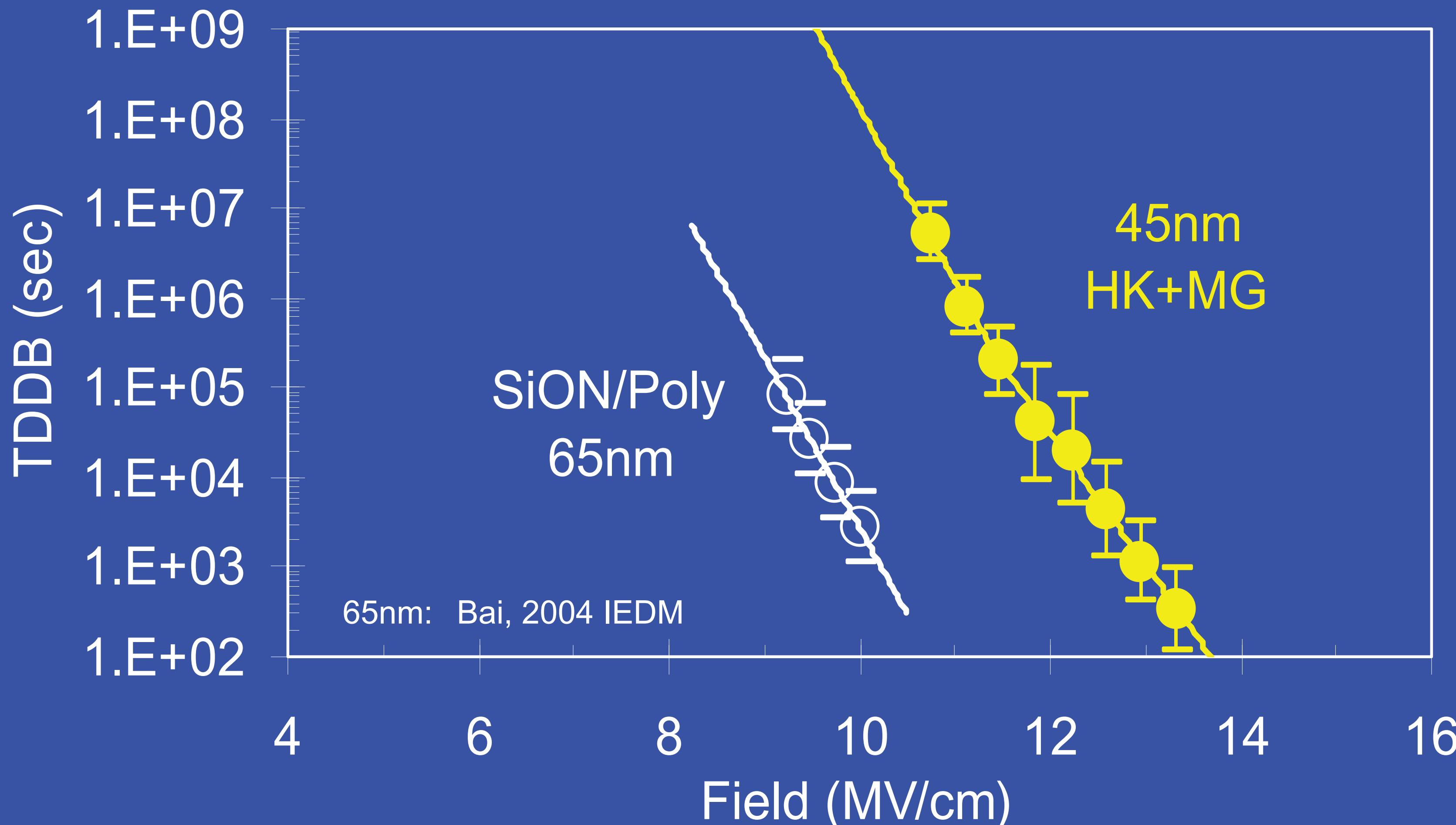
UMC v. AICP

Transistor Reliability Challenges

- Defect types in SiO_2 have been studied for decades
- New defect types for high-k need to be suppressed
- T_{INV} scaled ~0.7X relative to 65 nm
  - Need to support 30% higher E-field

Transistor Reliability - TDDB

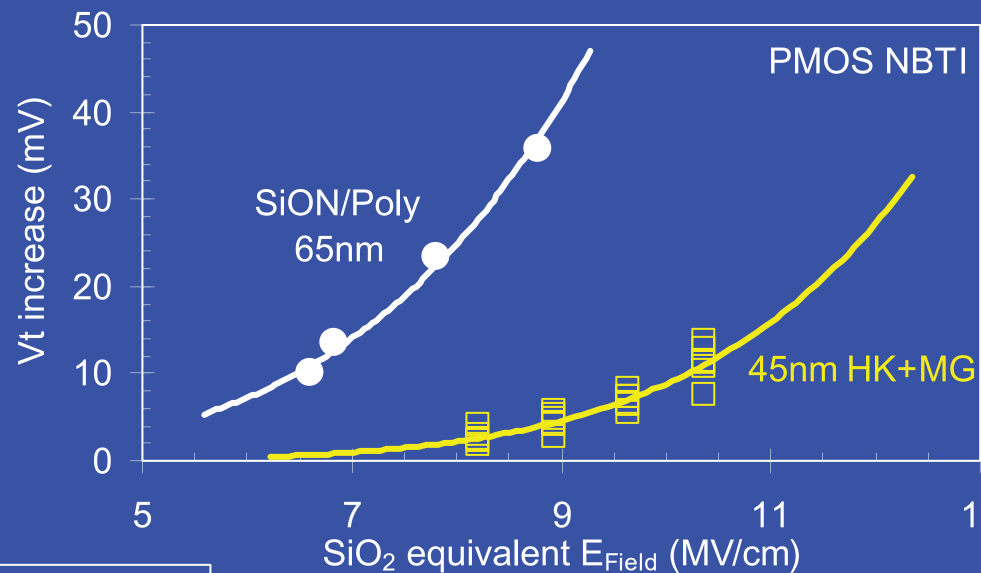


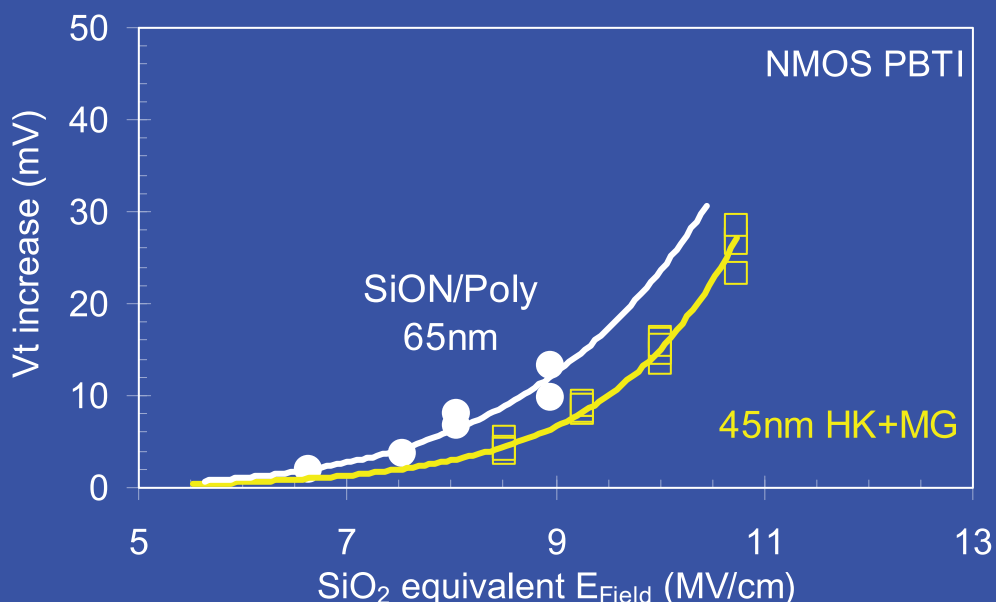
45nm High-k + Metal Gate supports 30% higher E-field

Transistor Reliability: Bias Temperature

PMOS NBTI

45 nm Hi-k + MG supports 50% higher E-field





NMOS PBTI

45 nm Hi-k + MG supports 15% higher E-field

65nm: Bai, 2004 IEDM

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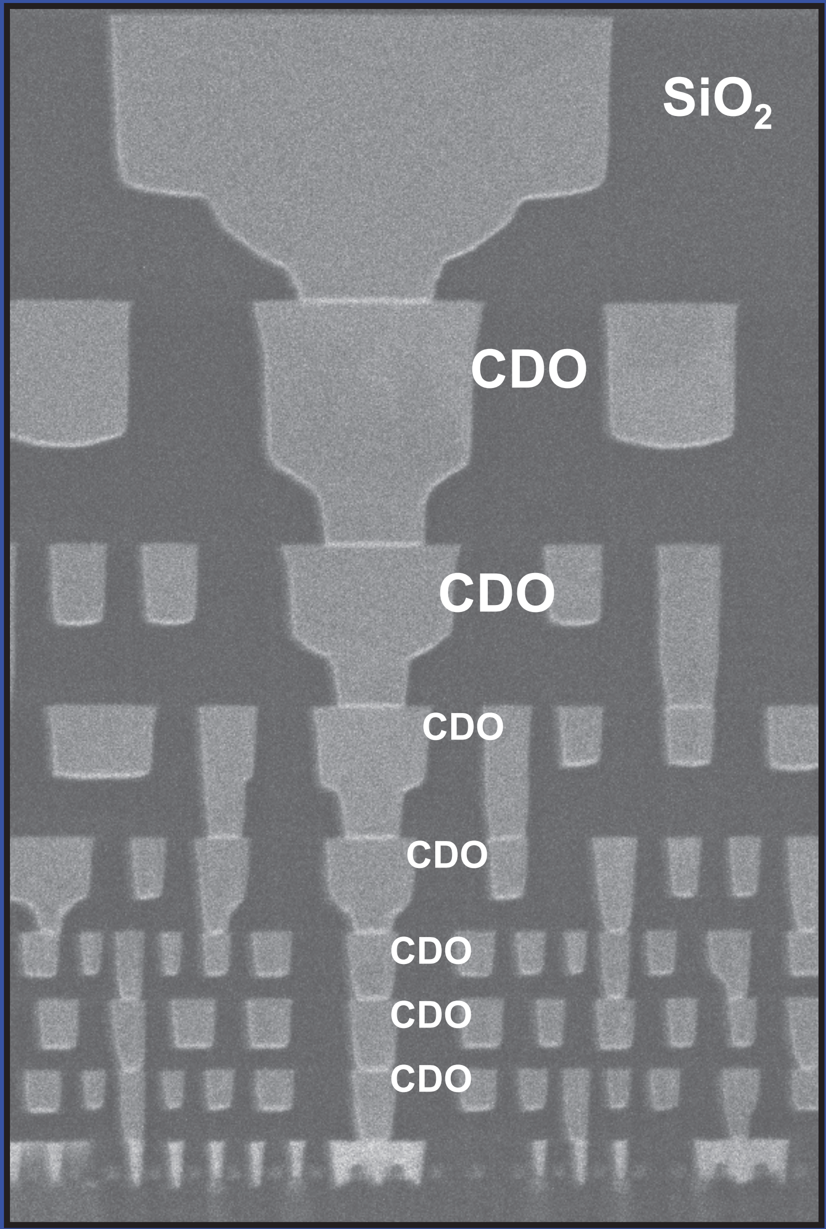
Interconnects

- Metal 1-3 pitches match transistor pitch
- Graduated upper level pitches optimize density & performance
- Lower layer SiCN etch stop layer thinned 50% relative to 65 nm
- Extensive use of low-k ILD



MT8
MT7
MT6
MT5
MT4
MT3
MT2
MT1

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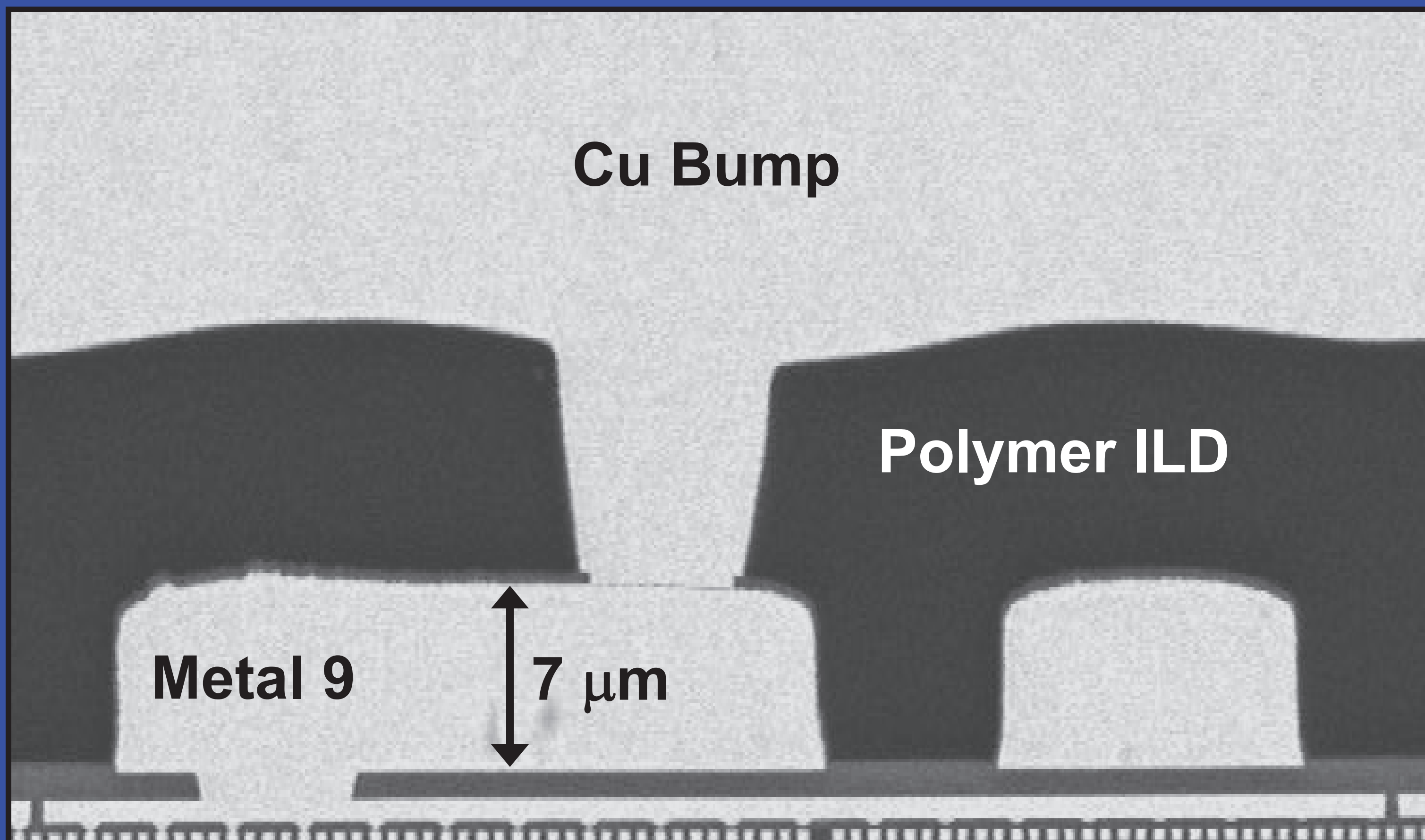
Metal 9: ReDistribution Layer (RDL)

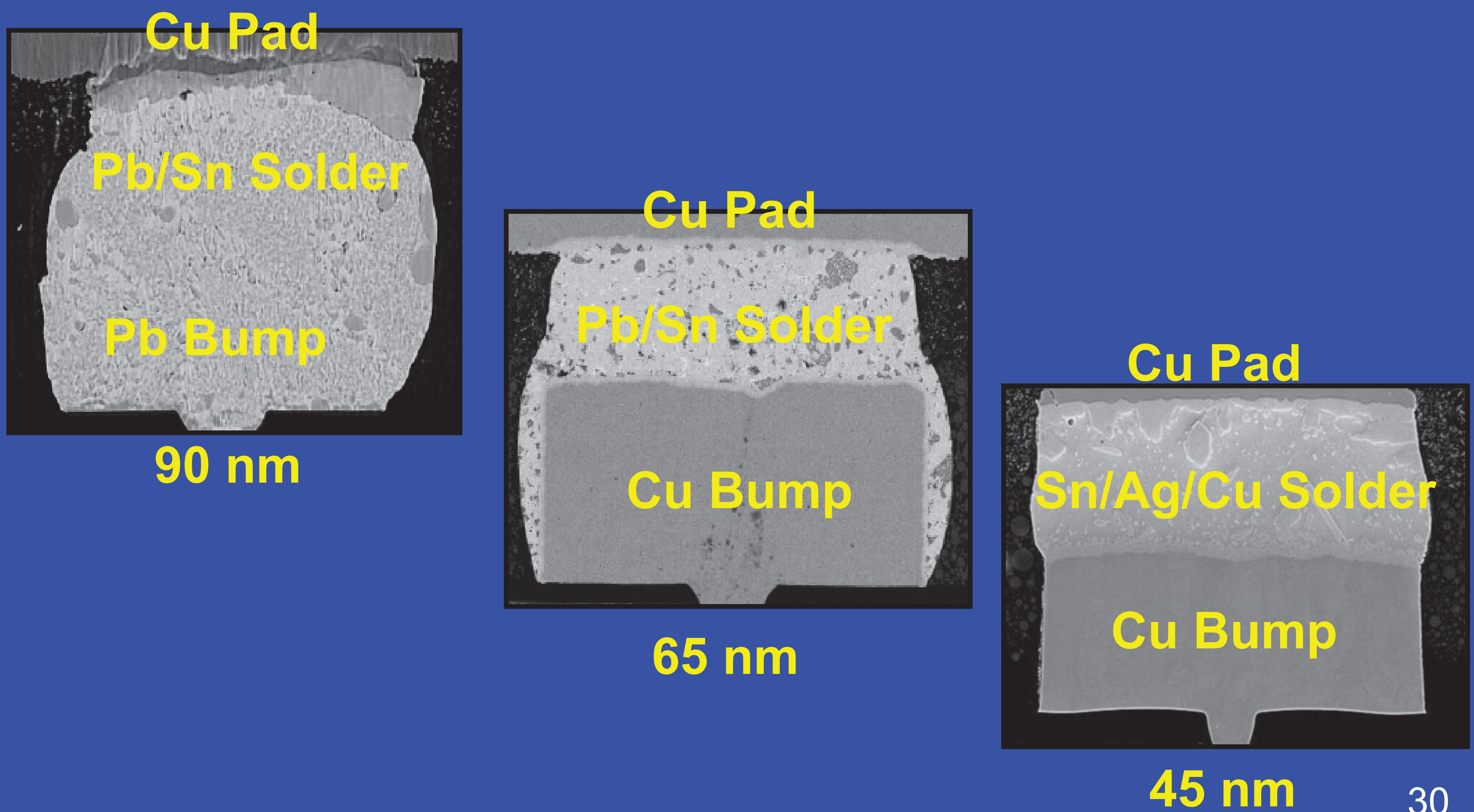
- **Metal 9 RDL: 7um thick with polymer ILD**
  - **Improved on-die power distribution**



MT8
MT7

100% Lead Free Packaging

- Environmental benefit, lower SER



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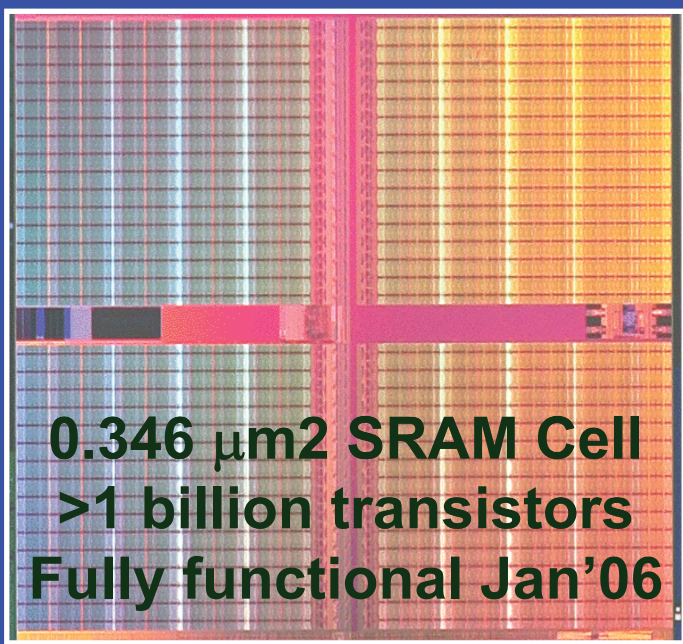
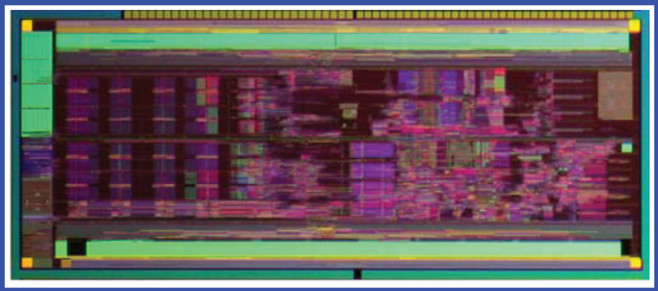
153Mb SRAM Test Vehicle

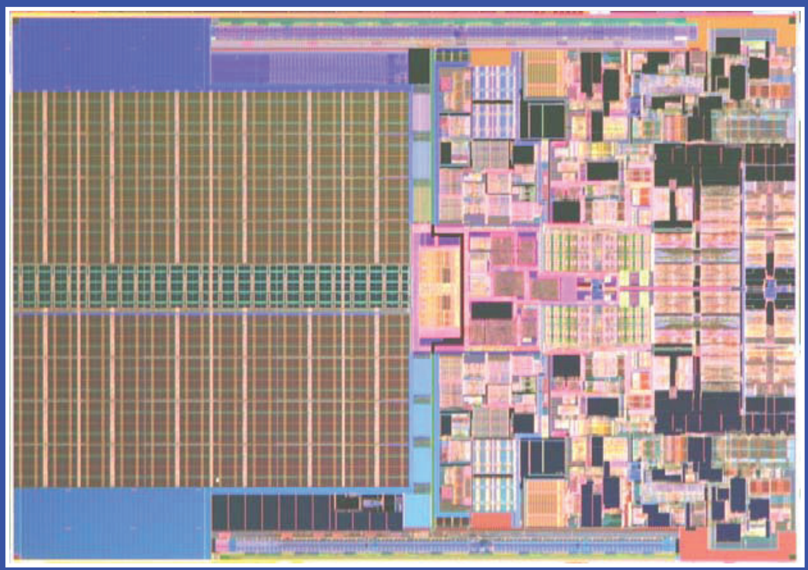
- **Process learning vehicle demonstrates**
  - High yield
  - High performance
  - Stable low voltage operation

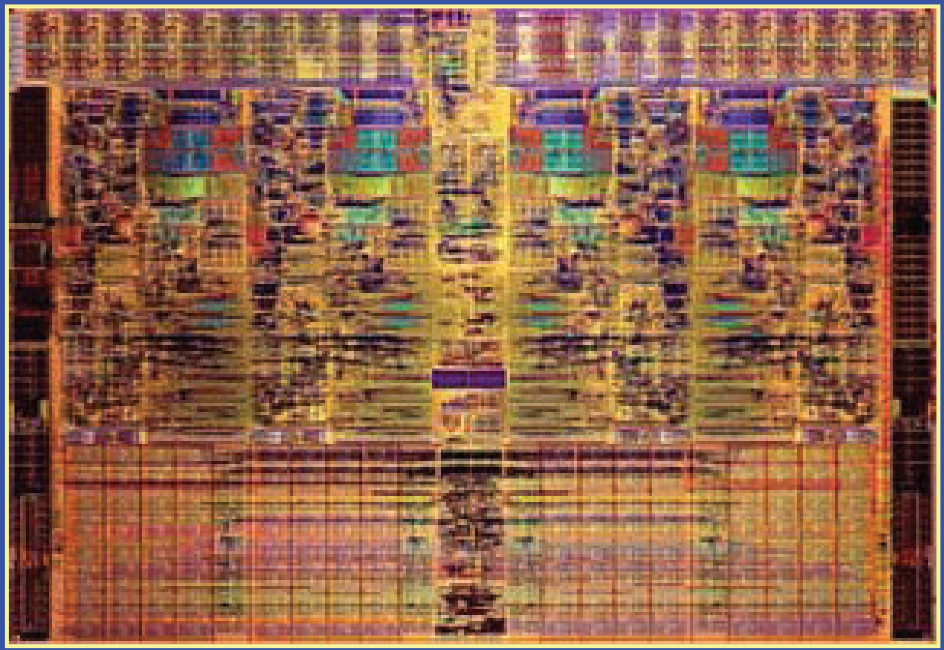



```
                                                    4.7GHz
1.3v   |****************************            .
1.2v   |**************************
                                               3.8GHz
1.1v   |************************                .
1.0v   |**********************                  .
0.9v   |****************         .              .
                      2GHz
0.8v   |******        .          .              .
        +---------+---------+---------+
      1.8GHz    2.3GHz    3.2GHz    5.3GHz
```

Multiple Microprocessors

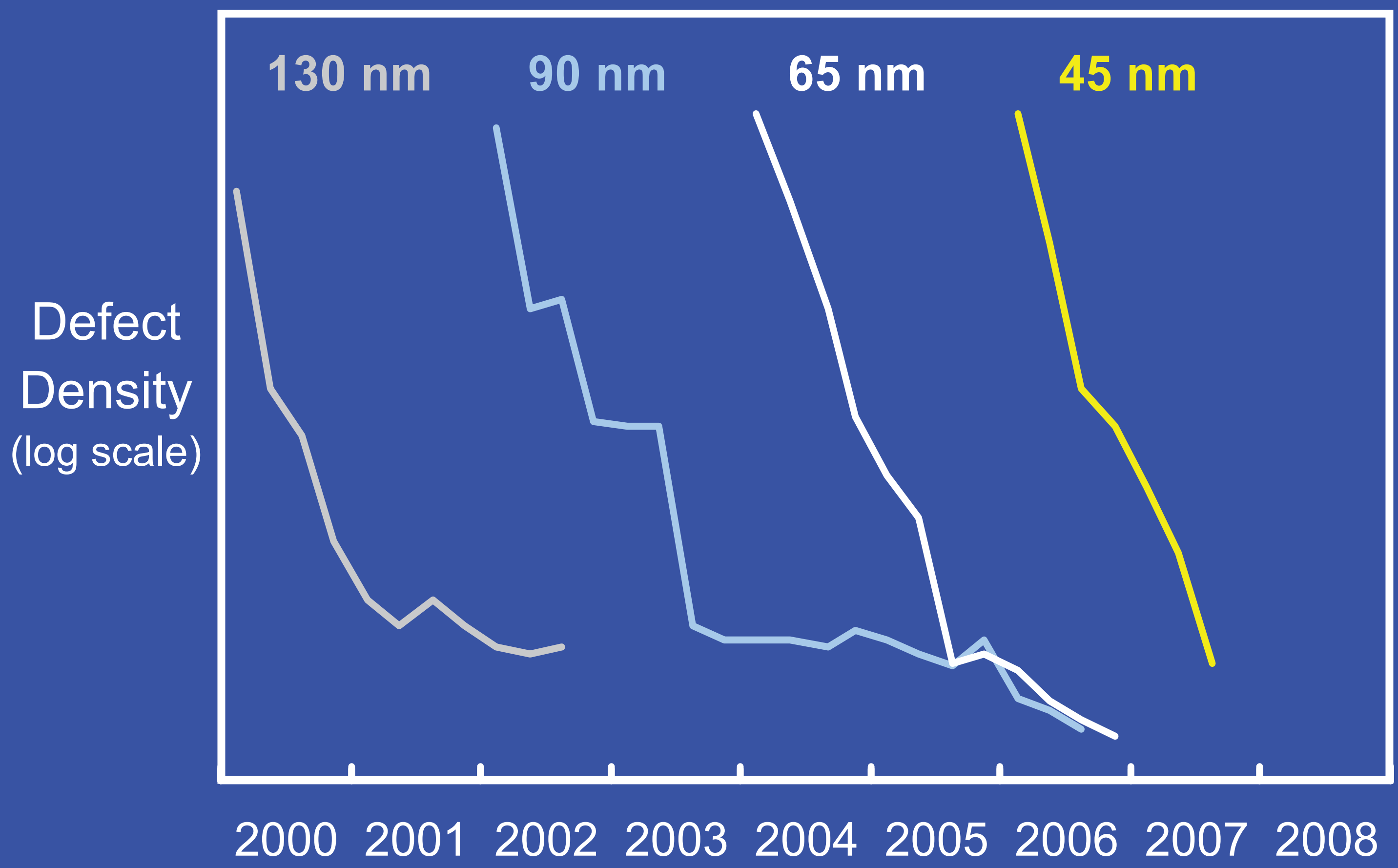

Single Core


Dual Core


Quad Core

Defect Reduction Trend

- **Mature yield demonstrated 2 years after 65 nm**



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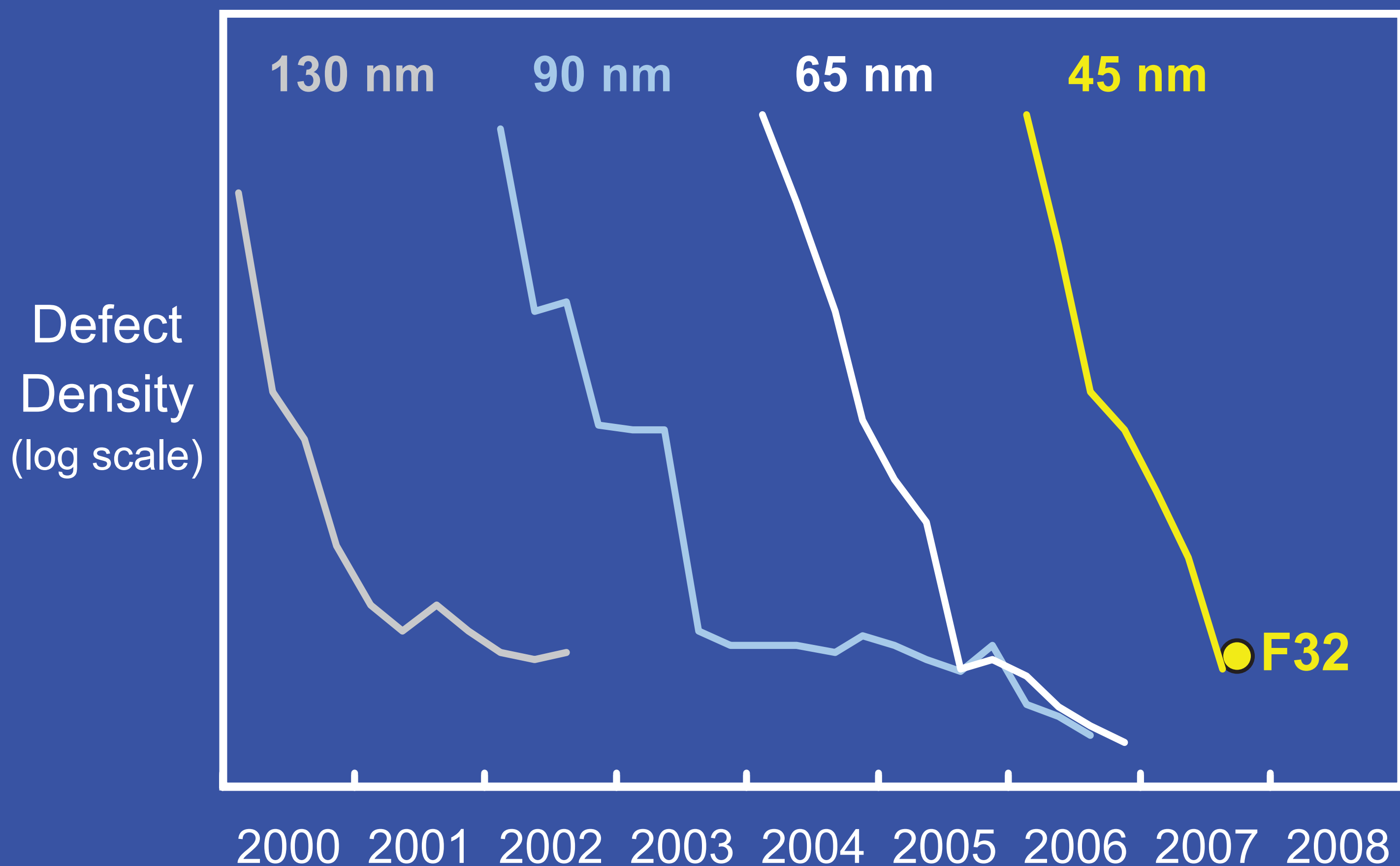
UMC v. AICP

Defect Reduction Trend

- **Mature yield demonstrated 2 years after 65 nm**
- **Matched yield in 2ND Fab – Copy Exactly!**



Conclusions

- A 45 nm technology is described with
  - Design rules supporting ~2X improvement in transistor density
  - 193nm dry lithography at critical layers for low cost
  - Trench contacts supporting local routing
  - 8 standard Cu interconnect layers with extensive use of low-k
  - Thick Metal 9 Cu RDL with polymer ILD
- High-k + Metal gate transistors implemented for the first time in a high volume manufacturing process
  - Integrated with 3[RD] generation strained silicon
  - Achieve record drive currents at low I_{OFF} and tight gate pitch
- The technology is already in high volume manufacturing
  - High yields demonstrated on SRAM and 3 microprocessors
  - High yields demonstrated in two 300mm fabs

Acknowledgements

- The authors gratefully acknowledge the many people in the following organizations at Intel who contributed to this work:
  - Portland Technology Development
  - Quality and Reliability Engineering
  - Process & Technology Modeling
  - Assembly & Test Technology Development

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