

UNITED STATES PATENT AND TRADEMARK OFFICE

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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UNITED MICROELECTRONICS CORPORATION,  
AND  
UMC GROUP USA INC.,  
Petitioners,  
v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,  
Patent Owner.

**U.S. PATENT NO. 8,796,779**

Case IPR2025-01053

**DECLARATION OF DR. SANJAY BANERJEE IN SUPPORT OF  
PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,796,779**

**UMC Ex.1101**

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I, Dr. Sanjay Banerjee, declare as follows:

1. My name is Sanjay Banerjee.
2. I have been retained as an expert witness on behalf of United Microelectronics Corporation and UMC Group (USA) (collectively, “Petitioner”) for the above-captioned Petition for *Inter Partes* Review (“IPR”) (“Petition”) of U.S. Patent No. 8,796,779 (“the ’779 patent”) (Ex.1001). I am being compensated for my time in connection with this Petition at my standard consulting rate of \$675 per hour. My compensation is not affected by the outcome of, or my testimony in, this IPR, or any litigation proceedings. I am informed that the assignee for the patent in the present proceeding is Advanced Integrated Circuit Process LLC (“Patent Owner”). I am also informed that the Petition names United Microelectronics Corporation and UMC Group (USA) as real-parties-in-interest.
3. I have been asked to provide my opinions regarding whether claims 1, 2, 7, 12, and 13 of the ’779 patent (the “Challenged Claims”) are invalid as anticipated, or as obvious to a person having ordinary skill in the art at the time of the alleged invention of the ’779 patent (“POSITA”).
4. The ’779 patent issued on August 5, 2014, from U.S. Patent Application No. 13/665,305, filed on October 31, 2012. The ’779 patent claims priority to Japan Application No. 2010-205599, filed on September 14, 2010.

5. I am not currently, and have not at any time in the past been, an employee of any Petitioner or any real-party-in-interest. Other than set out above, I have no affiliation, contractual connection, or financial connection with any Petitioner or any real-party-in-interest, or any of their respective subsidiaries or parents. I similarly have no financial interest in, or affiliation with the Patent Owner.

## **I. BACKGROUND AND QUALIFICATIONS**

6. I am currently the Cockrell Family Chair Professor of Electrical and Computer Engineering at the University of Texas at Austin. At UT Austin, I was also the director of the Microelectronics Research Center from September 1999 through January 2025. I have been a faculty member at UT Austin since 1987.

7. I have also been active in industries related to the relevant field of art. As a Member of the Technical Staff, Corporate Research, Development and Engineering of Texas Instruments Incorporated from 1983–1987, I worked on polysilicon transistors and dynamic random access trench memory cells used by Texas Instruments in the world’s first 4-Megabit DRAM, for which I was co-recipient of the Best Paper Award, IEEE International Solid State Circuits Conference, 1986.

8. I received a B. Tech. degree from the Indian Institute of Technology, Kharagpur, and M.S. and Ph.D. degrees from the University of Illinois at Urbana-Champaign, all in Electrical Engineering.

9. I am a leading researcher and educator in various areas of transistor device fabrication technology, including the fabrication, characterization and application of memory devices, transistors, and nanotechnology. My research has been funded by the Texas Advanced Technology Program (ATP), the Texas Higher Education Coordinating Board, the National Science Foundation, the SEMATECH (Semiconductor Manufacturing Technology) consortium, the SRC (Semiconductor Research Corporation) consortium, DARPA, and the Department of Energy, among others.

10. At the University of Texas, I served as the director of the South West Academy of Nanoelectronics from its inception through the end (2006 - 2017), one of three centers in the United States established to develop a replacement for MOSFETs.

11. I have published over 1,200 technical articles, many related to semiconductor fabrication technology, most at highly competitive refereed conferences and rigorously reviewed journals. I have also published 8 books or chapters on transistor device physics and fabrication, and have supervised over 80 Ph.D. and 60 MS students.

12. I have been a member of scientific organizations and committees, including the IEEE Dan Noble Award Committee from 2010–2013, serving as Chair from 2012–2013, the International Technology Roadmap for Semiconductors, the

International Conference on MEMS (Microelectromechanical Systems) and Nanotechnology, the IEEE International Conference on Communications, Computers, Devices, the International Electron Devices Meeting, the International Conference on Simulation of Semiconductor Processes and Devices, and the IEEE Symposium on VLSI (Very-Large-Scale Integration) Technology. I have served as the Session Chair for the “Device Technology” Session conducted at the IEEE International Electron Devices Meeting in 1989–1990. I have also served as the General Chairman for the IEEE University Government Industry Microelectronics Symposium in 1994–1995, and Chair of the IEEE Device Research Conference.

13. I have served on the Technical Advisory Boards of AstroWatt, DSM Semiconductors, Cambrios, Nanocoolers Inc., BeSang Memories, Organic ID and ITU Ventures; Gerson Lehmann Group, NY; Austin Community College; Asia Pacific IIT; Rochester Institute of Technology, and HSMC Foundry.

14. I received the Engineering Foundation Advisory Council Halliburton Award (1991), the Texas Atomic Energy Fellowship (1990–1997), Cullen Professorship (1997–2001) and the Hocott Research Award from UT Austin (2007). I also received the SIA/SRC University Researcher Award (2018), IEEE Grove Award (2014), Distinguished Alumnus Award, IIT (2005), Industrial R&D 100 Award (2004), ECS Callinan Award, 2003, IEEE Millennium Medal, 2000, NSF Presidential Young Investigator Award in 1988, and several SRC Inventor

Recognition and Best Paper Awards. I was a Distinguished Lecturer for IEEE Electron Devices Society, and am a Fellow of the Institute of the Electrical and Electronics Engineers (IEEE), the American Physical Society (APS) and the American Association for the Advancement of Science (AAAS).

15. I am the inventor or co-inventor of over 35 United States patents in various areas of transistor device fabrication technology. I was elected a Fellow of the National Academy of Inventors in 2021.

16. My qualifications and publications are set forth more fully in my curriculum vitae, attached as Ex.1102.

## **II. MATERIALS AND OTHER INFORMATION CONSIDERED**

17. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art and have considered the viewpoint of a POSITA at the time of the alleged invention.

18. I have considered the materials referenced herein, including the '779 patent (Ex.1001), the file history of the '779 patent (Ex.1002), the parent and related applications, the file histories of the parent and related applications, the Petition, and other documents listed in the Exhibit List of the Petition, including:

Description	Date of Availability
U.S. Patent No. 6,881,657 to Torii, et al. (“Torii”) (Ex.1005)	Issued April 19, 2005.
U.S. Patent No. 6,787,421 to Gilmer, et al. (“Gilmer”) (Ex.1009)	Issued September 7, 2004.
U.S. Patent No. 7,382,023 to Chen, et al. (“Chen”) (Ex.1010)	Issued June 3, 2008.

19. It is my understanding that the references listed above are prior art to the '779 patent, which is entitled to a priority date not earlier than September 14, 2010. Torii, Gilmer, and Chen (Exs. 1005, 1009, and 1010) were not discussed during the prosecution of the '779 patent.

### III. UNDERSTANDING OF PATENT LAW

20. I am not an attorney. For purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law is as listed below.

#### A. Claim Construction

21. I understand that in an IPR petition filed after November 13, 2018, a claim must be construed under the *Phillips* standard. Under that standard, words of a claim are given their plain and ordinary meaning as understood by a POSITA at the time of invention, in light of the specification and prosecution history, unless those sources show an intent to depart from such meaning, as well as pertinent evidence extrinsic to the patent.

22. I have applied this understanding in my declaration. I do not believe any claim terms require explicit construction in this proceeding to resolve the patentability of the Challenged Claims.

**B. Anticipation and Obviousness**

23. I have been informed that a patent claim is anticipated if a single prior art reference, such as a patent or a publication, discloses all the limitations of the claimed invention.

24. I have been informed and understand that a patent claim can be considered to have been obvious to a POSITA at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a POSITA at the time the application was filed. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

25. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to a POSITA. In determining whether a combination based on either a single reference or multiple references would have been obvious, I have been informed that it is appropriate to consider at least the following factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;
- whether a POSITA could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed limitations represent one of a limited number of known design choices, and would have a reasonable expectation of success by a POSITA;
- whether a POSITA would have recognized a reason to combine known limitations in the manner described in the claim;

- whether there is some teaching or suggestion in the prior art to make the modification or combination of limitations claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

26. I understand that a POSITA has ordinary creativity and is not an automaton.

27. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

28. I understand that prior art to the '779 patent for purposes of my opinion herein includes patents and printed publications in the relevant art that predate the priority date of the '779 patent.

29. I understand that certain factors—often called “secondary considerations”—may support or rebut an assertion of obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the alleged invention, skepticism of those having ordinary skill in the art at the time of the alleged invention, unexpected results of the alleged invention, any long-felt but unsolved need in the art that was satisfied by the alleged

invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field.

30. I further understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

#### **IV. SUMMARY OF OPINIONS**

31. It is my opinion that claims 1, 2, 7, 12, and 13 are anticipated by Torii (Ground I).

32. It is my opinion that claims 1, 12, and 13 are obvious in view of Gilmer (Ground II).

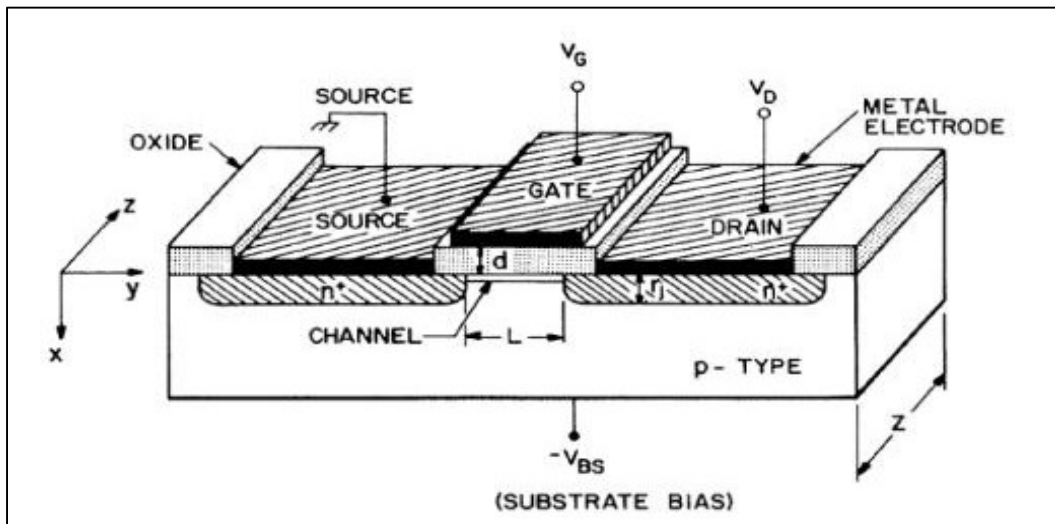
33. It is my opinion that claims 1, 12, and 13 are obvious in view of a combination of Gilmer and Chen (Ground III).

#### **V. OVERVIEW OF THE TECHNOLOGY**

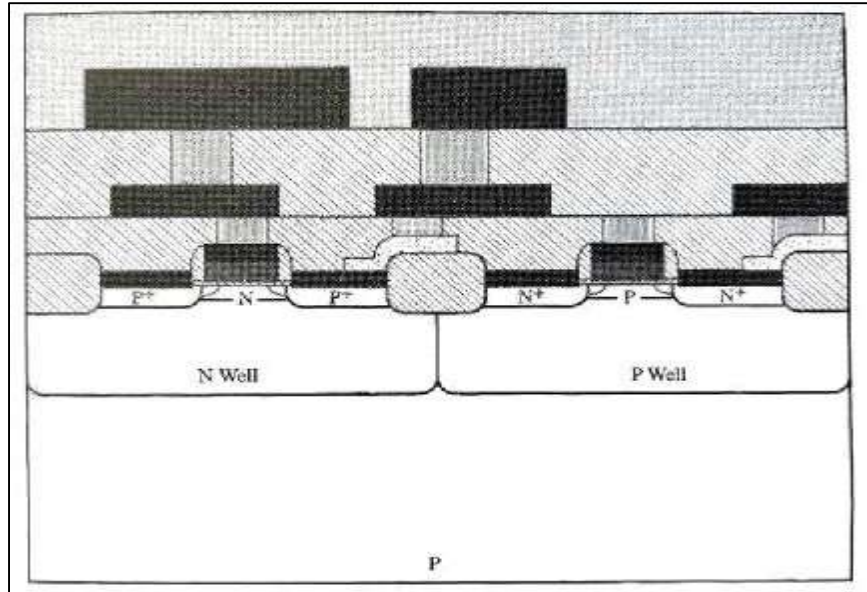
34. Broadly speaking, a semiconductor device is an electrical device made of semiconductor material like silicon or germanium. This includes many types of devices like light-emitting diodes (LEDs) and metal oxide semiconductor (MOS) transistors. Field effect transistors are just one type of semiconductor devices and have been in commercial use for decades, as discussed in more detail below.

## A. MISFET/MOSFET

35. A metal insulating semiconductor field-effect transistor (MISFET), commonly referred to as a metal oxide semiconductor field-effect transistor (MOSFET) if the insulator is an oxide, is a transistor that switches from an OFF state to an ON state when a voltage greater than the threshold voltage is applied to a gate terminal. In the ON, or active state, current flows from a source to a drain through a channel region. For the transistor types at issue in this IPR, the channel region is located under the gate electrode (which can be made of stacked metal layers) and the gate insulating layer (often called a gate oxide or gate dielectric), and between the source and drain. Sze-1981, Ex.1413, 433-34, Fig. 3 (below); Plummer, Ex.1215, 71-76, Figs. 1-11 (further below).

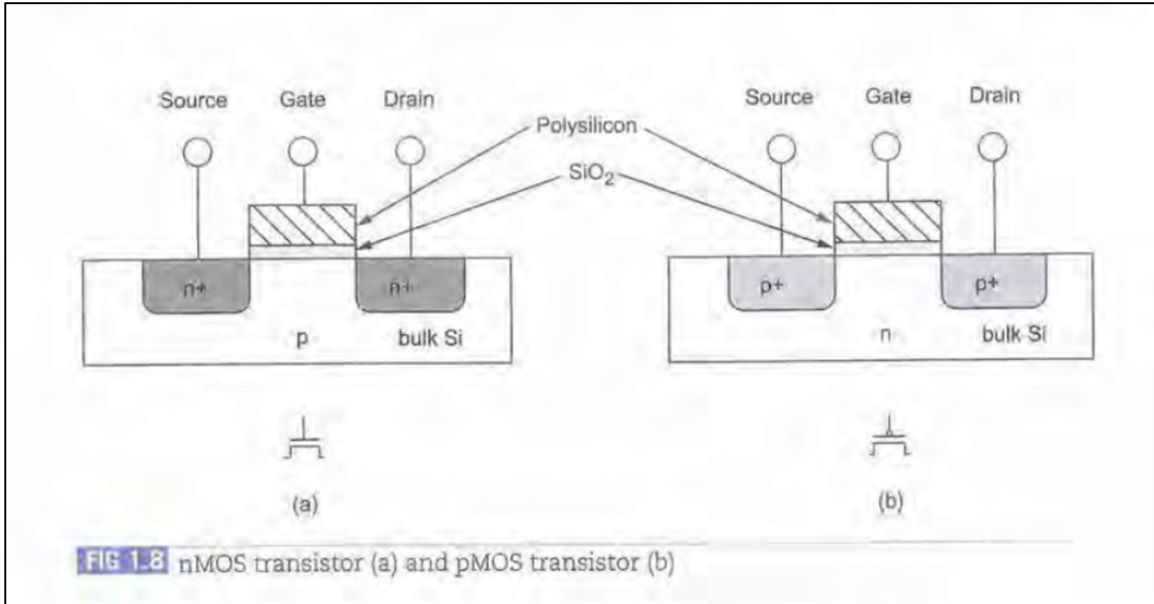


Sze-1981, Ex.1413, Fig. 3



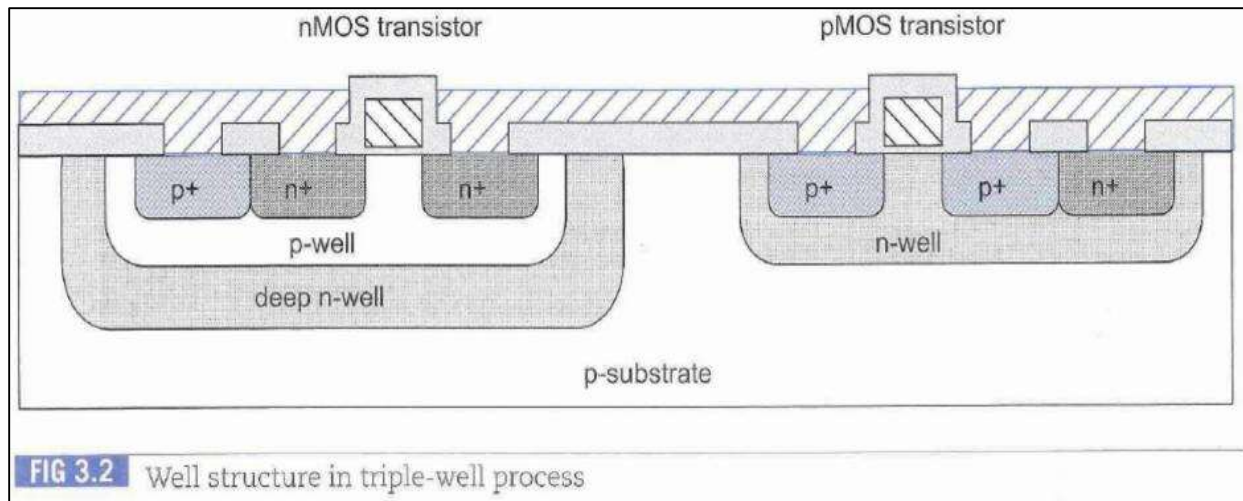
**Plummer, Ex.1215, Fig. 1-11**

36. MOSFETs are characterized by the material used in the source and drain. A MOSFET with source/drain regions made from “p-type” material is known as a PMOS or p-FET, while a MOSFET with source/drain regions made from “n-type” material is known as a NMOS or n-FET. Thus, MOSFETs generally include a gate electrode, a gate insulating layer, and “the silicon wafer, also called the substrate, body or bulk.” Weste, Ex.1212, 8. An nMOS transistor “is built with a p-type body and has regions of n-type semiconductor adjacent to the gate called the source and drain.” *Id.*, 8 (emphasis omitted), FIG. 1.8(a). A pMOS transistor “is just the opposite, consisting of p-type source and drain regions with an n-type body.” *Id.*



*Id.*, 8, FIG. 1.8(b) (above, right).

37. In the mid-1980s, complementary MOS (CMOS) devices became popular, which have both PMOS (p-FET) and NMOS (n-FET) transistors on the same substrate or integrated circuit (IC). In such devices, the active areas (and associated transistors) are generally formed in regions called “wells,” and a transistor can even have more than one well, as seen below. *See Weste, Ex.1212, 117-118, FIG. 3.2 (below).*

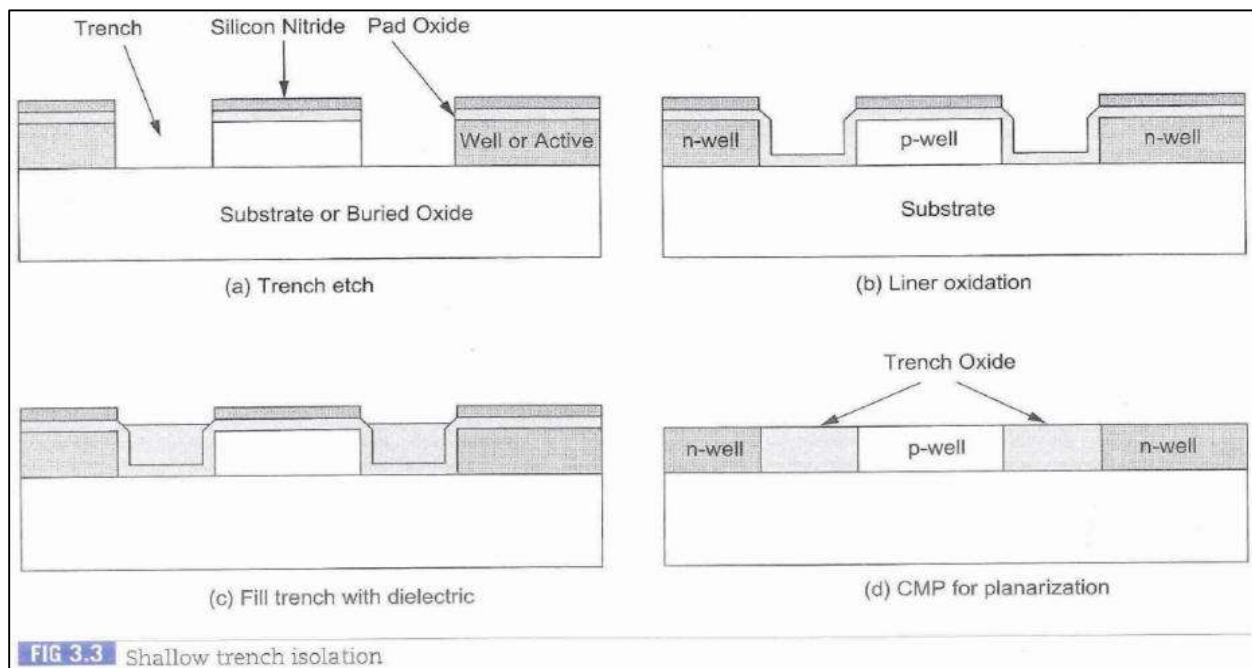


**Weste, Ex.1212, Fig. 3.2**

38. Impurities known as “dopants” are added to the active areas and wells to add charge carriers and tailor the electrical properties of these regions, such as their conductivity. The wells have opposite dopant types to the dopants of the source/drain. As such, an n-FET is formed in a p-well, and a p-FET is formed in an n-well. *See Weste, Ex.1212, 8, FIG. 1.8(b).*

39. With respect to dopants, charge carriers can be electrons (which are negatively charged) or holes (which are positively charged). When a region is doped with p-type dopants (like boron), the holes are majority carriers and the electrons are minority carriers. *See Weste, Ex.1212, 7; Plummer, Ex.1215,, 17.* When a region is doped with n-type dopants (like arsenic), the electrons are majority carriers and the holes are minority carriers. *See Weste, Ex.1212, 7; Plummer, Ex.1215,, 17 (“The electrons or holes are introduced on a one for one basis by the dopants.”).*

40. One issue with ICs relates to forming multiple devices on the same chip, and often it is necessary to isolate two structures from each other to ensure proper operation on the chip. One example of this isolation is forming a shallow trench isolation on the substrate between devices. *See Weste, Ex.1212, 117.* In the example below, a trench is etched between a p and n-well to form the shallow trench isolation. *Id.*, 119, Fig. 3.3 (below).



**Weste, Ex.1212, Fig. 3.3**

41. Once the dopants are added, or implanted, into the silicon substrate, they need to be annealed, for example to repair the silicon crystal lattice from any damage caused by the dopant implantation. Plummer, Ex.1215,, 81-82. “Because the ion implantation process creates damage, most dopants are not electrically active at the end of the implantation.” *Id.*, 470. A rapid thermal anneal, often at temperatures over 1000

degrees Celsius, can activate the dopants and repair some of the damage done by implantation. *Id.*, 81. Annealing can also cause diffusion of the implanted dopants throughout the substrate (and in certain circumstances, other layers of the device). The interaction of the implanted dopants between the source/drain, the gate electrode and the gate insulating layer, and the channel were all well understood by a POSITA long before the priority date of the challenged patents. In fact, a POSITA would often use the various interactions of the manufacturing process, for example the shape of the source/drain after dopant implantation and annealing, to improve and optimize the performance of the semiconductor device, as discussed further below.

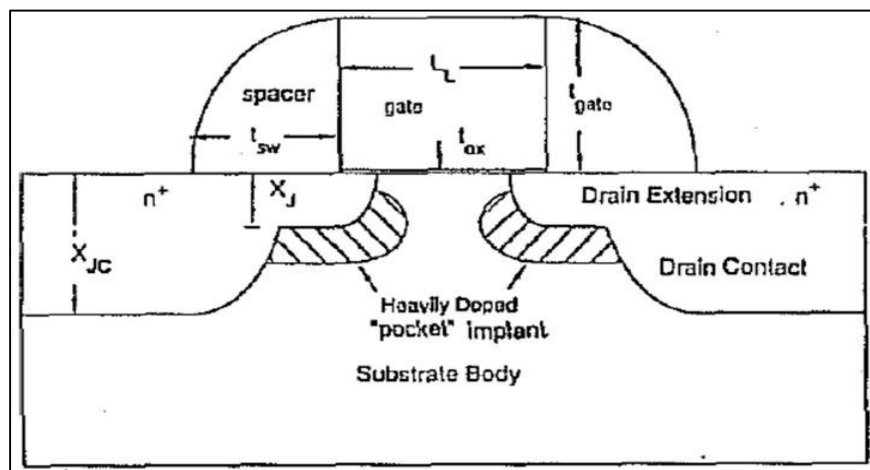
42. For example, varying the amount of dopants at different positions in the semiconductor device can have significant impacts on the device's performance. Where a source/drain may be heavily doped, other areas may only be lightly doped. As one example, the prior art has recognized that as transistors continue to scale down in size, using source and drain extensions may provide certain benefits, and these extensions can have varying dopant levels, including what are commonly referred to as lightly doped drain (LDD) and highly doped drain (HDD). Plummer, Ex.1215,, 77; Rodder, Ex.1323, 2:61-62, 3:65-67.

43. Source/drain extensions were known to assist in suppressing short channel effects of scaled-down transistors by varying the dopants and having a gradual transition in the electrical field between the source, the source extension, the channel,

the drain extension, and the drain. Plummer, Ex.1215,, 77-78 (using a LDD “allows the drain voltage to be dropped over larger distance than would be the case if an abrupt N<sup>+</sup>P junction were formed” and even “modest reductions in the field strength obtained through the LDD structure can make a significant difference in device reliability”).

44. As I discuss further below, sidewall structures placed on the edge of gate electrodes can serve many purposes, including to control the shape and position of source/drain extensions after annealing of the implanted dopants, as well as the overlap of the extension regions and the gate/gate insulating film. *See* Plummer, Ex.1215,, 78.

45. As another example of varying dopants, the prior art also taught using pocket or halo implants to further mitigate the short channel effect as transistor sizes decreased. Pocket implants are placed below the channel region, as shown below. Wolf-4, Ex.1214, 219-20, Fig. 5-27 (below).



**Wolf Vol. 4, Ex.1214, Fig. 5-27**

46. In this example, the pocket implants are doped opposite of the source/drain and source/drain extension. Wolf-4, Ex.1214, 219 (“Precise control of the placement and dose of this implant within the transistor-structure is needed to obtain the intended enhancements.”).

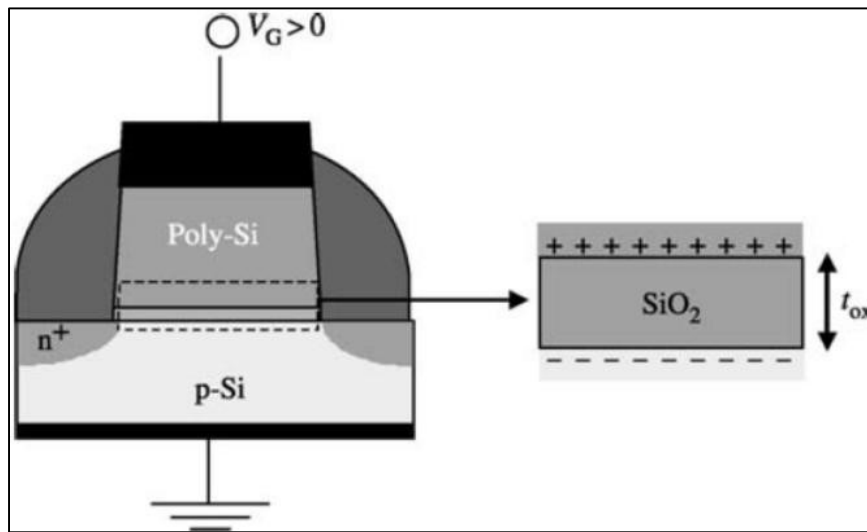
### **B. Gate Insulating Films & High-k Materials**

47. The gate insulating film or gate dielectric isolates the gate electrode from the channel. Plummer, Ex.1215,, 288. Silicon dioxide was primarily used as the gate dielectric material for many years (*id.*, 53), but silicon dioxide films presented problems when reduced in thickness for smaller and smaller transistors. In particular, “in ultrathin SiO<sub>2</sub> gate layers (thickness typically below 3 nm) charge carriers can flow through the gate dielectric by quantum mechanical tunnelling mechanism.” Houssa, Ex.1213, 5; *see also* Wolf-4, Ex.1214, 4-5.

48. The MOS transistor, from an electrical perspective, “behaves like parallel plate capacitor when gate voltage  $V_G$  is applied to the gate charges on the metal are compensated by opposite charges in the semiconductor, these latter charges forming the channel connecting the source and the drain of the transistor as illustrated in figure 1.1.4.” Houssa, Ex.1213, 8, Fig. 1.1.4 (below). The capacitance  $C$  can thus be represented by the following equation:

$$C = \frac{A \epsilon_r \epsilon_0}{t_{ox}} \quad (1.1.1)$$

49. In this equation, “ $A$  is the capacitor area,  $\epsilon_r$  the relative dielectric constant of the material (3.9 for  $\text{SiO}_2$ ),  $\epsilon_0$  the permittivity of free space ( $8.85 \times 10^{12} \text{ F m}^{-1}$ ) and  $t_{ox}$  the gate oxide thickness.” Houssa, Ex.1213, 8. From this formula, the gate oxide thickness has an inverse relationship to capacitance: decreasing the gate oxide thickness increases the capacitance of the structure, with a corresponding “increase in the number of charges in the channel for a fixed value of  $V_G$ .” *Id.*



Houssa, Ex.1213, Fig. 1.1.4

50. In practical uses, however, problems occur when decreasing the gate oxide thickness of silicon dioxide past a certain point. Houssa, Ex.1213, 8. As one prior art textbook proposed, “[a]n alternative way of increasing the capacitance is to use an insulator with a higher relative dielectric constant than  $\text{SiO}_2$  (it should be noticed that the relative dielectric constant is also represented by the letter  $k$  and one speaks about high- $k$  materials).” *Id.*, 8-9. “One could then use a thicker gate layer and, hopefully,

reduce the leakage current flowing through the structure and also improve the reliability of the gate dielectric.” *Id.*

51. Equivalent oxide thickness (EOT) is one measure of high-k gate dielectrics. The EOT of a high-k material “is defined as the thickness of the SiO<sub>2</sub> layer that would be required to achieve the same capacitance density as the high-k material in consideration” (Ex.1213, 9), which can be represented by the following equation:

$$\frac{t_{eq}}{\epsilon_{r,SiO_2}} = \frac{t_{high-\kappa}}{\epsilon_{r,high-\kappa}} \quad (1.1.2)$$

52. In this equation, “ $t_{high-k}$  and  $\epsilon_{r,high-k}$  are the thickness and relative dielectric constant of the high-k material, respectively.” *Id.* In one example shown by Houssa, “using ZrO<sub>2</sub> as gate dielectric ( $\epsilon_r \approx 20$ ) would allow us to use a 5.1 nm thick layer in order to achieve a capacitance equivalent to a 1 nm thick SiO<sub>2</sub> layer; the equivalent oxide thickness of this ZrO<sub>2</sub> layer is thus 1 nm.” *Id.*

53. But make no mistake, more than just a hope, the use of high-k gate dielectrics were a well-known, well-understood, and well-documented component to improve transistor performance as a substitute for silicon dioxide gate dielectrics, especially as transistors continued to decrease in size in the early 2000s. Long before 2005, numerous industry publications and other prior art readily recognized the advantages of using high-k materials as a gate dielectric.

54. In 2002, for example, numerous industry papers identified high-k materials, and hafnium oxide HfO<sub>2</sub> in particular, as a significant contributor to increased transistor performance. A paper by Rim et al. titled “Mobility Enhancement in Strained Si NMOSFETs with HfO<sub>2</sub> Gate Dielectrics” recognized that POSITAs had already been looking to high-k materials to solve known problems: “[g]ate leakage reduction in ultra thin gate dielectric is the main motivation for the search of high-k materials.” Rim-2002, Ex.1109, at Introduction; *see also id.*, Conclusion (“Strained Si NFETs with high-K dielectrics exhibit significantly enhanced NFET mobility, even over the universal mobility of the SiO<sub>2</sub>/bulk Si devices, and hold the promise for the best trade-off between mobility and gate leakage reduction, which is especially attractive for low power, high performance CMOS technology.”). Another article at the same industry conference concluded that “[h]igh-temperature FG annealing improved channel carrier mobility as well as subthreshold slopes in both N and PMOSFET with HfO<sub>2</sub> gate dielectrics,” which are “advantageous in achieving large on current while suppressing off current, and give more flexibility in V<sub>t</sub> adjustment.” Onishi-2002, Ex.1107, Conclusion.

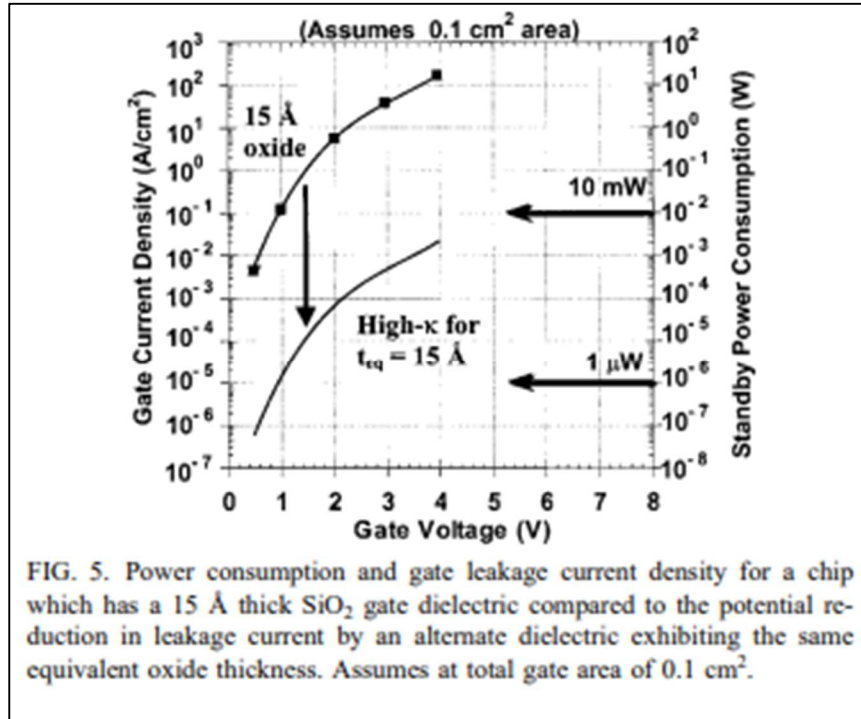
55. Yet another article at the same conference by Pidin et al., titled “Low Standby Power CMOS with HfO<sub>2</sub> Gate Oxide for 100-nm Generation,” concluded that HfO<sub>2</sub> was particularly suited for low standby current applications. Pidin-2002, Ex.1108, Conclusion (“55-nm CMOS with 3-nm HfO<sub>2</sub> gate dielectric was fabricated using conventional process flow with high-temperature anneal of  $\geq 1000^{\circ}\text{C}$  and cobalt

silicide. Gate current reduction of more than 3 orders of magnitude was achieved and low off-state current devices were obtained demonstrating very promising characteristics of HfO<sub>2</sub> for low standby current applications.”).

56. But more than just the structure and use of high-k materials, the industry had already begun optimizing the process for making transistors with high-k gate dielectrics, with one article from the 2002 VLSI Symposium comparing two gate first approaches using HfO<sub>2</sub>, one via physical vapor deposition and another via chemical vapor deposition. *See* Lee-2002, Ex.1105, Conclusion (“Compared with PVD TaN devices, the CVD TaN/HfO<sub>2</sub> devices exhibit lower leakage current and CV hysteresis, superior interface properties, higher transconductance, and superior effective electron and hole mobility.”).

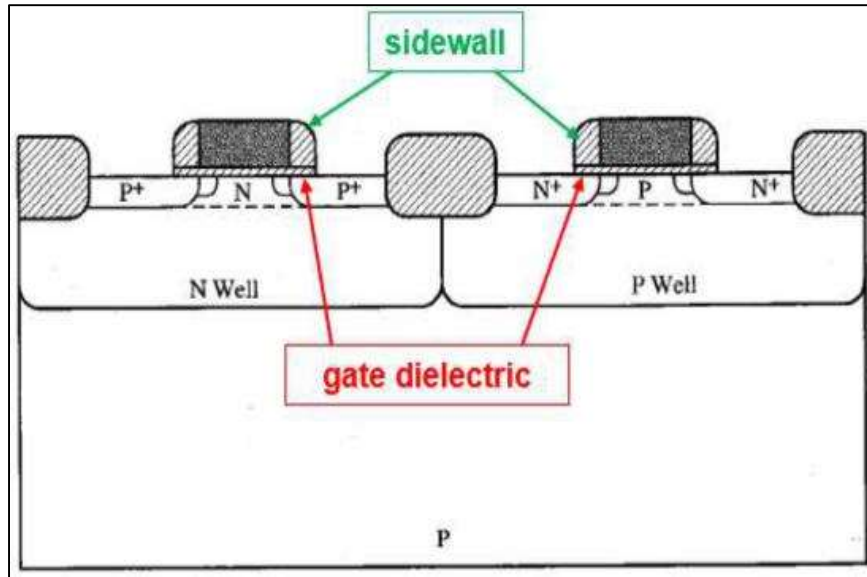
57. Numerous other prior art references recognized the ability of high-k gate dielectrics to make up for the shortcomings of too-thin silicon dioxide gate dielectrics. One article in the Journal of Applied Physics titled “High-k Gate Dielectrics: Current Status and Materials Properties Considerations” recognized that already by 2001 “much work has been done on high-k metal oxides as a means to provide a substantially thicker (physical thickness) dielectric for reduced leakage and improved gate capacitance.” Wilk, Ex.1318, 5250; *see also* Wolf-4, Ex.1214, 146-47 (“The use of high-k dielectrics as the gate dielectric in submicron MOSFET structures also improves other device characteristics,” including in threshold voltage V<sub>t</sub> and in the subthreshold-swing S<sub>t</sub>.”).

58. For example, as shown by Figure 5 below in Wilk, using high-k materials in place of silicon dioxide for the gate dielectric improved both power consumption and gate leakage current.



Wilk, Ex.1318, Fig. 5.

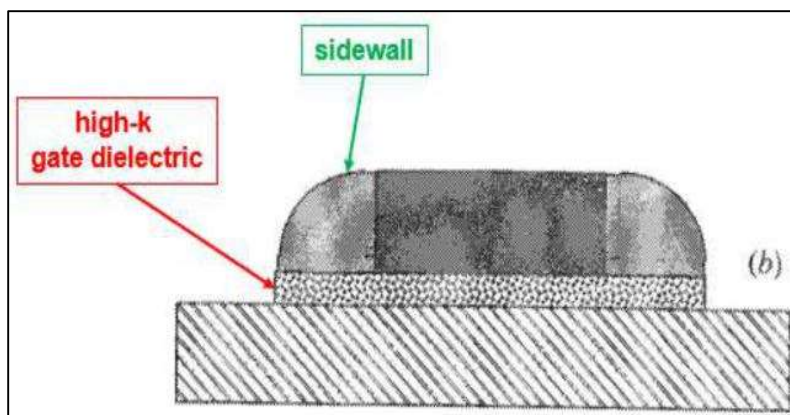
59. Not only did the prior art recognize the use of high-k materials as a substitute for silicon dioxide gate dielectrics, but the prior art also showed it was common to extend the gate dielectric out from underneath the gate electrode to underneath the sidewalls. For example, in Figure 2-34 below in Plummer, the gate dielectric is wider than the gate electrode.



**Plummer, Ex.1215, Fig. 2-34**

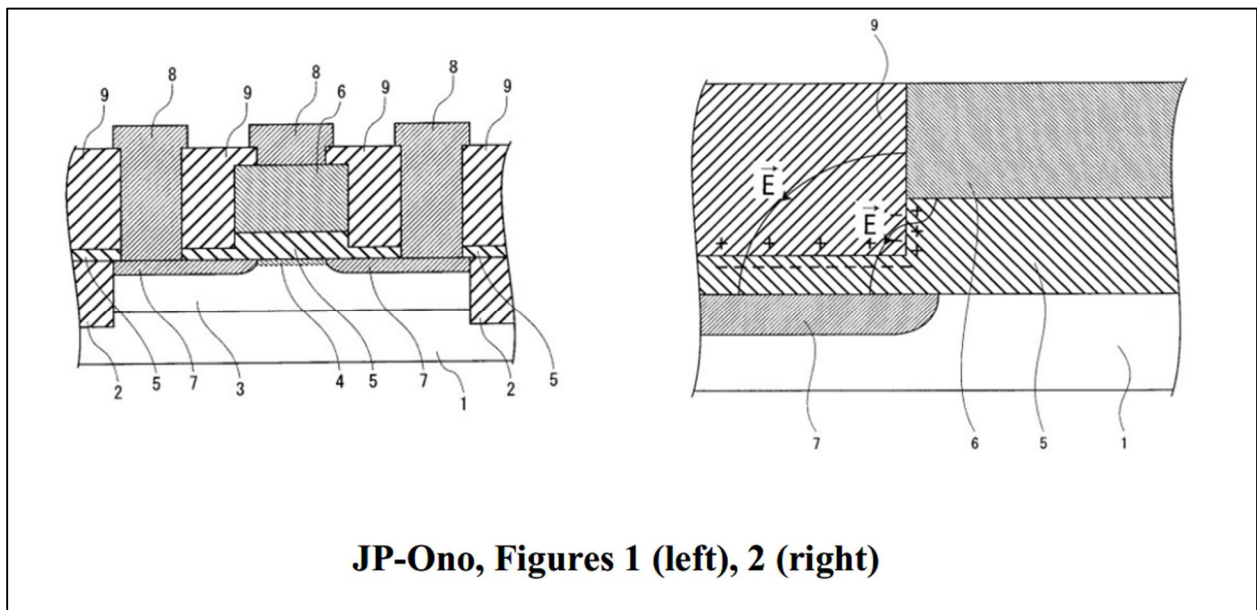
Plummer, Ex.1215,, Fig. 2-34.

60. As another textbook example, Houssa shows using  $\text{HfO}_2$  as the high-k gate dielectric, with and without extending the gate dielectric underneath the sidewalls. Houssa explains that by extending the gate dielectric “with the approach of figure 5.1.9(b), the etch requirements are relaxed but they will require LDD implants through the high-k layer.” Houssa, Ex.1213, 510, Fig. 5.1.9(b).

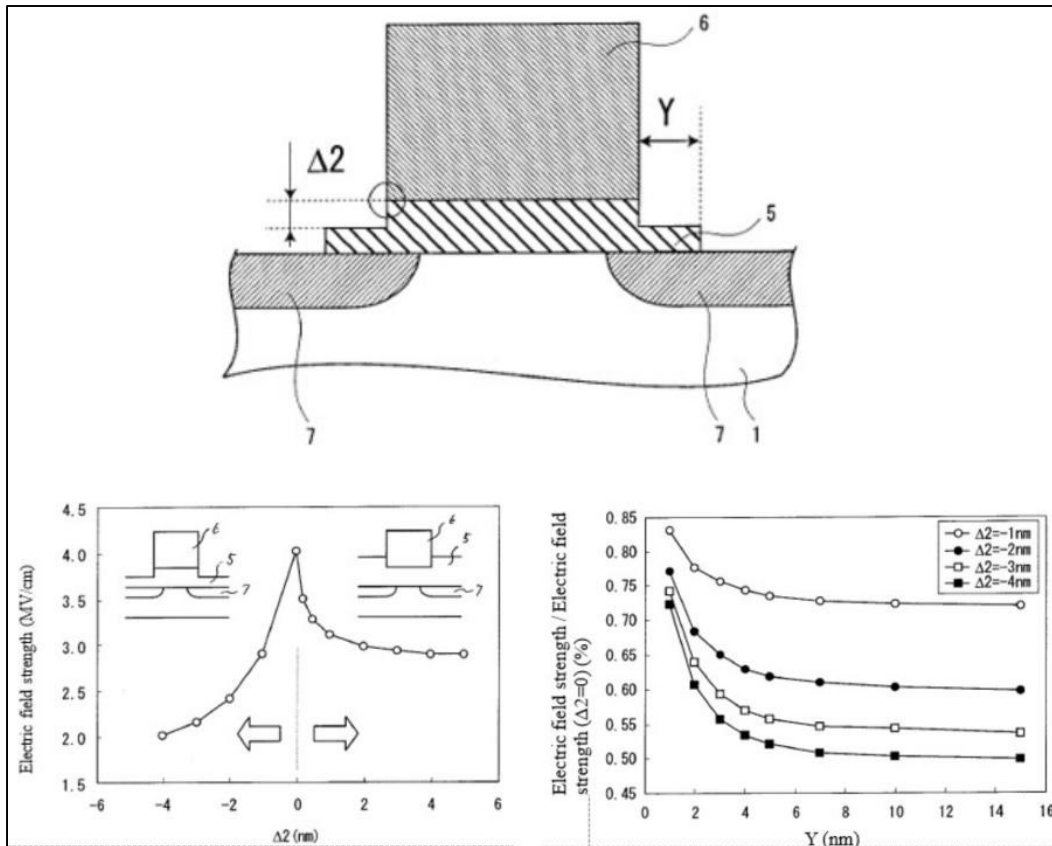


**Houssa, Ex.1213, Fig. 5.1.9(b)**

61. Japanese Publication No. 2005/064190 by Ono, et al. (“JP-Ono”) published on March 11, 2005 and described some of the known benefits of expanding the high-k gate dielectric wider than the gate electrode, including that “protruding the gate insulating film outside the gate electrode during processing results in higher values of the electric field.” JP-Ono, Ex.1340, ¶7. Further, JP-Ono suggests that extending the gate dielectric over the source/drain region, as well as reducing the thickness of the gate dielectric over the source/drain regions compared with under the gate electrode, “mitigate[s] the electric field at the lower end corner of the gate electrode 6” and “suppresses problems such as insulation breakdown and decreased reliability of the gate insulating film.” *Id.*, Abstract. Specifically, JP-Ono detailed how thinning the gate dielectric over the source/drain region minimizes the electric field at the edge of the gate. *Id.*, ¶¶29-32, Fig.1-2.

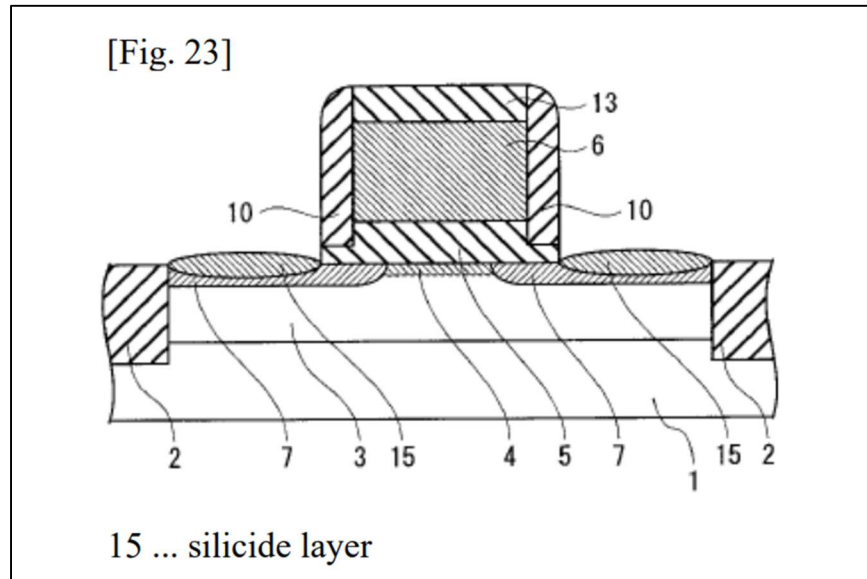


62. Further, JP-Ono studied how varying the thickness and length of the gate dielectric over the source/drain regions affects the electric field distribution. Figure 4 shows that when the gate dielectric over the source/drain region is the same thickness as under the gate, e.g. at  $0 \Delta 2$ , the electric field is strongest. JP-Ono, Ex.1340, ¶¶29-32, Fig.1-2. As the gate dielectric becomes thinner compared with under the gate electrode, e.g. when  $\Delta 2$  is negative, the electric field weakens more than with a thicker gate dielectric, which favors a thinner dielectric over the source/drain regions. *Id.*, ¶35. Figure 24 further shows that the electric field is further reduced as the gate dielectric protrudes farther from the corner of the gate, i.e., as  $Y$  increases. *Id.*, ¶87.



JP-Ono, Figs. 3 (top), 4 (bottom-left), 24 (bottom-right)

63. These improvements are explicitly taught in a FET having a gate sidewall made of “materials like silicon oxide, silicon nitride, or silicon oxynitride,” as shown Figure 23 below. JP-Ono, Ex.1340, ¶83.

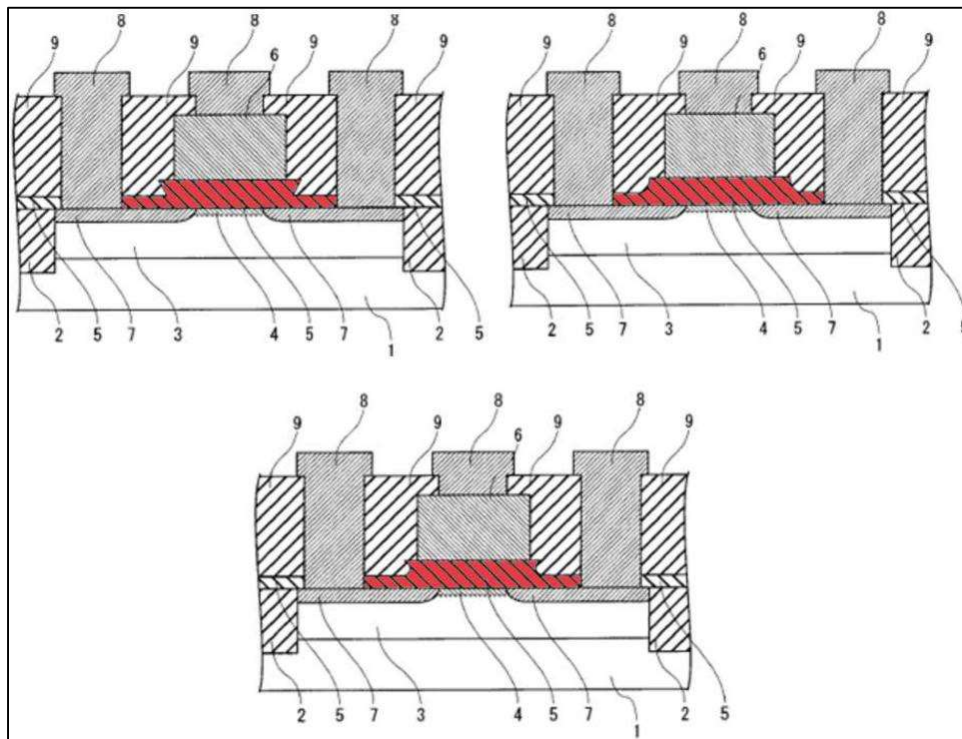


**JP-Ono, Ex.1340, Fig. 23**

64. Thus, JP-Ono teaches a POSITA the benefits of changing not only the location of the gate dielectric, e.g. outside the gate electrode, but also the shape of the gate dielectric, e.g. with thinner ends over the source/drain regions than underneath the gate electrode. In reference to Figure 23, JP-Ono explained that “it is not essential for the side of the gate insulating film 5 to be located inside or outside of the outer surface of the gate-side wall 10,” but instead, the gate dielectric can be located both farther than the end of the sidewall, or closer than the end of the sidewall, with similar benefits. JP-Ono, Ex.1340, ¶83 (“Therefore, it is preferable that the side of the gate insulating film

does not protrude too far outward [or inward] from the outer surface of the gate-side wall.”).

65. JP-Ono demonstrated several different shapes for the protruding portions of the gate dielectric in Figures 36-44, as can be seen by some examples below in red. JP-Ono, Ex.1340, Figs. 38, 41-42 (below). “By changing the shape of the gate insulating film near the lower corner of the gate electrode, as shown in the various examples here, it is possible to adjust the capacitance formed between the gate electrode 6 and the source-drain region 7, allowing for optimization.” *Id.*, ¶108. Although shown without any sidewalls, JP-Ono explained that “gate-side wall 10 may be removed after processing the gate insulating film, or it may be left as it is.” *Id.*, ¶103.



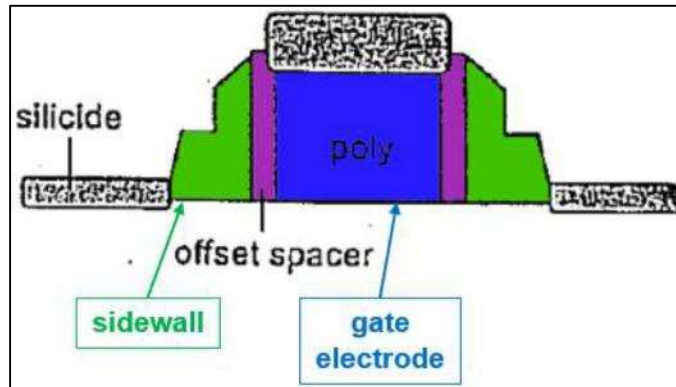
**JP-Ono, Ex.1340, Figs. 38 (top-left), 41 (top-right), 42 (bottom)**

### C. Sidewall Structures

66. Varying the sidewall structure on the sides of the gate electrode is another way a POSITA had to further optimize device performance in the prior art. Sidewalls, also referred to as spacers or sidewall spacers, are formed on the side of the gate electrode for a variety of reasons. As discussed above, various sidewall structures may be used on the gate electrode to control the shape and position of source/drain extensions after annealing of the implanted dopants, as well as the overlap of the extension regions and the gate/gate insulating film. *See* Houssa, Ex.1213, 511; Weste, Ex.1212, 122; Wolf-4, Ex.1214, 9, 217, 219; Plummer, Ex.1215,, 78. Alternatively, sidewall spacers can prevent shorts between the source/drain and the gate, for example if the source/drain regions have silicide portions. Plummer, Ex.1215,, 742. These spacers are often made with silicon dioxide or silicon nitride, or combinations of multiple oxide and nitride layers. Houssa, Ex.1213, 511-12.

67. Varying the sidewall structure to control the source/drain extensions is one example of device optimization. As one textbook noted, “it has also been reported that the amount of overlap of the SDE-region with the gate-edge is also critical for optimum device performance.” Wolf-4, Ex.1214, 217. As shown in Wolf’s Figure 5-25 below, a POSITA knew that varying the size of the spacer at the gate electrode would affect formation of the source/drain extension and the resulting overlap with the gate edge: “an offset-spacer is fabricated on the side of the gate after the gate-poly is etched (but

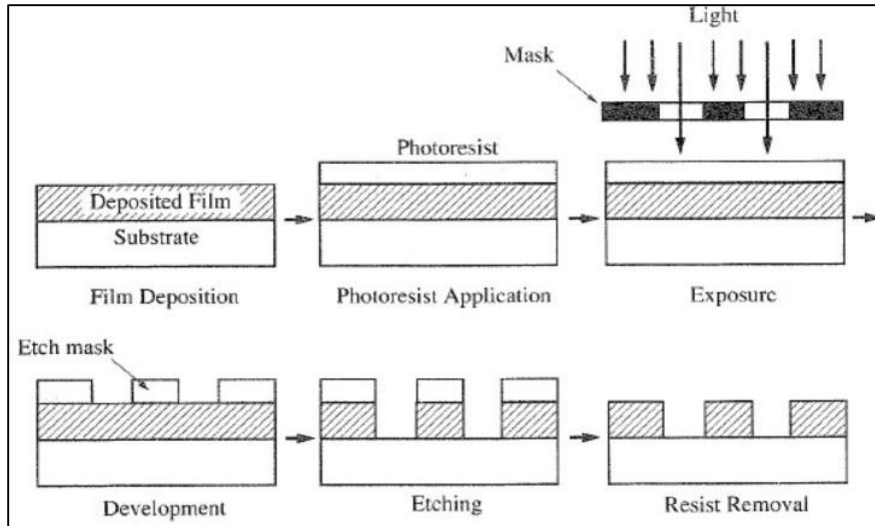
before the SDE implant step is carried out,” with the spacer width “varied from zero (no-spacer) to some upper-bound (e.g., 50-nm)” to control gate overlap and optimize device performance. *Id.*



**Wolf-4, Ex.1214, Fig. 5-25**

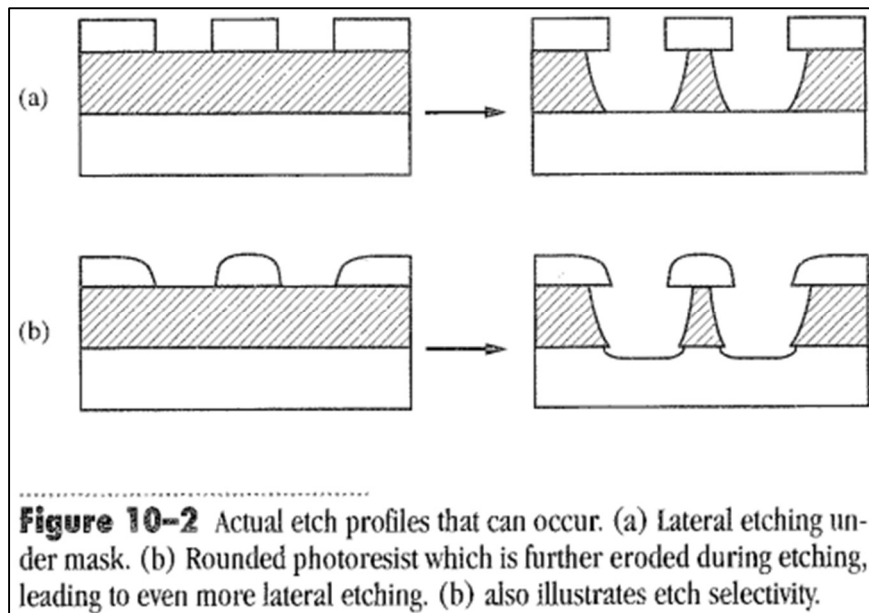
#### **D. Etching**

68. The process of manufacturing a semiconductor device, particularly one with varying transistor structures, often involves a series of material deposition and etching, including by deposition of thin films with selective etching to pattern a desired structure. Plummer, Ex.1215,, 609-11. For example, a mask may be used in selective portions of a semiconductor device to “mask” or protect the underlying structure from further processing. As seen below, some areas may be masked while other areas are left unprotected such that a subsequent etching step etches the unmasked areas, while leaving the masked areas relatively intact. *Id.*, 609-10; Fig. 10-1.



**Plummer, Ex.1215, Fig. 10-1**

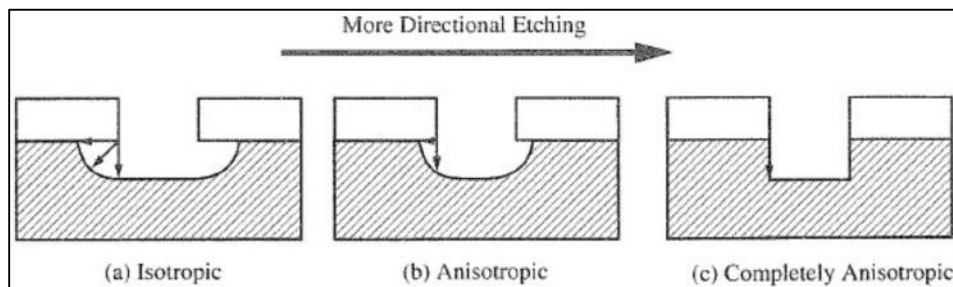
69. A POSITA can further optimize the structure of the semiconductor device by varying the etching process, as some processes are more selective than others. While the ideal etch profile “has perfectly straight sidewalls exactly under the edge of the mask,” as seen above in Figure 10-1, in practice etching has both lateral and vertical components, as seen below in Figure 10-2.



Plummer, Ex.1215,, Fig. 10-2.

70. Etching is accomplished through both wet and dry processes, where wet etching often entails immersing the wafers in liquid like hydrofluoric acid to perform chemical etching, while dry etching uses plasma instead to etch material through both a physical and chemical process. Plummer, Ex.1215,, 609, 612.

71. Under certain circumstance, etching can also be targeted to etch directionally. Anisotropic etching, for instance, is considered a vertical etch with little to no etching in the lateral direction, while isotropic etching has more equal etching rates both vertically and laterally. Plummer, Ex.1215, 610-13. These differences can be seen below in Figure 10-3.



**Plummer, Ex.1215, Fig. 10-3**

*Id.*, Fig. 10-3.

### **E. Replacement Metal Gate Stacks**

72. While the industry recognized the benefits of high-k gate dielectrics, the prior art also recognized that using metal gates on top of high-k gate dielectrics further enhanced transistor performance, particularly as transistor sizes became smaller. When

formed on top of high-k gate dielectrics like HfO<sub>2</sub>, metal gate stacks addressed issues like Fermi-level pinning, eliminated polysilicon gate depletion, provided lower resistance, enhanced switching speeds, and improved overall transistor performance.

73. For example, a 2002 article by Samavedam et al. titled “Metal Gate MOSFETs with HfO<sub>2</sub> Gate Dielectric” recognized “[m]etal gates will eliminate gate depletion and address other issues like boron penetration and increased gate resistance, which will be aggravated as the poly gate thickness is scaled down.”). Samavedam-2002, Ex.1110, Introduction; *see also id.*, Conclusion (“We have successfully fabricated and characterized HfO<sub>2</sub> n-MOSFETs with TaSiN and PVD TiN gates and p-MOSFETs with CVD and PVD TiN gates using a conventional CMOS process. Metal-gated HfO<sub>2</sub> n-MOSFETs show a 10<sup>4</sup>X gate leakage reduction compared to poly/SiO<sub>2</sub> devices. Reasonable Ion/Ioff performance and reliability were observed in PVD TiN/HfO<sub>2</sub> PMOS.”); *see also* Lee-2002, Ex.1105, Introduction (“As CMOS devices are scaled into sub-0.1 um regime, poly-depletion effects and boron penetration become significant concerns. Therefore, metal gate electrodes are being explored to replace the polysilicon gate.”). Just two years later, a 2004 article titled “55nm high mobility SiGe(:C) pMOSFETs with HfO<sub>2</sub> gate dielectric and TiN metal gate for advanced CMOS” concluded that “[f]or the first time, MOS transistors with compressively strained SiGe(:C) channel, metal gate and high-k dielectric are demonstrated down to 55nm gate length,” with significant improvements: “SiGe(:C) surface channel

pMOSFETs with HfO<sub>2</sub> gate dielectric exhibit a 10<sup>4</sup> gate leakage reduction and a 65% mobility enhancement at high transverse effective field (1MV/cm) when compared to the universal SiO<sub>2</sub>/Si reference.” Weber-2004, Ex.1111.

74. Other prior art references further recognized the problem of using polysilicon gates with high-k gate dielectrics specifically, or decreased transistor size in general. As gate dielectrics grew smaller consistent with transistor sizes, the polysilicon depletion effect worsened. Saito631, Ex.1518, 1:31-34; Hou, Ex.1519, 1:36-44. And where a high-k material is substituted for the silicon dioxide gate dielectric with a polysilicon gate electrode, diffusion of the polysilicon dopants into the high-k material can cause a large threshold voltage offset. Colombo, Ex.1520, ¶5; Kavalieros277, Ex.1515, ¶3. As discussed above, metal gate stacks were considered the next step to address these problems. Saito631, Ex.1518, 1:31-34; Iriyama, Ex.1521, 1:28-34, 1:41-42; ITRS\_FEP, Ex.1512, 2-3, 20; ITRS\_PIDS, Ex.1216, 1, 3, 27, Fig. PIDS5.

75. In particular, the prior art recognized that metal gates for PMOS and NMOS transistors would need separate metal gate stacks, and replacement metal gates (or gate-last processes) were well known to provide significant benefits compared with gate-first approaches. A material’s “work function” is “the minimum energy required to bring an electron from the Fermi level to the vacuum level.” Wolf-3, Ex.1229, 117. However, in MOS/MIS structures, the metal is in direct contact with a dielectric, not

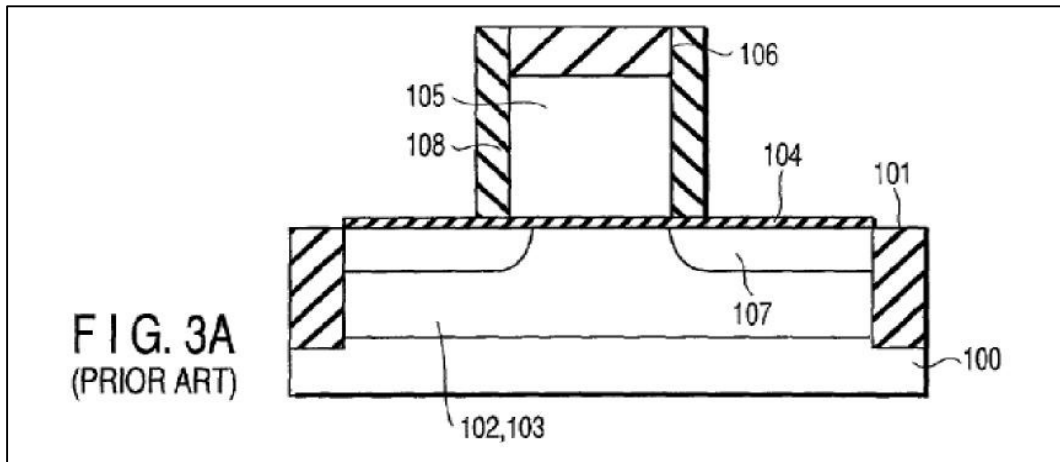
with the vacuum. Moreover, work functions of metal gates are highly dependent on material properties and interfaces. To differentiate this, an “effective work function” of the metal gate is commonly used to refer to the metal work function as measured (e.g., through the threshold voltage of the device).

76. In a CMOS device, PMOS transistors require a work function greater than about 4.8 eV, while NMOS transistors require a work function of less than about 4.6 eV. Hou, Ex.1519, 1:17-22; Colombo, Ex.1520, ¶¶20-21; ITRS\_FEP, Ex.1512, Tbl. FEP4a ( $|E_{c,v}-\phi_m|$  (eV) < 0.2). Where the same polysilicon gate electrode can be doped to adjust the work function for both NMOS and PMOS transistors, this is not the case for metal gates. Different metal gate stacks must be used. *See* Kavalieros<sup>277</sup>, Ex.1515, ¶3 (“When making a CMOS device that includes metal gate electrodes, it may be necessary to make the NMOS and PMOS gate electrodes from different materials.”).

77. Some of the metals considered in the prior art for the PMOS metal gate stack showed less thermal stability than necessary, adversely affecting device performance when subjecting the metal to the high temperatures used to anneal the dopants in the source/drain regions. Hou, Ex.1519, 1:45-57; Iriyama, Ex.1521, 1:41-48.

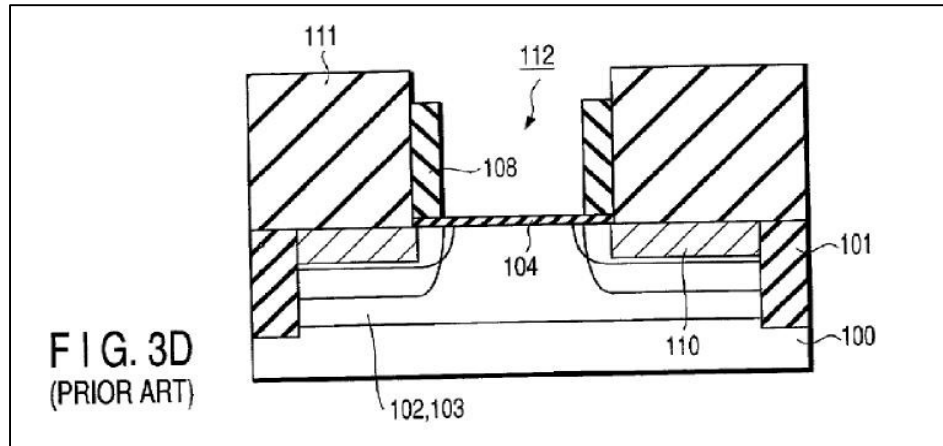
78. One solution already considered by the prior art was replacement metal gates (“RMG”), which is a “gate-last” approach because a dummy gate is often manufactured first and then replaced by the metal gate. By making the metal gate last, the POSITA avoids subjecting the metal gate stacks to high temperatures during the

source/drain annealing (because the annealing is done before placement of the metal gate). As seen below from one prior art reference, source/drain regions (107), the polysilicon dummy gate (105), a SiN film (106), and sidewalls (108) are formed for the NMOS and PMOS transistors before the replacement metal gate. Matsuo, Ex.1522, ¶¶9-10, 16, FIG. 3A.



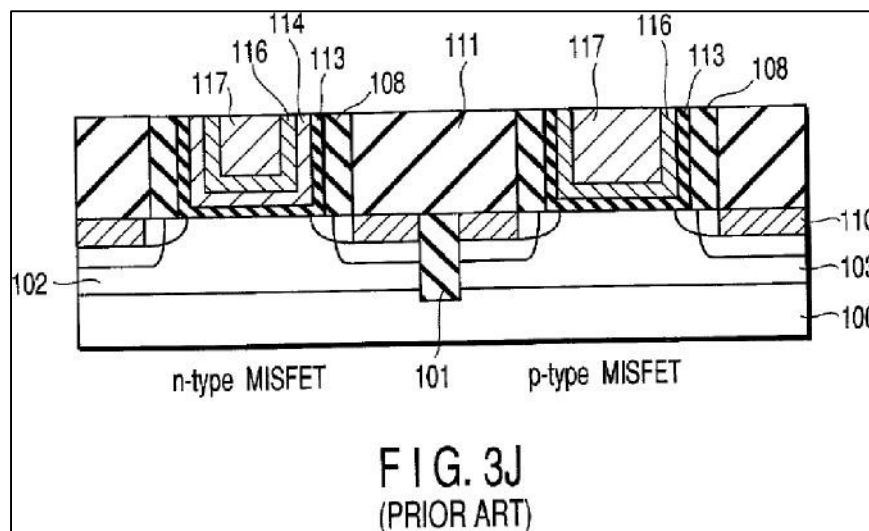
**Matsuo, Ex.1522, FIG. 3A**

79. Before the dummy gate is replaced, the source/drain regions are doped and annealed. *See* Matsuo, Ex.1522, ¶10, FIGS. 3B-C; *see also* Hou, Ex.1519, 2:8-11; Iriyama, Ex.1521, 1:59-2:6. As one of the last steps, the dummy gates are removed to allow for placement of the metal gate stack. Matsuo, Ex.1522, ¶¶11-13, FIG. 3D.



**Matsuo, Ex.1522, FIG. 3D**

80. In this example, after removal of the dummy gate, both the NMOS and PMOS metal gate electrodes are formed, as seen below. Matsuo, Ex.1522, ¶¶12-16, FIG. 3J. First, gate dielectric (113) is formed, and then metal layers 114, 116, and 117 after. *Id.*, ¶¶12-16. This sequence can prevent damage to metal gate stacks susceptible to deterioration by high temperature annealing. Iriyama, Ex.1521, 2:22-29.



**Matsuo, Ex.1522, FIG. 3J**

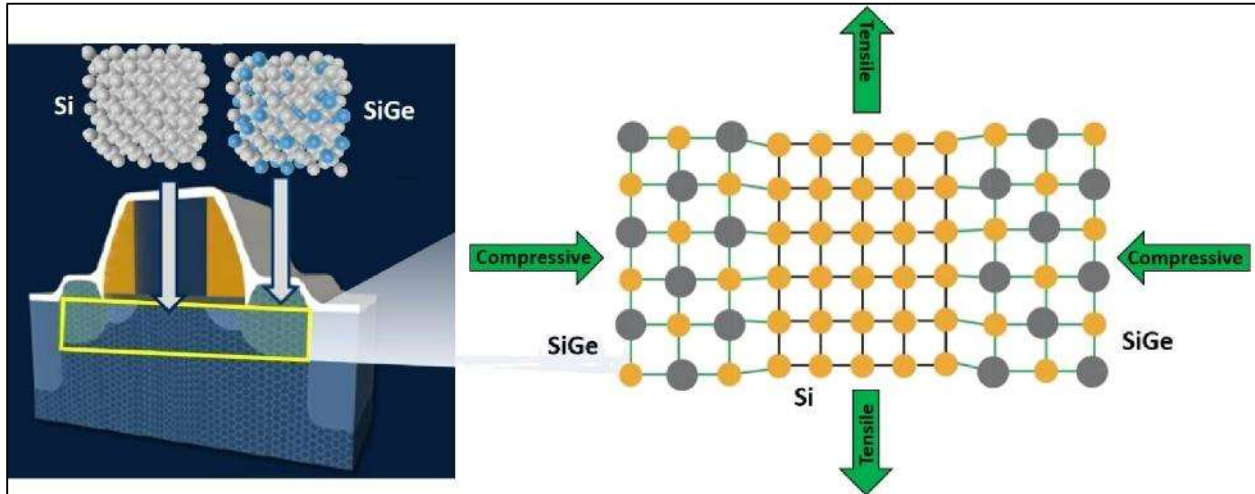
81. In Fig. 3J above, the metal layer 114 is directly formed on the gate dielectric 113 for NMOS gate electrode (shown on the left), but a different metal gate stack is used for the PMOS gate electrode (shown on the right), which does not include metal layer 114. Matsuo, Ex.1522, ¶21. The two gate electrodes thus have different metal work functions, one for NMOS and one for PMOS. *Id.*, ¶21, FIG. 3J; Hou, Ex.1519, 2:11-14; Iriyama, Ex.1521, 2:10-12; Mistry2007, Ex.1516, 247; Mistry\_Presentation, Ex.1517, 16, 18.

#### **F. Strained Silicon**

82. In the early 2000s, strained silicon technology was recognized as another mechanism to improve transistor performance as transistor sizes continued to shrink. Until the large-scale adoption of strained silicon, PMOS transistors used to be slower than NMOS transistors and much effort was spent on improving PMOS transistor performance compared with NMOS transistors. But the prior art quickly realized that compressively strained PMOS transistors could be improved by as much as 50%, leading to a reversal in efforts spent trying to improve NMOS transistors compared with PMOS transistors.

83. Germanium is one source of compressive stress in PMOS transistors. The Ge atoms are larger in size than Si atoms, such that silicon-germanium (“SiGe”) can be used in the source/drain regions of PMOS transistors to apply compressive stress to the PMOS channel region. *See* Thompson2004, Ex.1523, 1790-96; Sun-2007, Ex.1524, 2.

By 2005, SiGe source/drain regions increased PMOS “hole mobility by as much as 50%” (James, Ex.1525, 2), doubling PMOS operating speeds.



84. Numerous prior art references recognized the benefits of strained silicon, for both PMOS and NMOS transistors. For example, in a 2004 paper titled “35% Drive Current Improvement from Recessed-SiGe Drain Extensions on 37 nm Gate Length PMOS,” Chidambaram et al. recognized that “Epitaxial SiGe, grown in recessed Si, has been used to compressively strain the PMOS channel and increase the hole mobility.” Chidambaram-2004, Ex.1104, Introduction; *see id.*, Abstract (“A highly compressive SiGe layer, in close proximity to the channel, results in large hole mobility improvements.”). Another 2004 article by Mistry et al. proclaimed that “[t]he use of strain to improve mobility has been known for 50 years,” concluding that “[u]ni-axial strained silicon has been implemented in a high volume manufacturing 90nm logic technology for the first time, with impressive performance results and improved power scaling.” Mistry-2004, Ex.1106.

85. Where a PMOS transistor benefits from compressive strain, NMOS transistors benefit from tensile stress along the channel region. As seen in Figs. 2-4 from Mistry-2004, compressive stress from SiGe source/drain regions on PMOS transistors and tensile stress on NMOS transistors from a high tensile stress nitride overlayer were well known to improve transistor performance.

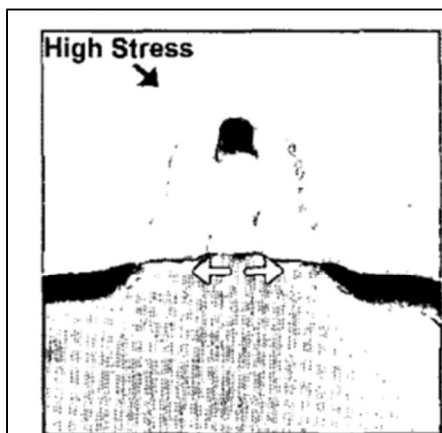
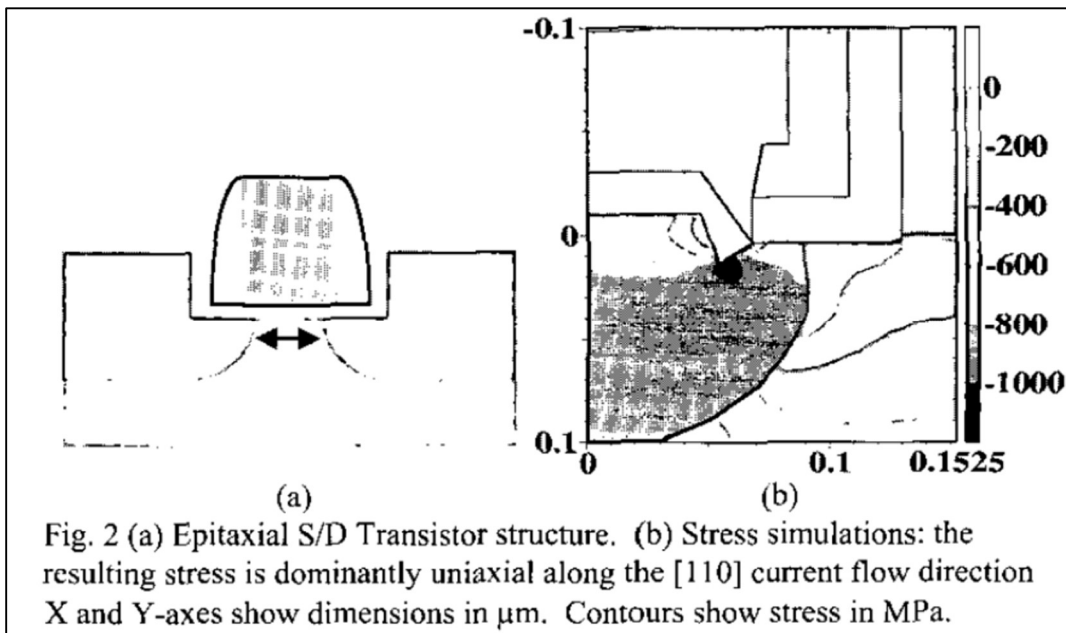


Fig. 3 TEM of NMOS transistor showing high tensile stress nitride overlayer.

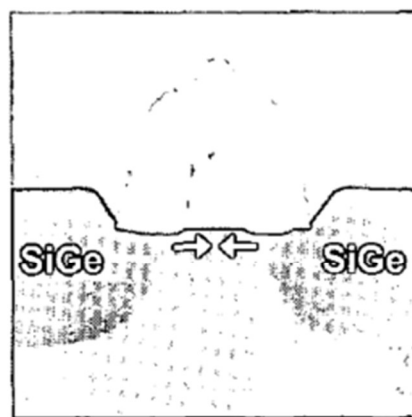


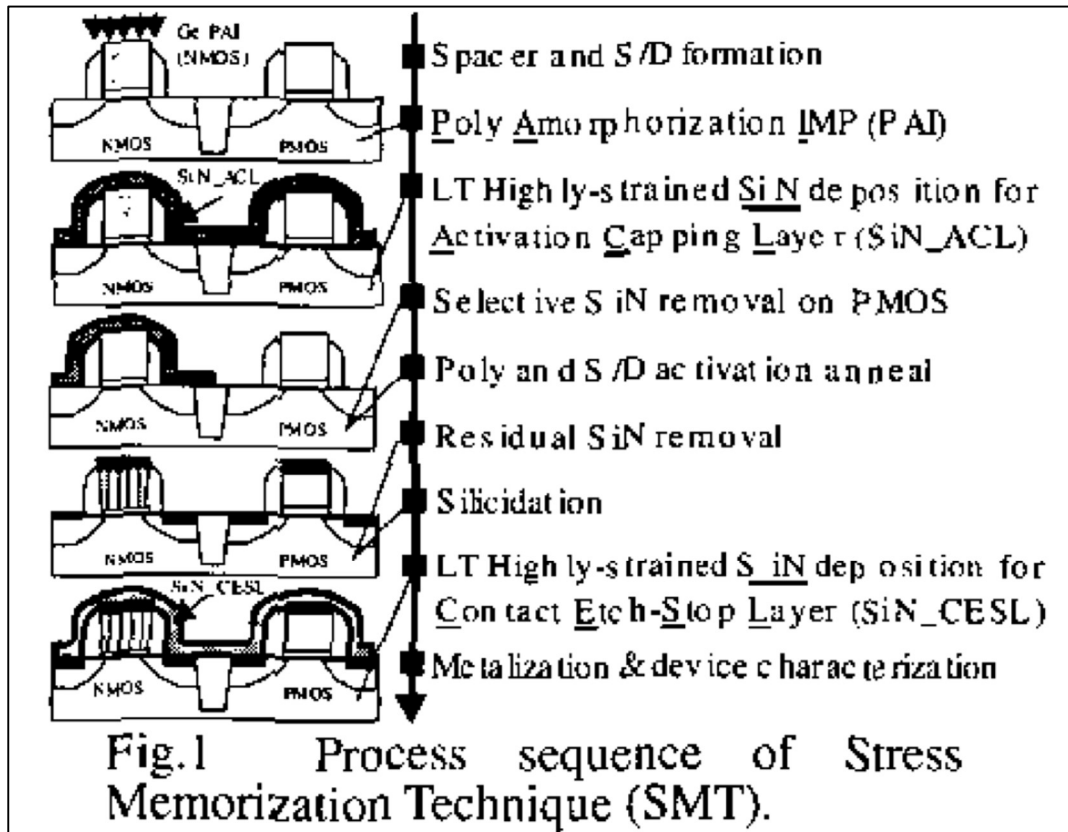
Fig. 4 TEM of PMOS showing SiGe heteroepitaxial S/D inducing uniaxial strain.

Mistry-2004, Ex.1106, FIGS. 2-4.

86. In another article that same year by Chen et al. titled “Stress Memorization Technique (SMT) by Selectively Strained-Nitride Capping for Sub-65nm High-Performance Strained-Si Device Application,” the prior art recognized that “[c]hannel stress control has become a critical technique for electron and hole mobility improvements as down scaling the device dimension.” Chen-2004, Ex.1103, Introduction. The article further recognized the tradeoffs inherent in stressing both PMOS and NMOS transistors on the same chip. *Id.* (“In addition, recent studies of high tensile capping layer on top of the silicide have demonstrated the NMOSFET driving current improvement capability, but with the PMOS performance degradation.”).

87. Searching for a cost-conscious method to effectively stress the NMOS transistor without degrading PMOS performance, the article proposed (1) selectively applying a high tensile nitride activation capping layer to the NMOS transistor, and (2) applying a low temperature, high-tensile nitride film as a contact etch stop layer to both the NMOS and PMOS transistors. Chen-2004, Ex.1103, Channel Stress Control by SMT; *see id.*, Introduction (“In this paper, we proposed a novel stress memorized technique (SMT) to improve the device performance without PMOS degradation. A high tensile nitride capping layer acts as a temporary stressor to effectively modulate the channel stress. The stress effect is then enhanced and memorized by well-controlled poly amorphization and re-crystallization procedures. This high tensile nitride capping layer will be removed after the annealing step. Therefore, a much thicker

capping layer can be used to increase the stress level without any process limitation to impact the subsequent gap filling process steps.”); *id.*, Channel Stress Control by SMT (“After the silicide formation, the low temperature, high-tensile Nitride film is deposited as Contact-Etch-Stop-Layer (SiN-CESL) to add up the stress effect.”).



Chen-2004, Ex.1103, Fig. 1.

88. Additional prior art references taught straining both PMOS and NMOS transistors. See Murthy151, Ex.1526, ¶¶5, 48, 72; James, Ex.1525, 2. For example, it was known to create tensile strain with epitaxial source/drain regions, similar to SiGe for PMOS transistors, but it requires using an atom smaller than silicon, like carbon, to

grow a material like silicon carbide (SiC) instead of SiGe,. *See* Murthy151, Ex.1526, ¶¶5, 48, 72; James, Ex.1525, 2; Bohr, Ex.1527, ¶45.

89. As either an alternative or a supplement to source/drain epitaxy, the semiconductor industry was also already depositing compressive and tensile stress-inducing films over PMOS and NMOS devices to induce a desired strain, as shown above. *See also* James, Ex.1525, 2, 4; Morin-2007, Ex.1528, 355-56, 367; Hsu823, Ex.1506, ¶3; Jung, Ex.1529, Abstract, ¶90 (“In addition to being deposited as part of a structure to control electron mobility, as shown in FIG. 1B, a stress-tuned silicon nitride film can be deposited for other purposes . . . , for example . . . , to provide an etch stop layer . . .”). A contact etch stop layer (“CESL”) made of silicon nitride was frequently used, and if prepared under certain conditions, a silicon nitride CESL may apply stress to the channel and increase device performance. Hsu823, Ex.1506, ¶3; *see also* Ex.1531, Ke, ¶3 (“A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device.”); Jung, Ex.1529, ¶90 (“In addition to being deposited as part of a structure to control electron mobility, as shown in FIG. 1B, a stress-tuned silicon nitride film can be deposited for other purposes in various steps in the fabrication process, for example (and not by way of limitation), to provide an etch stop layer . . . , as well as to enhance channel mobility in various portions of the device structure.”); Morin-2007, Ex.1528, 355-56. It was well known that a silicon nitride CESL may provide tensile stress, compressive stress, or no

stress at all, depending on the process used to apply the layer. *See, e.g.,* Jung, Ex.1529, ¶¶17, 99-100, 131-32, Tbls. IV-V, VII, Fig. 15.

90. As evidenced by the prior art, strained silicon has been well known long before the priority date of the challenged patents. *See, e.g.,* Sun-2007, Ex.1524, 1 (“Strain is a relatively old topic in semiconductor physics.”). In fact, strained silicon was already commercially used in at least three generations of devices by 2007. *See* Thompson2004, Ex.1523, 1790-91 (Intel’s 90nm devices); Bai-2004, Ex.1532, 657-58 (Intel’s 65nm devices); Mistry2007, Ex.1516, 247-48 (Intel’s 45nm devices); Mistry\_Presentation, Ex.1517, 1-19 (same).

#### **G. Stress Buffering Layers**

91. Not only were tensile stress contact etch stop layers and SiGe source/drains well known in the prior art, but using buffer layers to mitigate the unwanted effects of those stress layers were also well understood concepts in the prior art.

92. If a tensile contact etch stop layer is deposited over a PMOS device, it generally applies a tensile stress to the channel region. Morin-2007, Ex.1528, 355-56, 367; Doris, Ex.1429, ¶¶ 5, 13; Hsu823, Ex.1506, ¶37. Where the PMOS device is already compressively stressed, for example with epitaxial SiGe source/drain regions, the tensile stress from the contact etch stop layer offsets some portion of the compressive stress, reducing improvements from the SiGe. Morin-2007, Ex.1528, 355-

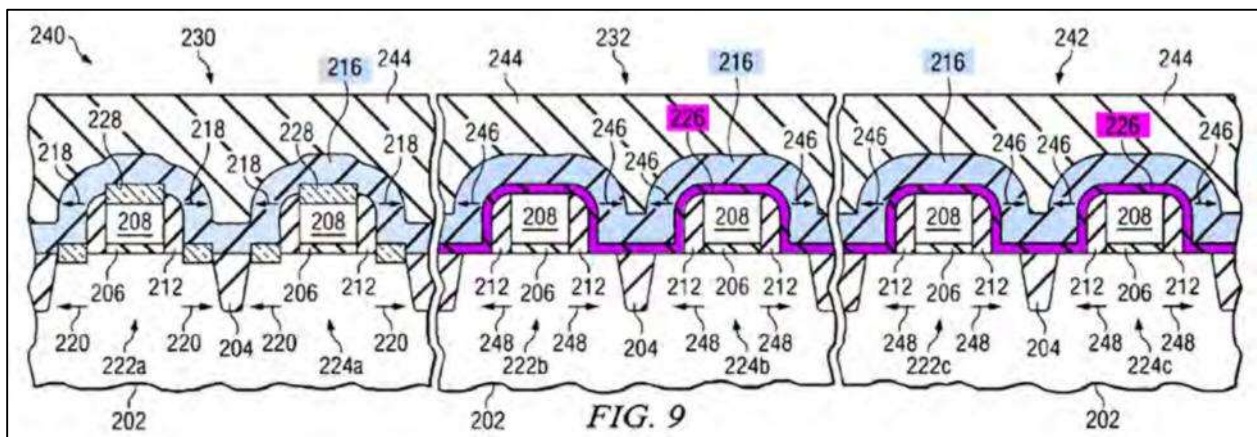
56, 367; Kavalieros729, Ex.1419, ¶¶2, 26; Doris, Ex.1429, ¶5. The tensile stress may even degrade performance, particularly in PMOS devices without SiGe source/drains. Morin-2007, Ex.1528, 355-56, 367.

93. A POSITA would have understood how to mitigate or negate performance decreases on the PMOS devices from tensile stress. First, a POSITA may choose to apply both a SiGe source/drain to a PMOS device as well as a tensile contact etch stop layer over both the NMOS and PMOS devices to optimize performance of both devices. If the compressive stress from the SiGe is greater than the tensile stress from the contact etch stop layer, the overall compressive stress may still increase PMOS performance, though it may be lessened by the contact etch stop layer. The tradeoff is that the tensile stress improves NMOS transistor performance.

94. A POSITA knew of other ways to mitigate the performance loss. For example, the tensile stress could be reduced for the PMOS device by using a stress-relief layer as a buffer between the SiGe and the tensile contact etch stop layer. Murthy556, Ex.1430, 9:27-29, FIGS. 2, 9, 13-15; Doris, Ex.1429, ¶42, Figs. 1-2, 14-15; Alvarez, Ex.1406, Abstract, ¶43, FIG. 9; Lee870, Ex.1431, ¶29, ¶¶46-67 (pFET performance degradation “is reduced/eliminated due to the inclusion of the stress relief layer 64 under the nitride layer 70 that reduces the tensile stress in the channel region”), FIGS. 2-5; Cheng810, Ex.1432, ¶¶22-31, Figs. 1B-1F (describing similar); Baik, Ex.1433, ¶37 (“the tensile stresses of the [stressor layer] ha[ve] relatively little or no

adverse impact [on] the adjacent PMOS device” because the intermediate layer “reduce[s] the amount of stresses induced in the PMOS device by acting as a physical barrier”).

95. A number of prior art references taught that using an intermediate layer “buffers the large stress inherent silicon nitride layer.” Murthy556, Ex.1430, 9:27-29; Alvarez, Ex.1406, ¶¶49, 66, 68, 77, FIGS. 9-11. As seen below, Alvarez depicts on example with a stress-inducing layer 216 (shown in blue below) that is buffered by stress-control layer 226 (shown in purple) to mitigate the adverse effects of the stress layer on the PMOS devices 224b and 224c (while still improving performance of the NMOS devices).

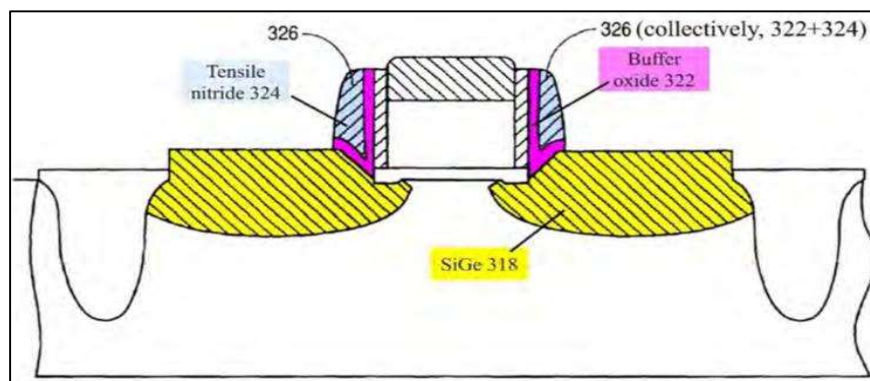


Alvarez, Ex.1406, FIG. 9

96. While the buffer layer above in Figure 9 is shown to be selectively applied, the prior art also explained that these layers could be applied to multiple areas, similar to the one Alvarez discloses (e.g., dual-purpose stress-controlling and masking layer), as a way to save manufacturing cost or complexity. Alvarez, Ex.1406, ¶¶43, 45, 47, 49,

53-55, 78, FIGS. 7-9. This is particular advantageous where “different types of transistors . . . hav[e] different operating parameters and requirements” and/or “due to the performance requirements of transistors in the particular regions.” *Id.*, ¶¶27, 32, FIGS. 7-9. Leaving the buffer layer over both the NMOS and PMOS, for example, can reduce the number of fabrication steps and lower the cost of manufacturing. *Id.*, ¶[0075]; *see also id.*, ¶¶74, 78.

97. In another example shown below, a buffer layer can be formed immediately between the SiGe source/drain regions and the gate electrode, particularly when raised SiGe source/drain regions are used. *See* Murthy556, Ex.1430, 9:11-15, 9:30-35, FIGS. 7-9; *see also* Miyashita, Ex.1435, ¶¶[0052]-[0053], FIGS. 1U-1W; Koutny, Ex.1434, ¶¶88, 108 (silicon dioxide liner 485A between tensile stress-inducing layer 504A and source/drain “reduces the cumulative stress” caused by the tensile layer); Doris, Ex.1429, ¶¶34, 42; Cheng810, Ex.1432, ¶30; Lee870, Ex.1431, ¶67.



**Murthy556, Ex.1430, FIG. 9 (annotated)**

98. These buffer layers can prevent “the tension from materially adversely influencing the charge carrier mobility in the pFET,” such that the pFET “experiences a performance improvement” through “enhanc[ed] hole mobility in the pFET channel” compared to no buffer layer. Doris, Ex.1429, ¶¶34-35, Figs. 2, 14, 15. Using low-stress dielectric films like silicon oxides can create “a neutral buffer layer” between a compressively stressed source/drain and a tensile contact etch stop layer, which allows the compressively stressed region “to have maximum influence on the pFET channel mobility and minimizes the influence of the tensile barrier etch stop layer.” *Id.*, ¶42; *see also* Lee870, Ex.1431, ¶¶29, 46-67 (explaining that an intermediate stress relief layer “with neutral stress or opposite stress relative to the [CESL]” reduces or eliminates any pFET performance degradation because it “reduces the tensile stress in the channel region”), FIGS. 2-5; Cheng810, Ex.1432, ¶¶22-31, Figs. 1B-1F.

#### **H. System-on-Chip Design Advancements**

99. Threshold voltage is an important characteristic when considering what a particular transistor will be used for. Threshold voltage is the minimum voltage applied at the gate to create a conductive channel between the source and drain—i.e., the ON or active voltage of the transistor. Van Zant, Ex.1211, 526, 474 (“Every MOS transistor is designed to operate at a specific threshold voltage.”). Because PMOS and NMOS transistors use different dopants for the source/drain and source/drain extensions, a POSITA understands that PMOS and NMOS transistors have opposite gate voltages.

That is, NMOS transistors require a positive voltage at the gate to induce the active state (and thus a positive threshold voltage), while PMOS transistors require a negative voltage at the gate to induce the active state (and thus a negative threshold voltage). *See, e.g., Weste, Ex.1212, 74, 293-296, 302.*

100. Threshold voltage has three main components: flatband voltage ( $V_{FB}$ ), voltage drop across the gate oxide ( $V_o$ ), and semiconductor potential at the semiconductor surface during strong inversion ( $\psi_s(\text{inv})$ ). *Sze-2002, Ex.1223, 175, 178, 194.* For a given semiconductor and dielectric material, substrate doping, oxide thickness  $t_{ox}$ , and the metal work function  $\Phi_m$  can be used to predictably tune a transistor's threshold voltage. *Houssa, Ex.1213, 535, 537.* When the substrate doping and gate oxide thickness are carefully engineered to control channel mobility and the gate capacitance, respectively, the gate electrode work function can be altered to optimize or fine-tune the threshold voltage further.

101. Consumer devices often have multiple transistors on the same chip, including transistors of the same conductivity types but with different threshold voltages, to cope with various demands on standby power and operation speed. For example, a device may include transistors for low operating power (LOP), transistors for low stand-by power (LSTP), and/or transistors for high performance (HP). *ITRS-PIDS, Ex.1216, 5.* HP transistors have the highest operating speed, the shortest gate length, the thinnest gate oxide, and the lowest threshold voltage among the three. *ITRS-*

PIDS, Ex.1216, 11, 17, 21. LSTP transistors are designed for low performance and low leakage current and therefore have thicker gate oxides and higher threshold voltage, while LOP transistors are between the HP and LSTP devices in terms of performance, leakage current, and threshold voltage. *Id.*

102. As recognized by the prior art, instead of making different chips for different purposes, HP, LOP, and LSTP transistors can be formed on a single chip by varying the manufacturing process parameters. Because “[a]n increasing number of mixed-signal and system-on-a-chip applications require dual on-chip power-supply-voltages[,]” different transistors of the same type (e.g., PMOS or NMOS) are needed for different power-supply-voltages. Wolf-4, Ex.1214, 121. For example, “[t]he higher-voltage may be used for the analog and input/output (I/O) circuitry, and the lower-voltage for the core-digital-logic devices.” *Id.* And because analog and I/O regions must handle higher operating voltages, “the analog and I/O devices require thicker gate oxides than the core logic devices.” *Id.* As such, forming different transistors with different gate oxide thickness can be used where needed, for instance where both higher-voltage and lower-voltage transistors are desired on the same chip.

103. The prior art teaches different processes to vary oxide thickness across different transistors on the same chip. *See, e.g.,* Karve, Ex.1226, 3:45-4:36 (describing formation of nMOS with thicker gate oxide than core nMOS), Figs. 5-6, 8; Luo, Ex.1227, 5:61-7:58 (describing formation of nMOS-DGO and nMOS core devices). As

explained by one textbook, one process is to include two oxidation steps “with a masked etch-step in between to remove the first oxide from regions intended to have thinner oxide.” Wolf-4, Ex.1214, 121. Yet another process uses nitrogen implants to impede oxide growth in certain areas, which occurs because “the rate of thermal-oxidation on silicon is reduced by nitrogen implants.” *Id.* “Hence, nitrogen implantation into the silicon substrate prior to the oxidation process can be used to facilitate the implementation of such ‘dual-gate-oxide’ ICs.” *Id.*

## **VI. THE '779 PATENT**

104. The '779 patent issued on August 5, 2014, from U.S. Patent Application No. 13/665,305, filed on October 31, 2012. Ex.1001, cover. The '779 patent claims priority to Japan Patent Application No. 2010-205599, filed on September 14, 2010. *Id.*

### **A. Claims**

105. The '779 patent has 15 claims, including one independent claim numbered 1, and dependent claims numbered 2-15. Ex.1001, 13:64-15:30. Claims 1, 2, 7, 12, and 13 are the Challenged Claims.

106. The Challenged Claims are reproduced below:

**1. Preamble:** A semiconductor device comprising:

**1[a]:** a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate,

**1[b]:** wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film,

**1[c]:** the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film,

**1[d]:** the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer,

**1[e]:** the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer,

**1[f]:** the first interface layer has a thickness larger than that of the second interface layer, and

**1[g]:** each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film.

Ex.1001, 13:64-14:22.

**2[a]:** The semiconductor device of claim 1, wherein the first gate electrode includes first sidewall spacers formed on side surfaces thereof and first insulating spacers interposed between the first gate electrode and the first sidewall spacers,

**2[b]:** the second gate electrode includes second sidewall spacers formed on side surfaces thereof and second insulating spacers interposed between the second gate electrode and the second sidewall spacers, and

**2[c]:** the first insulating spacers are thinner than the second insulating spacers.

Ex.1001, 14:23-33.

7. The semiconductor device of claim 2, wherein each of the first insulating spacers and the second insulating spacers is made of a silicon nitride film.

Ex.1001, 14:60-62.

**12.** The semiconductor device of claim 1, wherein each of the first and second high dielectric constant insulating films contains hafnium or zirconium.

Ex.1001, 15:20-22.

**13.** The semiconductor device of claim 1, wherein the first and second high dielectric constant insulating films are equal in thickness.

Ex.1001, 15:23-25.

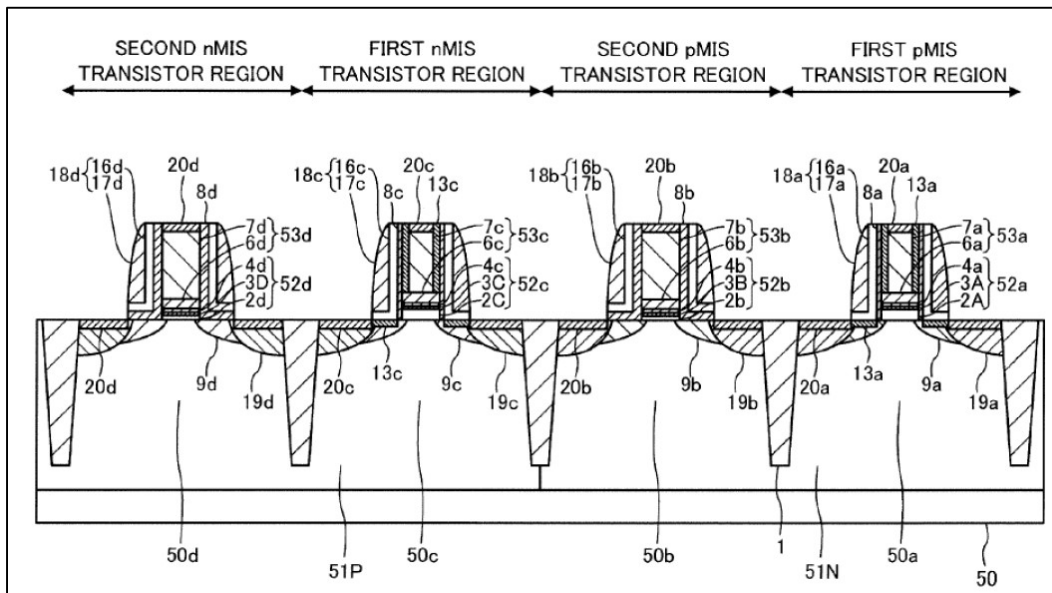
## **B. Summary of the Specification**

107. The '779 Patent is directed to “a metal insulator semiconductor (MIS) device including a gate insulating film formed on a semiconductor substrate and a gate electrode formed on the gate insulating film.” Ex.1001, 1:17-19. The '779 patent purports to enable “formation of a plurality of transistors of the same conductivity type and different from each other in work function in a semiconductor device having a MIS structure in which a high-k film is used as a gate insulating film.” *Id.*, 6:35-39. Thus, the '779 patent explains that “the present disclosure is useful as a semiconductor device having a CMIS structure including a plurality of MIS transistors different in threshold voltage ( $V_{th}$ ) . . . .” *Id.*, 6:39-43.

108. The Challenged Claims recite a semiconductor device with at least two transistors of the same type (p or n), each with a gate insulating film that includes an interface layer, where one interface layer is thicker than the other (claim 1); and a semiconductor device with two such transistors, each including sidewalls that

include insulating spacers, where the insulating spacers on one transistor are thinner than the insulating spacers on the other transistor (claim 2, dependent from claim 1). Ex.1001, 14:23-15:25. The other dependent Challenged Claims specify that the insulating spacers are made of a silicon nitride film (claim 7, dependent from claim 2), that the insulating films contain hafnium or zirconium (claim 12, dependent from claim 1), and that the insulating films are equal in thickness (claim 13, dependent from claim 1). *Id.*

109. Thus, the '779 patent described that each of the transistors includes a gate electrode (53a-d) with gate insulating film (52a-52d) interposed between the gate electrode and an active region of the substrate (50a-d), as illustrated below:



Ex.1001, 8:47-60, FIG. 9. Each gate insulating film includes interface layer 2a-2d, high-k film 3a-3d, and cap film 4a-4d. *Id.*, 8:61-67. The interface layers 2A and 2C

in the first nMIS and pMIS regions are thicker than the interface layers 2b and 2d in the second nMIS and pMIS regions. *See id.*, 9:55-10:5.

110. The '779 patent notes, “transistors different in threshold voltage ( $V_{th}$ ) can be formed in a semiconductor integrated circuit, and a semiconductor integrated circuit device with improved performance can be produced by employing a low- $V_{th}$  transistor in a circuit requiring high-speed performance and a high- $V_{th}$  transistor in a circuit requiring a reduced standby leakage current.” Ex.1001, 2:61-67.

111. The '779 patent describes a semiconductor device with multiple transistors intended to operate at different voltages. Because they are intended to operate at different voltages, they have different dielectric layers under their gate electrodes, with thicker layers being used for the higher-voltage transistors:

In the semiconductor device of the present disclosure, **the interface layer included in the gate insulating film of the first MIS transistor has a thickness larger than that of the interface layer included in the gate insulating film of the second MIS transistor** which is of the same conductivity type as the first MIS transistor. Accordingly, since an EOT of the gate insulating film of the first MIS transistor increases, an effective work function of the first MIS transistor increases. Therefore, according to the present disclosure, a plurality of transistors of an identical conductivity type having different effective work functions can be formed in a semiconductor device having a MIS structure in which a high-k film is used as a gate insulating film.

Ex.1001, 4:24-37 (emphasis added).

112. The '779 patent also describes the use of transistor sidewalls with spacers of varying thickness:

In the semiconductor device of the present disclosure, the first gate electrode may include first sidewall spacers formed on side surfaces thereof and first insulating spacers interposed between the first gate electrode and the first sidewall spacers, the second gate electrode may include second sidewall spacers formed on side surfaces thereof and second insulating spacers interposed between the second gate electrode and the second sidewall spacers, and **the first insulating spacers may be thinner than the second insulating spacers.**

Ex.1001, 4:38-46 (emphasis added).

### C. Summary of the Prosecution History

113. During prosecution of the application that led to the '779 patent, the Examiner issued a prior-art rejection of all pending claims as being anticipated by U.S. Patent No. 8,492,230 to Ishikawa, et al. ("Ishikawa"). Ex.1002, 204-205. In response, the Applicant argued that Ishikawa's gate insulating films "are formed above different base substrate[s]" and therefore Ishikawa does not anticipate claim 1. *Id.*, 300-301. Notably, the Applicant did not dispute that Ishikawa discloses two transistors with different interface layer thicknesses. *See id.*

114. The Applicant also amended claim 1 in response to the rejection to include the limitation, "each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film." *Id.*, 294. The application was allowed thereafter. *Id.*, 312-313.

## **VII. LEVEL OF ORDINARY SKILL IN THE ART**

115. I understand that there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including the educational level of active workers in the field at the time of the alleged invention, the sophistication of the technology, the type of problems encountered in the art, and the prior art solutions to those problems.

116. In determining the characteristics of a hypothetical person of ordinary skill in the art of the '779 patent at the time of the alleged invention, I considered several things, including the type of problems encountered in this field, and the rapidity with which innovations were made. I also considered the sophistication of the technology involved, and the educational background and experience of those actively working in the field, and the level of education that would be necessary to understand the '779 patent. Finally, I placed myself back in the relevant periods of time, and considered the state of the art and the level of skill of the engineers working in this field in those times.

117. It is my opinion that a POSITA at the time of the '779 patent would have had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or a related field, and three years of work experience in semiconductor design and manufacturing, including with respect to planar

transistors, or equivalent work experience. Additional graduate education might compensate for a deficiency in experience, and vice-versa.

118. I also note that my opinions provided in this Declaration would not change in view of any minor modifications to this level of skill.

## **VIII. CLAIM CONSTRUCTION**

119. It is my opinion that for purposes of this proceeding, the claim terms need not be construed to resolve the prior art issues presented in this Petition.

120. Nothing in this section should be construed as expressing any opinion as to whether the claims constitute patentable subject matter under 35 U.S.C. § 101, or whether they satisfy the definiteness, enablement, best mode, or written description requirements under 35 U.S.C. § 112.

## **IX. OVERVIEW OF THE PRIOR ART**

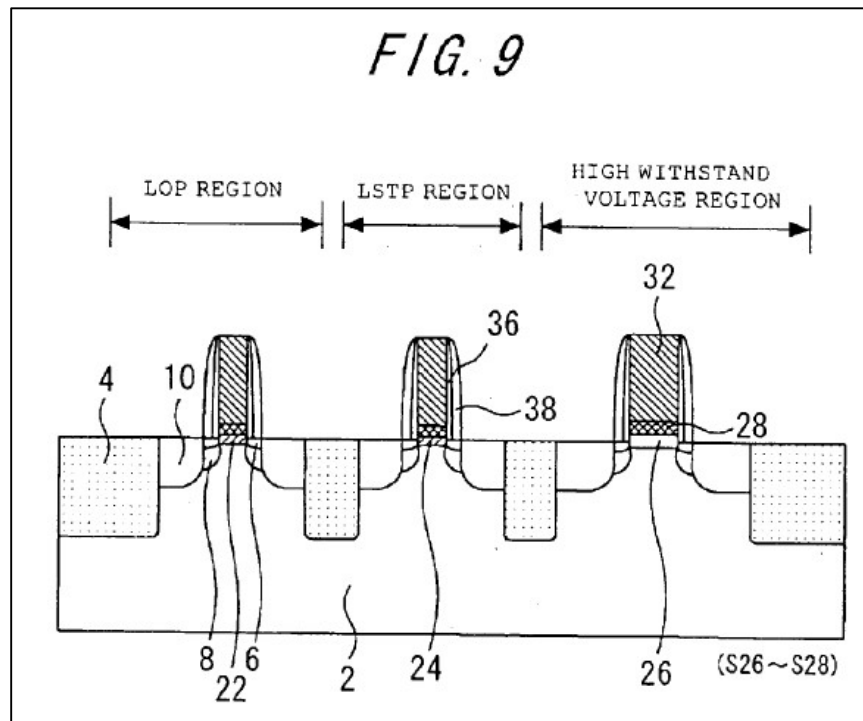
### **A. Torii**

121. Torii discloses “a semiconductor device having a plurality of transistors comprising gate insulating films of different film thickness.” Ex.1005, 1:11-14.

122. Torii explains that different transistors have differing voltage requirements, and thus, different gate insulating films; for example, logic transistors have a lower driving voltage than transistors “in the peripheral circuit portions,” and therefore the gate insulating film in a logic transistor can be thinner than the gate

insulating film in one of the peripheral, “high withstand voltage” transistors.  
Ex.1005, 1:24-30, 1:31-40.

123. In its first embodiment, Torii describes a set of three n-type transistors (Ex.1005, 10:39-45) with varying voltage requirements, and therefore varying gate insulating films. See FIG. 9 below:



124. As shown in the figure, Torii also teaches the use of sidewall spacers in its three transistors. The sidewall spacers 38 are three-layered:

Next, as FIG. 9 shows, sidewall spacers 38 are further formed on the sidewall spacers 36 (Step S26). Concretely, a silicon oxide film, a silicon nitride film, and a silicon oxide film are deposited in this order on the entire surface of the substrate. At this time, the thicknesses of the films

are about 15 nm, about 25 nm, and about 35 nm, respectively. Thereafter, anisotropic dry etching is performed using the silicon nitride film of the middle layer as the etching stopper to etch the overlying silicon oxide film; and then, the silicon nitride film exposed on the surface is removed by anisotropic dry etching using the underlying silicon oxide film as the etching stopper. Furthermore, the underlying silicon oxide film is removed using wet etching. **Thereby, sidewall spacers 38 each composed of a silicon oxide film, a silicon nitride film, and a silicon oxide film are formed on the outside of each sidewall spacer 36.**

Ex.1005, 7:38-53 (emphasis added).

125. Torii describes how its semiconductor device is made. The device has three transistors: “a MISFET (metal insulator semiconductor field effect transistor) 110 for LOP (low operating power) (hereafter referred to as MISFET for LOP 110); an MISFET 120 for LSTP (low stand-by power) (hereafter referred to as MISFET for LSTP 120); and an MISFET 130 for high withstand voltage (hereafter referred to as MISFET for high withstand voltage 130).” Ex.1005, 4:61-67.

126. The process begins with a substrate 2. Areas for forming the three transistors are isolated by shallow trench isolation, in which source-drain regions are formed later, after the gates are patterned, as can be seen in Figs. 2 and 12. Ex.1005, 5:1-4, 5:5-13, Figs. 2 & 12.

127. Then, films are formed over the substrate in the three transistor areas:

In the MISFET for LOP 110, a silicon oxynitride film 22 is formed as an interfacial gate insulating film in the area sandwiched by source-drain extensions 6 on the Si substrate 2. In the MISFET for LSTP 120, a silicon oxynitride film 24 is formed in the equivalent area. In the MISFET for high withstand voltage 130, a surface-nitrided thermally-oxidized ( $\text{SiO}_2$ ) film 26 is formed in the equivalent area. Here, the thickness of the silicon oxynitride film 22 in the MISFET for LOP 110 is about 0.9 to 0.95 nm, and the EOT thereof is about 0.7 nm. The thickness of the silicon oxynitride film 24 in the MISFET for LSTP 120 is about 1.3 nm; and the EOT thereof is about 1.0 nm. Furthermore, the thickness of the thermally-oxidized film 26 is about 5 nm. In short, the silicon oxynitride film 22 for the MISFET for LOP 110 is thinnest, and the thermally-oxidized film 26 for the MISFET for high withstand voltage 130 is thickest.

Ex.1005, 5:14-29.

128. Then, “On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia ( $\text{HfO}_2$ ) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed. The EOT of the high-k film 28 is about 0.5 nm. In each of MISFET 110, 120, and 130 for LOP, LSTP, and for high withstand voltage, respectively, a high-k film 28 is laminated on the

silicon oxynitride films 22 and 24 or the thermally-oxidized film 26, thereby each gate insulating film is formed.” Ex.1005, 5:33-41.

129. Thus, the gate insulating film for the low-power (LOP) transistor 110 is a silicon oxynitride film 22 about .9–.95 nm thick (Ex.1005, 5:20-22) covered with a high-k (*e.g.*, hafnia) film of about 3 nm thickness (*id.*, 5:33-36).

130. Thus, the gate insulating film for the low-standby-power (LSTP) transistor 120 is a silicon oxynitride film 24 about 1.3 nm thick (Ex.1005, 5:23-25) covered with a high-k (*e.g.*, hafnia) film 28 of about 3 nm thickness (*id.*, 5:33-36).

131. Thus, the gate insulating film for the high-withstand-voltage transistor 130 is a surface-nitrided thermally-oxidized (SiO<sub>2</sub>) film 26 about 5 nm thick (Ex.1005, 5:14-29) covered with a high-k (*e.g.*, hafnia) film 28 of about 3 nm thickness (*id.*, 5:33-36).

132. Then, gate electrodes are formed on top of the gate insulating films. Ex.1005, 5:42-51.

133. Then, “[o]n the sidewalls of each gate electrode 32 and the underlying gate insulating film, sidewall spacers 36 and 38 are formed.” Ex.1005, 5:49-51. As Torii explains, each inner sidewall spacer 36 is “a silicon nitride film of a thickness of about 5 nm.” *Id.*, 7:26-28. Each outer sidewall spacer 38 is “composed of a silicon oxide film, a silicon nitride film, and a silicon oxide film . . . formed on the outside of each sidewall spacer 36.” *Id.*, 7:50-53. I will consider the inner silicon oxide film

to be element 38a, the middle silicon nitride film to be element 38b, and the outer silicon oxide film to be element 38c. Element 38a is about 15 nm thick, element 38b is about 25 nm thick, and element 38c is about 35 nm thick. *Id.*, 7:38-43.

134. Source-drain regions are then formed, and the transistors completed by following the steps given in 7:54-8:13 of Torii.

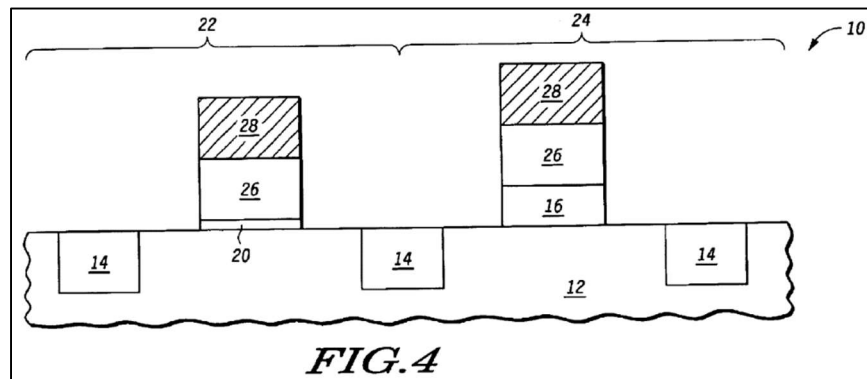
**B. Gilmer**

135. Gilmer recognized that in the prior art, “there is often a need to form transistors with different gate dielectric thicknesses on the same semiconductor substrate or wafer.” Ex.1009, 1:13-15. As an example, Gilmer explains that “transistors for input/output (I/O) devices may require thicker gate dielectrics than, e.g., transistors used for the core logic.” *Id.*, 1:15-17. Gilmer describes a “conventional process for forming differing thickness” called Dual Gate Oxide (DGO). *Id.*, 1:18-19.

136. Gilmer notes that this approach has problems “as transistor sizes shrink” because “there is a move ... to replace traditional silicon dioxide gate dielectrics with higher-k dielectric materials” such as metal oxides. Ex.1009, 1:36-40. For example, “because metal oxides cannot be thermally grown on a silicon substrate as silicon dioxide can, there are problems associated with multiple metal oxide depositions to form differing oxide thicknesses.” *Id.*, 1:40-46.

137. Gilmer purportedly addresses these problems and is directed “to semiconductor devices formed having dual gate dielectric thicknesses and utilizing high-k gate dielectric materials such as metal oxides.” Ex.1009, 1:7-10. Gilmer’s “invention integrates a high-k dielectric material, preferably a metal oxide, in a dual gate process sequence using a single metal oxide deposition to form multiple gate dielectric stacks of differing thicknesses.” *Id.*, 2:14-17. The “metal oxide is formed over prepared surfaces of the substrate that already provide a difference in equivalent oxide thickness (EOT) between two different regions of the substrate (e.g. the core logic region and the I/O region).” *Id.*, 2:17-22.

138. Gilmer’s Figure 4 (reproduced below) illustrates its semiconductor device 10:



Ex.1009, FIG. 4. Device 10 includes a semiconductor substrate having trench isolation regions 14 which “electrically isolat[e] different individual devices.” Ex.1009, 2:36-46. The device includes core device region 22 and I/O device region 24. *Id.*, 2:58-60.

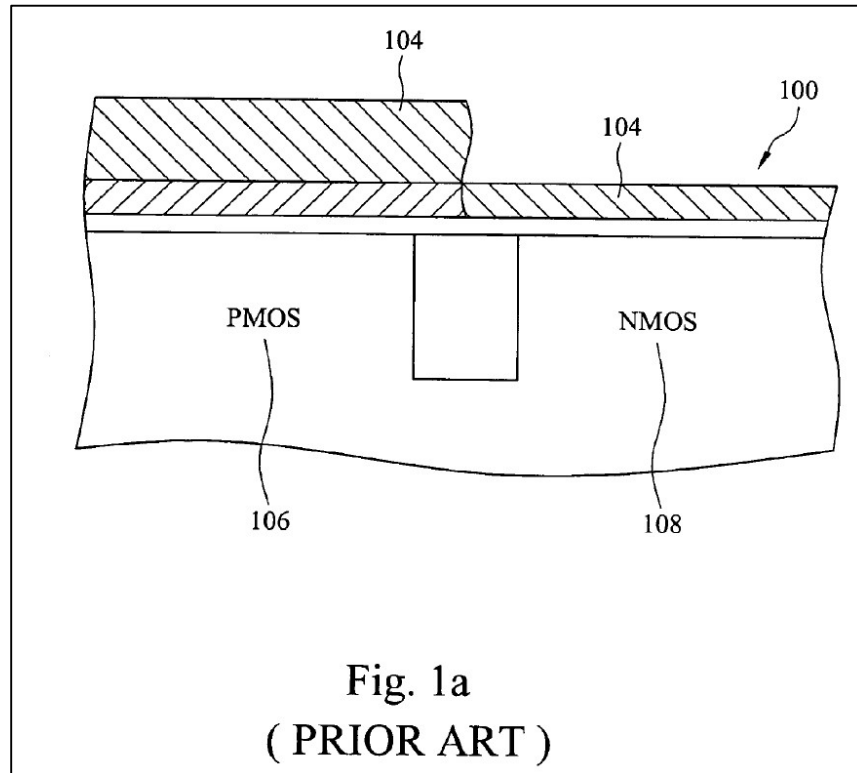
139. Core device region 22 includes a gate dielectric 20, high-k dielectric (metal oxide) 26, and gate electrode 28 “patterned and etched to form the gate stack[.]” Ex.1009, 4:35-38. Similarly, I/O device includes gate dielectric 16, high-k dielectric (metal oxide) 26, and gate electrode 28 “patterned and etched to form the gate stack[.]” *Id.*, 4:35-38. After the device of Figure 4 is formed, “conventional processing occurs to complete the transistor and integrated circuit formation (e.g. implants, spacers, interlayer dielectrics, interconnects, and passivation formation).” *Id.*, 4:43-47.

### **C. Chen**

140. Chen explains that “to produce competitive electronic devices, it is often desired to produce semiconductor chips with several different regions (e.g., core region, low power region, I/O region) having semiconductor devices that vary according to speed and power, for example.” Ex.1010, 1:18-22.

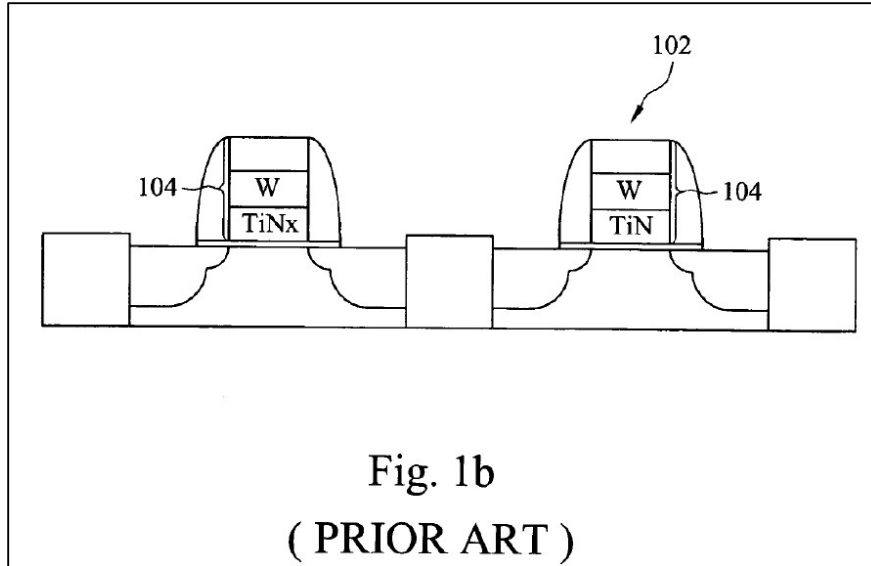
141. Chen describes prior art methods for controlling  $V_{th}$  of these transistors including “controlling the body potential of the SOI transistor” (Ex.1010, 1:37-45) and “channel region doping” (*id.*, 1:46-49). Chen also notes that “[a]nother known and accepted method of achieving a desired  $V_{th}$  is to modify the gate electrode work function by modifying the material composition of the gate electrode.” *Id.*, 1:63-65. For example, in prior art device 100 shown in Figure 1A (below), “the gate electrode

104 material composition, and correspondingly the gate electrode 104 work function, is varied to control the voltage threshold of the devices.”



*Id.*, 1:66-2:2, FIG. 1A. Specifically, gate electrode 104 “compris[es] nickel and titanium over the PMOS region 106 and comprising titanium over the NMOS region 108.” *Id.*, 2:7-9.

142. Chen’s prior art Figure 1B (reproduced below) illustrates transistors 102 that “have gate electrode 104 material compositions of tungsten W, titanium Ti, a first concentration of nitrogen N and a second concentration of nitrogen Nx.”



Ex.1010, 2:10-17, FIG. 1B. “The variation of material composition varies the gate work function of each gate electrode 104, thereby varying the voltage threshold of the FD SOI transistors 102.” *Id.*, 2:17-20.

143. Chen describes that one “method to achieve a different threshold voltage for a fully depleted SOI device is to change the gate work function,” as demonstrated by the following equation from Chen.

$$V_{th} = \underbrace{\Phi_{ms} - \frac{Q_f}{C_{ox}}}_{V_{FB}} + \Phi_s + \frac{\sqrt{2\epsilon q N_{A(D)} \Phi_s}}{C_{ox}}$$

Ex.1010, 2:38-45.

144. If the substrate concentration ( $N_{A(D)}$ ) is kept constant, another variable is needed “to control the threshold voltage to a desired value in a different application.” Ex.1010, 2:45-49. The gate work function (the  $\Phi_m$  component of  $\Phi_{ms}$ )

“is a good candidate for  $V_{th}$  tuning because recently metal gate development has become mainstream technology.” *Id.*, 2:49-51.

145. Chen discloses the combination of (1) buried dielectric thickness variation, (2) gate dielectric thickness variation, and (3) gate electrode work function variation provides a high degree of control of the voltage threshold of the transistors and other devices on the same chip die or in the same wafer. Ex.1010, 8:43-49. Chen’s third embodiment illustrates each of these control mechanisms.

146. As shown in Figures 3a-3h (third embodiment), the substrate “has a core region 202 and an input/output (I/O) region 204.” Ex.1010, 4:49-50. In Figure 3a (reproduced below), STI structures 220 “are formed in the silicon region 222 overlying the buried dielectric 210.”

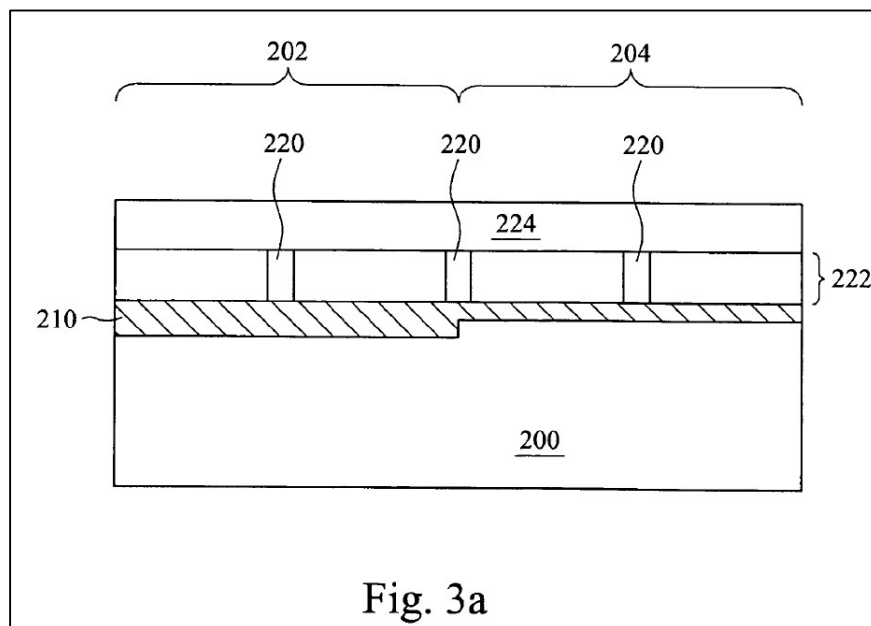
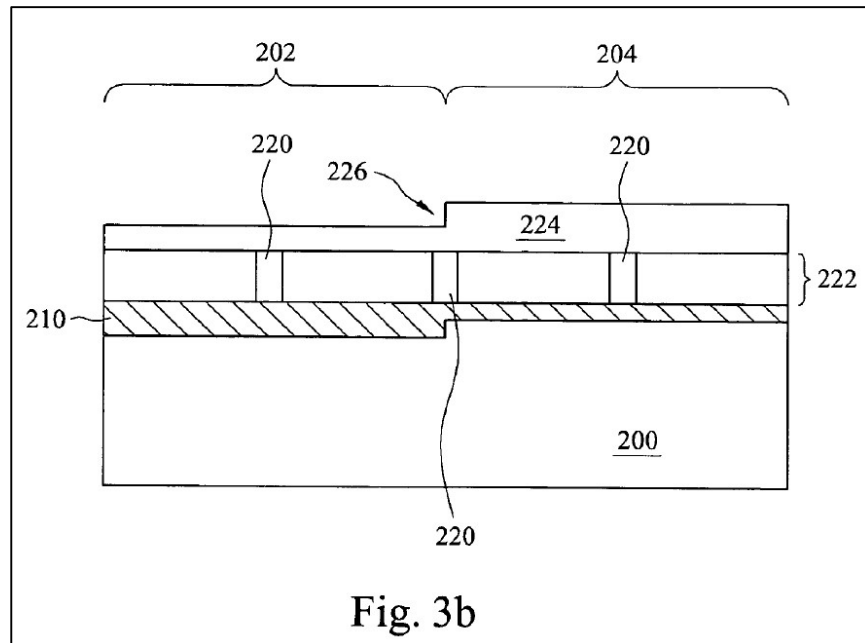


Fig. 3a

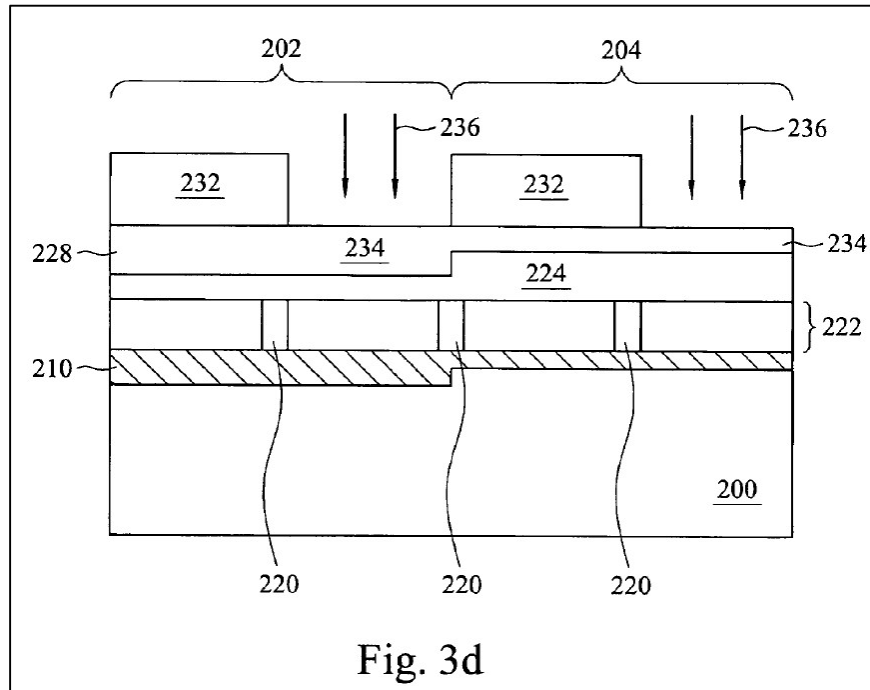
*Id.*, 7:3-5, FIG. 3a. Gate dielectric 224 is then deposited. *Id.*, 7:9-10. The gate dielectric is “formed of a high k dielectric material having a high dielectric constant, greater than about 4” such as a “metal dielectric, including metal oxide such as Al<sub>2</sub>O<sub>3</sub>, Ta<sub>2</sub>O<sub>5</sub>, ZrO<sub>2</sub>, and HfO<sub>2</sub>, or HfSi for example.” *Id.*, 7:12-17.

147. The gate dielectric 224 in the I/O region 204 is masked “and a portion of the exposed gate dielectric 224 in the core region 202 is removed.” Ex.1010, 7:20-23, FIG. 3b (below).



The “thicker portion of the gate dielectric 224 will enable a higher voltage threshold in the FD SOI devices that will subsequently be formed in the I/O region 204.” *Id.*, 7:30-32. In contrast, the “devices to be formed in the core region 202 will have a thinner gate dielectric 224 and a corresponding lower voltage threshold.” *Id.*, 7:32-35.

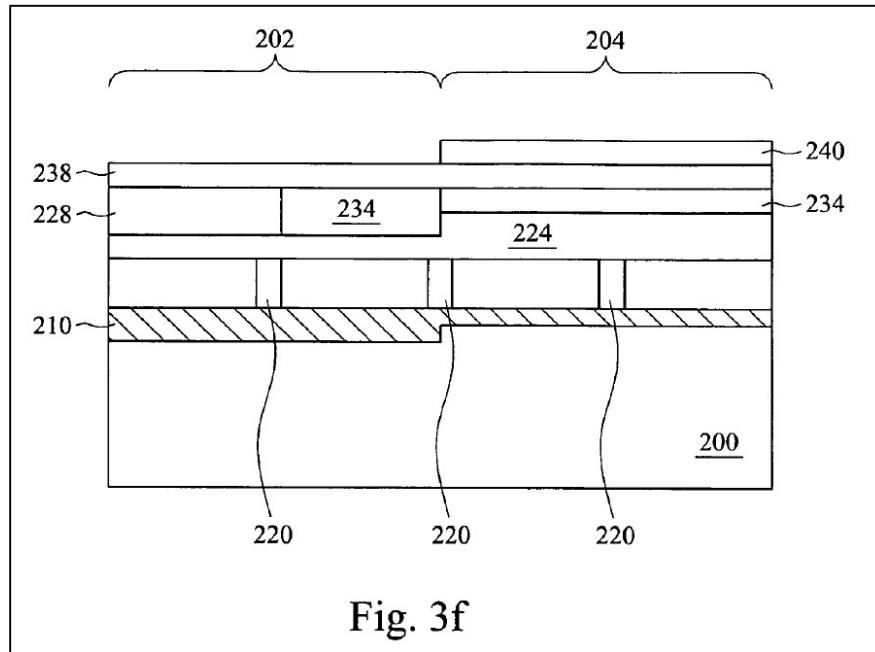
148. Polysilicon 228 “is deposited on the gate dielectric 224.” Ex1.008, 7:35-36. A photoresist is formed on the polysilicon, as shown in Figure 3d:



*Id.*, FIG. 3d. “Unmasked portions 234 of the polysilicon 228 are doped 236 with an n-type dopant, forming n-doped polysilicon region 234.” *Id.*, 7:44-46.

149. Once the mask (photoresist material 232) is removed, first metal layer 238, preferably comprising titanium, and second metal layer 240, preferably comprising platinum, “are consecutively deposited over the gate dielectric 224.” Ex.1010, 7:53-63. The first 238 and second 240 metal layers may, for example, “alternatively comprise nickel, palladium, platinum, iridium, ruthenium, rhodium, molybdenum, hafnium, aluminum, cobalt, tungsten, or combinations thereof” including “metal alloys such as binary metal alloys, metal silicides, metal silicon nitrides, doped metal alloys, and doped silicide alloys, for example.” *Id.*, 7:63-8:3.

Subsequently, a portion of the second metal layer 240 in the I/O region is masked and the second metal layer 240 in the core region is removed. *Id.*, 8:4-7, FIG. 3f (below).



*Id.*, FIG. 3f.

150. A thermal anneal then “causes the metals 238 and 240 to diffuse into the undoped 228 and doped 234 regions of the polysilicon.” Ex.1010, 8:10-13. This anneal process “produces a silicon titanium alloy gate electrode 250 and an n-doped silicon titanium alloy gate electrode 252 in the core region and a titanium, platinum and silicon alloy 254 and an n-doped titanium, platinum and silicon alloy 256 in the I/O region 204.” *Id.*, 8:13-18.

151. After further processing, transistors are produced as shown in Figure 3h below.

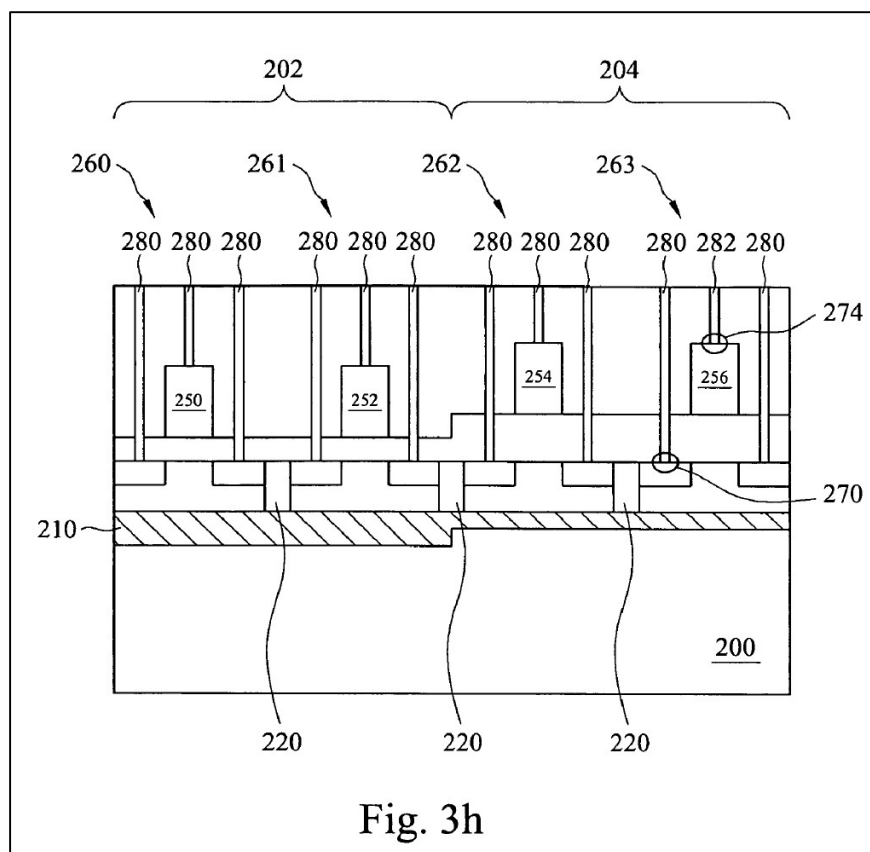
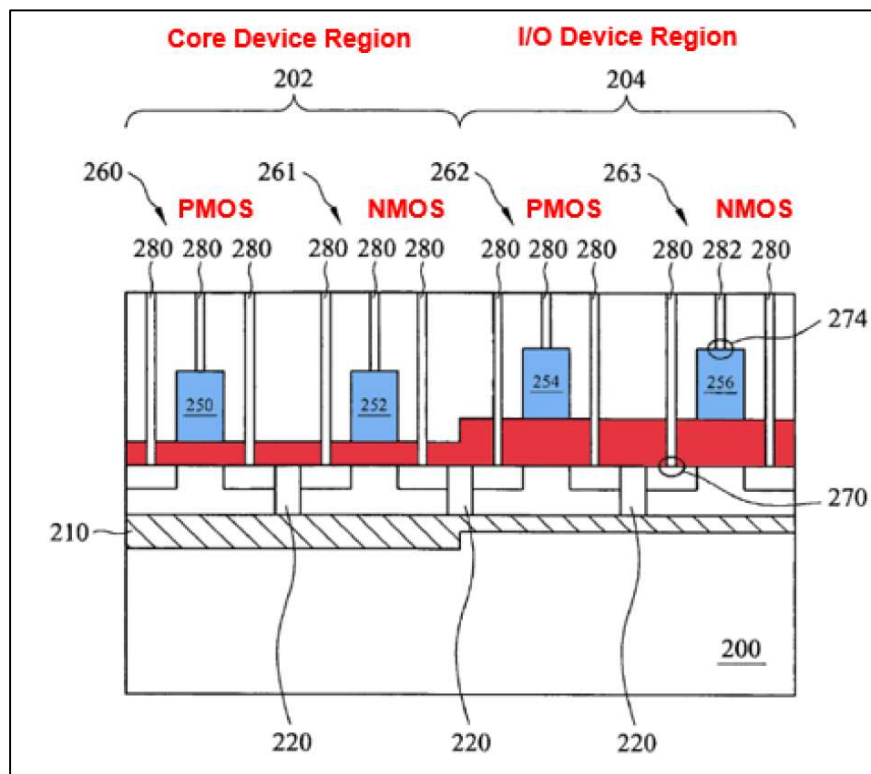


Fig. 3h

Ex.1010, FIG. 3h. Chen discloses that the resulting chip includes a first pMOS transistor with a “first gate electrode having a first work function” and a first nMOS transistor with a “second gate electrode having a second work function” in the “core region.” *Id.*, 3:39-46. The chip also includes a second pMOS transistor with a “third gate electrode having a third work function” and a second nMOS transistor with a “fourth gate electrode having a fourth work function” in the I/O region. *Id.*, 3:49-58.

152. I note that Chen has a typographic error referring to devices 260 and 261 as pMOS devices and devices 262 and 263 as nMOS devices. *See* Ex.1010, 8:27-29. A POSITA would have understood devices 260 and 262 to be pMOS devices and devices 261 and 263 to be nMOS devices because Chen makes clear each of the

core and I/O regions include, respectively, a pMOS and an nMOS transistor pair. See, e.g., *id.*, 3:34-60. This is also evident from Chen’s claim 31. Further evidence for devices 261 and 263 being nMOS devices is the description of the n-type implants for source/drain regions (*id.*, 7:45 and Figure 3d), as well as the description of device 263 being an nMOS device (*id.*, 9:1). Conversely, the other two devices, 260, and 262, are pMOS devices, as illustrated below:



*Id.*, FIG. 3h (annotated).

153. Chen teaches that “[v]arying the material composition, and thereby the work function of the gate electrodes 250, 252, 254, and 256, provides a corresponding difference in voltage threshold” between the devices 260, 261, 262, and 263. Ex.1010, 8:29-33. That is, the threshold voltages of the transistors 260, 261,

262, and 263 “are partially controlled by the work function of the gate electrodes 250, 252, 254, and 256.” *Id.*, 8:33-35. The gate electrode 252 of the first region nMOS transistor has a work function ranging between about 4.2 eV and about 4.5 eV and the gate electrode 256 of the second region nMOS transistor has a higher work function, ranging between about 4.5 eV and about 4.8 eV. *Id.*, 8:39-42. The gate electrode 250 of the first region pMOS transistor has a work function ranging between about 4.7 eV and about 5.0 eV and the gate electrode 254 of the second region pMOS transistor has a work function ranging between about 4.4 eV and about 4.7 eV. *Id.*, 8:36-38.

## **X. SPECIFIC GROUNDS FOR PETITION**

### **A. Ground I**

154. In my opinion, Torii anticipates all of the Challenged Claims 1, 2, 7, 12, and 13 of the '779 patent (Ground I).

#### **1. Independent Claim 1**

##### **a. Preamble: “A semiconductor device comprising:”**

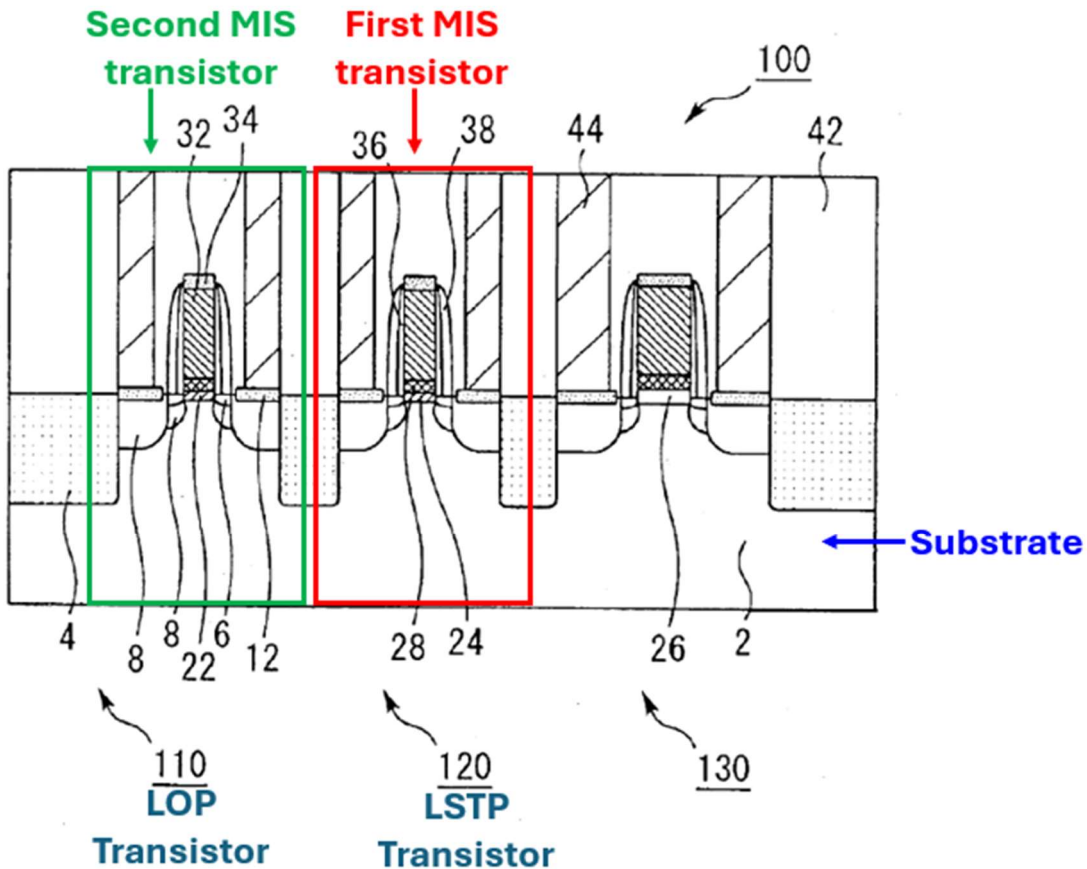
155. Torii is directed to a semiconductor device. Ex.1005, 1:9-10 (“The present invention relates to a semiconductor device and a method for manufacturing a semiconductor device.”) Therefore, it is my opinion that Torii discloses the preamble of claim 1 of the '779 patent.

**b. Limitation 1[a]: “a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate”**

156. As can be seen in Figures 1 and 9 below, Torii teaches a semiconductor device comprising three MIS transistors: one for low operating power (LOP) (element 110), one for low stand-by power (LSTP) (element 120), and one for high withstand voltage (HWV) (element 130). Ex.1005, 4:61-67. For purposes of my analysis in this ground, I identify the LSTP transistor 120 as the claimed “first MIS transistor” and the LOP transistor 110 as the claimed “second MIS transistor,” although the claimed “first MIS transistor” is also disclosed by the HWV transistor 130, as I explain in more detail below.

157. The first (LSTP) transistor 120 and the second (LOP) transistor 110 are of identical conductivity type, n-type in this embodiment. Ex.1005, 6:24-27, 10:39-45. Further, both the first transistor and the second transistor are formed on an identical semiconductor substrate, indicated by element 2 in Figures 1 and 9:

FIG. 1



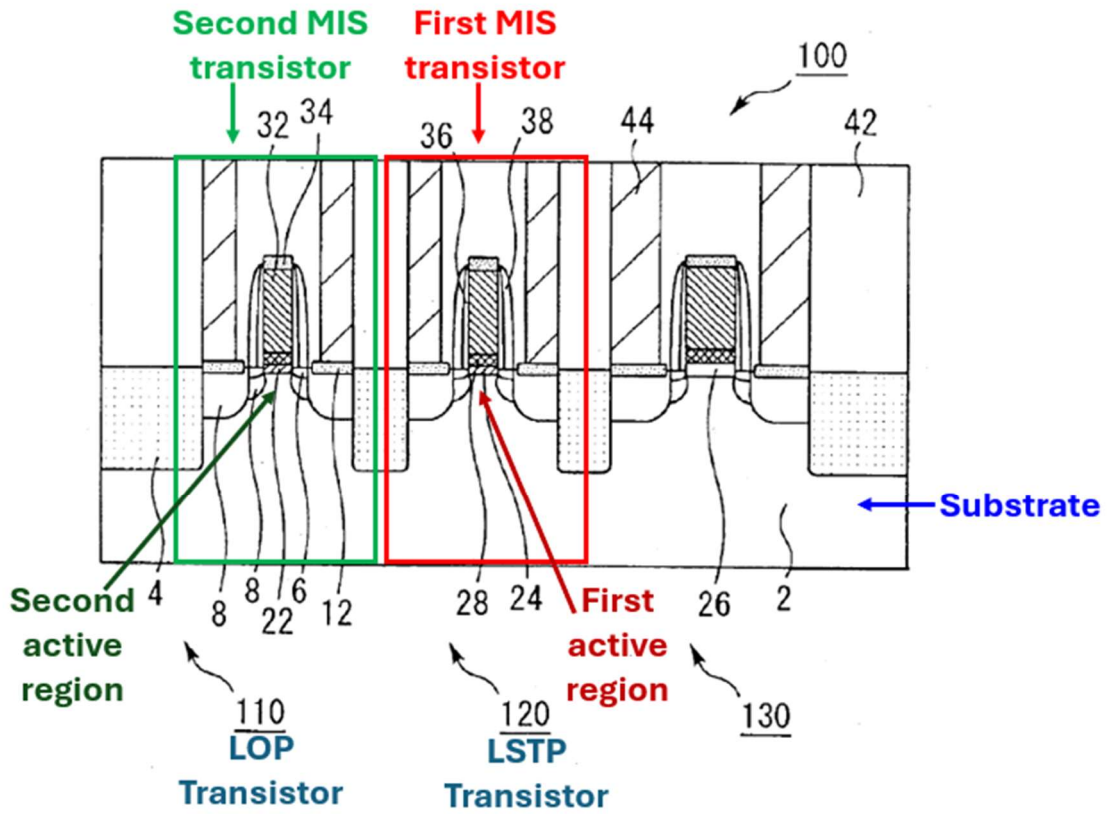
Ex.1005, Figure 1

Ex.1005, 5:1-4, FIGS. 1 (annotated), 9. Therefore, it is my opinion that Torii discloses this limitation.

- c. **Limitation 1[b]:** “wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film,”

158. Torii teaches a first MIS transistor (LSTP transistor 120), outlined below in red.

FIG. 1

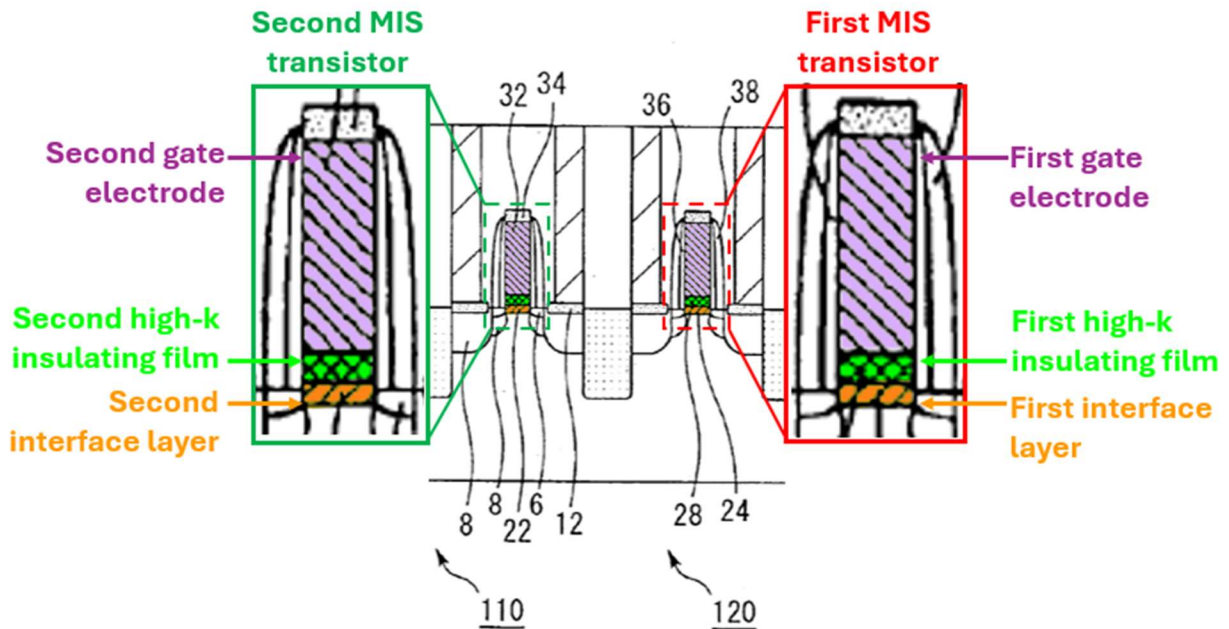


Ex.1005, Figure 1

Ex.1005, FIG. 1 (annotated).

159. The LSTP transistor 120 includes a first gate insulating film 26 and 28, collectively, formed on the active region in the semiconductor substrate. Ex.1005, 5:37-41 (“In each of MISFET 110, 120, and 130 for LOP, LSTP, and for high withstand voltage, respectively, a high-k film 28 is laminated on the silicon oxynitride films 22 and 24 or the thermally-oxidized film 26, thereby each gate insulating film is formed.”)

FIG. 1



Ex.1005, Excerpt from Figure 1 with enlargements

*Id.*, FIG.1 (annotated). “The MISFET for LSTP 120 is a low-standby-power transistor using the laminated film of the silicon oxynitride film 24 and the high-k film 28 as gate insulating film . . . .” *Id.*, 5:65-6:3.

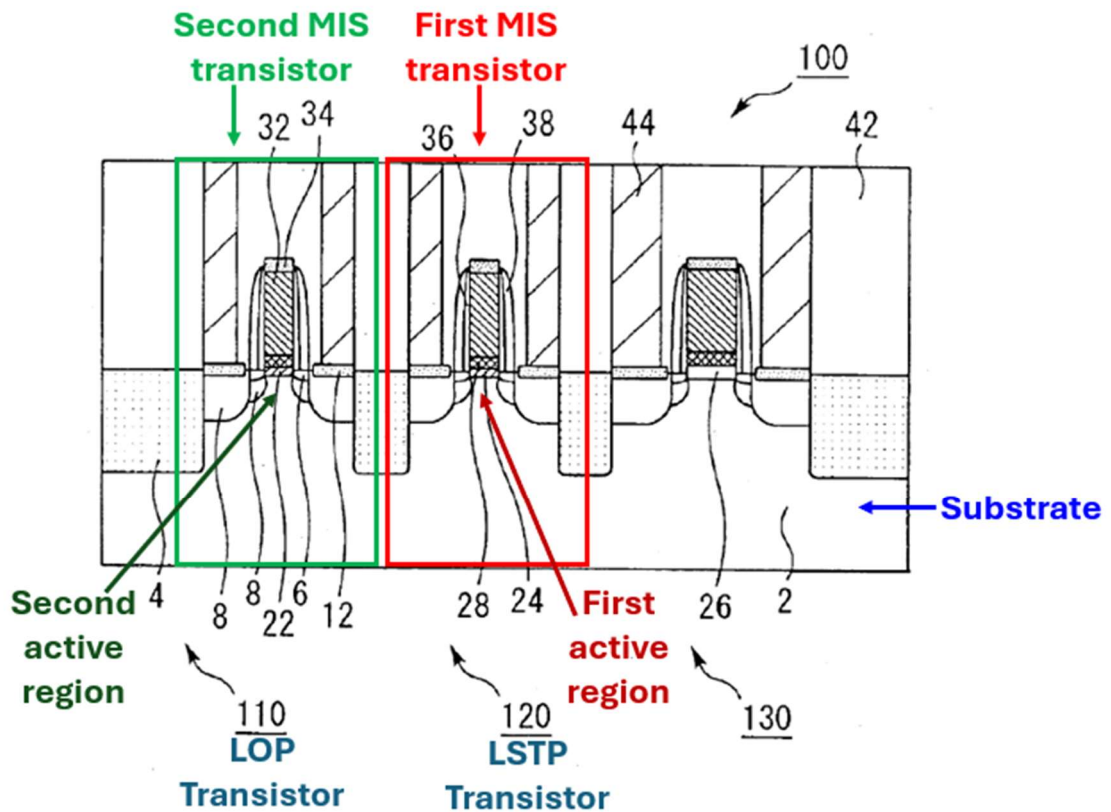
160. The LSTP transistor 120 also includes a first gate electrode 32 formed on the first gate insulating film. Ex.1005, 5:42 (“On each high-k film 28, a gate electrode 32 is formed.”)

161. For the foregoing reasons, it is my opinion that Torii discloses this limitation.

- d. **Limitation 1[c]: “the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film,”**

162. Torii teaches a second MIS transistor (LOP transistor 110), outlined below in green. Ex.1005, 4:61-67 (“MISFET . . . 110 for LOP”).

*FIG. 1*



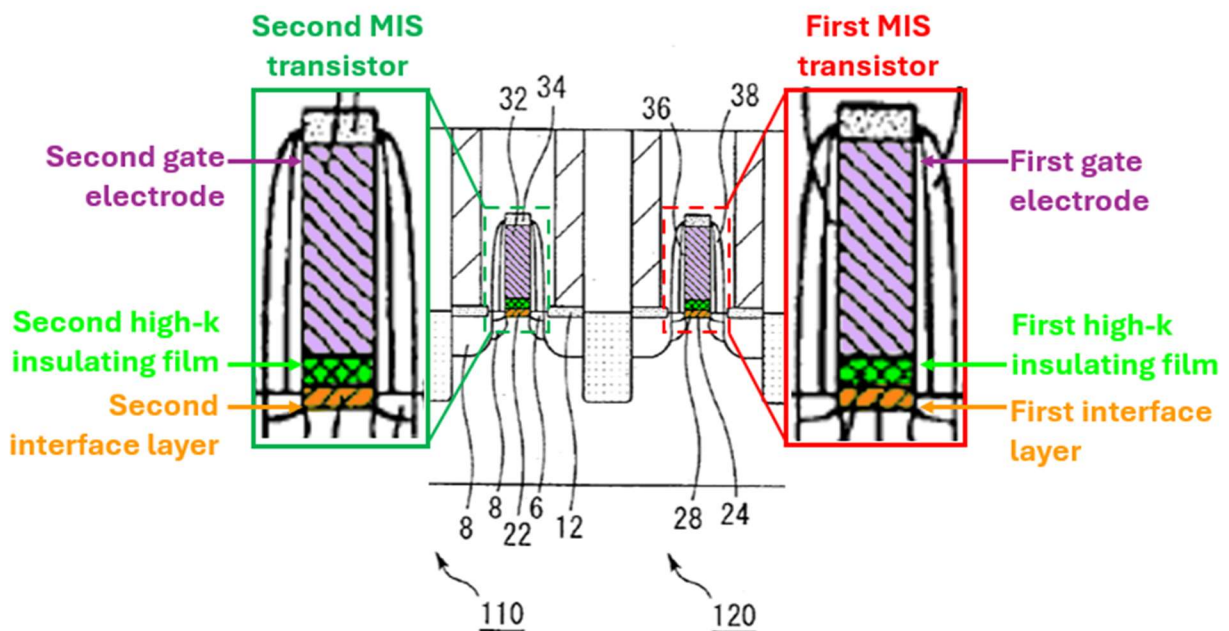
**Ex.1005, Figure 1**

Ex.1005, FIG. 1 (annotated).

163. The second transistor 110 includes a second gate insulating film 22 and 28, collectively, formed on the active region in the semiconductor substrate.

Ex.1005, 5:37-41 (“In each of MISFET 110, 120, and 130 for LOP, LSTP, and for high withstand voltage, respectively, a high-k film 28 is laminated on the silicon oxynitride films 22 and 24 or the thermally-oxidized film 26, thereby each gate insulating film is formed.”)

FIG. 1



Ex.1005, Excerpt from Figure 1 with enlargements

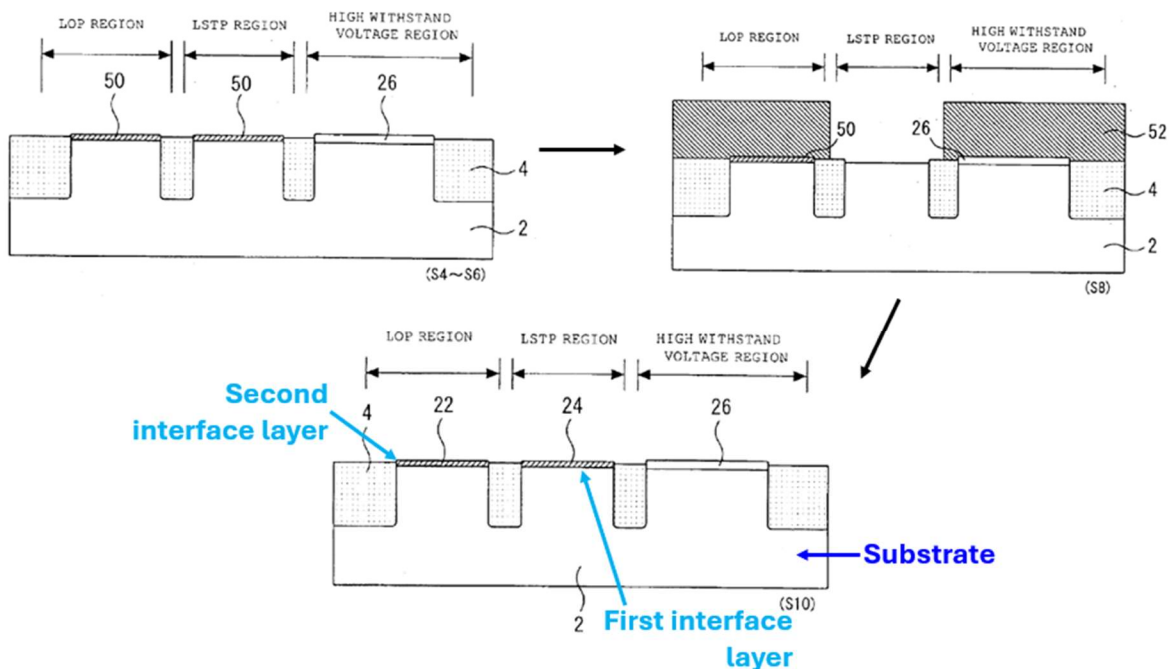
*Id.*, FIG. 1 (annotated). “[T]he MISFET for LOP 110 is a low-power-consumption transistor included (*sic*) the laminated film of the silicon oxynitride film 22 and the high-k film 28 as gate insulating film . . .” *Id.*, 5:62-65.

164. The second transistor 110 also includes a second gate electrode 32 formed on the second gate insulating film. Ex.1005, 5:42 (“On each high-k film 28, a gate electrode 32 is formed.”)

165. For the foregoing reasons, it is my opinion that Torii discloses this limitation.

- e. **Limitation 1[d]: “the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer,”**

166. In the first MIS transistor (*i.e.*, LSTP transistor 120), there is “a silicon oxynitride film 24” formed “as an interfacial gate insulating film.” Ex.1005, 5:14-18. This film is formed “on the Si substrate 2” and is the claimed first interface layer for purposes of my analysis in this ground. *Id.*, 5:14-18.

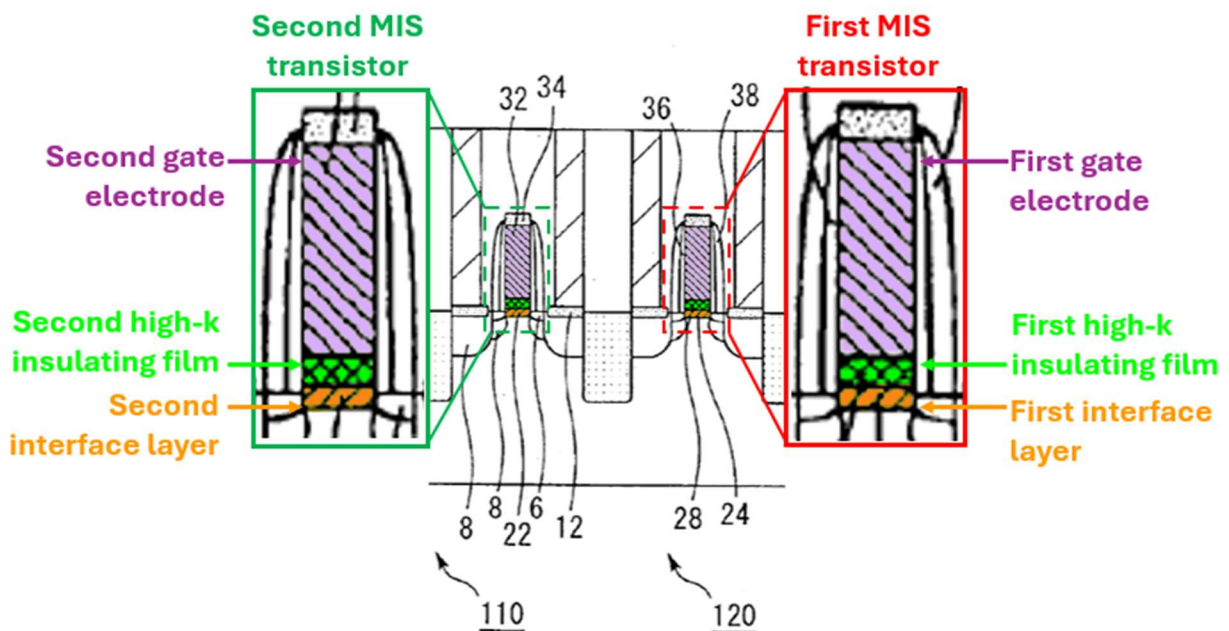


**Ex.1005, Figures 4 (top-left), 5 (top-right), 6 (bottom)**

167. On top of the interfacial gate insulating film (*i.e.*, the first interface layer), there is a high dielectric constant (high-k) insulating film. Ex.1005, 5:33-36

(“On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia (HfO<sub>2</sub>) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed.”) Therefore, it is my opinion that Torii discloses this limitation.

FIG. 1



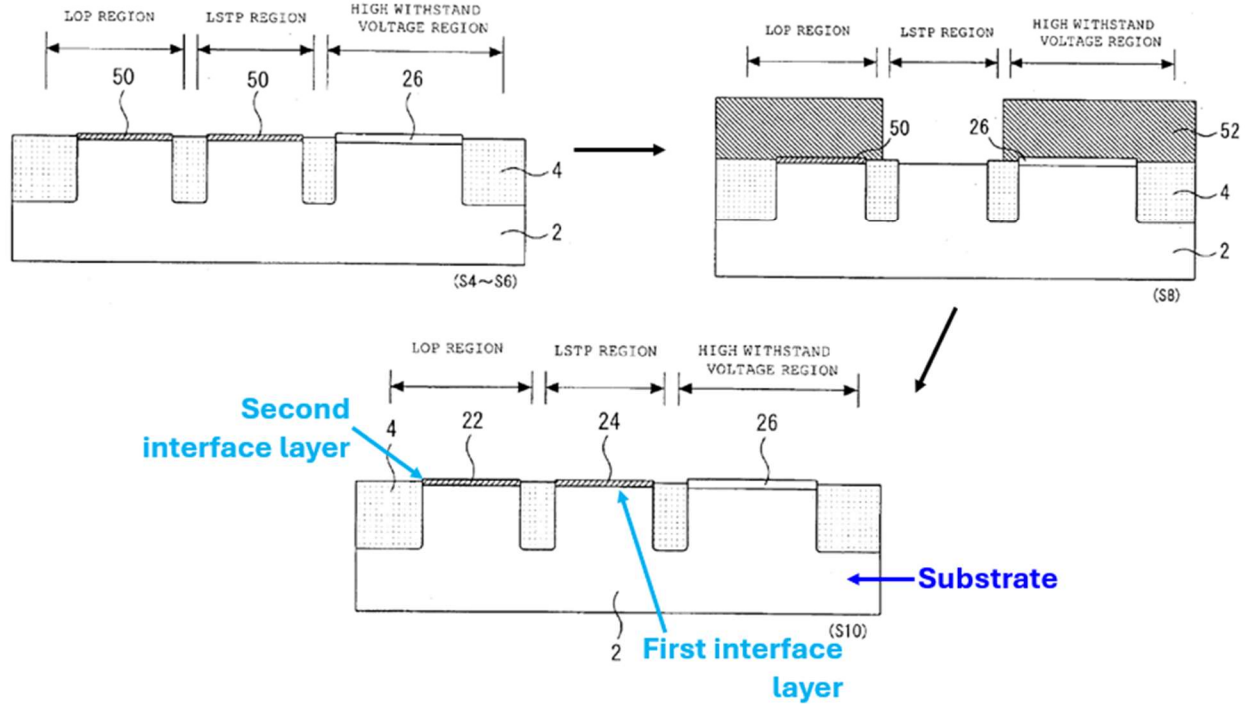
Ex.1005, Excerpt from Figure 1 with enlargements

Ex.1005, FIG. 1 (annotated).

- f. **Limitation 1[e]:** “the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer,”

168. In the second MIS transistor (*i.e.*, LOP transistor 110), there is “a silicon oxynitride film 22 . . . formed as an interfacial gate insulating film . . .”

Ex.1005, 5:14-18. This film is formed “on the Si substrate 2” and is the claimed second interface layer for purposes of my analysis in this ground. *Id.*

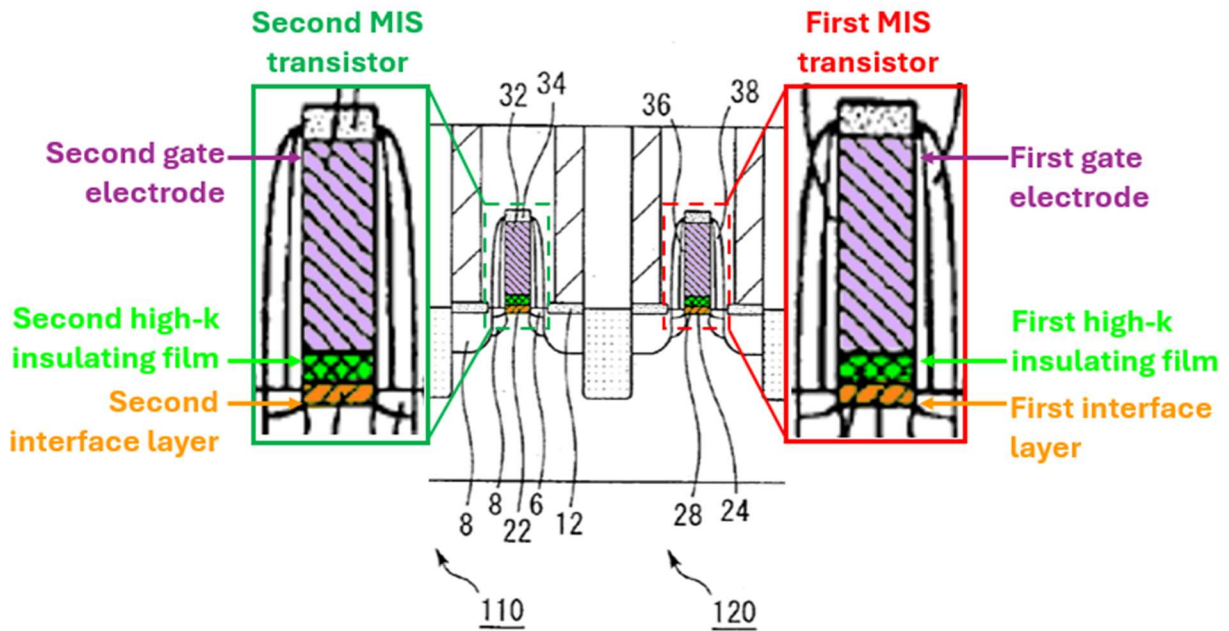


**Ex.1005, Figures 4 (top-left), 5 (top-right), 6 (bottom)**

Ex.1005, FIGS. 4-6 (annotated).

169. On top of the interfacial gate insulating film, there is a high dielectric constant (high-k) insulating film. Ex.1005, 5:33-36 (“On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia ( $\text{HfO}_2$ ) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed.”) Therefore, it is my opinion that Torii discloses this limitation.

FIG. 1



Ex.1005, Excerpt from Figure 1 with enlargements

Ex.1005, FIG. 1 (annotated).

- g. **Limitation 1[f]:** “the first interface layer has a thickness larger than that of the second interface layer,”

170. In the first (LSTP) transistor 120, the first interface layer 24 is “about 1.3 nm” thick. Ex.1005, 5:23-25. In the second (LOP) transistor 110, the second interface layer 22 is “about 0.9 to 0.95 nm” thick. *Id.*, 5:20-22. The first interface layer 24 is therefore thicker than the second interface layer 22 and it is therefore my opinion that Torii discloses this limitation.

- h. Limitation 1[g]: “each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film.”**

171. In the first (LSTP) transistor 120, the first interface layer 24 is “silicon oxynitride film 24.” Ex.1005, 5:23-25. In the second (LOP) transistor 110, the second interface layer 22 is “a silicon oxynitride film 22.” *Id.*, 5:14-17 Therefore, it is my opinion that Torii discloses this limitation.

## **2. Dependent Claim 2**

- a. Limitation 2[a]: “The semiconductor device of claim 1, wherein the first gate electrode includes first sidewall spacers formed on side surfaces thereof and first insulating spacers interposed between the first gate electrode and the first sidewall spacers,”**

172. Torii discloses that “[o]n the sidewalls of each gate electrode 32 and the underlying gate insulating film, sidewall spacers 36 and 38 are formed.” Ex.1005, 5:49-51. The inner spacers 36 are the first insulating spacers for purposes of this ground. *Id.*, 7:23-26 (“[O]n the sidewalls of each gate electrode 32 and each underlying gate insulating film of regions for LOP, LSTP, and high withstand voltage, sidewall spacers 36 are formed.”). These inner spacers are silicon nitride, which is an insulator. *Id.*, 7:23-27 (“a silicon nitride film”). The inner spacers 36 are about 5 nm thick. *Id.*, 7:23-28.

173. The outer sidewall spacers 38 in Torii comprise a triple layer structure, with an inner layer of silicon oxide about 15 nm thick (referred to hereafter as “38a”), a middle layer of silicon nitride about 25 nm thick (referred to hereafter as “38b”),

and an outer layer of silicon oxide about 35 nm thick (referred to hereafter as “38c”). Ex.1005, 7:38-43 (“Next, as FIG. 9 shows, sidewall spacers 38 are further formed on the sidewall spacers 36 (Step S26). Concretely, a silicon oxide film [38a]<sup>1</sup>, a silicon nitride film [38b], and a silicon oxide film [38c] are deposited in this order on the entire surface of the substrate. At this time, the thicknesses of the films are about 15 nm, about 25 nm, and about 35 nm, respectively.”)

174. After deposition, a series of anisotropic etching is performed to form the sidewall spacers 38, including “anisotropic dry etching . . . using the silicon nitride film of the middle layer as the etching stopper to etch the overlying silicon oxide film,” “anisotropic dry etching using the underlying silicon oxide film as the etching stopper” to remove the silicon nitride film on the surface of the substrate, and removing the remaining silicon oxide film “using wet etching.” Ex.1005, 7:44-50. Anisotropic etching is vertical etching that would remove the films from the surface of the substrate but leave the horizontal thicknesses of the different sidewall layers formed on sidewall spacer 36 relatively unchanged. *Id.*, 7:50-53 (“Thereby, sidewall spacers 38 each composed of a silicon oxide film, a silicon nitride film, and a silicon oxide film are formed on the outside of each sidewall spacer 36.”)

175. I consider elements 38a, the inner silicon oxide layer of elements 38 on the LSTP transistor, to be the claimed first sidewall spacers for purposes of my

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<sup>1</sup> Bracketed element callouts added.

analysis of this ground. Elements 38 “are further formed on the [inner] sidewall spacers 36.” Ex.1005, 7:38-39.

176. The inner spacers 36 are therefore interposed between the gate electrode and the first sidewall spacers 38a. The first insulating spacers (*i.e.*, inner spacers 36) and the first sidewall spacers (inner silicon oxide layer 38a) are formed on side surfaces of the first gate electrode (*i.e.*, of LSTP transistor 120). Ex.1005, FIG. 9. For the foregoing reasons, it is my opinion that Torii discloses this limitation.

**b. Limitation 2[b]: “the second gate electrode includes second sidewall spacers formed on side surfaces thereof and second insulating spacers interposed between the second gate electrode and the second sidewall spacers, and”**

177. As I explained above, the outer sidewall spacers 38 in Torii comprise a triple layer structure, with an inner layer of silicon oxide about 15 nm thick, a middle layer of silicon nitride about 25 nm thick, and an outer layer of silicon oxide about 35 nm thick. Ex.1005, 7:38-43 (“Next, as FIG. 9 shows, sidewall spacers 38 are further formed on the sidewall spacers 36 (Step S26). Concretely, a silicon oxide film [38a], a silicon nitride film [38b], and a silicon oxide film [38c] are deposited in this order on the entire surface of the substrate. At this time, the thicknesses of the films are about 15 nm, about 25 nm, and about 35 nm, respectively.”).

178. I consider the claimed second insulating spacers to be the middle silicon nitride layers 38b of elements 38 on the LOP transistor for purposes of my analysis

of this ground. These second insulating spacers are deposited about 25 nm thick and would have the same thicknesses relative to the two silicon oxide layers 38a and 38c and silicon oxide layer 36 after anisotropic etching. Ex.1005, 7:38-53.

179. I consider the outer silicon oxide layers 38c of elements 38 of the LOP transistor to disclose the claimed second sidewall spacers for purposes of my analysis of this ground. The second insulating spacers (*i.e.*, middle silicon nitride layers 38b) and the second sidewall spacers (*i.e.*, outer silicon oxide layers 38c) are formed on side surfaces of the second gate electrode (*i.e.*, of LOP transistor 110).

180. For the foregoing reasons, it is my opinion that Torii discloses this limitation.

**c. Limitation 2[c]: “the first insulating spacers are thinner than the second insulating spacers.”**

181. As I explained above, I consider the first insulating spacers to be the inner spacers 36 on the LSTP transistor for purposes of my analysis of this ground, which are about 5 nm thick. Ex.1005, 7:26-28. As I also described above, I consider the second insulating spacers for purposes of my analysis of this Ground to be element 38b (*i.e.*, middle silicon nitride layers of element 38) on the LOP transistor, which are about 25 nm thick. Ex.1005, 7:38-43. Therefore, the first insulating spacers are thinner than the second insulating spacers and it is therefore my opinion that Torii discloses this limitation.

### 3. Dependent Claim 7

- a. **Limitation 7: “The semiconductor device of claim 2, wherein each of the first insulating spacers and the second insulating spacers is made of a silicon nitride film.”**

182. Both inner spacer 36 (*i.e.*, first insulating spacer) on the LOP transistor and middle silicon nitride layers 38b (*i.e.*, second insulating spacer) on the LSTP transistor are made of a silicon nitride film. Ex.1005, 7:26-28, 7:38-43. Therefore, it is my opinion that Torii discloses dependent claim 7 of the '779 patent.

### 4. Dependent Claim 12

- a. **Limitation 12: “The semiconductor device of claim 1, wherein each of the first and second high dielectric constant insulating films contains hafnium or zirconium.”**

183. Both the first and the second high-k films are made of hafnia (*i.e.*, hafnium dioxide), which contains hafnium. Ex.1005, 5:33-36 (“On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia (HfO<sub>2</sub>) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed.”) Therefore, it is my opinion that Torii discloses dependent claim 12 of the '779 patent.

## **5. Dependent Claim 13**

- a. Limitation 13: “The semiconductor device of claim 1, wherein the first and second high dielectric constant insulating films are equal in thickness.”**

184. Both the first and the second high-k films are about 3 nm in thickness. Ex.1005, 5:33-36 (“On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia (HfO<sub>2</sub>) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed.”) Therefore, it is my opinion that Torii discloses dependent claim 13 of the ’779 patent.

## **B. Ground II**

185. In my opinion, Gilmer renders obvious claims 1, 12, and 13 of the ’779 patent.

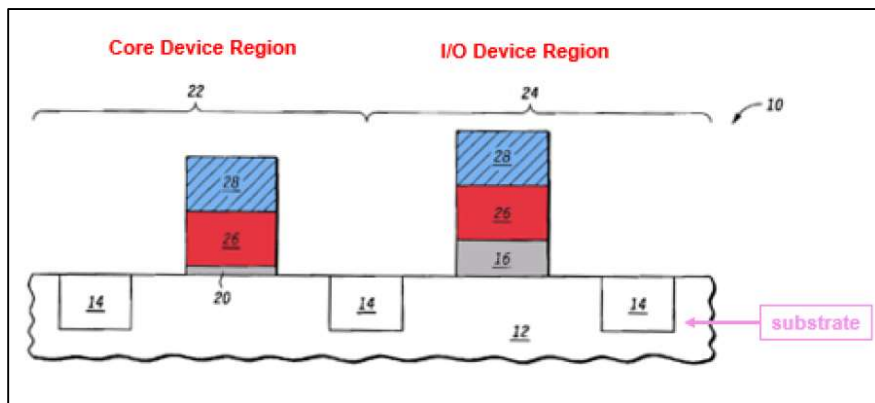
### **1. Independent Claim 1**

- a. Preamble: “A semiconductor device comprising:”**

186. Gilmer discloses that “[t]he present invention relates generally to semiconductor devices, and more particularly to semiconductor devices formed having dual gate dielectric thicknesses and utilizing high-k gate dielectric materials such as metal oxides.” Ex.1009, 1:7-10. Therefore, it is my opinion that Gilmer discloses the preamble of claim 1 of the ’779 patent.

**b. Limitation 1[a]: “a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate”**

187. Gilmer discloses a substrate. Ex.1009, 2:38-39 (“[S]emiconductor device 10 includes a semiconductor substrate 12.”) Gilmer also discloses two transistors provided on the same substrate. Ex.1009, FIG. 4, elements 22 and 24, and, e.g., 4:35-47 (“conventional processing occurs to complete the transistor and integrated circuit formation”). Core device region 22 and I/O device region 24 of Gilmer each includes a transistor, as illustrated below.



Ex.1009, FIG. 4 (annotated).

188. These two transistors are MIS transistors in my opinion. The gate stacks of both transistors include gate dielectric 16/20, high-k metal oxide layer 26, and gate electrode material 28. Ex.1009, 4:40-41, 2:46-48 (dielectric 16), 3:9-11 (dielectric 20), 3:44-47 (high-k layer), 4:38-40 (gate electrode), FIG. 4. Gate dielectric 16, gate dielectric 20, and high-k metal oxide 26 are each dielectrics (insulators) and gate electrode material 28 is “conductive (doped) polysilicon or a

metal (e.g., titanium nitride).” Ex.1009, 2:38-40. Each transistor therefore has a metal-insulator-silicon (MIS) structure in my opinion.

189. These two transistors are of an identical conductivity type, or at least, in my opinion, it would have been obvious to a POSITA to make the two transistors of the same type.

190. First, Gilmer provides I/O transistors (with higher voltage requirements) and logic transistors (with lower voltage requirements) having interface layers of different thicknesses. Ex.1009, 2:60-65 (discussing voltages for core and I/O devices). Gilmer compares electrical characteristics of these I/O and core transistors. Ex.1009, 2:58-65 (discussing voltages for core and I/O devices). In my opinion, A POSITA would have understood such comparisons apply to transistors of an identical conductivity type.

191. Second, Gilmer extensively discusses the concept of Dual Gate Oxide (DGO), which relates to the formation of transistors having different gate dielectric thickness on the same semiconductor substrate or wafer. Ex.1009, 1:13-19. In my opinion, A POSITA would have understood the core and I/O transistors of Gilmer are formed by a DGO process to have the same conductivity type.

192. Third, a substrate typically has a conductivity type (e.g., n-type or p-type). To form a transistor of a different conductivity type on the same substrate, a structure (e.g., a well) having a different conductivity type must be present in the

substrate. In my opinion, a POSITA would ascertain from Gilmer's description that both transistors share at least the same conductivity type because Gilmer does not disclose (i) the formation of any particular doped regions (*i.e.*, wells) within the substrate in either the core or I/O regions which would provide for a conductivity type separate from that of the substrate, or (ii) any indication that each of the transistors in the core or I/O regions are formed on different conductivity type regions (*i.e.*, wells) on the substrate.

193. Fourth, a POSITA would have further understood CMOS was the dominant processing technology in the semiconductor industry prior to the '779 patent. CMOS processing technology integrates both n- and p-type MOS devices side-by-side. Therefore, although only one is depicted in Gilmer's figures, a POSITA would have understood the I/O device had both an n-type and a p-type transistor and the core device had both an n-type and p-type device. That is, for every pair of DGO nMOS transistors, there is a corresponding pair of DGO pMOS transistors.

194. Additionally, making both transistors the same conductivity type would have been obvious to try in my opinion. A POSITA would have understood only two alternatives exist for the conductivity type of Gilmer's transistors: (1) core and I/O transistors are of an identical conductivity type or (2) core and I/O transistors are of different conductivity types.

195. It is my opinion that a POSITA would have had a reasonable expectation of success in pursuing both alternatives. Forming transistors of the same conductivity type (e.g., nMIS/nMOS or pMIS/pMOS transistors) in a substrate was well-known long before the '779 patent. Additionally, CMOS processing which forms both nMIS/nMOS and pMIS/pMOS transistors was also well-known before the '779 patent. For at least these reasons, trying these two alternatives would have led a POSITA to anticipated success with either alternative in my opinion.

196. Therefore, it is my opinion that this limitation would have been obvious to a POSITA in view of Gilmer.

**c. Limitation 1[b]: “wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film,”**

197. Gilmer’s I/O transistor in region 24 discloses the claimed first MIS transistor in my opinion. The I/O transistor in region 24 includes “a first gate dielectric 16 . . . formed over substrate 12” (Ex.1009, 2:47-48), which “is preferably silicon dioxide or silicon oxynitride,” (*id.*, 2:48-49), as well as a high-k dielectric layer 26 on top of the gate dielectric 16, (*id.*, 2:44-49). The gate dielectric 16 and the high-k layer 26 comprise the claimed first gate insulating film in my opinion.

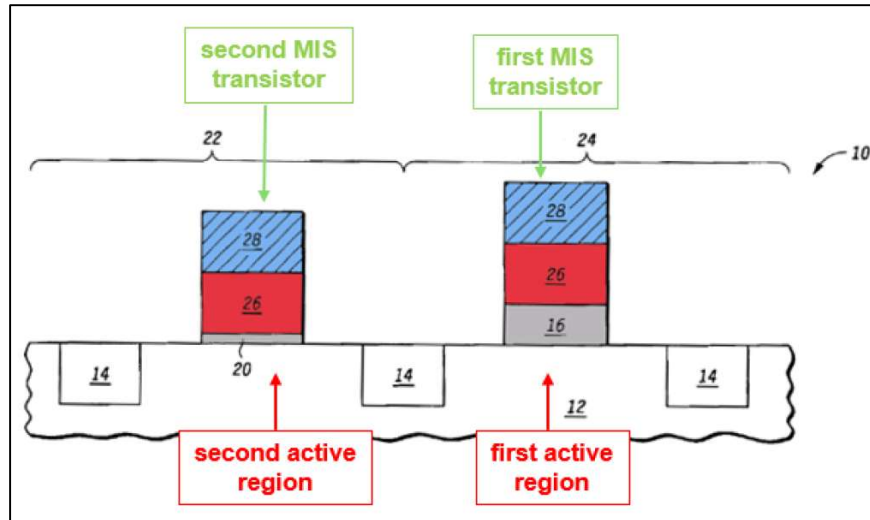
198. The I/O transistor in region 24 also includes a gate electrode formed on top of high-k layer 26. Ex.1009, 4:35-38 (“After metal oxide layer 26 has been deposited, a gate electrode material 28 is deposited over the metal oxide, and

semiconductor device 10 is patterned and etched to form the gate stacks as shown in FIG. 4.”) Therefore, it is my opinion that Gilmer renders this limitation obvious.

**d. Limitation 1[c]: “the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film,”**

199. Gilmer’s core transistor in region 22 discloses the claimed second MIS transistor in my opinion. The core transistor in region 22 includes a “second gate dielectric 20 formed on” the substrate. Ex.1009, 3:9-11. “In a preferred embodiment, second gate dielectric 20 is also silicon dioxide or silicon oxynitride.” Ex.1009, 3:12-14. The core transistor in region 22 also includes as a high-k dielectric layer 26 on top of the gate dielectric 16. *Id.*, 2:44-49. The gate dielectric 16 and the high-k layer 26 comprise the claimed second gate insulating film in my opinion.

200. The core transistor in region 22 also includes a gate electrode formed on top of high-k layer 26. Ex.1009, 4:35-38 (“After metal oxide layer 26 has been deposited, a gate electrode material 28 is deposited over the metal oxide, and semiconductor device 10 is patterned and etched to form the gate stacks as shown in FIG. 4.”) The first and second active regions in the semiconductor substrate 12, with the first and second gate insulating films of the first and second MIS transistors, respectively, formed thereon, and first and second gate electrodes formed on the first and second gate insulating films, respectively, are illustrated below.



Ex.1009, FIG. 4 (annotated). Therefore, it is my opinion that Gilmer renders this limitation obvious.

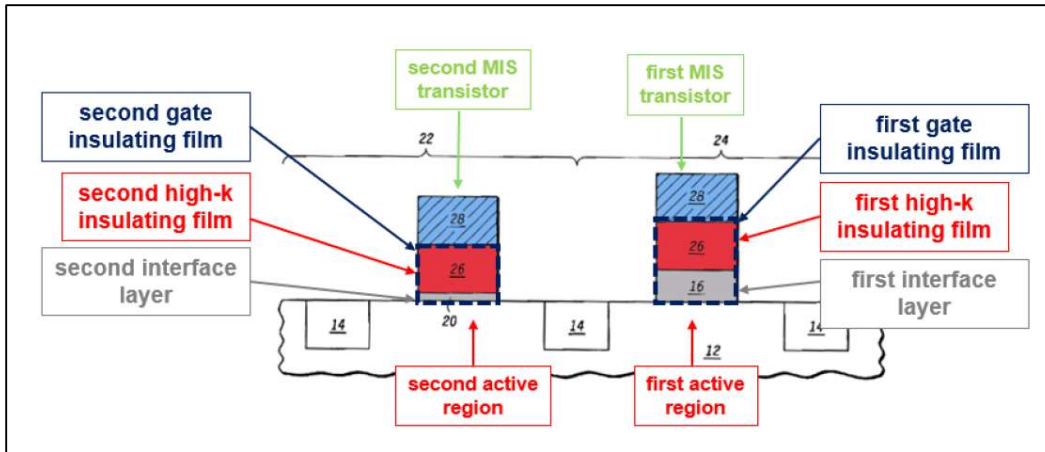
- e. **Limitation 1[d]: “the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer,”**

201. The first gate insulating film, comprised of gate dielectric 16 and the high-k layer 26, includes a first interface layer (gate dielectric 16) that is in contact with the substrate. Ex.1009, 2:47-48 (“a first gate dielectric 16 is formed over substrate 12”). FIG. 4. The first gate insulating film also includes a high dielectric constant insulating film, the high-k dielectric layer 26, formed on top of the gate dielectric 16. *Id.*, 2:44-49. Accordingly, Gilmer renders this limitation obvious in my opinion.

- f. Limitation 1[e]: “the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer,”**

202. The second gate insulating film, comprised of gate dielectric 20 and the high-k layer 26, includes an interface layer (gate dielectric 20) that is in contact with the substrate. Ex.1009, 3:10-12 (“a second gate dielectric 20 is formed on exposed portions of substrate 12 within the core device region 22”), FIG. 4. The second gate insulating film also includes a high dielectric constant insulating film, the high-k dielectric layer 26, formed on top of the gate dielectric 16. *Id.*, 2:44-49.

203. Thus, gate dielectric 16 is the claimed first interface layer being in contact with the semiconductor substrate, metal oxide 26 is the claimed first high dielectric constant insulating film formed on the first interface layer (*i.e.*, gate dielectric 16), and these dielectric layers collectively are the claimed first gate insulating film formed on a first active region in the semiconductor substrate, as illustrated below. *See* Ex.1009, 2:46-48, 3:44-47.

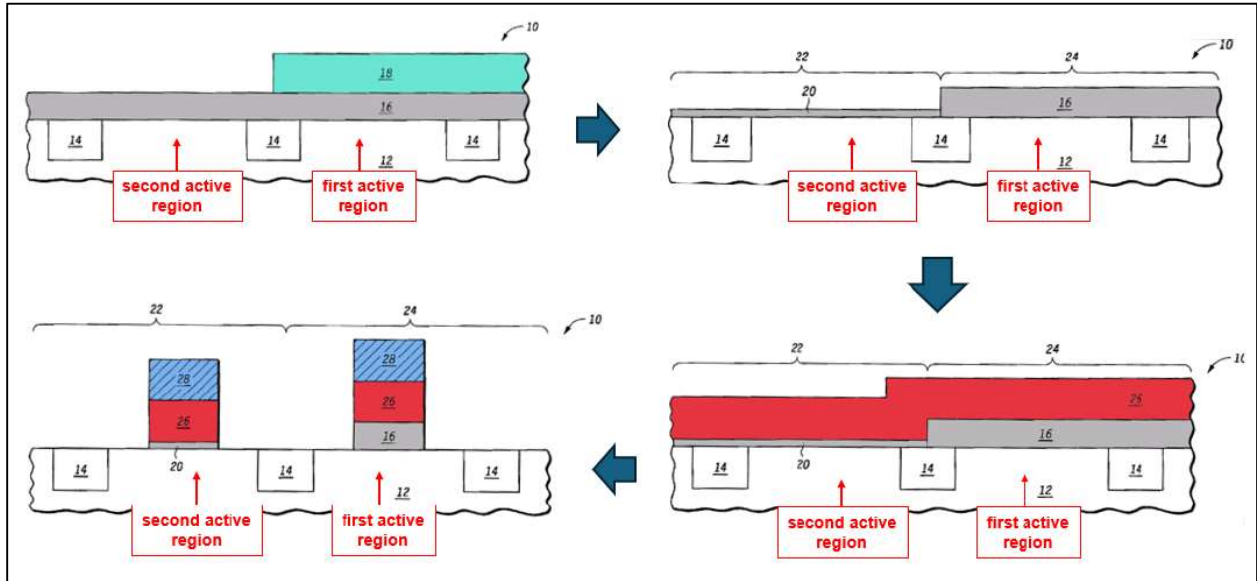


Ex.1009, FIG. 4 (annotated).

204. As illustrated above, gate dielectric 20 is the claimed second interface layer being in contact with the semiconductor substrate, metal oxide 26 is the claimed second high dielectric constant insulating film formed on the second interface layer (*i.e.*, gate dielectric 20), and these dielectric layers collectively are the claimed second gate insulating film formed on a second active region in the semiconductor substrate. *See* Ex.1009, 2:46-48, 3:44-47, FIG. 4 (above).

205. The semiconductor fabrication process disclosed by Gilmer confirms the semiconductor device structure of Figure 4, as explained above. Gilmer teaches that “[a]fter forming trench isolation regions 14, a first gate dielectric 16 is formed over substrate 12.” Ex.1009, 2:46-48, FIG. 1 (top-left below). After masking a portion of the first gate dielectric layer, the semiconductor device 10 is then etched “to remove unprotected portions of first gate dielectric 16 in core device region 22” and, after removal of the mask, “second gate dielectric 20 is formed on exposed

portions of substrate 12 within the core device region 22.” Ex.1009, 2:25-67, 3:7-12, FIG. 2 (top-right below).



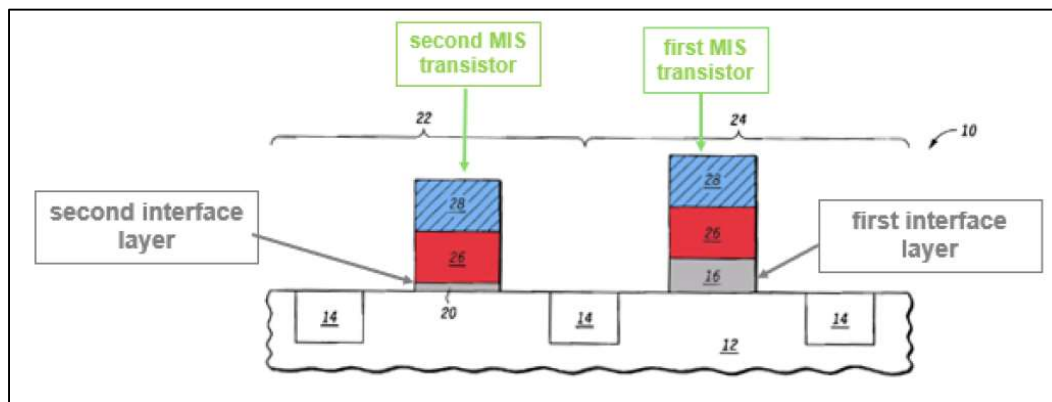
Ex.1009, FIGS. 1-4.

206. After the first and second gate dielectrics with “two different thicknesses have been formed, a high-k dielectric ... is deposited over semiconductor device 10.” Ex.1009, 3:44-47, FIG. 3 (bottom-right above). Gate electrode material 28 is subsequently “deposited over the metal oxide, and semiconductor device 10 is patterned and etched to form the gate stacks.” Ex.1009, 4:35-38, FIG. 4 (bottom-left above). Therefore, Gilmer teaches this limitation in my opinion.

- g. Limitation 1[f]: “the first interface layer has a thickness larger than that of the second interface layer,”**

207. Gilmer states that the thickness of first gate dielectric 16 “generally will be in a range of 30–50 Angstroms (3–5 nanometers),” (Ex.1009, 2:53-55), and the thickness of second gate dielectric 20 “generally will be within a range of 4–12 Angstroms (0.4–1.2 nanometers),” (*id.*, 3:17-21). Therefore, the first interface layer in Gilmer (gate dielectric 16) has a thickness greater than the second interface layer (gate dielectric 20). *See* Ex.1009, 2:60-65, Abstract, claim 1.

208. As shown below, the gate dielectric 16, which is the claimed first interface layer, has a thickness larger than that of the gate dielectric 20, which is the claimed second interface layer.



Ex.1009, FIG. 4. Thus, in my opinion, Gilmer teaches this limitation.

- h. Limitation 1[g]: “each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film.”**

209. Gilmer states that first and second interface layers (gate dielectrics 16 and 20) are “silicon dioxide or silicon oxynitride.” Ex.1009, 2:48-49 (gate dielectric 16), 3:13 (gate dielectric 20). Therefore, Gilmer teaches this limitation in my opinion.

## **2. Dependent Claim 12**

- a. Limitation 12: “The semiconductor device of claim 1, wherein each of the first and second high dielectric constant insulating films contains hafnium or zirconium.”**

210. Gilmer discloses that after the “gate dielectrics of two different thicknesses have been formed, a high-k dielectric ... is deposited over semiconductor device 10.” Ex.1009, 3:44-47. Gilmer further explains that preferably the high-k dielectric is a metal oxide 26 for which “[s]uitable materials for metal oxide 26 preferably include hafnium oxide . . . .” Ex.1009, 3:49-50. Therefore, it is my opinion that Gilmer teaches dependent claim 12 of the '779 patent.

### 3. Dependent Claim 13

- a. **Limitation 13: “The semiconductor device of claim 1, wherein the first and second high dielectric constant insulating films are equal in thickness.”**

211. Metal oxide film 26 is the same thickness in both the first (I/O) and the second (core) transistors. Ex.1009, FIG. 3, 4:8-24 (“a single metal oxide layer can be used . . . With the present invention, a single metal oxide deposition is used . . . .”)

212. Gilmer explains that “[b]ecause metal oxide 26 is deposited as a single blanket deposition, its thickness will not vary much across the substrate surface.” Ex.1009, 4:2-4. In my opinion, a POSITA would have understood that the metal oxide film 26, which is deposited as a single blanket deposition, is “equal in thickness” in both the I/O and core regions subject to very minor variations. It is also my opinion that Gilmer’s teaching is consistent with the disclosure of the ’779 patent, which only indicates that the “first and second high dielectric constant insulating films may be substantially equal in thickness.” Ex.1001, 5:31-33.

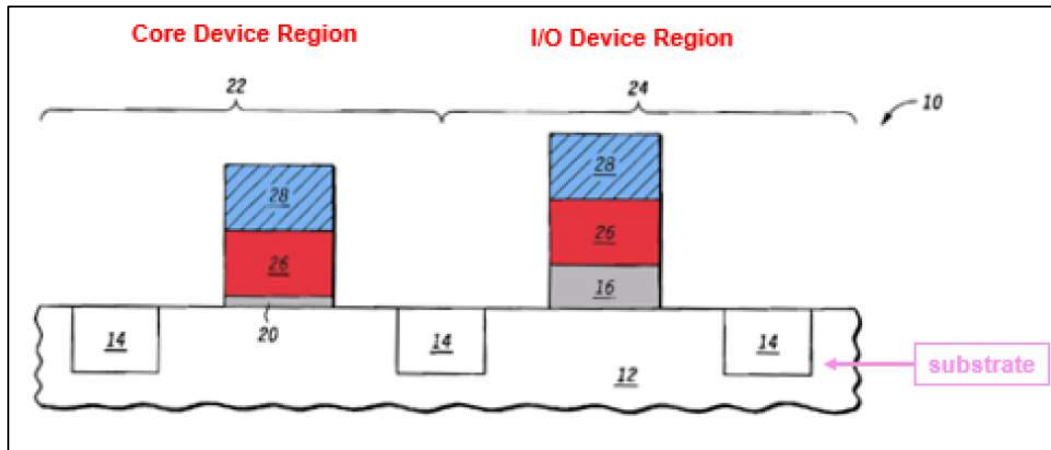
213. Therefore, it is my opinion that Gilmer teaches dependent claim 13 of the ’779 patent.

#### C. Ground III

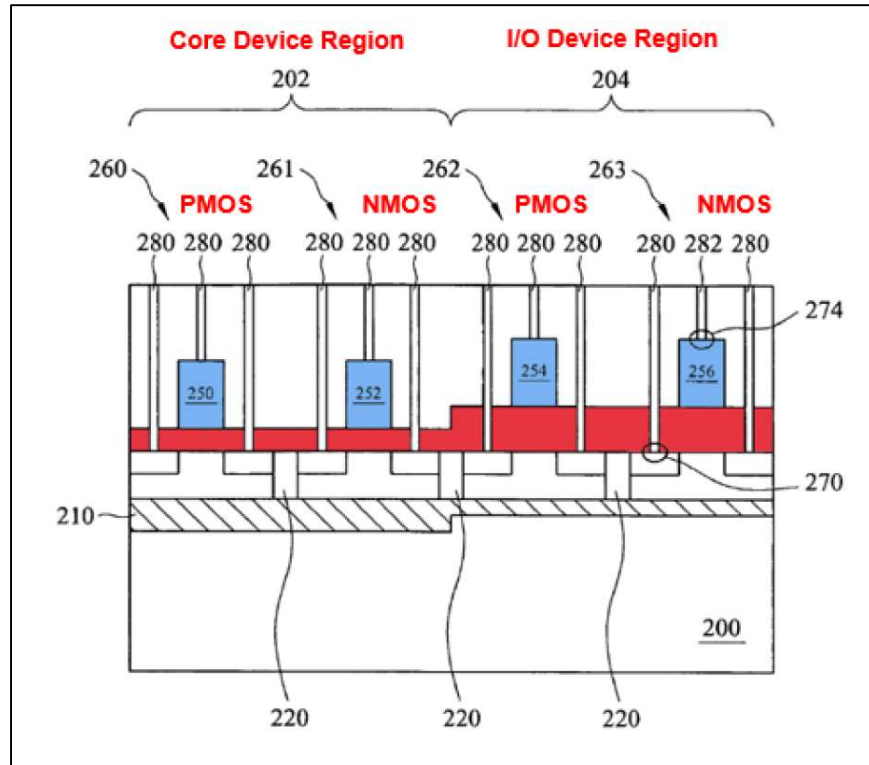
214. In my opinion, Gilmer combined with Chen renders obvious claims 1, 12, and 13 of the ’779 patent. As explained above, it is my opinion that Gilmer alone renders obvious all of the limitations of claims 1, 12, and 13 of the ’779 patent.

However, Gilmer in combination with Chen also renders obvious claims 1, 12, and 13 of the '779 patent in my opinion.

215. Gilmer discloses core and I/O transistors formed on a shared substrate, as illustrated in Figure 4:



Ex.1009, FIG. 4 (annotated). Chen teaches core and I/O transistors having similar structures formed in the same substrate and having “the same conductivity type,” as shown below in Figure 3h. Ex.1010, 3:39-60, 8:27-42 (describing two pMOS and two nMOS transistors).



Ex.1010, FIG. 3h (annotated).

216. Both Gilmer and Chen are in the same field as the '779 patent, “semiconductor devices and methods for fabricating the same.” Ex.1001, 1:15-16; *see* Ex.1009, 1:7-10, 2:36-38; Ex.1010, 1:12-14, 4:14-16. In my opinion, a POSITA would have been motivated to combine Chen’s teachings regarding forming transistors having the same conductivity type (e.g., two nMIS transistors or two pMIS transistors) with Gilmer’s semiconductor device. Gilmer suggests forming transistors of the same conductivity type, as explained above. For these same reasons, in my opinion, Gilmer suggests the combination with Chen.

217. Additionally, it is my opinion that a POSITA would have been motivated to make the combination based on his/her background knowledge in the

relevant art and common sense. The '779 patent acknowledges in its background section the well-known fact that devices have conductivity types and describes use of an n-well for pMIS transistors and a p-well for nMIS transistors. Ex.1001, 1:61-2:15. Based on this background knowledge, in my opinion, a POSITA would have been motivated to combine Gilmer and Chen and would have had a reasonable expectation of success in forming devices of the same conductivity type in Gilmer, as taught by Chen.

218. Since Gilmer teaches every other limitation of claim 1 of the '779 patent, as discussed above with reference to Ground II, the combination of Gilmer and Chen renders claim 1 obvious in my opinion. For this reason, and the reasons discussed above, it is my further opinion that the combination of Gilmer and Chen also renders obvious claims 12-13 of the '779 patent, which depend from claim 1.

## **XI. CONCLUSION**

219. For the aforementioned reasons, in my opinion, to a POSITA, the Challenged Claims of the '779 patent are anticipated and rendered obvious by the prior art.

220. I understand that the Patent Owner has not asserted secondary considerations of non-obviousness. I reserve the right to respond to any such assertions.

221. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the results of the proceedings.

Date: May 23, 2025

Respectfully submitted,



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Sanjay Banerjee, Ph.D.