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(54) **METHOD FOR SELECTIVELY FORMING STRAINED ETCH STOP LAYERS TO IMPROVE FET CHARGE CARRIER MOBILITY**

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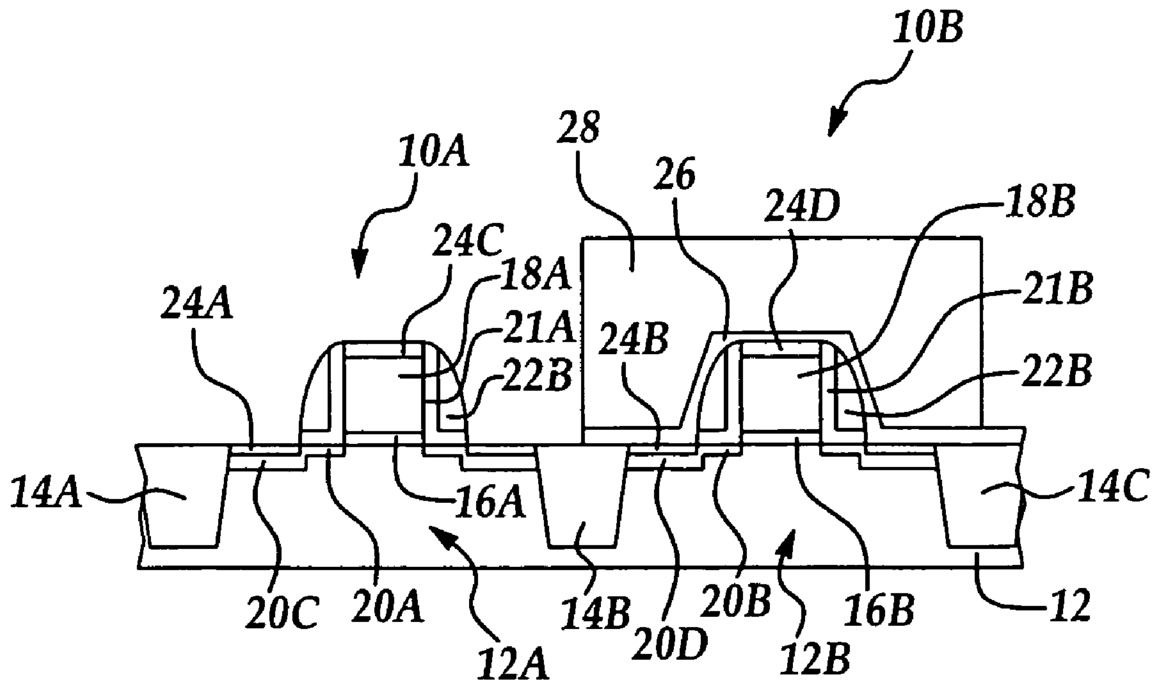
(57) **ABSTRACT**

A strained channel MOSFET device with improved charge carrier mobility and method for forming the same, the method including providing a first and second FET device having a respective first polarity and second polarity opposite the first polarity on a substrate; forming a strained layer having a stress selected from the group consisting of compressive and tensile on the first and second FET devices; and, removing a thickness portion of the strained layer over one of the first and second FET devices to improve charge carrier mobility.



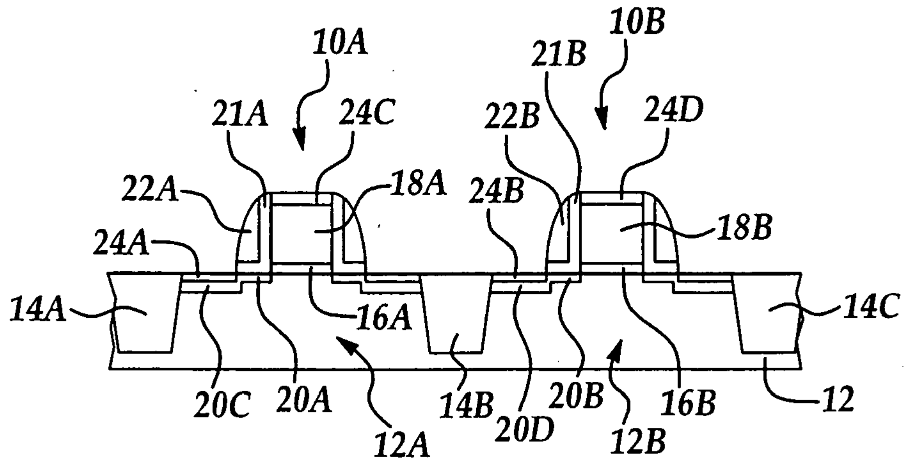


Figure 1A

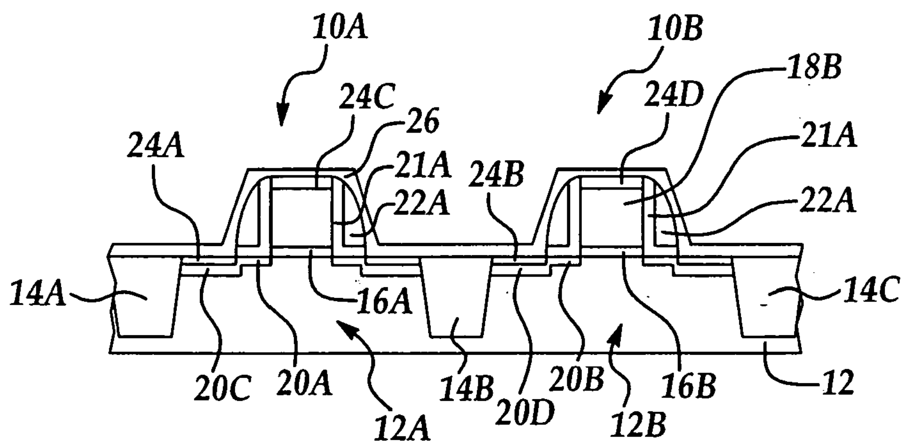


Figure 1B

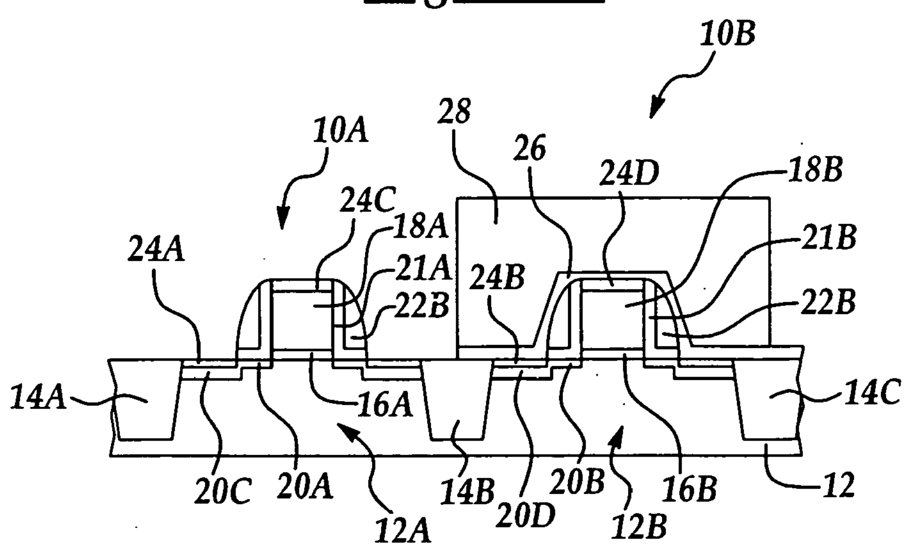


Figure 1C

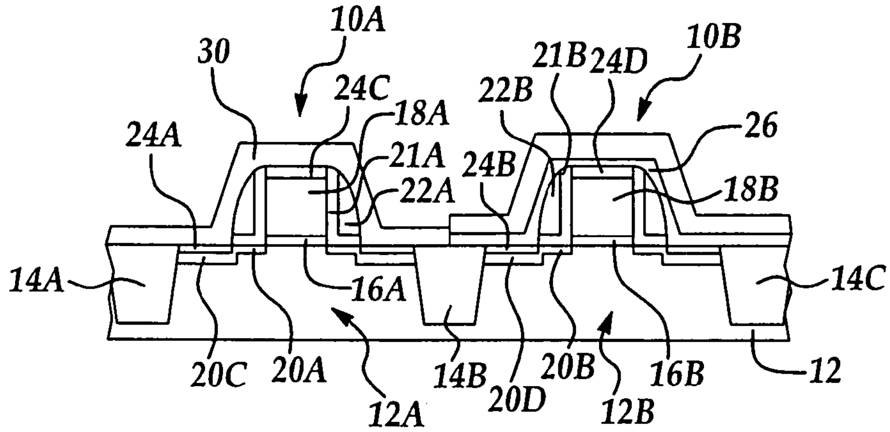


Figure 1D

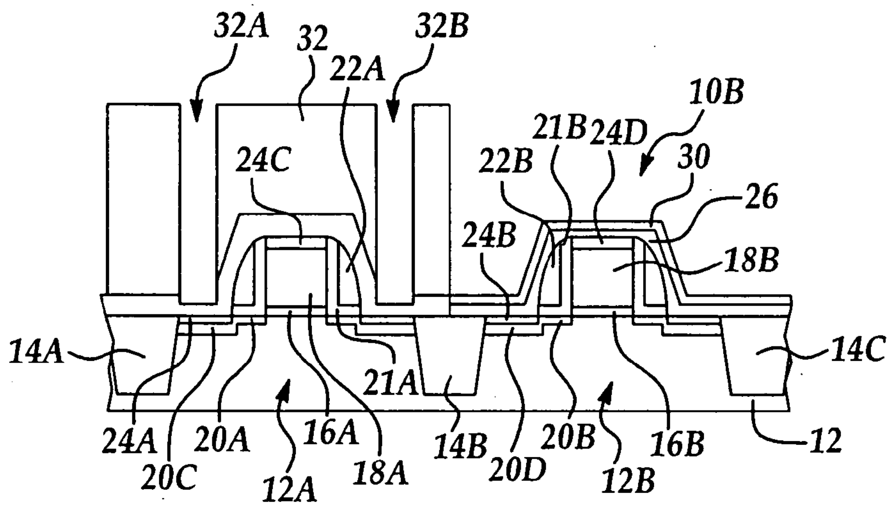


Figure 1E

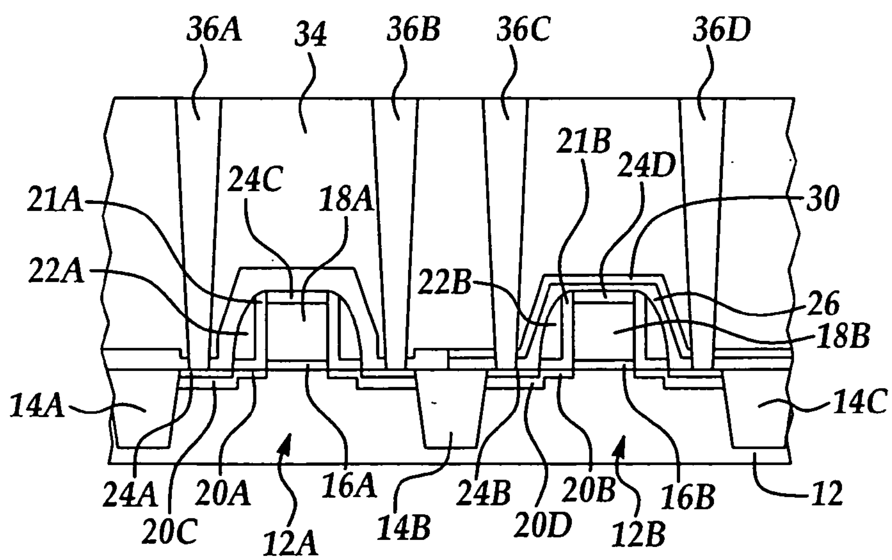


Figure 1F

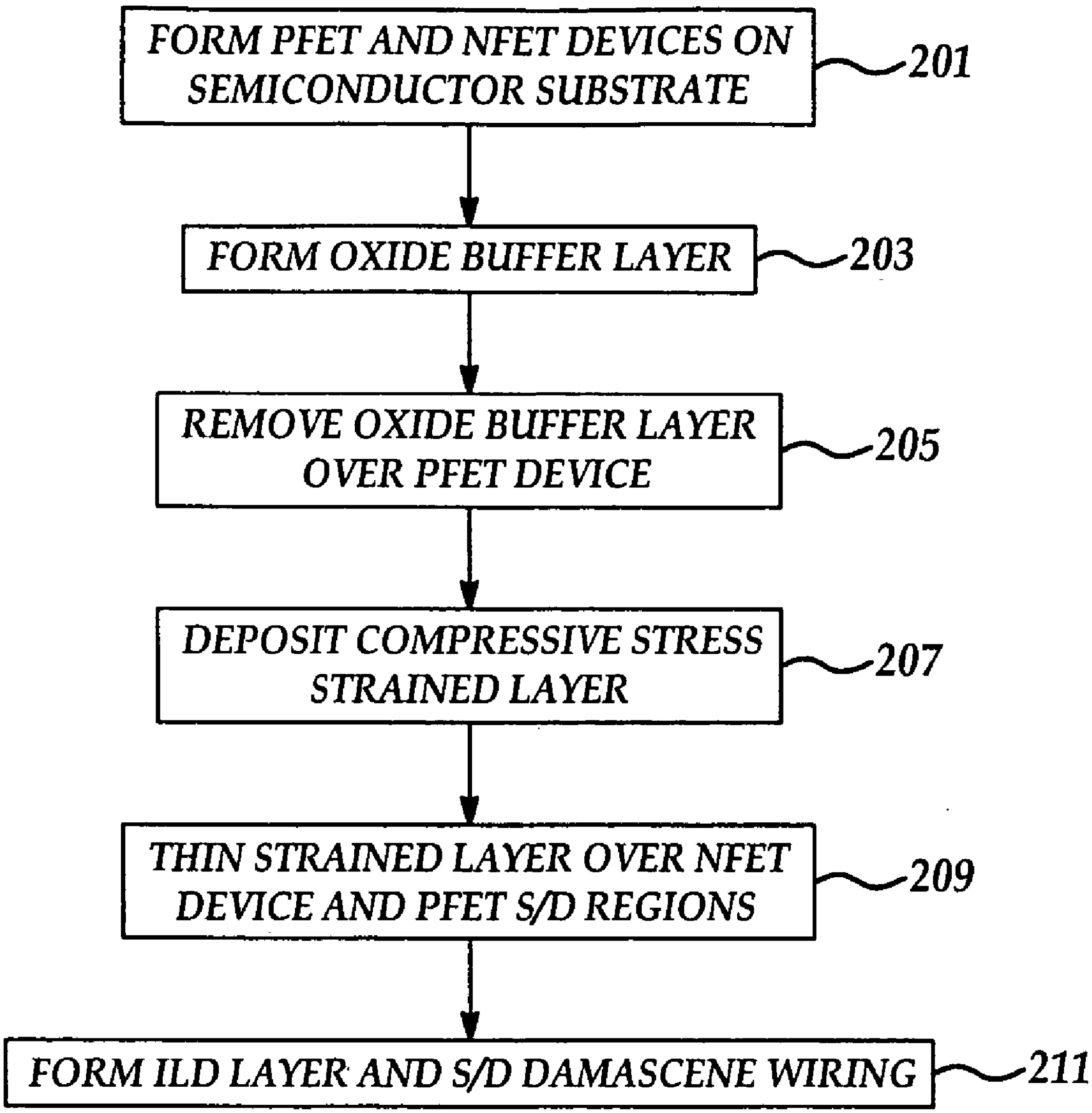

FORM PFET AND NFET DEVICES ON SEMICONDUCTOR SUBSTRATE
201
FORM OXIDE BUFFER LAYER
203
REMOVE OXIDE BUFFER LAYER OVER PFET DEVICE
205
DEPOSIT COMPRESSIVE STRESS STRAINED LAYER
207
THIN STRAINED LAYER OVER NFET DEVICE AND PFET S/D REGIONS
209
FORM ILD LAYER AND S/D DAMASCENE WIRING
211

Figure 2

METHOD FOR SELECTIVELY FORMING STRAINED ETCH STOP LAYERS TO IMPROVE FET CHARGE CARRIER MOBILITY

FIELD OF THE INVENTION

[0001] This invention generally relates to formation of MOSFET devices in integrated circuit manufacturing processes and more particularly to a method of selectively forming stressed (strained) contact etch stop layers over a MOSFET device to improve both electron and hole charge carrier mobility in respective NMOS and PMOS FET channel regions.

BACKGROUND OF THE INVENTION

[0002] Mechanical stresses are known to play a role in charge carrier mobility which affects Voltage threshold shifts. The effect of mechanical stresses to induce a strain on an FET channel region and thereby influence charge carrier mobility is believed to be due to complex physical processes related to acoustic and optical phonon scattering.

[0003] Generally, manufacturing processes are known to introduce strain into the MOSFET device channel region. For example, some strain (stress) is typically introduced into the channel region by formation of an overlying polysilicon gate structure and silicide formation processes. In addition, ion implantation and annealing processes following formation of the gate structure typically introduce additional stresses into the polysilicon gate structure which translate a strain into the underlying channel region altering device performance.

[0004] Prior art processes have attempted to introduce offsetting stresses into the channel region by forming stressed dielectric layers over the polysilicon gate structure following a silicide formation process. These approaches have met with limited success, however, since the formation of the stressed dielectric layer of a particular type of stress e.g., tensile or compressive, has a degrading electrical performance effect on a CMOS device formed to operate with an opposite type of majority charge carrier (e.g., NMOS vs. PMOS). For example, as NMOS device performance is improved, PNMOS device performance is degraded.

[0005] Other shortcomings in prior art approaches are the adverse affect of the dielectric stressed layers on subsequent gap filling ability of a subsequent inter-layer dielectric (ILD) layer deposition. For example, the thickness of the dielectric stress layer, and therefore the stress altering influence, is limited due to the formation of narrower gaps between devices, a limitation that will increase as device sizes and gap sizes between devices decreases. For example, increasing the dielectric layer stressed layer thickness over one device to increase a stress to improve a charge carrier mobility has the offsetting effect of degrading an opposite polarity FET device performance including drain current (I_{dsat}).

[0006] These and other shortcomings demonstrate a need in the semiconductor device integrated circuit manufacturing art for improved strained channel FET devices and methods for forming the same to selectively control an induced stress type and level to improve both NMOS and PMOS device performance and reliability.

[0007] It is therefore an object of the present invention to provide improved strained channel FET devices and methods for forming the same to selectively control an induced stress type and level to improve both NMOS and PMOS device performance and reliability, in addition to overcoming other shortcomings in the prior art.

SUMMARY OF THE INVENTION

[0008] To achieve the foregoing and other objects, and in accordance with the purposes of the present invention, as embodied and broadly described herein, the present invention provides a strained channel MOSFET device with improved charge carrier mobility and method for forming the same.

[0009] In a first embodiment, the method includes providing a first and second FET device having a respective first polarity and second polarity opposite the first polarity on a substrate; forming a strained layer having a stress selected from the group consisting of compressive and tensile on the first and second FET devices; and, removing a thickness portion of the strained layer over one of the first and second FET devices to improve charge carrier mobility.

[0010] These and other embodiments, aspects and features of the invention will be better understood from a detailed description of the preferred embodiments of the invention which are further described below in conjunction with the accompanying Figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] **FIGS. 1A-1F** are cross sectional schematic representations of exemplary portions of a MOSFET device pair including NMOS and PMOS portions formed at stages of manufacture according to an embodiment of the present invention.

[0012] **FIG. 2** is an exemplary process flow diagram including several embodiments of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0013] Although the method of the present invention is explained with reference to exemplary NMOS and PMOS MOSFET devices, it will be appreciated that the method of the present invention may be applied to the formation of any MOSFET device where a strain is controllably introduced into a charge carrier channel region by selective formation and subsequent removal of buffer layers and/or stressed dielectric layers overlying the respective NMOS and/or PMOS device regions.

[0014] Referring to **FIGS. 1A-1F** in an exemplary embodiment of the method of the present invention, are shown cross-sectional schematic views of a portion of a semiconductor wafer during stages in production of MOSFET structures including NMOS and PMOS devices **10**A and **10**B. For example, referring to **FIG. 1A**, is shown a semiconductor substrate **12**, which may include silicon, strained semiconductor, compound semiconductor, and multi-layered semiconductors, or combinations thereof. For example, the substrate **12** may include, but is not limited to, silicon on insulator (SOI), stacked SOI (SSOI), stacked SiGe on insulator (S—SiGeOI), SiGeOI, and GeOI, or combinations thereof. For example the substrate may include doped well regions **12**A and **12**B making up respective PMOS and NMOS device regions formed by conventional methods, for example a masking process followed by ion implantation and activation annealing. Electrical isolation regions, preferably (STI) structures e.g., **14**A, **14**B, and **14**C, back filled with an oxide dielectric, for example TEOS oxide, are formed by conventional processes prior to forming the doped well regions.

[**0015**] Still referring to **FIG. 1A**, gate structures are formed by conventional processes including gate dielectric portions e.g., **16**A and **16**B and overlying gate electrode portions e.g., PMOS device gate electrode **18**A and NMOS device gate electrode **18**B. For example, gate dielectric layers and gate electrode layers are deposited by CVD processes followed by photolithographic patterning and plasma assisted etching (e.g., RIE) to form the respective PMOS and NMOS gate structures.

[**0016**] The gate dielectric portions e.g., **16**A and **16**B may be formed of silicon oxide, silicon oxynitride, silicon nitride, nitrogen doped silicon oxide, high-K dielectrics, or combinations thereof. The high-K dielectrics may include metal oxides, metal silicates, metal nitrides, transition metal-oxides, transition metal silicates, metal aluminates, and transition metal nitrides, or combinations thereof. The gate dielectric portions e.g., **16**A and **16**B may be formed by any process known in the art, e.g., thermal oxidation, nitridation, sputter deposition, or chemical vapor deposition. The physical thickness of the gate dielectric portions e.g., **16**A and **16**B may be in the range of 5 to 100 Angstroms. When using a high permittivity (high-K) gate dielectric, the dielectric constant is preferably greater than about 8. The high-K dielectric may be selected from a group comprising aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), hafnium oxynitride (HfON), hafnium silicate ($HfSiO_4$), zirconium oxide (ZrO_2), zirconium oxynitride (ZrON), zirconium silicate ($ZrSiO_2$), yttrium oxide (Y_2O_3), lanthanum oxide (La_2O_3), cerium oxide (CeO_2), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), or combinations thereof.

[**0017**] The gate electrode portions e.g., **18**A and **18**B may be formed of polysilicon, polysilicon-germanium, metals, metal silicides, metal nitrides, or conductive metal oxides. In a preferred embodiment, the gate electrodes are formed of polysilicon. Metals and silicides thereof such as titanium, cobalt, nickel, molybdenum, tungsten, tantalum, platinum, and hafnium may be used in an upper portion of the gate electrodes e.g., **16**A, **16**B to form conductive contact regions.

[**0018**] Following formation of the gate electrodes, source/drain extension (SDE) regions e.g., **20**A and **20**B on either side of a channel region are formed by a conventional ion implant process adjacent the gate structures to a shallow depth e.g., (30 to 100 nm) beneath the silicon substrate surface according to a low energy ion implantation including forming pocket implant regions (not shown).

[**0019**] Still referring to **FIG. 1A**, sidewall spacers e.g., **22**A and **22**B, also referred to as offset spacers, are formed on either side of the gate structures and may include offset liners e.g., **21**A, **21**B lining the sidewalls of the gate structures by depositing one or more layers of silicon nitride (e.g., Si_3N_4), silicon oxynitride (e.g., SiON), and silicon oxide (e.g., SiO_2) e.g., to form oxide/nitride layers followed by etching away portions of the one or more layers to form self-aligned sidewall spacers and liners on either side of the gate structures.

[**0020**] Following sidewall spacer formation, the NMOS and PMOS device areas are sequentially doped according to a conventional high dose ion implantation (HDI) process to form the high density implant portions of doped source/drain (S/D) regions e.g., **20**C and **20**D in the substrate **12** adjacent the sidewall spacers. The gate electrodes **18**A and **18**B may be doped at the same time the HDI is carried out to lower a sheet resistance of the gate electrode material.

[**0021**] Still referring to **FIG. 1A**, silicide portions e.g., **24**A, **24**B, **24**C, and **24**D are optionally formed overlying the source and drain regions and the upper portion of the gate electrodes e.g., **18**A and **18**B. The silicide portions may be formed of $TiSi_2$, $CoSi_2$, and NiSi, PtSi or WSi_2 or combinations thereof by known processes.

[**0022**] Referring to **FIG. 1B**, according to an important aspect of the invention, a buffer oxide layer e.g., **26**, for example PECVD, or LPCVD oxide, e.g., TEOS oxide, having a thickness of from about 10 Angstroms to about 1000 Angstroms, more preferably less than about 200 Angstroms is formed to overlie both the NMOS and PMOS device regions.

[**0023**] Referring to **FIG. 1C**, following formation of the buffer oxide layer e.g., **26**, a resist patterning process is carried out to form resist portion **28** covering the PMOS region **12**B, including about half of the STI structure **14**B. A conventional wet and/or dry etching process is then carried out to remove the oxide buffer layer **26** portion overlying the uncovered PMOS region **12**B.

[**0024**] Referring to **FIG. 1D**, following removal of buffer oxide layer e.g., **26**, and removal of the photoresist portion **28**, in an important aspect of the invention, a stressed dielectric layer **30**, preferably a compressively stressed nitride in the embodiment shown, is blanket deposited over both the NMOS and PMOS regions to form an oxide/nitride bilayer over the NMOS region **12**B and a nitride layer over the PMOS device region. It will be appreciated that the term 'nitride' includes silicon nitride and/or silicon oxynitride.

[**0025**] For example, it has been found that a compressively stressed dielectric layer deposited directly over an NMOS device region substrate degrades electron mobility, while a compressively stressed dielectric layer deposited directly on a PMOS device regions (without intervening layers, e.g., buffer layers) enhances hole mobility. Thus, by retaining the buffer oxide layer **26** over the NMOS device region and removing the buffer oxide layer over the PMOS device region, a subsequently deposited compressively stressed dielectric layer e.g., **30** both enhances hole mobility as well as avoids degrading electron mobility, thereby simultaneously improving NMOS and PMOS device performance including a drain current (I_{dsat}) at a given applied Voltage. In addition, as shown below in another embodiment, the degrading effect of a compressive stress dielectric layer over an NMOS device or a tensile stress dielectric layer over a PMOS device may be further, or alternatively minimized, by selectively thinning the stressed dielectric layer e.g., **30** over a respectively charge carrier mobility degraded device e.g., thinning a tensile stress layer over a PMOS device region and thinning a compressive stress layer over a NMOS device region.

[0026] In the exemplary embodiment as shown, the stressed dielectric layer **30** is preferably a compressive stress nitride film, for example silicon nitride (e.g., SiN, Si_xN_y) and/or silicon oxynitride (e.g., Si_xON_y), more preferably silicon nitride, where the stoichiometric proportions x and y may be selected according to CVD process variables as are known in the art to achieve a desired stress in a deposited dielectric layer. Preferably the stressed dielectric layer **30** is formed by a CVD process for example, a low pressure chemical vapor deposition (LPCVD) process, an atomic layer CVD (ALCVD) process, or a plasma enhanced CVD (PECVD) process.

[0027] It will be appreciated that the level of stress can be varied by a number of factors including the thickness of the dielectric film, preferably being from about 50 Angstroms to about 1000 Angstroms in thickness. In addition, the relative reactant flow rates, deposition pressure, and temperature may be varied to vary a composition of the dielectric layer thereby controlling the level of stress. Preferably, the stressed dielectric layer **30** is deposited to a stress level of between about 200 MPa and about 2 GPa.

[0028] Conventional CVD precursors such as, silane (SiH_4), disilane (Si_2H_6) dichlorosilane (SiH_2Cl_2), hexacholorodisilane (Si_2Cl_6), BTBAS and the like, may be advantageously used in the CVD process to form the stressed nitride dielectric layer **30**. For example, a low temperature PECVD process for forming a compressive stress nitride layer may include supplying silane (SiH_4) and NH_3 gaseous precursors at a deposition temperature of from about 300° C. to about 700° C. carried out at pressures of from about 50 mTorr to about 5 Torr and RF powers of from about 100 Watts to about 3000 Watts. The RF power frequency is from about 50 KHz to about 13.56 MHz. It will be appreciated that compressive stress increases with increasing power and frequency of the RF power source.

[0029] Referring to **FIG. 1E**, in another embodiment, the stressed dielectric layer **30** is selectively thinned over the NMOS device region following stressed dielectric layer formation. For example, a resist patterning process is carried out to form patterned resist portions e.g., **32** covering PMOS device region **12**A portions including forming resist patterned openings e.g., **32**A, **32**B over the respective PMOS source and drain contact regions e.g., silicide portions **24**A, while leaving the NMOS device region **12**B uncovered. A conventional dry nitride etching process is then carried out to thin the exposed stressed nitride layer portions **30**, preferably by at least about 10 percent of the thickness of the nitride layer to reduce a stress level. For example, the stressed nitride layer is a deposited having a thickness of from about 10 Angstroms to about 1000 Angstroms, more preferably less than about 300 Angstroms. Thinning the stressed nitride layer **30** over the NMOS device reduces the level of compressive stress thereby further avoiding the electron carrier mobility degradation caused by the compressively stressed nitride layer on the NMOS channel region. Advantageously, the enhancement in hole mobility in the PMOS channel region is not affected as the compressive stress level remains about the same.

[0030] It will be appreciated that the stressed dielectric layer **30**, may be formed in tensile stress with the respective process steps shown in **FIGS. 1A through 1E** carried out with respect to devices of opposite polarity. For example, the stressed dielectric layer thinning process for a tensile stress dielectric layer formed over a PMOS device may be carried out to avoid degradation of hole charge carrier mobility. For example, a tensile stress dielectric layer (e.g., **30**) may be formed over the respective NMOS and PMOS devices with or without first forming an underlying oxide buffer layer **26** and which may or may not be removed over the NMOS device region prior to forming a tensile stress dielectric layer over both the NMOS and PMOS devices. It will be appreciated that in this embodiment, with reversed device polarity and stress type of the stressed dielectric layer (e.g., tensile), that the oxide buffer layer **26** need not be formed and removed over the NMOS device **12**B. Alternatively, the oxide buffer layer **26** may be formed over the PMOS device but not removed prior to forming a tensile stress dielectric layer over both the NMOS and PMOS devices followed by the thinning process.

[0031] Referring to **FIG. 1F**, following thinning of the stressed dielectric layer **30**, conventional subsequent processes are carried out to form integrated circuit wiring. For example, an overlying inter-layer dielectric (ILD) layer e.g., **34**, is formed by depositing a conventional oxide e.g., PECVD oxide, PETEOS, BPTEOS, BTEOS, PTEOS, TEOS, PEOX, low-K (K<2.9) dielectrics, and fluorinated silicate glass (e.g., FSG), or PSG, followed by a planarization step and conventional photolithographic patterning and etching process to form metal filled damascene contacts e.g., **36**A, **36**B, **36**C, and **36**D, for example tungsten filled damascenes, to form electric contact wiring to the source and drain regions e.g., salicide regions **24**A and **24**B.

[0032] Referring to **FIG. 2** is a process flow diagram including several embodiments of the present invention. In process **201**, a semiconductor substrate including respective PFET and NFET devices and device regions is provided. In process **203** a buffer oxide layer is formed over the respective gate structures and device regions. In process **205**, the buffer oxide layer is removed over the PFET device region. In process **207**, a strained compressive stress dielectric layer is formed over the respective device regions. In process **209**, the strained compressive stress dielectric layer is thinned over the NFET device region and S/D regions of the PFET device. In process **211**, an overlying ILD layer is formed and wiring damascene contacts formed to the respective FET device source and drain regions.

[0033] The preferred embodiments, aspects, and features of the invention having been described, it will be apparent to those skilled in the art that numerous variations, modifications, and substitutions may be made without departing from the spirit of the invention as disclosed and further claimed below.

What is claimed is:

1. A method for improving charge carrier mobility in a P and N type polarity strained channel MOSFET device pair comprising the steps of:

providing a first and second FET device having a respective first polarity and second polarity opposite the first polarity on a substrate;

forming a strained layer having a stress selected from the group consisting of compressive and tensile on the first and second FET devices; and, removing a thickness portion of the strained layer over one of the first and second FET devices to improve charge carrier mobility.

2. The method of claim 1, further comprising the step of forming a buffer oxide layer on the first and second FET devices prior to the step of forming a strained layer.

3. The method of claim 2, further comprising the step of removing the buffer oxide layer on one of the first and second FET devices.

4. The method of claim 3, wherein the buffer oxide layer is removed on the first polarity FET device having P-type polarity.

5. The method of claim 4, wherein the strained layer is formed in compressive stress.

6. The method of claim 1, wherein the step of removing comprises removing a thickness portion of the strained layer over respective source and drain regions comprising the first and second FET devices.

7. The method of claim 1, wherein the step of removing comprises removing a thickness portion of the strained layer formed in compressive stress over the second FET device having N-type polarity.

8. The method of claim 1, wherein the step of removing comprises removing a thickness portion of the strained layer formed in tensile stress over the first FET device having P-type polarity.

9. The method of claim 1, wherein the step of removing comprises removing greater than about 10 percent of the thickness of the strained layer.

10. The method of claim 1, further comprising the steps of:

forming a dielectric insulating layer on the strained layer; and,

forming metal damascenes through the dielectric insulating layer to contact the source and drain regions of the respective first and second FET devices.

11. The method of claim 1, wherein the step of removing comprises the steps of:

forming a patterned resist layer over the first and second FET devices; and,

dry etching the strained layer to remove the thickness portion.

12. The method of claim 1, wherein the strained layer consists essentially of silicon nitride.

13. The method of claim 1, wherein the strained layer is selected from the group consisting of silicon nitride and silicon oxynitride.

14. The method of claim 1, wherein the wherein the strained layer is formed having a stress level up to about 2 GPa.

15. The method of claim 1, wherein the strained layer is formed having a thickness from about 10 Angstroms to about 1000 Angstroms.

16. A method for improving charge carrier mobility in a P and N type conductivity strained channel MOSFET device pair comprising the steps of:

providing a first and second FET device having a respective first and second conductivity type on a substrate;

forming a buffer oxide layer on the second FET devices; and

forming a strained layer having primarily one of compressive stress and tensile stress over the first and second FET devices.

17. The method of claim 16, wherein the buffer oxide layer is removed on the first FET device having P-type polarity.

18. The method of claim 17, wherein the strained layer is formed in compressive stress.

19. A MOSFET device pair with improved strained channel charge carrier mobility comprising:

a first and second FET device having a respective first polarity and second polarity opposite the first polarity disposed on a substrate;

a strained layer having a stress selected from the group consisting of compressive and tensile over the first and second FET devices;

wherein the strained layer comprises respective first and second thickness portions over respective first and second FET devices the first thickness portion less than the second thickness portion.

20. The MOSFET device pair of claim 19, further comprising a buffer oxide layer on one of the first and second FET devices underlying the strained layer.

21. The MOSFET device pair of claim 19, wherein the buffer oxide layer is on the second FET device having N-type polarity.

22. The MOSFET device pair of claim 19, wherein the second FET device has a third strained layer thickness portion overlying respective source and drain regions about equal to the first thickness portion.

23. The MOSFET device pair of claim 19, wherein the first strained layer thickness portion is in compressive stress over the first FET device having N-type polarity.

24. The MOSFET device pair of claim 19, wherein the first strained layer thickness portion is in tensile stress over the first FET device having P-type polarity.

25. The MOSFET device pair of claim 19, wherein the first thickness portion is less than the second thickness portion by greater than about 10 percent.

26. The MOSFET device pair of claim 19, further comprising:

a dielectric insulating layer on the strained layer; and,

metal damascenes extending through the dielectric insulating layer to contact the source and drain regions of the respective first and second FET devices.

27. The MOSFET device pair of claim 19, wherein the strained layer consists essentially of silicon nitride.

28. The MOSFET device pair of claim 19, wherein the strained layer is selected from the group consisting of silicon nitride and silicon oxynitride.

29. The MOSFET device pair of claim 19, wherein the wherein the strained layer has a stress level up to about 2 GPa.

30. The MOSFET device pair of claim 19, wherein the strained layer has a thickness from about 10 Angstroms to about 1000 Angstroms.

31. A MOSFET device pair having respective P and N type conductivity with improved strained channel charge carrier mobility comprising:

a first and second FET device having a respective first and second conductivity type on a substrate;

a buffer oxide layer on one of the first and second FET devices; and

a strained layer having primarily one of compressive stress and tensile stress over the first and second FET devices.

32. The MOSFET device pair of claim 31, wherein the buffer oxide layer is on the second FET device having N-type polarity.

33. The MOSFET device pair of claim 31, wherein the strained layer has primarily compressive stress.

34. The MOSFET device pair of claim 31, wherein the second FET device has a third strained layer thickness portion overlying respective source and drain regions about equal to the first thickness portion.

35. The MOSFET device pair of claim 31, wherein the first strained layer thickness portion is in compressive stress over the first FET device having N-type polarity.

36. The MOSFET device pair of claim 31, wherein the first strained layer thickness portion is in tensile stress over the first FET device having P-type polarity.

37. The MOSFET device pair of claim 31, wherein the first thickness portion is less than the second thickness portion by greater than about 10 percent.

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