

An Adjustable Work Function Technology Using Mo Gate for CMOS Devices

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Abstract—Nitrogen implantation of Mo gate was used to fabricate MOS capacitors and CMOS transistors. Initial studies demonstrate that the work function of Mo is sensitive to nitrogen implantation energy. Mo with (110) orientation exhibits a high work function, making it suitable for bulk p-MOSFET gate electrodes. Nitrogen implantation can be used to lower the Mo work function, making it suitable for n-MOSFET gate electrodes. A gate work function reduction of 0.42 eV was achieved for the n-FETs on CMOS wafers. With further optimization, this single metal gate technology may potentially replace conventional poly-Si gate technology for CMOS and can also be used for multiple- V_T technologies.

Index Terms—CMOS, gate implantation, metal gate, molybdenum, MOSFET, work function.

I. INTRODUCTION

AS CMOS devices are scaled beyond the 100-nm node, stringent performance targets will require the integration of metal gate electrode as well as high-k gate dielectrics. The conventional poly-Si gate technology is limited by the well-known gate depletion effect, which reduces drive current. The gate depletion region adds 3–5 Å to the effective oxide thickness (EOT) of the gate dielectric, exacerbating the challenge of achieving sub-10 Å EOT [1]. In addition, high resistivity and thermal instability with high-k dielectrics also limit the scalability of poly-Si gate technology [2].

A metal gate technology can overcome these issues provided the appropriate gate work functions can be achieved. In order to maintain good short-channel performance and proper threshold voltages, the gate work functions of the n-FETs and p-FETs must be close to those of n+ and p+ doped poly-Si for bulk-Si CMOS devices and within ± 0.2 eV of Si mid-gap in novel structures such as double-gate MOSFETs [3]. A gate-first CMOS process using two different metal gate materials has previously been demonstrated [4]. However, the dual-metal gate approach relies on a single reactive ion etching (RIE) process to simultaneously pattern dissimilar gate metals, with high selectivity to the ultrathin gate dielectric. Clearly, a more robust process would be one that uses a single metal gate material for both n- and p-FET devices while still enabling separate work function

control. The implementation of this single metal gate concept requires a viable gate work function adjustment technique.

Molybdenum (Mo) has very low resistivity ($5 \times 10^{-6} \Omega\text{-cm}$) and high melting point ($>2600^\circ\text{C}$), and thin films of Mo with (110) crystallographic texture have been shown to exhibit work functions close to 5 eV on several candidate dielectrics [5]. It has also been reported that the work function of Mo can be significantly reduced by high-dose nitrogen implantation [6], similar to an earlier report using TiN gate [7]. These observations suggest that Mo is a potential candidate for a *single-metal dual-work function* technology provided that a sufficient and stable work function shift can be obtained. In this study, the process window for nitrogen implantation of Mo was characterized, and CMOS transistors were fabricated to demonstrate the feasibility of a tunable work function single metal gate CMOS technology.

II. DEVICE FABRICATION

In order to characterize the correlation between work function and the nitrogen implantation energy, MOS capacitors with Mo gate electrodes (650 Å) and various dielectric (SiO_2) thickness were fabricated with ^{14}N implant energies, E_{Imp} , ranging from 15 keV to 45 keV. A fixed nitrogen implant dose of $5 \times 10^{15} \text{ cm}^{-2}$ was used on all samples. Work function of the gate electrode was extracted using a quantum $C-V$ simulator and the $V_{FB}-t_{OX}$ method [6], [8], which excludes the effect of fixed charge. The theoretical projected ranges, R_P , as simulated by SRIM (IBM), are summarized in Table I along with the respective experimental MOS work function shift $\Delta\Phi_m$ obtained (as compared to the unimplanted samples). A positive correlation between E_{Imp} and $\Delta\Phi_m$ was observed. As expected, beyond an implant energy threshold, excessive damage to the gate dielectric resulted in nonyielding devices. These results suggested that implant energies between 20 and 30 keV would be appropriate for subsequent fabrication of CMOS transistors.

An n-well CMOS process with LOCOS isolation was used. Gate SiO_2 deposition was followed by sputter deposition of 650 Å Mo. The p-FETs were then masked with photoresist while n-FET gates received a nitrogen implant (dose $5 \times 10^{15} \text{ cm}^{-2}$, energy 29 keV). The Mo film was then capped with *in-situ* doped n+ LPCVD poly-Si (1000 Å). After gate lithography, the gate stack was etched in two steps. Poly-Si was etched with a Cl_2 -based RIE, while Mo was etched using a $\text{Cl}_2\text{-O}_2$ based RIE. In comparison to previously reported CF_4 RIE of Mo [5], the $\text{Cl}_2\text{-O}_2$ chemistry provides a higher etch rate and improved SiO_2 selectivity, both of which can be tuned via the Cl_2/O_2 flow ratio. The source/drain regions were subsequently formed by

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TABLE I
SHIFT IN Mo WORK FUNCTION AFTER NITROGEN IMPLANTATION AND 700 °C
10 MIN RTA, MEASURED ON SiO₂ MOS CAPACITORS. FOR 35 keV AND 45
keV IMPLANTED NON-YIELDING DEVICES, MOS C-V CURVES WERE
DISTORTED, INDICATING GATE OXIDE DAMAGE

Implantation energy E_{imp} (keV)	Projected R_p (Å)	Straggle (Å)	$\Delta\Phi_m$ (eV)
15	205	112	0.26
22	279	148	0.40
29	353	180	0.56
35	415	209	Non-yielding
45	500	232	Non-yielding

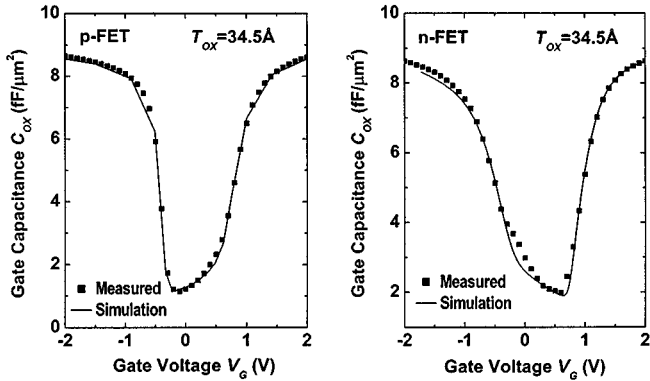


Fig. 1. Typical high-frequency $C-V$ curves of p-FET (left), with unimplanted Mo gate electrode, and n-FET (right), with nitrogen implanted Mo gate electrode measured from $W/L = 50 \mu\text{m}/50 \mu\text{m}$ MOSFETs on the same wafer. $C-V$ curves measured at 100 kHz and 20 kHz showed negligible shift or distortion. The work function of the p-FET gate is 4.95 eV, and that of the n-FET gate is 4.53 eV, as extracted by a quantum $C-V$ simulator. The good agreement between real data and simulation suggests good interface quality of the gate oxide.

¹¹B and ³¹P implantation for p-FET and n-FET respectively, followed by N₂ furnace annealing at 800 °C for 30 min. After LTO passivation and Al metallization, forming gas anneal was performed at 400 °C for 30 min.

III. RESULTS AND DISCUSSION

Fig. 1 shows the $C-V$ characteristics of n-FETs and p-FETs and the best fitting quantum $C-V$ simulations [8]. The measured $C-V$ curves agree very well with the theoretical results. Both n-FET and p-FET curves showed the same gate oxide thickness of 34.5 Å. In contrast, for a dual-metal gate process it was previously reported that the n-FET and p-FET gate dielectric EOTs are different, due to the etching of dissimilar metal gates [4]. Mo shows a work function of 4.95 eV for the p-FETs, and a work function of 4.53 eV for the n-FETs. After a full CMOS process, the gate work function of the p-FET is close to the desired value, while that of the n-FET is ~ 0.5 eV higher than desired. Although the work function shift demonstrated here is insufficient for bulk CMOS devices, it is acceptable for ultra-thin body MOSFET devices in which the channel is undoped [3]. Since the n-FET and p-FET work function measurements were made on the same wafer, the relative shift in work function can be attributed to nitrogen implantation, rather than any other common factors. The $I_{DS}-V_{DS}$ and $I_{DS}-V_{GS}$ curves of the n-FETs and p-FETs are shown in Fig. 2. Normal transistor

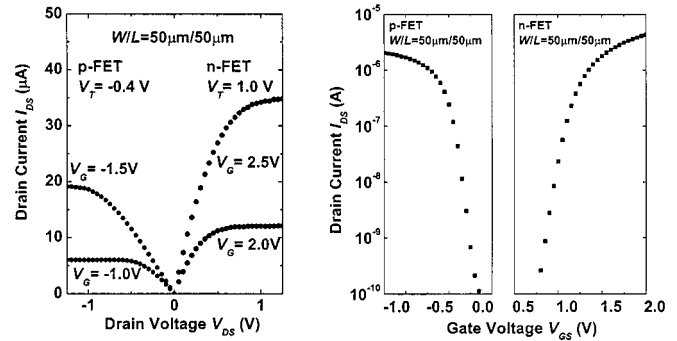


Fig. 2. (Left) $I_{DS}-V_{DS}$ and (right) $I_{DS}-V_{GS}$ curves of p-FET and n-FET on the same CMOS wafer, with unimplanted and nitrogen-implanted Mo gate electrodes, respectively. Normal transistor characteristics are observed on both p-FETs and n-FETs. The subthreshold swing of p-FET (87 mV/dec) and n-FET (91 mV/dec) are comparable, indicating that the nitrogen implantation into the n-FET gate did not seriously degrade the gate oxide interface.

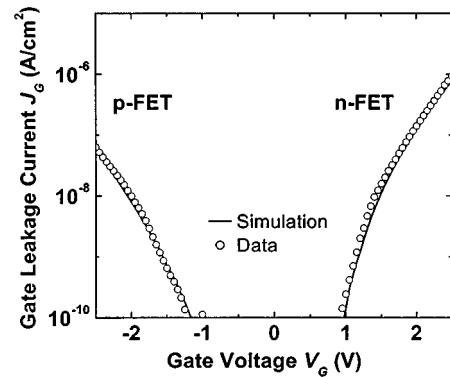


Fig. 3. Gate leakage current of n-FET and p-FET are very close to the results simulated by a SiO₂ gate tunneling current model, indicating possible damage to the gate oxide by metal sputtering or nitrogen implantation (for n-FET) is not significant.

characteristics indicate that Mo is a viable MOSFET gate material, and that nitrogen implantation can be used to adjust the Mo gate work function in a controllable way without degrading transistor performance. High-energy nitrogen implants into the gate could potentially damage the gate oxide. Since gate oxide damage usually results in increased gate leakage current, the I_G-V_G curves of n-FETs and p-FETs were investigated in order to evaluate the gate oxide integrity. As shown in Fig. 3, the measured gate leakage data of both p-FET and n-FET are very comparable to the SiO₂ leakage current simulated by an empirical model whose accuracy has been verified by extensive data [9], with all device parameters being the same as in the real devices. This indicates that the gate oxide damage from nitrogen implantation is insignificant in this case. Nevertheless, a comprehensive study of the reliability of this technology is necessary.

It is difficult to attribute the work function lowering to a single structural or chemical change in the Mo film. Nitrogen concentration in the film is $\sim 0.1-0.2\%$ atomic, roughly the dose divided by the film thickness. However, nitrogen implantation into Mo gate followed by high-temperature annealing has been observed to produce significant segregation of N at the Mo/SiO₂ interface [10]. X-Ray diffraction studies also reveal substantial amorphization of the Mo film after implantation, and a significant recrystallization upon subsequent thermal processing [10].

It is known that metal work functions depend on bulk and surface material properties, crystalline orientation, and the permittivity of the dielectric interfacing with the metal [11]–[13]. Work function engineering is thus an emerging critical requirement for future CMOS technology. The compatibility of Mo with several high-k dielectrics has been studied in the past [5], indicating the applicability of Mo as p-FET gate electrode. With the simple technique of nitrogen implantation to lower its work function, Mo may also be suitable for use as an n-FET gate electrode. It will however be necessary to control the microstructure of deposited Mo film and any postgate thermal processing that could alter the interface and the microstructure of the Mo film.

IV. CONCLUSION

CMOS devices were fabricated using Mo as the single gate electrode material. Mo (110) exhibits a high work function that is suitable for bulk p-FETs, and this value can be lowered for n-FETs with nitrogen implantation. With further optimization, this technology can potentially be used to achieve dual gate work functions for CMOS devices. In multiple V_T technologies optimized for performance and power, this gate work function adjustment technique provides another flexible approach to implementing multiple threshold voltage CMOS circuits.

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