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Metal Gate MOSFETs with HfO_2 Gate Dielectric

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Abstract

We report for the first time electrical characterization of HfO_2 p- and n-MOSFETs with CVD TiN and PVD TaSiN gates respectively fabricated using conventional CMOS integration. Their performance is compared to PVD TiN-gated HfO_2 and SiO_2 n- and p-MOSFETs. To understand the issues with metal gates on high K gate dielectrics, PVD TiN MOSFETs were extensively characterized. At 10nA/µm leakage, 0.345mA/µm drive current was obtained from PVD TiN/HfO_2 p-MOSFETs. HfO_2 n-MOSFETs with metal gates show about 10^4 times reduction in gate leakage compared to poly/SiO_2 devices.

Introduction

The decrease in the inversion capacitance due to depletion in polysilicon (poly) gates will be significant as the gate dielectric is scaled below 10Å equivalent oxide thickness (EOT). Metal gates will eliminate gate depletion and address other issues like boron penetration and increased gate resistance, which will be aggravated as the poly gate thickness is scaled down. Extensive simulations have shown that the optimal gate work-function for sub-50 nm gate lengths is 0.2 eV below (above) the conduction (valence) band edge of silicon for NMOS (PMOS) [1]. Recently, PVD Ta_xSi_yN (TaSiN) has been reported to be an NMOS-compatible metal gate [2,3]. CVD TiN on HfO_2 has a work-function of 4.8eV, suitable for a PMOS gate. We report for the first time electrical characterization of HfO_2 n-MOSFETs with PVD TaSiN gates and p-MOSFETs with CVD TiN gates. PVD TiN-gated HfO_2 and SiO_2 n- and p-MOSFETs were used for comparison and understanding the difference between metal gates on SiO_2 versus HfO_2.

Experiment

Metal gate MOSFETs were processed using a 0.13µm CMOS technology [4]. The HfO_2 gate dielectric was deposited by MOCVD at 550°C. PVD TaSiN and PVD TiN gates were reactively sputtered. CVD TiN was deposited using Tetrakis-dimethylamino-titanium at 450° C. SiO_2 devices with PVD TiN gates were used as controls.

Results and Discussion

A. Work-function and thermal stability

TEM studies (Fig. 1) indicate that PVD TaSiN films on HfO_2 remain amorphous after a high temperature anneal unlike TiN (PVD and CVD) gates. The absence of grain boundary diffusion minimizes reaction at the TaSiN/HfO_2 interface. However, post-gate annealing increases the CETacc (capacitance equivalent thickness under accumulation) of TaSiN/HfO_2 MOSCAPs more than PVD or CVD TiN/HfO_2 (Fig. 2). The work-functions of PVD TaSiN and CVD TiN on HfO_2 were determined to be 4.4eV and 4.8eV which makes them suitable candidates for NMOS and PMOS respectively. Post-gate annealing can change the Vfb, fixed charge and work-function in metal-gated HfO_2 devices.

B. Transistor characterization

Figs. 3 and 4 show typical high frequency CVs from HfO_2 p- and n-MOSFETs with different metal gates. Note the absence of gate depletion (Cinv/Cacc~1) as expected. The kink in the TaSiN/HfO_2 devices is suggestive of the interface defect state recently identified in HfO_2 MOSCAPs [5]. Fig. 5 shows well-behaved Id-Vd characteristics of 10µm x 10µm (W/L) HfO_2 p- and n-MOSFETs with CVD TiN and TaSiN gates respectively. Fig. 6 shows the sub-threshold characteristics of long channel n- and p-MOSFETs with different metal gates. PVD and CVD TiN-gated devices show excellent sub-threshold swings of ~70mV/dec. The poor sub-threshold behavior of TaSiN/HfO_2 n-MOSFETs suggests a high interface state density consistent with the existence of a kink in CVs (Fig. 4).

Fig. 7 shows HfO_2 PMOS Ion/Ioff characteristics with a PVD TiN gate. At 10nA/µm leakage, drive current is 0.375mA/µm. Short-channel n-MOSFETs with metal gates has a steep Vt roll-off and hence degraded Ion/Ioff characteristics at 10nA/µm leakage. Controlling Vt roll-off at sub-90nm gate lengths when metal gate work-functions are displaced from the band-edges requires optimization of channel and halo doping and thermal budget. Fig. 8 shows nmos and pmos linear Gm normalized to Vt and CETinv (capacitance equivalent thickness under inversion) to compare electron and hole mobilities. The peak electron (hole) mobility for HfO_2 devices is 39%-48% (27%-48%) lower compared to SiO_2 devices at comparable channel doping.

C. Gate leakage and reliability

Fig. 9 shows the gate leakage in n-MOSFETs at Vt+1V as a function of CETinv. PVD TiN and TaSiN-gated HfO_2 devices show about 10^4X reduction in gate leakage compared to poly/SiO_2 devices at comparable inversion capacitance. Fig. 10 shows a similar plot for PMOS. Higher charge pumping current in HfO_2 devices compared to SiO_2 devices with PVD TiN gates suggests ~4X higher interface trap density (Fig. 11). Fig. 12 shows variation in Vt and Gm with time under 7.6 MV/cm (Vg=-1.3V, CETinv~17Å) stressing in PVD TiN/HfO_2 p-MOSFETs. A -100mV shift in Vt and peak Gm was observed due to charge trapping after 100s, which remains unchanged up to 1000s. Fig. 13 shows 105° C TDDB (time-dependent dielectric breakdown) data from PVD TiN/HfO_2 p-MOSFETs suggesting that these devices are capable of reasonably high operating voltages to meet a 10-year lifetime criterion.

Conclusion

We have successfully fabricated and characterized HfO_2 n-MOSFETs with TaSiN and PVD TiN gates and p-MOSFETs with CVD and PVD TiN gates using a conventional CMOS process. Metal-gated HfO_2 n-MOSFETs show a 10^4X gate leakage reduction compared to poly/SiO_2 devices. Reasonable Ion/Ioff performance and reliability were observed in PVD TiN/HfO_2 PMOS. CET and work-function variation with thermal budget, mobility degradation, Vt roll-off control and charge trapping are key issues that need to be addressed with metal gates on high-K gate dielectrics. Identification of optimum metal gate materials and processes requires further study.

References

[1] B. Cheng et al. *2001 IEEE Intl. SOI Symp. Proc.*, pp. 91-92, 2001.
[2] Y-S. Suh et al. *VLSI Tech Digest*, pp. 47-48, 2001.
[3] D-G. Park et al. *IEDM Tech Digest*, pp. 671-74, 2001.
[4] A. H. Perera et al. IEDM Tech Digest, pp. 571-74, 2000.
[5] S. Mudanai et al. Unpublished, 2001.

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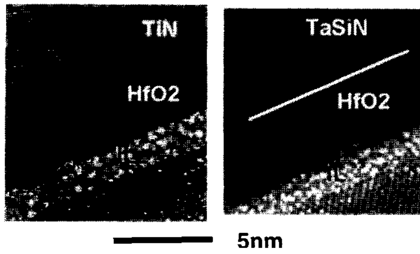

Fig. 1 Cross-section TEM images of TiN/HfO_2 and $TaSiN/HfO_2$ films after a 900° C/60s anneal showing TaSiN remains amorphous. (IL=interfacial layer)

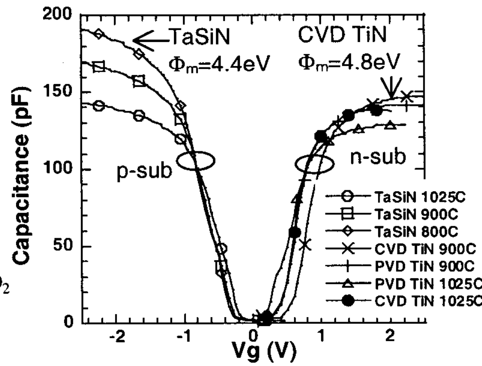

Fig. 2. CVs of n- and p-substrate HfO_2 capacitors with different metal gates and post-gate anneal temperatures. (area=1E-4 cm^2)

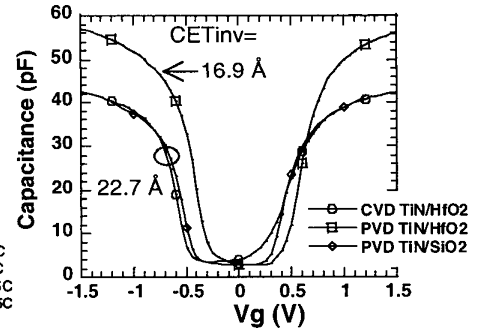

Fig. 3 High frequency CV characteristics of HfO_2 p-MOSFETs with different metal gates.

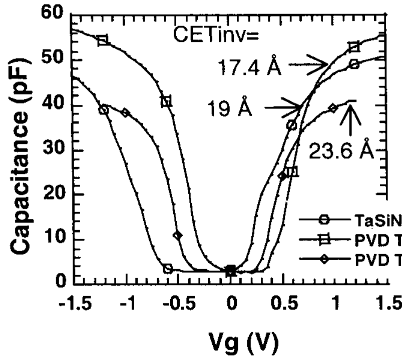

Fig. 4 High frequency CV characteristics of HfO_2 n-MOSFETs with different metal gates. (area=2.8E-5 cm^2 in Figs. 3 and 4)

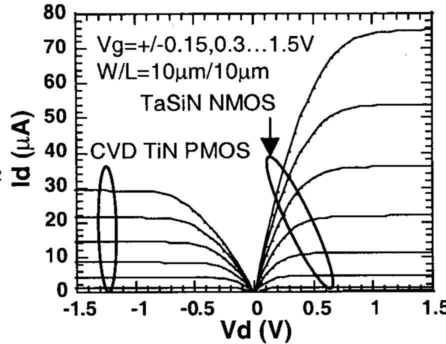

Fig. 5 Id-Vd characteristics of HfO_2 (p) n-MOSFET with (CVD TiN) TaSiN gate.

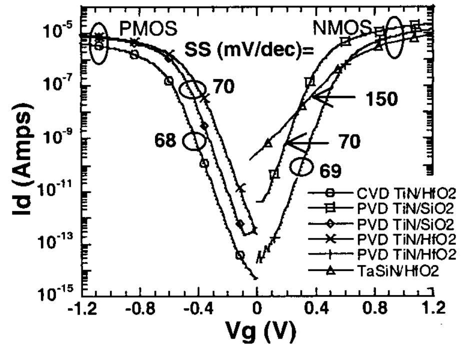

Fig. 6 Sub-threshold characteristics of 10μmx10μm (W/L) HfO_2 n and p-MOSFETs with metal gates.

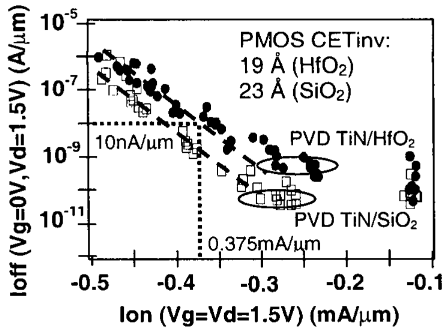

Fig. 7 PMOS Ion/Ioff data comparing HfO_2 and SiO_2 with PVD TiN gate.

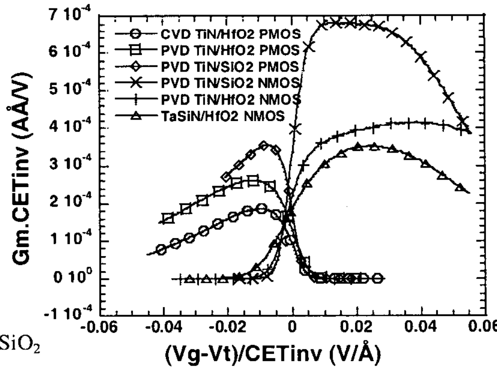

Fig. 8 PMOS and NMOS linear Gm normalized to CETinv and Vt

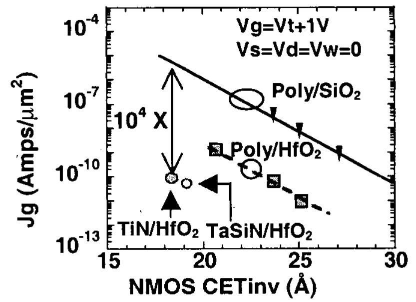

Fig. 9 NMOS gate leakage as a function of CETinv

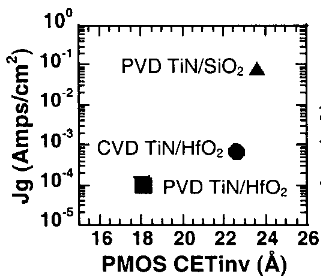

Fig.10 PMOS gate leakage as a function of CETinv.

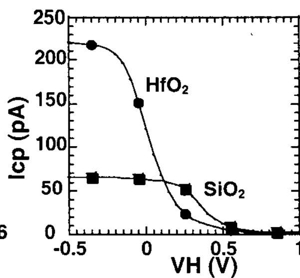

Fig. 11 Charge pumping current from SiO_2 and HfO_2 p-MOSFETs with PVD TiN gates. The current is proportional to interface trap density.

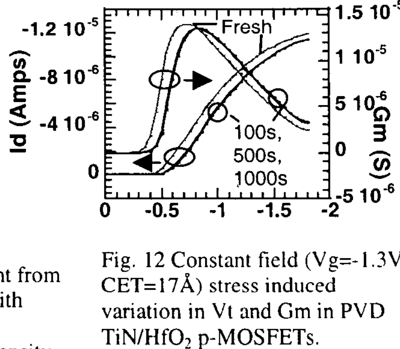

Fig. 12 Constant field (Vg=-1.3V, CET=17Å) stress induced variation in Vt and Gm in PVD TiN/HfO_2 p-MOSFETs.

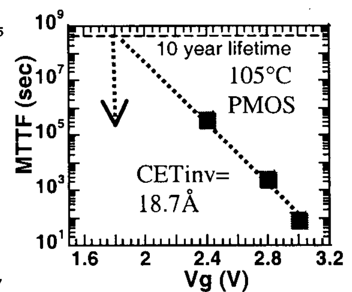

Fig. 13 TDDB data from PVD TiN/HfO_2 p-MOSFETs.

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