

## EXHIBIT 779A1

### Invalidity of U.S. Patent No. 8,796,779 in View of U.S. Patent Publication No. US 2005/0014352 to Torii et al.

U.S. Patent Publication No. US 2005/0014352 to Torii et al. (“Torii”) was filed as Application No. 10/889,100 on July 13, 2004 and published on January 20, 2005 as demonstrated by at least the document itself, the records of the United States Patent and Trademark Office, and/or the testimony of knowledgeable witnesses and corroborating documents. Torii is therefore prior art to the ’779 Patent under at least 35 U.S.C. § 102(a), (b), and/or (e) as discussed in greater detail in the chart that follows.<sup>1</sup>

To the extent that AICP alleges that Torii does not disclose any particular limitation of claims 1, 2, 7, 12, and 13 (the “Asserted Claims”) of the ’779 Patent, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the priority date of the ’779 Patent to modify Torii and/or combine the teachings of Torii with other prior art references, including but not limited to, the other prior art references in Exhibits 779A1–A2 and 779B, and the relevant sections of the charts for other prior art to the ’779 Patent in a manner that would have rendered the Asserted Claim invalid as obvious.

Defendants reserve the right to amend or supplement this claim chart at a later date as more fully set forth in the Preliminary Invalidation Contentions. The cited portions of the prior art references are merely illustrative, and Defendants reserve the right to rely on alternative or additional evidence, including uncited portions of the prior art references.

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<sup>1</sup> These preliminary invalidity charts, in some instances, rely, at least in part, on AICP’s apparent positions regarding the scope of its claims for purposes of asserting infringement. Defendants’ assertion that a particular limitation is disclosed by a prior art reference, or Defendants’ assertion that a particular limitation is disclosed by a prior art reference in a particular manner, may be based in part on AICP’s apparent claim interpretations. In relying in part on AICP’s apparent claim interpretations, Defendants do not admit that AICP’s apparent claim interpretations are supportable or proper or that the claim limitations in question are definite or otherwise amenable to construction. Nor do Defendants admit that the claims are enabled, adequately described, or cover patentable subject matter, or that any of the Accused Instrumentalities infringe any claim of the Asserted Patents. Nor shall anything stated herein be construed as an admission or waiver of any particular construction of any claim term, or argument under 35 U.S.C. § 112. Nothing in these claim charts should be understood as an admission relating to infringement, either literally or under the doctrine of equivalents, or as an admission relating to the Defendants’ understanding of the proper interpretation or scope of the Asserted Claim. Moreover, Defendants reserve the right to rely on additional citations or sources of evidence that may also be applicable, or that may become applicable in light of any Court order on claim construction, changes in AICP’s Preliminary Invalidation Contentions, or information obtained during discovery as the case proceeds.

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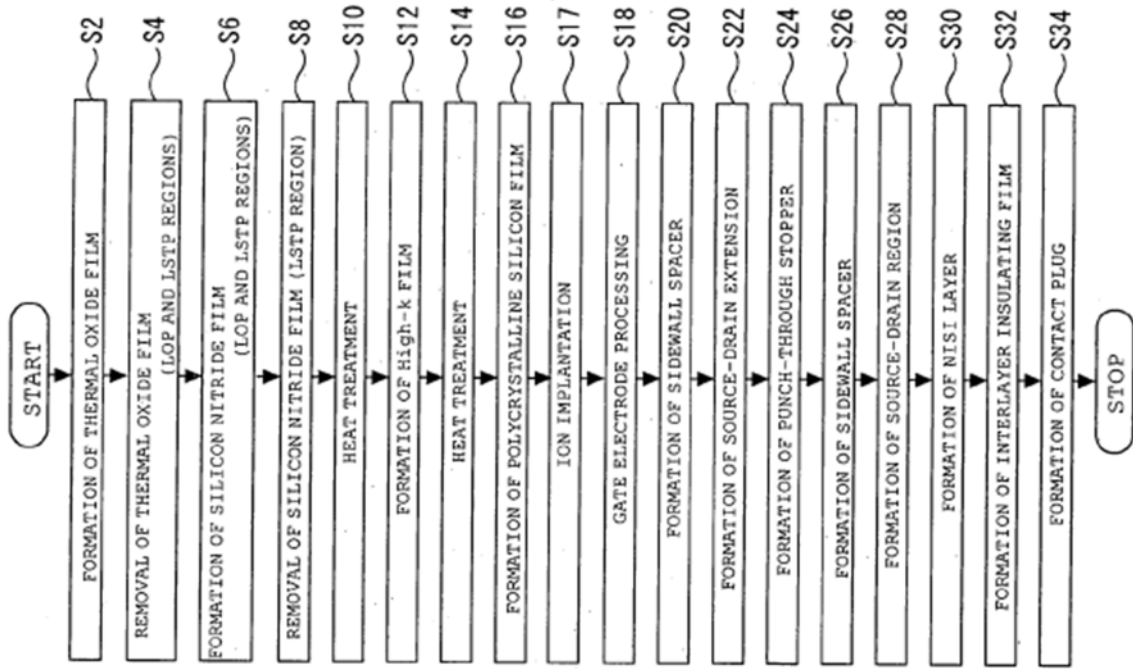
Where the chart below states that the reference “discloses” or “describes” or “teaches” a limitation, such disclosure may be express, inherent, or implicit. Unless otherwise indicated, all citations to other claim charts in the discussion of claim elements below refer specifically to the corresponding claim element of the other claim chart.

Claim	Claim Language	Exemplary Disclosures in Torii
1 [pre]	A semiconductor device comprising:	<p>Torii, as evidenced by the example citations below, discloses a semiconductor device.</p> <p>[0002] The present invention relates to a semiconductor device and a method for manufacturing a semiconductor device. More specifically, the present invention relates to a semiconductor device having a plurality of transistors comprising gate insulating films of different film thickness, and a method for manufacturing such a semiconductor device.</p> <p>[0010] With the miniaturization of semiconductor devices in recent years, the further reduction of the thickness of gate insulating films has been demanded. However, in the case when a silicon oxide film is used as a gate insulating film, if the thickness thereof is 2 nm or less, leak current increases resulting in the increase of power consumption. Since such a thin silicon oxide film is formed of several atomic layers, it is difficult to form evenly, and since a strict manufacturing control is required to improve the uniformity of film thickness, mass production becomes difficult.</p> <p>[0011] Therefore, in order to produce finer elements and reduce power consumption, the use of a high-dielectric constant film (hereafter referred to as high-k film) as a gate insulating film has been studied. The high-k film can be formed thicker than the silicon oxide film, while maintaining the effective film thickness that determines the transistor current sufficiently thin, and can inhibit the increase of power consumption.</p> <p>[0012] As such an SoC, there has been proposed a semiconductor device that uses a high-k film as the gate insulating film of an MISFET (metal insulator semiconductor field effect transistor) for the logic circuit, and a thick silicon oxide film and a high-k film as the gate insulating film for the peripheral circuit. When this semiconductor device is formed, a silicon oxide film is first formed on the entire surface of a substrate using an ordinary method. Thereafter, the silicon oxide film in the region for forming the MISFET for the logic circuit is removed, and then, a high-k film is formed on the entire surface using a CVD method or the like. Thereby, the gate insulating films having different thickness between the peripheral circuit side and the logic circuit side can be formed (for example, refer to Japanese Patent Laid Open No. 2002-164439).</p>

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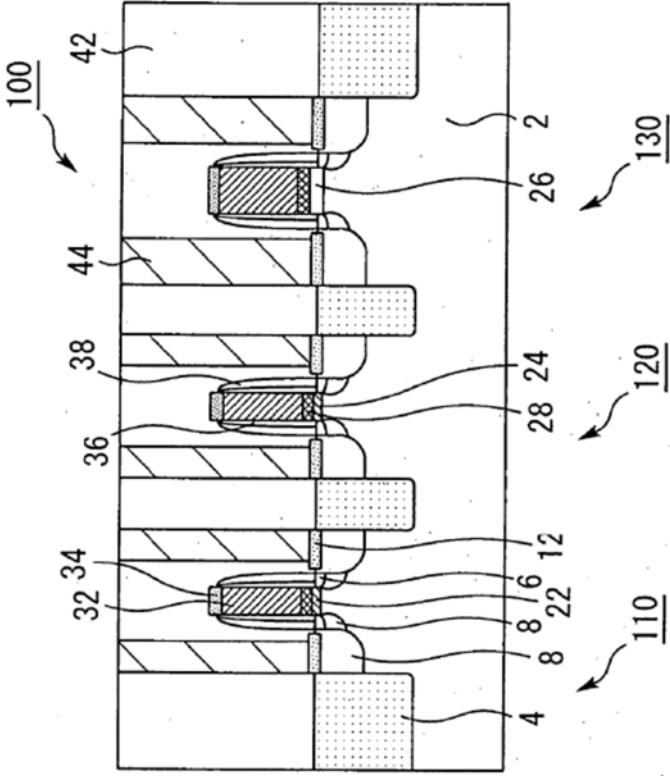
Claim	Claim Language	Exemplary Disclosures in Torii
1 [a]	a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate,	<p>[0018] Therefore, the present invention proposes the solution of the above-described problems, and it is the object of the present invention to provide a semiconductor device wherein gate insulating films highly controlled their thickness are formed when a plurality of transistors are formed on a chip, even if the difference between the thickness of the gate insulating films is small, and to provide a method for manufacturing such a semiconductor device.</p> <p>[0019] According to one aspect of the present invention, a semiconductor device comprises a substrate, and a first field-effect transistor and a second field-effect transistor formed on the substrate. The first field-effect transistor includes a first gate insulating film and a first gate electrode. The second field-effect transistor includes a second gate insulating film and a second gate electrode. Each of the first gate insulating film and the second gate insulating film includes a silicon oxynitride film and a high-dielectric constant film. The equivalent-oxide thickness of the first gate insulating film is thicker than the equivalent-oxide thickness of the second gate insulating film. The high dielectric-constant film in the first gate insulating film has the same thickness as the high-dielectric-constant film in the second gate insulating film.</p>
	a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate,	<p>Torii, as evidenced by the example citations below, discloses a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate.</p> <p>[0022] FIG. 1 is a schematic sectional view for illustrating an SoC (system on chip) 100 according to the first embodiments of the present invention.</p> <p>[0023] FIG. 2 is a flow diagram for illustrating the method for manufacturing an SoC 100 in the first embodiment of the present invention.</p>

FIG. 2



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Claim	Claim Language	Exemplary Disclosures in Torii
		<p>[0024] FIGS. 3 to 9 are schematic sectional views for illustrating the states in the process of manufacturing the SoC 100 in the first embodiment of the present invention.</p> <p>[0029] First Embodiment</p> <p>[0031] As FIG. 1 shows, the SoC 100 is composed of a MISFET (metal insulator semiconductor field effect transistor) 110 for LOP (low operating power) (hereafter referred to as MISFET for LOP 110); an MISFET 120 for LSTP (low stand-by power) (hereafter referred to as MISFET for LSTP 120); and an MISFET 130 for high withstand voltage (hereafter referred to as MISFET for high withstand voltage 130).</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><i>FIG. 1</i></p>  <p>[0032] The MISFETs for LOP 110, for LSTP 120, and for high withstand voltage 130 are formed in regions of an Si substrate 2 isolated by STI (shallow trench isolation) 4, respectively.</p> <p>[0073] Furthermore, in the first embodiment, the case wherein an n-type transistor is formed is described. However, the present invention may be applied to the case wherein a p-type transistor is formed. Moreover,</p>

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<b>Claim</b>	<b>Claim Language</b>	<b>Exemplary Disclosures in Torii</b>
		<p>within the scope of the present invention, the application of the present invention can be considered to the case wherein both p-type and n-type transistors are formed in one chip.</p> <p>The description and annotation below are an example of a first transistor and a second transistor and their respective elements. A person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 120, as depicted in the annotations throughout. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 110. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 120 and the second transistor may be 110.</p> <p>As can be seen below in Torii Figure 1 above, and Figure 9 below, Torii teaches a first MIS transistor and a second MIS transistor, for example, the high voltage 130 and LSTP 120, respectively. The first transistor and the second transistor are of identical conductivity type, n-type in this disclosure. <i>See</i> [0073]. Further, both the first transistor and the second transistor are formed on an identical semiconductor substrate, indicated by element 2.</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><b>FIG. 9</b></p> <p>[0075] Second Embodiment</p> <p>[0076] FIG. 12 is a flow diagram for illustrating the method for manufacturing an SoC according to the Second embodiment of the present invention.</p> <p>[0077] The SoC manufactured in the second embodiment is structurally similar to the SoC 100 described in the first embodiment. However, in the SoC of the second embodiment, the EOT of the silicon oxynitride film 22 of the MISFET for LOP 110 is about 0.7 nm, and the nitrogen content in the silicon oxynitride film is 15 to 25%.</p>

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<b>Claim</b>	<b>Claim Language</b>	<b>Exemplary Disclosures in Torii</b>
		<p>The thickness of the silicon oxynitride film 24 of the MISFET for LSTP120 is about 1.0 nm, and the EOT thereof is also about 1.0 nm. The nitrogen content in the silicon oxynitride film 24 is 1% or less.</p> <p>[0079] However, in the second embodiment, the heat treatment in a nitrogen monoxide atmosphere at about 800 to 900° C. for 5 to 60 seconds, described in Step S10 in the first embodiment, is substituted by the heat treatment in a mixed-gas atmosphere of dinitrogen oxide (N<sub>2</sub>O) and hydrogen (H) at about 850° C. for 5 seconds (Step S50). By doing this, as described above, a Silicon oxynitride film 22 having an EOT of about 0.7 nm, and the nitrogen content of 15 to 25% is formed in the region for LOP; and a silicon oxynitride film 24 of a thickness of about 1.0 nm, and the nitrogen content is 1% or less is formed in the region for LSTP</p> <p>[0081] In the SoC of the second embodiment, as in the SoC of the first embodiment, the thin gate insulating films having little thickness difference can be uniformly formed, by the use of the silicon oxynitride films 22 and 24. Therefore, the use of Such a structure enables a highly reliable semiconductor device to be formed even when both MISFETs for LOP and LSTP must be mounted in a chip.</p> <p>[0085] Since other parts are same as those in the first embodiment, the description thereof will be omitted.</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><b>FIG. 12</b></p> <pre> graph TD     Start([START]) --&gt; S2[FORMATION OF THERMAL OXIDE FILM]     S2 --&gt; S4[REMOVAL OF THERMAL OXIDE FILM (LOP AND LSTP REGIONS)]     S4 --&gt; S6[FORMATION OF SILICON NITRIDE FILM (LOP AND LSTP REGIONS)]     S6 --&gt; S8[REMOVAL OF SILICON NITRIDE FILM (LSTP REGION)]     S8 --&gt; S50[HEAT TREATMENT (IN NO + H2)]     S50 --&gt; S52[FORMATION OF HAFNIUM ALUMINATE FILM]     S52 --&gt; S14[HEAT TREATMENT]     S14 --&gt; S16[FORMATION OF POLYCRYSTALLINE SILICON FILM]     S16 --&gt; S17[ION IMPLANTATION]     S17 --&gt; S18[GATE ELECTRODE PROCESSING]     S18 --&gt; S20[FORMATION OF SIDEWALL SPACER]     S20 --&gt; S22[FORMATION OF SOURCE-DRAIN EXTENSION]     S22 --&gt; S24[FORMATION OF PUNCH-THROUGH STOPPER]     S24 --&gt; S26[FORMATION OF SIDEWALL SPACER]     S26 --&gt; S28[FORMATION OF SOURCE-DRAIN REGION]     S28 --&gt; S30[FORMATION OF NISI LAYER]     S30 --&gt; S32[FORMATION OF INTERLAYER INSULATING FILM]     S32 --&gt; S34[FORMATION OF CONTACT PLUG]     S34 --&gt; Stop([STOP])                     </pre>

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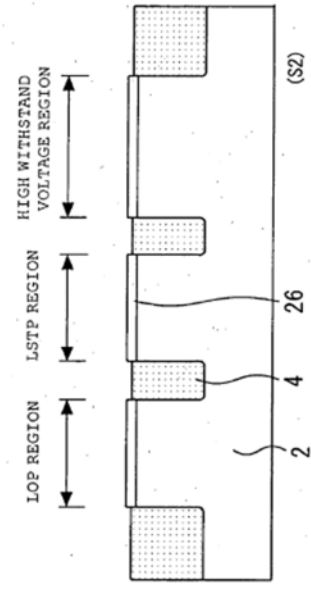
<b>Claim</b>	<b>Claim Language</b>	<b>Exemplary Disclosures in Torii</b>
1 [b]	<p>wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film,</p>	<p>Torii, as evidenced by the example citations below, discloses the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film,</p> <p>[0022] FIG. 1 is a schematic sectional view for illustrating an SoC (system on chip) 100 according to the first embodiments of the present invention.</p> <p>[0023] FIG. 2 is a flow diagram for illustrating the method for manufacturing an SoC 100 in the first embodiment of the present invention.</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><b>FIG. 2</b></p> <pre> graph TD     S2[FORMATION OF THERMAL OXIDE FILM] --&gt; S4[REMOVAL OF THERMAL OXIDE FILM (LOP AND LSTP REGIONS)]     S4 --&gt; S6[FORMATION OF SILICON NITRIDE FILM (LOP AND LSTP REGIONS)]     S6 --&gt; S8[REMOVAL OF SILICON NITRIDE FILM (LSTP REGION)]     S8 --&gt; S10[HEAT TREATMENT]     S10 --&gt; S12[FORMATION OF High-k FILM]     S12 --&gt; S14[HEAT TREATMENT]     S14 --&gt; S16[FORMATION OF POLYCRYSTALLINE SILICON FILM]     S16 --&gt; S17[ION IMPLANTATION]     S17 --&gt; S18[GATE ELECTRODE PROCESSING]     S18 --&gt; S20[FORMATION OF SIDEWALL SPACER]     S20 --&gt; S22[FORMATION OF SOURCE-DRAIN EXTENSION]     S22 --&gt; S24[FORMATION OF PUNCH-THROUGH STOPPER]     S24 --&gt; S26[FORMATION OF SIDEWALL SPACER]     S26 --&gt; S28[FORMATION OF SOURCE-DRAIN REGION]     S28 --&gt; S30[FORMATION OF NISI LAYER]     S30 --&gt; S32[FORMATION OF INTERLAYER INSULATING FILM]     S32 --&gt; S34[FORMATION OF CONTACT PLUG]     START([START]) --&gt; S2     S34 --&gt; STOP([STOP])     </pre>

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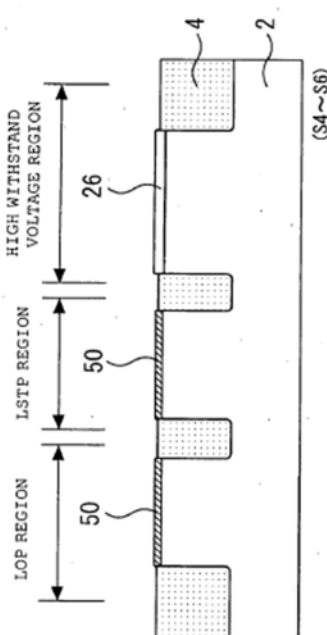
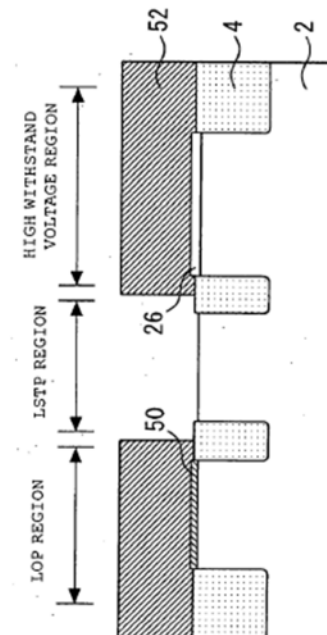
Claim	Claim Language	Exemplary Disclosures in Torii
		<p>[0024] FIGS. 3 to 9 are schematic sectional views for illustrating the states in the process of manufacturing the SoC 100 in the first embodiment of the present invention.</p> <p>[0033] On each region of the Si substrate 2 isolated by STI 4, a source-drain extension 6, which is a diffusion layer having a relatively shallow junction and a low impurity content is formed, and a punch-through stopper 8 is formed underneath the source-drain extension 6. Outside each source-drain extension 6, a source-drain region 10, which is a diffusion layer having a relatively deep junction and a high impurity content is formed. On each source-drain region 10, a nickel silicide (NiSi) layer 12 is formed.</p> <p>[0034] In the MISFET for LOP 110, a silicon oxynitride film 22 is formed as an interfacial gate insulating film in the area sandwiched by source-drain extensions 6 on the Si substrate 2. In the MISFET for LSTP 120, a silicon oxynitride film 24 is formed in the equivalent area. In the MISFET for high withstand voltage 130, a surface-nitrided thermally oxidized (SiO<sub>2</sub>) film 26 is formed in the equivalent area. Here, the thickness of the silicon oxynitride film 22 in the MISFET for LOP 110 is about 0.9 to 0.95 nm, and the EOT thereof is about 0.7 nm. The thickness of the silicon oxynitride film 24 in the MISFET for LSTP 120 is about 1.3 nm, and the EOT thereof is about 1.0 nm. Furthermore, the thickness of the thermally-oxidized film 26 is about 5 nm. In short, the silicon oxynitride film 22 for the MISFET for LOP 110 is thinnest, and the thermally-oxidized film 26 for the MISFET for high withstand voltage 130 is thickest.</p> <p>[0035] Here, the EOT is an abbreviation of equivalent oxide thickness and means an equivalent silicon oxide film thickness to which a thickness of a film is converted.</p> <p>[0036] On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia (HfO<sub>2</sub>) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed. The EOT of the high-k film 28 is about 0.5 nm. In each of MISFET 110, 120, and 130 for LOP, LSTP, and for high withstand voltage, respectively, a high-k film 28 is laminated on the silicon oxynitride films 22 and 24 or the thermally-oxidized film 26, thereby each gate insulating film is formed.</p> <p>[0037] On each high-k film 28, a gate electrode 32 is formed. The surface of the gate electrode 32 is silicided, thereby a nickel silicide layer 34 is formed. The gate length of the gate electrode 32 in the MISFET for LOP 100 is about 35 nm, and the gate length of the gate electrode 32 in the MISFET for LSTP 120 is about 50 nm. The</p>

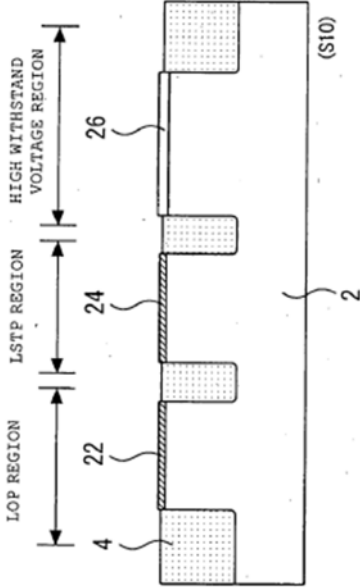
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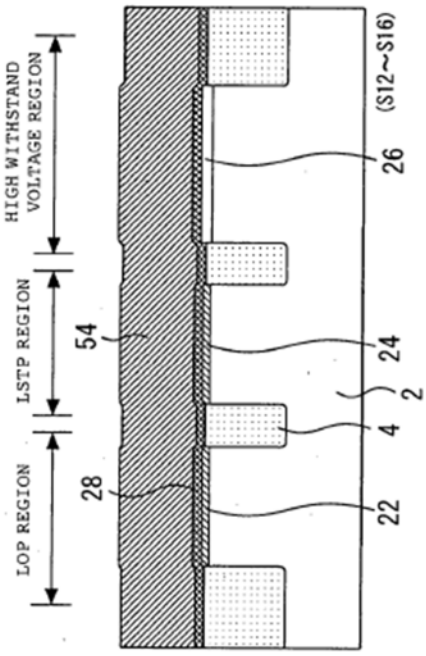
Claim	Claim Language	Exemplary Disclosures in Torii
		<p>gate length of the gate electrode 32 in the MISFET for high withstand voltage 130 is about 0.4 um. On the sidewalls of each gate electrode 32 and the underlying gate insulating film, side wall spacers 36 and 38 are formed.</p> <p>[0038] An interlayer insulating film 42 is formed on the Si substrate 2 so as to bury each gate insulating film, gate electrode 32, and sidewall spacers 36 and 38 formed as described above, and a contact plug 46 passing through the insulating film 42 and reaching the nickel silicide layer 12 on the source-drain region 10 is formed.</p> <p>[0042] The method for manufacturing an SoC 100 in the first embodiment of the present invention will be described below referring to FIGS. 1 to 9.</p> <p>[0045] On the Si substrate 2 in each region, a thermal oxide film 26 of a thickness of about 5 nm is formed (step S2). Next, as FIG. 3 shows, the thermal oxide films 26 on the regions for LOP and LSTP are removed (step S4). Concretely, after the region for high withstand voltage is coated with a resist mask, wet etching is performed using an aqueous solution of hydrofluoric acid to selectively remove the thermal oxide films 26. Thereafter, the resist mask is removed.</p> <p style="text-align: center;"><i>FIG. 3</i></p>  <p>The diagram shows a cross-section of a substrate 2. Three regions are defined: LOP REGION, LSTP REGION, and HIGH WITHSTAND VOLTAGE REGION. Thermal oxide films 26 are present on the substrate surface. In the LOP and LSTP regions, the oxide films are being removed, leaving gaps. In the HIGH WITHSTAND VOLTAGE region, the oxide film remains. Labels 2, 4, and 26 indicate different layers or regions.</p>

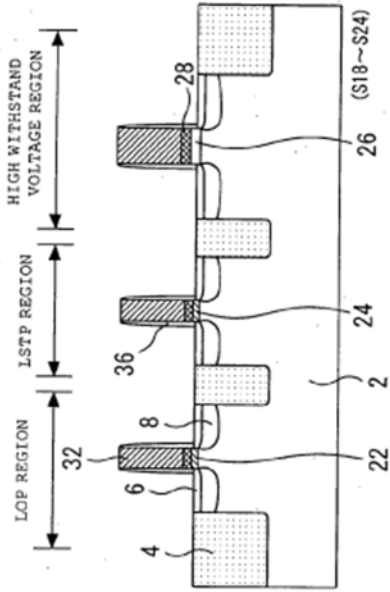
**EXHIBIT 779A1**

<b>Claim</b>	<b>Claim Language</b>	<b>Exemplary Disclosures in Torii</b>
		<p>[0046] Next, as FIG. 4 shows, a silicon nitride film 50 is formed in each of the regions for LOP and LSTP (step S6). Here, heat treatment is performed in an ammonia atmosphere at 600° C. to 700° C. for about 30 seconds. Thereby a silicon nitride film of a thickness of about 0.6nm is formed in each of the regions for LOP and LSTP. At this time, the surface of the thermal oxide film 26 is also simultaneously nitrided. Here, since the thickness of the silicon nitride film 50 can be easily controlled, a thin film of a uniform thickness to some extent can be formed. 0047 Next, as FIG. 5 shows, the silicon nitride film 50 in the region for LSTP is removed (step S8). Here, after the regions for LOP and high withstand voltage are coated with a resist mask 52, wet etching is performed to remove the silicon nitride film 50. Thereafter, the resist mask 52 is removed.</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><b>FIG. 4</b></p>  <p style="text-align: center;"><b>FIG. 5</b></p>  <p>[0048] Next, heat treatment is performed in a nitrogen monoxide (NO) environment (Step S10). The temperature of the heat treatment is about 800 to 900 C., and the treating time is about 5 to 60 seconds. Thereby, as FIG. 6 shows, a silicon oxynitride film 24 of a thickness of about 1.3 nm and an EOT of about 1.0 nm is formed in the</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p>region for LSTP The silicon nitride film 50 formed in the region for LOP is oxidized to form a silicon oxynitride film 22 of an EOT of about 0.7 nm. At this time, the nitrogen content in the silicon oxynitride film 22 in the region for LOP is about 15 to 20%, and the nitrogen content in the silicon oxynitride film 24 in the region for LSTP is about 9%. The surface of the thermal oxide films 26 is further nitrated to form a silicon oxynitride film.</p> <p style="text-align: center;"><i>FIG. 6</i></p>  <p>[0049] Next, as FIG. 7 shows, a high-k film 28 is formed on the entire surface of the substrate (Step S12). Here, a high-k film of a thickness of 3.0 nm is deposited using hafnium chloride and water as the materials using an ALD (atomic layer deposition) method. Thereafter, heat treatment at about 700 C. is performed in a reduced pressure oxygen atmosphere for about 5 seconds (Step S14).</p>

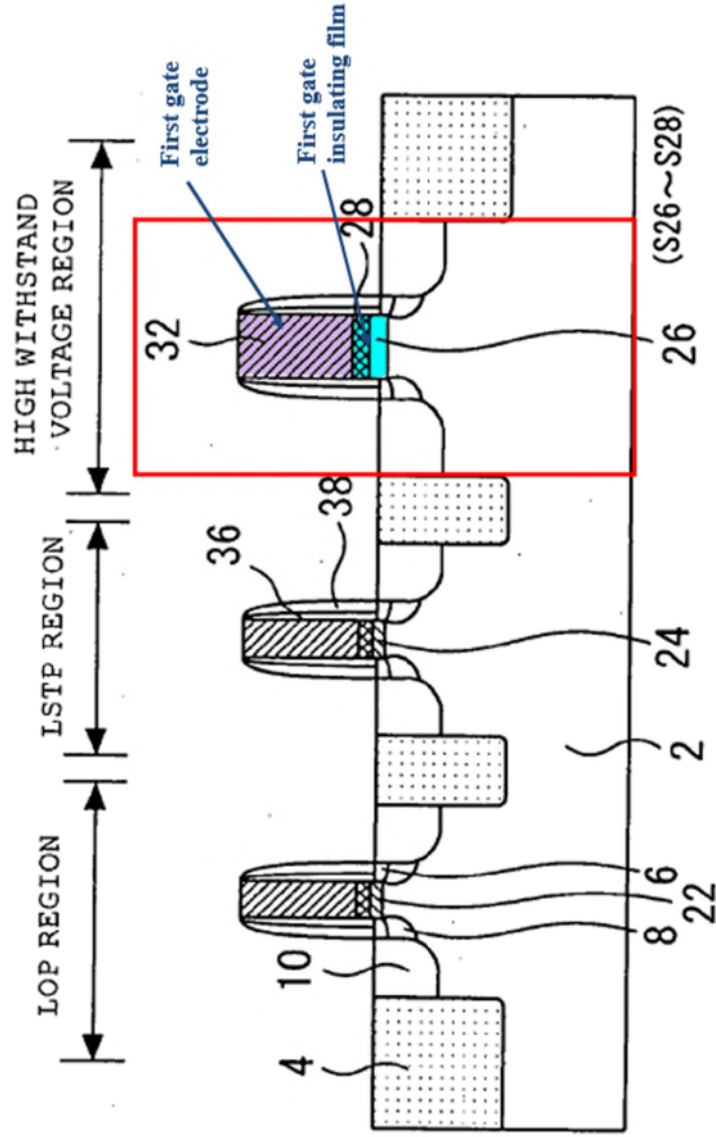
Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><b>FIG. 7</b></p>  <p>[0050] Next, a non-doped polycrystalline silicon film 54 is formed on the high-k film 28 (Step S16). The non-doped polycrystalline silicon film 54 is a material film for gate electrodes 32, and here, it is deposited to have a thickness of about 120 nm. Thereafter, impurity ions for the gate electrodes are implanted into the non-doped polycrystalline silicon film 54 (Step S17).</p> <p>[0051] Next, as FIG. 8 shows, the polycrystalline silicon film 54 is processed for a gate electrode 32 of each region (Step S18). Here, a resist mask of a width of the gate electrode is formed on the polycrystalline silicon film 54 using a conventional method, and etching is performed using the resist mask to process the polycrystalline silicon film 54 and the high-k film 28 to have the width of the gate electrode 32. Thereby, a gate electrode 32 and a gate insulating film are formed in each of the regions for LOP, LSTP, and high withstand voltage.</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p data-bbox="280 1157 321 1276"><i>FIG. 8</i></p>  <p data-bbox="834 113 1047 1549">The description and annotation below are an example of a first transistor and a second transistor and their respective elements. A person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 120, as depicted in the annotations throughout. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 110. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 120 and the second transistor may be 110.</p> <p data-bbox="1089 113 1268 1549">For example: as can be seen below in Torii Figure 9 and 1, and by the process described herein, Torii teaches a first transistor, outlined below in red, that includes a first gate insulating film, highlighted in light blue, formed on the active region in the semiconductor substrate, which a person of ordinary skill in the art would understand the active region encompasses elements 6, 8, and 10. Further, the first gate electrode, highlighted in purple, is formed on the first gate insulating film.</p>



Exemplary Disclosures in Torii

FIG. 9

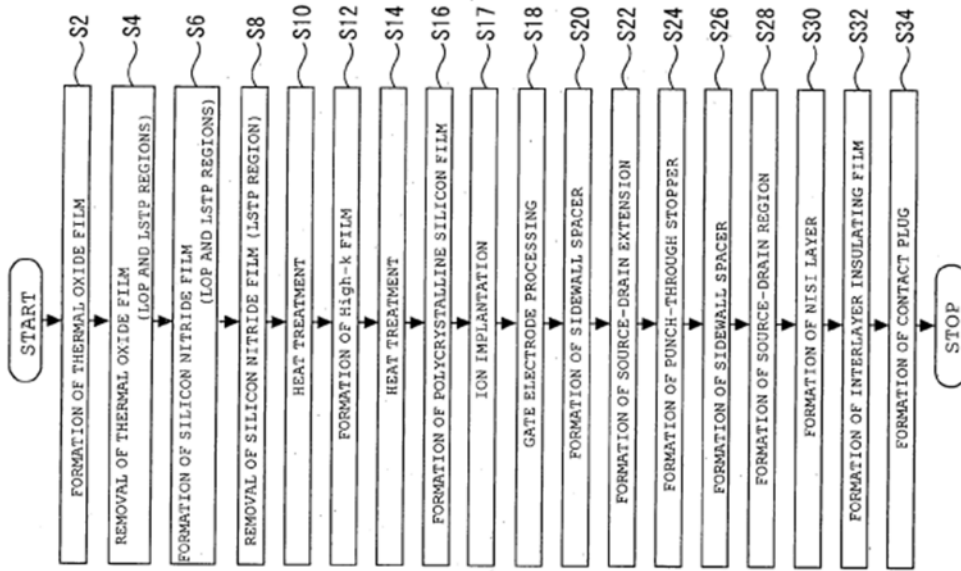


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<b>Claim</b>	<b>Claim Language</b>	<b>Exemplary Disclosures in Torii</b>
1 [c]	the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film,	<p>Torii, as evidenced by the example citations below, discloses the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film,</p> <p>[0022] FIG. 1 is a schematic sectional view for illustrating an SoC (system on chip) 100 according to the first embodiments of the present invention.</p> <p>[0023] FIG. 2 is a flow diagram for illustrating the method for manufacturing an SoC 100 in the first embodiment of the present invention.</p>

Exemplary Disclosures in Torii

FIG. 2

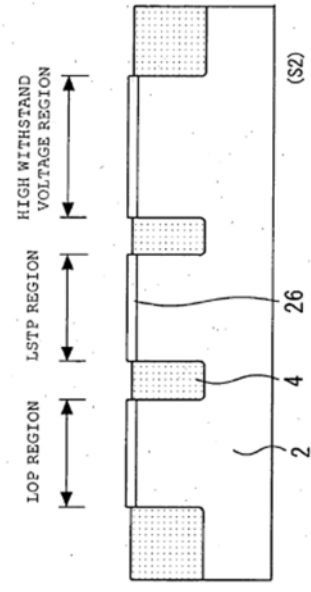


Claim Language

Claim

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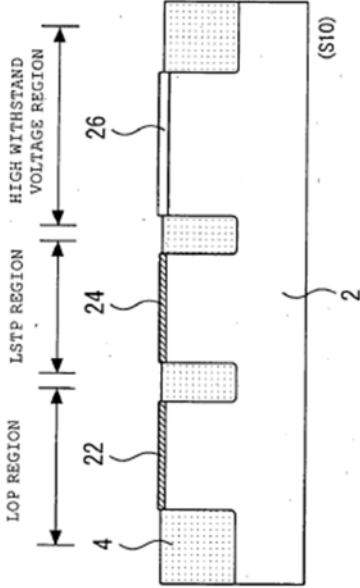
Claim	Claim Language	Exemplary Disclosures in Torii
		<p>[0024] FIGS. 3 to 9 are schematic sectional views for illustrating the States in the process of manufacturing the SoC 100 in the first embodiment of the present invention.</p> <p>[0033] On each region of the Si substrate 2 isolated by STI 4, a source-drain extension 6, which is a diffusion layer having a relatively shallow junction and a low impurity content is formed, and a punch-through stopper 8 is formed underneath the source-drain extension 6. Outside each source-drain extension 6, a source-drain region 10, which is a diffusion layer having a relatively deep junction and a high impurity content is formed. On each source-drain region 10, a nickel silicide (NiSi) layer 12 is formed.</p> <p>[0034] In the MISFET for LOP 110, a silicon oxynitride film 22 is formed as an interfacial gate insulating film in the area sandwiched by source-drain extensions 6 on the Si substrate 2. In the MISFET for LSTP 120, a silicon oxynitride film 24 is formed in the equivalent area. In the MISFET for high withstand voltage 130, a surface-nitrided thermally oxidized (SiO<sub>2</sub>) film 26 is formed in the equivalent area. Here, the thickness of the silicon oxynitride film 22 in the MISFET for LOP 110 is about 0.9 to 0.95 nm, and the EOT thereof is about 0.7 nm. The thickness of the silicon oxynitride film 24 in the MISFET for LSTP 120 is about 1.3 nm, and the EOT thereof is about 1.0 nm. Furthermore, the thickness of the thermally-oxidized film 26 is about 5 nm. In short, the silicon oxynitride film 22 for the MISFET for LOP 110 is thinnest, and the thermally-oxidized film 26 for the MISFET for high withstand voltage 130 is thickest.</p> <p>[0035] Here, the EOT is an abbreviation of equivalent oxide thickness and means an equivalent silicon oxide film thickness to which a thickness of a film is converted.</p> <p>[0036] On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia (HfO<sub>2</sub>) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed. The EOT of the high-k film 28 is about 0.5 nm. In each of MISFET 110, 120, and 130 for LOP, LSTP, and for high withstand voltage, respectively, a high-k film 28 is laminated on the silicon oxynitride films 22 and 24 or the thermally-oxidized film 26, thereby each gate insulating film is formed.</p> <p>[0037] On each high-k film 28, a gate electrode 32 is formed. The surface of the gate electrode 32 is silicided, thereby a nickel silicide layer 34 is formed. The gate length of the gate electrode 32 in the MISFET for LOP 100 is about 35 nm, and the gate length of the gate electrode 32 in the MISFET for LSTP 120 is about 50 nm. The</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p>gate length of the gate electrode 32 in the MISFET for high withstand voltage 130 is about 0.4 μm. On the sidewalls of each gate electrode 32 and the underlying gate insulating film, sidewall spacers 36 and 38 are formed.</p> <p>[0038] An interlayer insulating film 42 is formed on the Si substrate 2 so as to bury each gate insulating film, gate electrode 32, and sidewall spacers 36 and 38 formed as described above, and a contact plug 46 passing through the insulating film 42 and reaching the nickel silicide layer 12 on the source-drain region 10 is formed.</p> <p>[0042] The method for manufacturing an SoC 100 in the first embodiment of the present invention will be described below referring to FIGS. 1 to 9.</p> <p>[0045] On the Si substrate 2 in each region, a thermal oxide film 26 of a thickness of about 5 nm is formed (Step S2). Next, as FIG. 3 shows, the thermal oxide films 26 on the regions for LOP and LSTP are removed (Step S4). Concretely, after the region for high withstand voltage is coated with a resist mask, wet etching is performed using an aqueous solution of hydrofluoric acid to selectively remove the thermal oxide films 26. Thereafter, the resist mask is removed.</p> <p style="text-align: center;"><i>FIG. 3</i></p> 

**EXHIBIT 779A1**

<b>Claim</b>	<b>Claim Language</b>	<b>Exemplary Disclosures in Torii</b>
		<p>[0046] Next, as FIG. 4 shows, a silicon nitride film 50 is formed in each of the regions for LOP and LSTP (Step S6). Here, heat treatment is performed in an ammonia atmosphere at 600° C. to 700° C. for about 30 seconds. Thereby a silicon nitride film of a thickness of about 0.6nm is formed in each of the regions for LOP and LSTP. At this time, the surface of the thermal oxide film 26 is also simultaneously nitrided. Here, since the thickness of the silicon nitride film 50 can be easily controlled, a thin film of a uniform thickness to some extent can be formed. 0047 Next, as FIG. 5 shows, the silicon nitride film 50 in the region for LSTP is removed (Step S8). Here, after the regions for LOP and high withstand voltage are coated with a resist mask 52, wet etching is performed to remove the silicon nitride film 50. Thereafter, the resist mask 52 is removed.</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><b>FIG. 4</b></p> <p style="text-align: center;"><b>FIG. 5</b></p> <p>[0048] Next, heat treatment is performed in a nitrogen monoxide (NO) environment (Step S10). The temperature of the heat treatment is about 800 to 900 C., and the treating time is about 5 to 60 seconds. Thereby, as FIG. 6 shows, a silicon oxynitride film 24 of a thickness of about 1.3 nm and an EOT of about 1.0 nm is formed in the</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p>region for LSTP The silicon nitride film 50 formed in the region for LOP is oxidized to form a silicon oxynitride film 22 of an EOT of about 0.7 nm. At this time, the nitrogen content in the silicon oxynitride film 22 in the region for LOP is about 15 to 20%, and the nitrogen content in the silicon oxynitride film 24 in the region for LSTP is about 9%. The surface of the thermal oxide films 26 is further nitrated to form a silicon oxynitride film.</p> <p style="text-align: center;"><i>FIG. 6</i></p>  <p>[0049] Next, as FIG. 7 shows, a high-k film 28 is formed on the entire surface of the substrate (Step S12). Here, a high-k film of a thickness of 3.0 nm is deposited using hafnium chloride and water as the materials using an ALD (atomic layer deposition) method. Thereafter, heat treatment at about 700 C. is performed in a reduced pressure oxygen atmosphere for about 5 seconds (Step S14).</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><b>FIG. 7</b></p> <p>[0050] Next, a non-doped polycrystalline silicon film 54 is formed on the high-k film 28 (Step S16). The non-doped polycrystalline silicon film 54 is a material film for gate electrodes 32, and here, it is deposited to have a thickness of about 120 nm. Thereafter, impurity ions for the gate electrodes are implanted into the non-doped polycrystalline silicon film 54 (Step S17).</p> <p>[0051] Next, as FIG. 8 shows, the polycrystalline silicon film 54 is processed for a gate electrode 32 of each region (Step S18). Here, a resist mask of a width of the gate electrode is formed on the polycrystalline silicon film 54 using a conventional method, and etching is performed using the resist mask to process the polycrystalline silicon film 54 and the high-k film 28 to have the width of the gate electrode 32. Thereby, a gate electrode 32 and a gate insulating film are formed in each of the regions for LOP, LSTP, and high withstand voltage.</p>

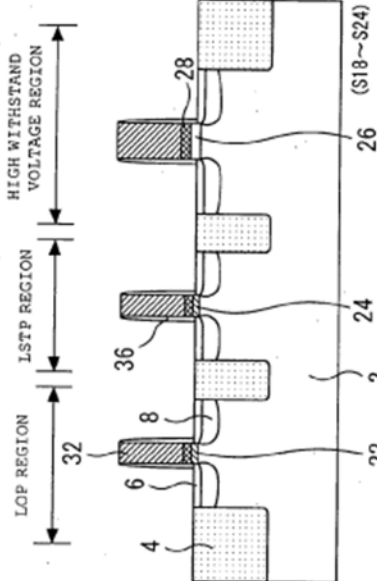
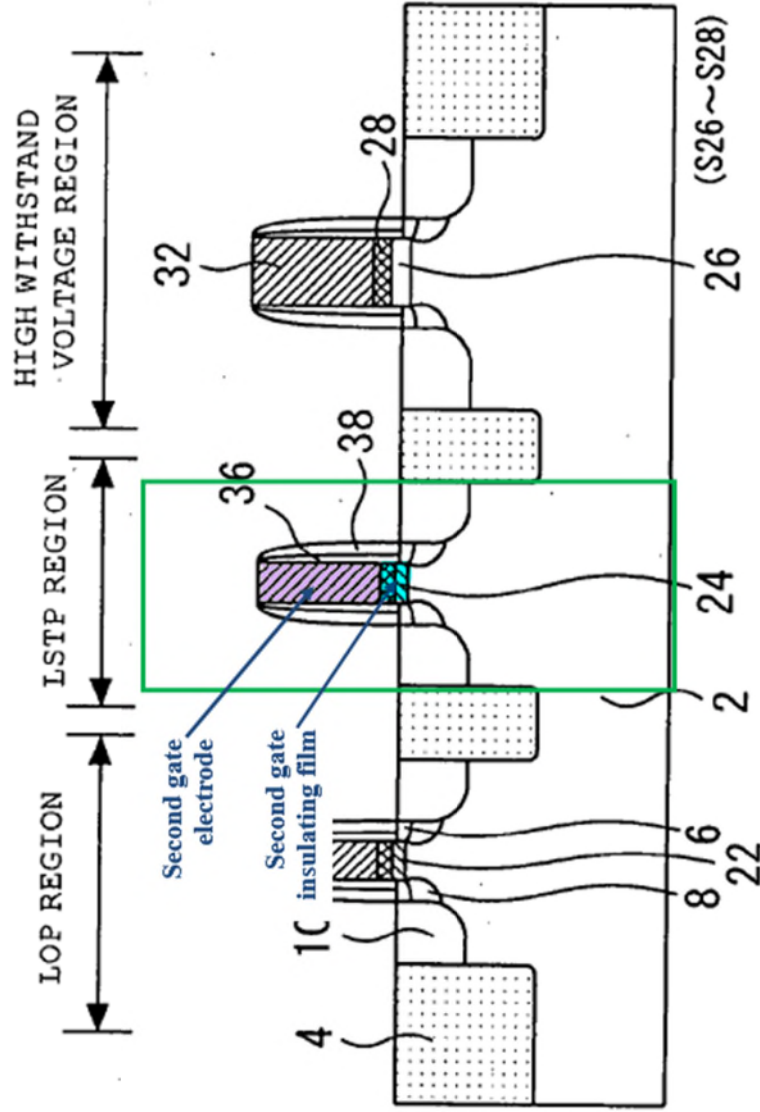
Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><b>FIG. 8</b></p>  <p>The description and annotation below are an example of a first transistor and a second transistor and their respective elements. A person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 120, as depicted in the annotations throughout. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 110. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 120 and the second transistor may be 110.</p> <p>For example, as can be seen below in Torii Figure 9 and 1, and by the process described herein, Torii teaches a second transistor, outlined below in green, that includes a first gate insulating film, highlighted in light blue, formed on the active region in the semiconductor substrate, which a person of ordinary skill in the art would understand the active region encompasses elements 6, 8, and 10. Further, the first gate electrode, highlighted in purple, is formed on the first gate insulating film.</p>



FIG. 9



See 1[b]

Claim Language

Claim

**EXHIBIT 779A1**

<b>Claim</b>	<b>Claim Language</b>	<b>Exemplary Disclosures in Torii</b>
1 [d]	<p>the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer,</p>	<p>Torii, as evidenced by the example citations below, discloses the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer.</p> <p>[0022] FIG. 1 is a schematic sectional view for illustrating an SoC (system on chip) 100 according to the first embodiments of the present invention.</p> <p>[0023] FIG. 2 is a flow diagram for illustrating the method for manufacturing an SoC 100 in the first embodiment of the present invention.</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><i>FIG. 2</i></p> <pre> graph TD     START([START]) --&gt; S2[FORMATION OF THERMAL OXIDE FILM]     S2 --&gt; S4[REMOVAL OF THERMAL OXIDE FILM (LOP AND LSTP REGIONS)]     S4 --&gt; S6[FORMATION OF SILICON NITRIDE FILM (LOP AND LSTP REGIONS)]     S6 --&gt; S8[REMOVAL OF SILICON NITRIDE FILM (LSTP REGION)]     S8 --&gt; S10[HEAT TREATMENT]     S10 --&gt; S12[FORMATION OF High-k FILM]     S12 --&gt; S14[HEAT TREATMENT]     S14 --&gt; S16[FORMATION OF POLYCRYSTALLINE SILICON FILM]     S16 --&gt; S17[ION IMPLANTATION]     S17 --&gt; S18[GATE ELECTRODE PROCESSING]     S18 --&gt; S20[FORMATION OF SIDEWALL SPACER]     S20 --&gt; S22[FORMATION OF SOURCE-DRAIN EXTENSION]     S22 --&gt; S24[FORMATION OF PUNCH-THROUGH STOPPER]     S24 --&gt; S26[FORMATION OF SIDEWALL SPACER]     S26 --&gt; S28[FORMATION OF SOURCE-DRAIN REGION]     S28 --&gt; S30[FORMATION OF NISI LAYER]     S30 --&gt; S32[FORMATION OF INTERLAYER INSULATING FILM]     S32 --&gt; S34[FORMATION OF CONTACT PLUG]     S34 --&gt; STOP([STOP])     </pre>

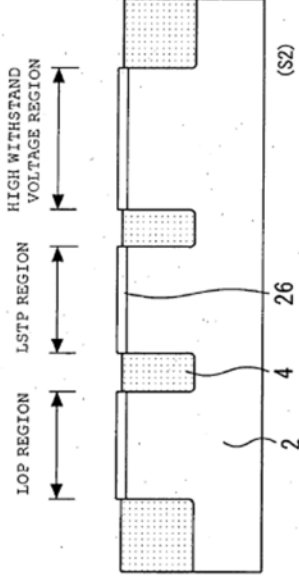
[0024] FIGS. 3 to 9 are schematic sectional views for illustrating the states in the process of manufacturing the SoC 100 in the first embodiment of the present invention.

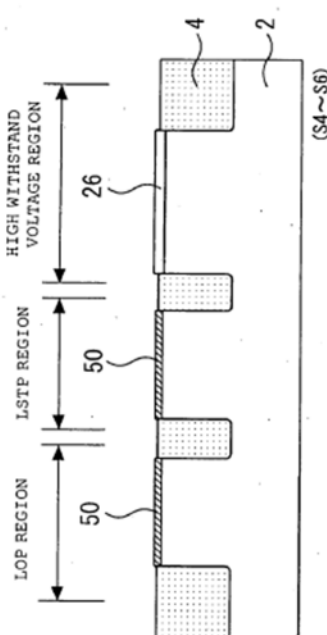
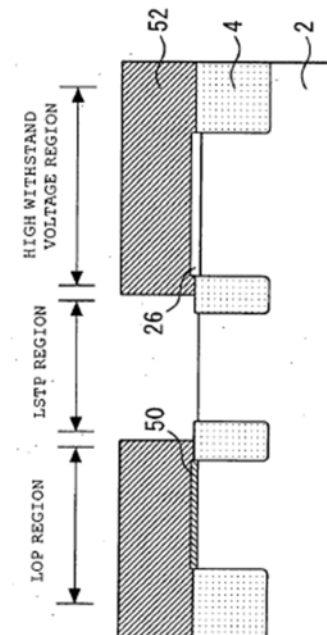
**EXHIBIT 779A1**

Claim	Claim Language	Exemplary Disclosures in Torii
		<p>[0033] On each region of the Si substrate 2 isolated by STI 4, a source-drain extension 6, which is a diffusion layer having a relatively shallow junction and a low impurity content is formed, and a punch-through stopper 8 is formed underneath the source-drain extension 6. Outside each source-drain extension 6, a source-drain region 10, which is a diffusion layer having a relatively deep junction and a high impurity content is formed. On each source-drain region 10, a nickel silicide (NiSi) layer 12 is formed.</p> <p>[0034] In the MISFET for LOP 110, a silicon oxynitride film 22 is formed as an interfacial gate insulating film in the area sandwiched by source-drain extensions 6 on the Si substrate 2. In the MISFET for LSTP 120, a silicon oxynitride film 24 is formed in the equivalent area. In the MISFET for high withstand voltage 130, a surface-nitrided thermally oxidized (SiO<sub>2</sub>) film 26 is formed in the equivalent area. Here, the thickness of the silicon oxynitride film 22 in the MISFET for LOP 110 is about 0.9 to 0.95 nm, and the EOT thereof is about 0.7 nm. The thickness of the silicon oxynitride film 24 in the MISFET for LSTP 120 is about 1.3 nm, and the EOT thereof is about 1.0 nm. Furthermore, the thickness of the thermally-oxidized film 26 is about 5 nm. In short, the silicon oxynitride film 22 for the MISFET for LOP 110 is thinnest, and the thermally-oxidized film 26 for the MISFET for high withstand voltage 130 is thickest.</p> <p>[0035] Here, the EOT is an abbreviation of equivalent oxide thickness and means an equivalent silicon oxide film thickness to which a thickness of a film is converted.</p> <p>[0036] On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia (HfO<sub>2</sub>) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed. The EOT of the high-k film 28 is about 0.5 nm. In each of MISFET 110, 120, and 130 for LOP, LSTP, and for high withstand voltage, respectively, a high-k film 28 is laminated on the silicon oxynitride films 22 and 24 or the thermally-oxidized film 26, thereby each gate insulating film is formed.</p> <p>[0037] On each high-k film 28, a gate electrode 32 is formed. The surface of the gate electrode 32 is silicided, thereby a nickel silicide layer 34 is formed. The gate length of the gate electrode 32 in the MISFET for LOP 100 is about 35 nm, and the gate length of the gate electrode 32 in the MISFET for LSTP 120 is about 50 nm. The gate length of the gate electrode 32 in the MISFET for high withstand voltage 130 is about 0.4 um. On the sidewalls of each gate electrode 32 and the underlying gate insulating film, sidewall spacers 36 and 38 are formed.</p>

**EXHIBIT 779A1**

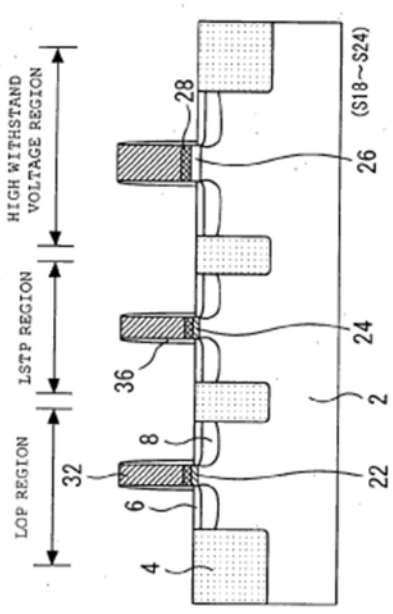
Claim	Claim Language	Exemplary Disclosures in Torii
		<p>[0038] An interlayer insulating film 42 is formed on the Si substrate 2 so as to bury each gate insulating film, gate electrode 32, and sidewall spacers 36 and 38 formed as described above, and a contact plug 46 passing through the insulating film 42 and reaching the nickel silicide layer 12 on the source-drain region 10 is formed.</p> <p>[0039] In The SoC 100, as described above, MISFETs 110, 120, and 130 for LOP, LSTP, and for high withstand voltage, respectively, having gate insulating films is different thickness are formed.</p> <p>[0040] Specifically, the MISFET for LOP 110 is a low power-consumption transistor included the laminated film of the silicon oxynitride film 22 and the high-k film 28 as gate insulating film having a reduced EOT. The MISFET for LSTP 120 is a low-standby-power transistor using the laminated film of the silicon oxynitride film 24 and the high-k film 28 as gate insulating film, controlling the EOT to be low to some extent, and sufficiently securing the effective film thickness. The MISFET for high withstand voltage 130 is a high-withstand-voltage transistor securing the thickness of the thermal oxide film so as to withstand the external high voltage.</p> <p>[0042] The method for manufacturing an SoC 100 in the first embodiment of the present invention will be described below referring to FIGS. 1 to 9.</p> <p>[0045] On the Si substrate 2 in each region, a thermal oxide film 26 of a thickness of about 5 nm is formed (Step S2). Next, as FIG. 3 shows, the thermal oxide films 26 on the regions for LOP and LSTP are removed (Step S4). Concretely, after the region for high withstand voltage is coated with a resist mask, wet etching is performed using an aqueous Solution of hydrofluoric acid to selectively remove the thermal oxide films 26. Thereafter, the resist mask is removed.</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><i>FIG. 3</i></p>  <p>[0046] Next, as FIG. 4 shows, a silicon nitride film 50 is formed in each of the regions for LOP and LSTP (Step S6). Here, heat treatment is performed in an ammonia atmosphere at 600° C. to 700° C. for about 30 seconds. Thereby a silicon nitride film of a thickness of about 0.6nm is formed in each of the regions for LOP and LSTP. At this time, the surface of the thermal oxide film 26 is also simultaneously nitrided. Here, since the thickness of the silicon nitride film 50 can be easily controlled, a thin film of a uniform thickness to some extent can be formed. 0047 Next, as FIG. 5 shows, the silicon nitride film 50 in the region for LSTP is removed (Step S8). Here, after the regions for LOP and high withstand voltage are coated with a resist mask 52, wet etching is performed to remove the silicon nitride film 50. Thereafter, the resist mask 52 is removed.</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><b>FIG. 4</b></p>  <p style="text-align: center;"><b>FIG. 5</b></p>  <p>[0048] Next, heat treatment is performed in a nitrogen monoxide (NO) environment (Step S10). The temperature of the heat treatment is about 800 to 900 C., and the treating time is about 5 to 60 seconds. Thereby, as FIG. 6 shows, a silicon oxynitride film 24 of a thickness of about 1.3 nm and an EOT of about 1.0 nm is formed in the region for LSTP. The silicon nitride film 50 formed in the region for LOP is oxidized to form a silicon oxynitride</p>



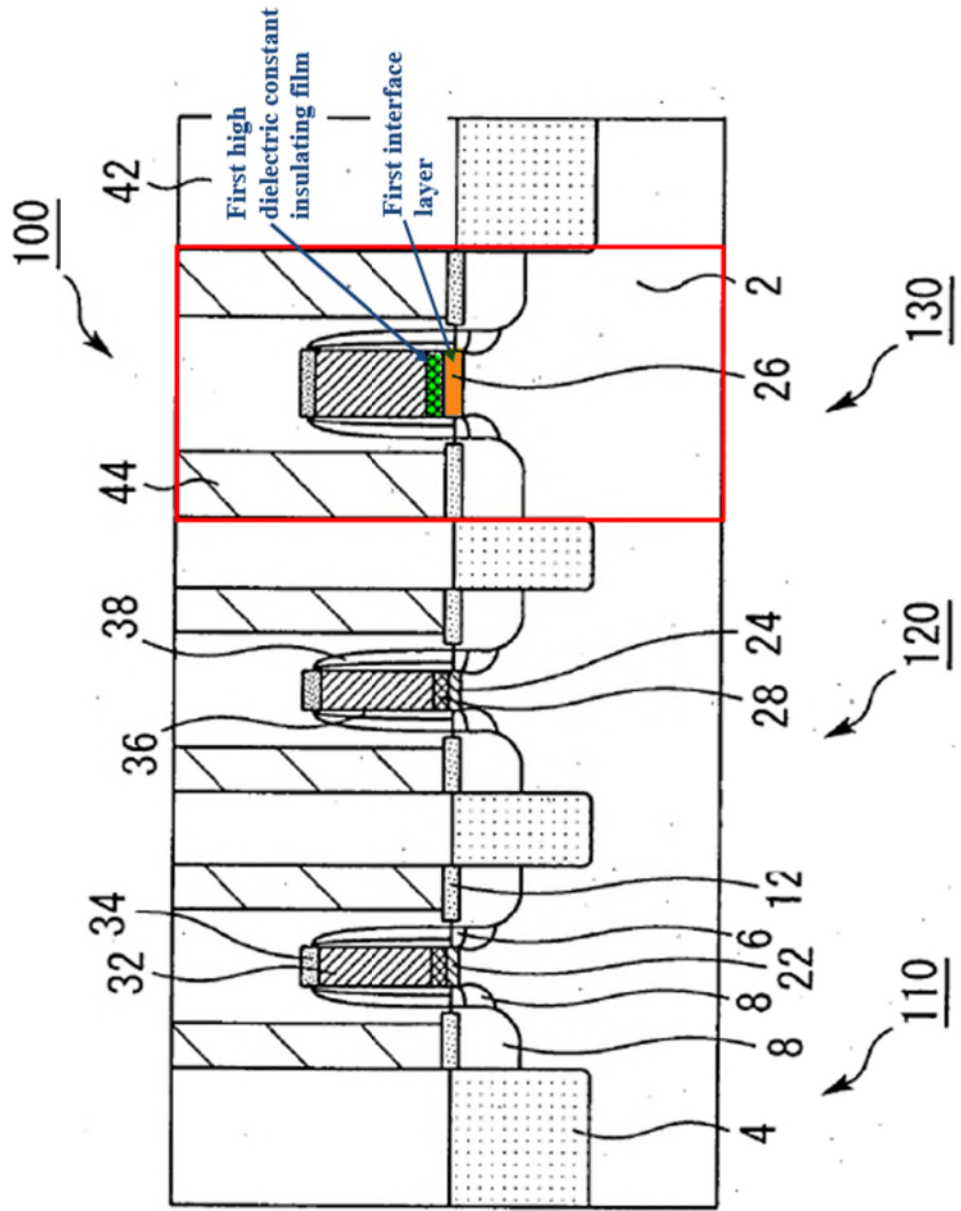


Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><b>FIG. 8</b></p>  <p>[0058] According to the first embodiment, as described above, the insulating film of a laminate Structure wherein a high-k film 28 is deposited on silicon oxynitride films 22 and 24 as the gate insulating film of MISFETs 110 and 120 for LOP and LSTP, respectively. Here, by the use of the silicon Oxynitride films 22 and 24, the thin gate insulating films having little thickness difference can be uniformly formed. Therefore, the use of Such a structure enables a highly reliable semiconductor device to be formed even when both MISFETs for LOP and LSTP must be mounted in a chip.</p> <p>[0059] In the first embodiment, the silicon nitride film in the region for LSTP is removed, leaving the silicon nitride film 50 only in the region for LOP. Thereafter, by performing heat treatment in a nitrogen monoxide atmosphere, the silicon nitride film 50 is oxidized to form a silicon oxynitride film 22 in the region for LOP; on the other hand, a silicon oxynitride film 24 is formed in the region for LSTP. Thus, the use of oxynitride films realizes the formation of highly controlled uniform thin films. Particularly in the first embodiment, by using the silicon nitride film 50, and by using a means for forming an oxynitride film at the same time as the Oxidation thereof, highly controlled uniform thin films can be formed even when both the silicon oxynitride films in the region for LOP and the region for LSTP are thin, and have little thickness difference. Thereby, the target value recommended by ITRS for the 65-nm technology can also be achieved.</p>

**EXHIBIT 779A1**

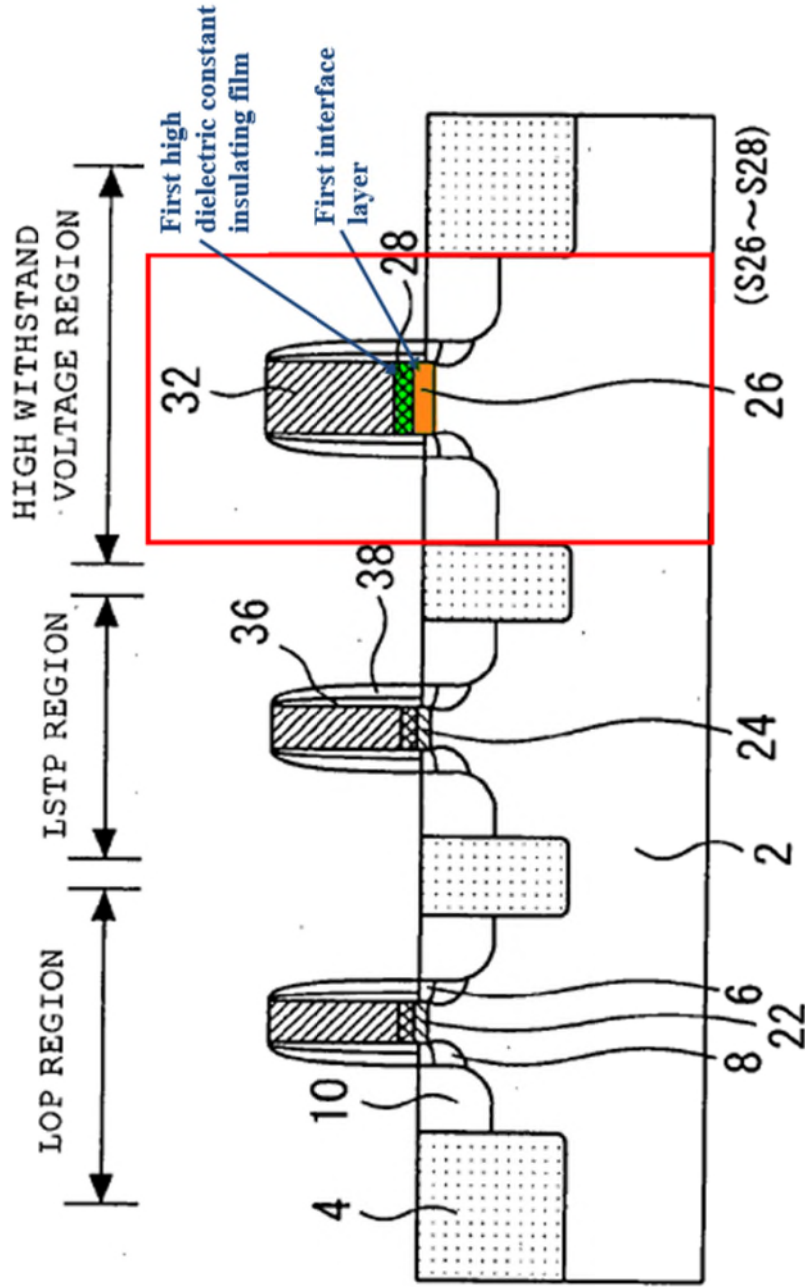
Claim	Claim Language	Exemplary Disclosures in Torii
		<p>[0060] The nitrogen content of the silicon oxynitride films 22 and 24 formed in the first embodiment is 15 to 20% and 9%, respectively.</p> <p>[0061] For example, if high-k films are laminated on an insulating film to use as a gate insulating film, the high-k films may react with (or mixed to) the underlying films. In this case, there is a problem of increasing of the variation of the thickness, withstand voltage, and the like in the Surface of the insulating films, or the occurrence of defect in the boundary of the insulating films, leading to the deterioration of the characteristics of the transistor, and the lowering of the reliability of the semiconductor device. In the first embodiment, however, silicon oxynitride films containing the above-described contents of nitrogen are used as the gate insulating film. Since the mixing of nitrogen in the silicon oxide film can increase the density of the film, the above described reaction of the insulating film and the high-k film can be inhibited, and a highly reliable Semiconductor device can be formed.</p> <p>The description and annotation below are an example of a first transistor and a second transistor and their respective elements. A person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 120, as depicted in the annotations throughout. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 110. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 120 and the second transistor may be 110.</p> <p>For example, as can be seen below in Torii Figures 1 and 9, and by the process described in the citations above, Torii teaches the first gate insulating film which includes a first interface layer, highlighted in orange and indicated by element 26, and is in contact with the semiconductor substrate. Torii further discloses the first gate insulating film also includes a first high dielectric constant insulating film, highlighted in light green and indicated by element 28, formed on the first interface layer. Torii discloses the first high dielectric constant insulating film, or element 28, as “the high-k film such as a hafnia (HfO<sub>2</sub>) film 28.” See [0036]. A person of ordinary skill in the art would understand that “k” (or kappa) is the dielectric constant.</p>

FIG. 1



Exemplary Disclosures in Torii

FIG. 9



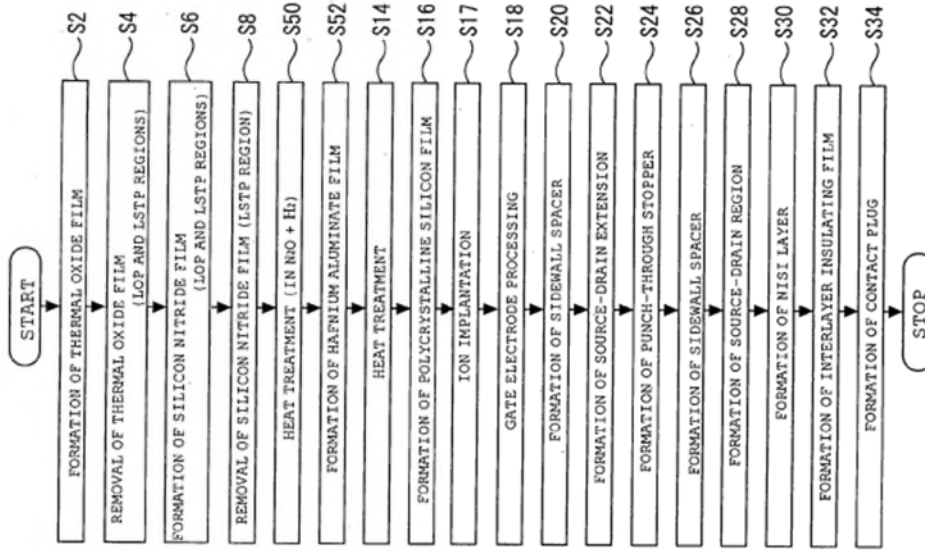
**EXHIBIT 779A1**

Claim	Claim Language	Exemplary Disclosures in Torii
		<p>[0075] Second Embodiment</p> <p>[0076] FIG. 12 is a flow diagram for illustrating the method for manufacturing an SoC according to the Second embodiment of the present invention.</p> <p>[0077] The SoC manufactured in the second embodiment is structurally similar to the SoC 100 described in the first embodiment. However, in the SoC of the second embodiment, the EOT of the silicon oxynitride film 22 of the MISFET for LOP 110 is about 0.7 nm, and the nitrogen content in the silicon oxynitride film is 15 to 25%. The thickness of the silicon oxynitride film 24 of the MISFET for LSTP120 is about 1.0 nm, and the EOT thereof is also about 1.0 nm. The nitrogen content in the silicon oxynitride film 24 is 1% or less.</p> <p>[0079] However, in the second embodiment, the heat treatment in a nitrogen monoxide atmosphere at about 800 to 900° C. for 5 to 60 seconds, described in Step S10 in the first embodiment, is substituted by the heat treatment in a mixed-gas atmosphere of dinitrogen oxide (N2O) and hydrogen (H) at about 850° C. for 5 seconds (Step S50). By doing this, as described above, a Silicon oxynitride film 22 having an EOT of about 0.7 nm, and the nitrogen content of 15 to 25% is formed in the region for LOP; and a silicon oxynitride film 24 of a thickness of about 1.0 nm, and the nitrogen content is 1% or less is formed in the region for LSTP</p> <p>[0081] In the SoC of the second embodiment, as in the SoC of the first embodiment, the thin gate insulating films having little thickness difference can be uniformly formed, by the use of the silicon oxynitride films 22 and 24. Therefore, the use of Such a structure enables a highly reliable semiconductor device to be formed even when both MISFETs for LOP and LSTP must be mounted in a chip.</p> <p>[0085] Since other parts are same as those in the first embodiment, the description thereof will be omitted.</p> <p>[0088] Also for example, by performing Steps S6 and S8 in the first and Second embodiments, the Step for forming the Silicon nitride film and the Step for removing the Silicon nitride film of the present invention are performed, respectively. Also by performing Step S10 in the first embodiment, or Step S50 in the second embodiment, the heat treating step of the present invention is performed. Also for example, by performing Step S12 in the first and Second embodiments, the Step for forming the high-k film of the present invention is performed. Also for example, by performing Steps S2 and S4 in the first and second embodiments, the step for</p>

Exemplary Disclosures in Torii

forming the Silicon oxide film and the Step for removing the Silicon oxide film of the present invention are performed, respectively.

FIG. 12



See 1[b]

**EXHIBIT 779A1**

<b>Claim</b>	<b>Claim Language</b>	<b>Exemplary Disclosures in Torii</b>
1 [e]	<p>the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer,</p>	<p>Torii, as evidenced by the example citations below, discloses the second gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer.</p> <p>[0022] FIG. 1 is a schematic sectional view for illustrating an SoC (system on chip) 100 according to the first embodiments of the present invention.</p> <p>[0023] FIG. 2 is a flow diagram for illustrating the method for manufacturing an SoC 100 in the first embodiment of the present invention.</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><b>FIG. 2</b></p> <pre> graph TD     START([START]) --&gt; S2[FORMATION OF THERMAL OXIDE FILM]     S2 --&gt; S4[REMOVAL OF THERMAL OXIDE FILM (LOP AND LSTP REGIONS)]     S4 --&gt; S6[FORMATION OF SILICON NITRIDE FILM (LOP AND LSTP REGIONS)]     S6 --&gt; S8[REMOVAL OF SILICON NITRIDE FILM (LSTP REGION)]     S8 --&gt; S10[HEAT TREATMENT]     S10 --&gt; S12[FORMATION OF HIGH-K FILM]     S12 --&gt; S14[HEAT TREATMENT]     S14 --&gt; S16[FORMATION OF POLYCRYSTALLINE SILICON FILM]     S16 --&gt; S17[ION IMPLANTATION]     S17 --&gt; S18[GATE ELECTRODE PROCESSING]     S18 --&gt; S20[FORMATION OF SIDEWALL SPACER]     S20 --&gt; S22[FORMATION OF SOURCE-DRAIN EXTENSION]     S22 --&gt; S24[FORMATION OF PUNCH-THROUGH STOPPER]     S24 --&gt; S26[FORMATION OF SIDEWALL SPACER]     S26 --&gt; S28[FORMATION OF SOURCE-DRAIN REGION]     S28 --&gt; S30[FORMATION OF NISI LAYER]     S30 --&gt; S32[FORMATION OF INTERLAYER INSULATING FILM]     S32 --&gt; S34[FORMATION OF CONTACT PLUG]     S34 --&gt; STOP([STOP])     </pre>

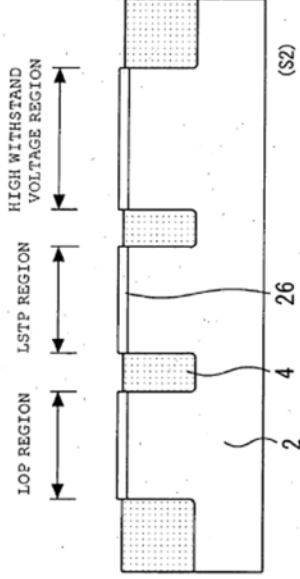
[0024] FIGS. 3 to 9 are schematic sectional views for illustrating the States in the process of manufacturing the SoC 100 in the first embodiment of the present invention.

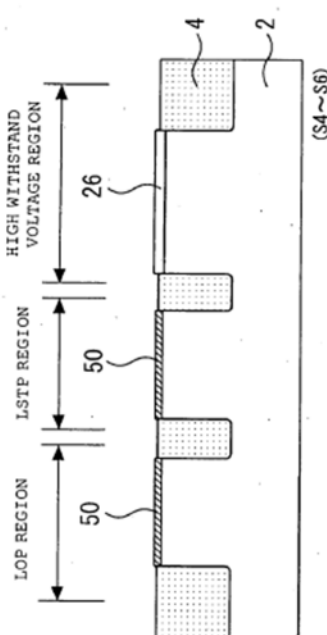
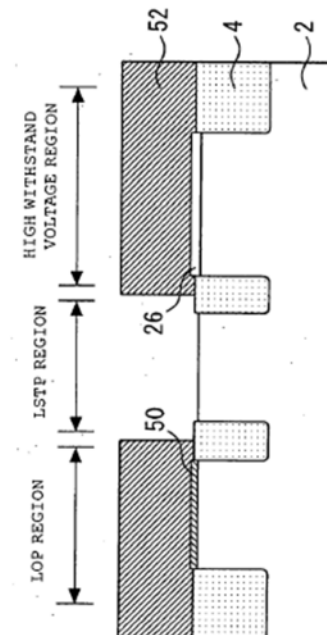
**EXHIBIT 779A1**

Claim	Claim Language	Exemplary Disclosures in Torii
		<p>[0033] On each region of the Si substrate 2 isolated by STI 4, a source-drain extension 6, which is a diffusion layer having a relatively shallow junction and a low impurity content is formed, and a punch-through stopper 8 is formed underneath the source-drain extension 6. Outside each source-drain extension 6, a source-drain region 10, which is a diffusion layer having a relatively deep junction and a high impurity content is formed. On each source-drain region 10, a nickel silicide (NiSi) layer 12 is formed.</p> <p>[0034] In the MISFET for LOP 110, a silicon oxynitride film 22 is formed as an interfacial gate insulating film in the area sandwiched by source-drain extensions 6 on the Si substrate 2. In the MISFET for LSTP 120, a silicon oxynitride film 24 is formed in the equivalent area. In the MISFET for high withstand voltage 130, a surface-nitrided thermally oxidized (SiO<sub>2</sub>) film 26 is formed in the equivalent area. Here, the thickness of the silicon oxynitride film 22 in the MISFET for LOP 110 is about 0.9 to 0.95 nm, and the EOT thereof is about 0.7 nm. The thickness of the silicon oxynitride film 24 in the MISFET for LSTP 120 is about 1.3 nm, and the EOT thereof is about 1.0 nm. Furthermore, the thickness of the thermally-oxidized film 26 is about 5 nm. In short, the silicon oxynitride film 22 for the MISFET for LOP 110 is thinnest, and the thermally-oxidized film 26 for the MISFET for high withstand voltage 130 is thickest.</p> <p>[0035] Here, the EOT is an abbreviation of equivalent oxide thickness and means an equivalent silicon oxide film thickness to which a thickness of a film is converted.</p> <p>[0036] On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia (HfO<sub>2</sub>) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed. The EOT of the high-k film 28 is about 0.5 nm. In each of MISFET 110, 120, and 130 for LOP, LSTP, and for high withstand voltage, respectively, a high-k film 28 is laminated on the silicon oxynitride films 22 and 24 or the thermally-oxidized film 26, thereby each gate insulating film is formed.</p> <p>[0037] On each high-k film 28, a gate electrode 32 is formed. The surface of the gate electrode 32 is silicided, thereby a nickel silicide layer 34 is formed. The gate length of the gate electrode 32 in the MISFET for LOP 100 is about 35 nm, and the gate length of the gate electrode 32 in the MISFET for LSTP 120 is about 50 nm. The gate length of the gate electrode 32 in the MISFET for high withstand voltage 130 is about 0.4 um. On the</p>

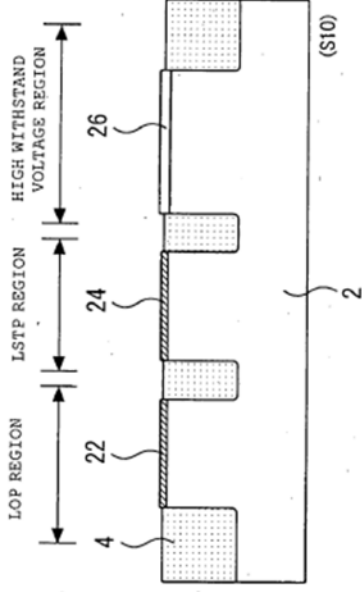
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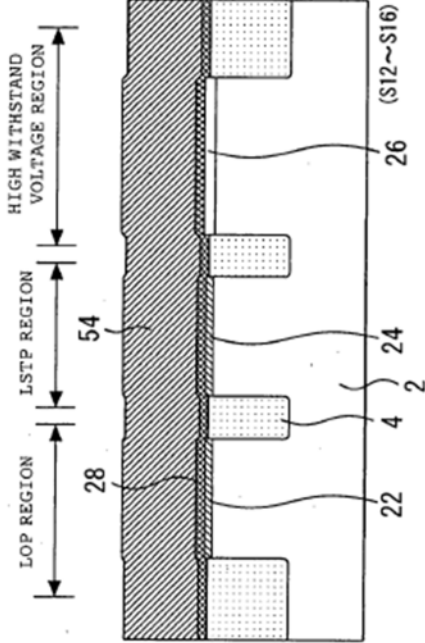
Claim	Claim Language	Exemplary Disclosures in Torii
		<p>sidewalls of each gate electrode 32 and the underlying gate insulating film, Side wall spacers 36 and 38 are formed.</p> <p>[0038] An interlayer insulating film 42 is formed on the Si substrate 2 so as to bury each gate insulating film, gate electrode 32, and sidewall spacers 36 and 38 formed as described above, and a contact plug 46 passing through the insulating film 42 and reaching the nickel silicide layer 12 on the source-drain region 10 is formed.</p> <p>[0039] In The SoC 100, as described above, MISFETs 110, 120, and 130 for LOP, LSTP, and for high withstand voltage, respectively, having gate insulating films is different thickness are formed.</p> <p>[0040] Specifically, the MISFET for LOP 110 is a low power-consumption transistor included the laminated film of the silicon oxynitride film 22 and the high-k film 28 as gate insulating film having a reduced EOT. The MISFET for LSTP 120 is a low-standby-power transistor using the laminated film of the silicon oxynitride film 24 and the high-k film 28 as gate insulating film, controlling the EOT to be low to some extent, and sufficiently securing the effective film thickness. The MISFET for high withstand voltage 130 is a high-withstand-voltage transistor securing the thickness of the thermal oxide film so as to withstand the external high voltage.</p> <p>[0042] The method for manufacturing an SoC 100 in the first embodiment of the present invention will be described below referring to FIGS. 1 to 9.</p> <p>[0045] On the Si substrate 2 in each region, a thermal oxide film 26 of a thickness of about 5 nm is formed (Step S2). Next, as FIG. 3 shows, the thermal oxide films 26 on the regions for LOP and LSTP are removed (Step S4). Concretely, after the region for high withstand voltage is coated with a resist mask, wet etching is performed using an aqueous Solution of hydrofluoric acid to selectively remove the thermal oxide films 26. Thereafter, the resist mask is removed.</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><i>FIG. 3</i></p>  <p>[0046] Next, as FIG. 4 shows, a silicon nitride film 50 is formed in each of the regions for LOP and LSTP (Step S6). Here, heat treatment is performed in an ammonia atmosphere at 600° C. for about 30 seconds. Thereby a silicon nitride film of a thickness of about 0.6nm is formed in each of the regions for LOP and LSTP. At this time, the surface of the thermal oxide film 26 is also simultaneously nitrided. Here, since the thickness of the silicon nitride film 50 can be easily controlled, a thin film of a uniform thickness to some extent can be formed. 0047 Next, as FIG. 5 shows, the silicon nitride film 50 in the region for LSTP is removed (Step S8). Here, after the regions for LOP and high withstand voltage are coated with a resist mask 52, wet etching is performed to remove the silicon nitride film 50. Thereafter, the resist mask 52 is removed.</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><b>FIG. 4</b></p>  <p style="text-align: center;"><b>FIG. 5</b></p>  <p>[0048] Next, heat treatment is performed in a nitrogen monoxide (NO) environment (Step S10). The temperature of the heat treatment is about 800 to 900 C., and the treating time is about 5 to 60 seconds. Thereby, as FIG. 6 shows, a silicon oxynitride film 24 of a thickness of about 1.3 nm and an EOT of about 1.0 nm is formed in the</p>

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Claim	Claim Language	Exemplary Disclosures in Torii
		<p>region for LSTP The silicon nitride film 50 formed in the region for LOP is oxidized to form a silicon oxynitride film 22 of an EOT of about 0.7 nm. At this time, the nitrogen content in the silicon oxynitride film 22 in the region for LOP is about 15 to 20%, and the nitrogen content in the silicon oxynitride film 24 in the region for LSTP is about 9%. The surface of the thermal oxide films 26 is further nitrided to form a silicon oxynitride film.</p> <p style="text-align: center;"><i>FIG. 6</i></p>  <p>[0049] Next, as FIG. 7 shows, a high-k film 28 is formed on the entire surface of the substrate (Step S12). Here, a high-k film of a thickness of 3.0 nm is deposited using hafnium chloride and water as the materials using an ALD (atomic layer deposition) method. Thereafter, heat treatment at about 700 C. is performed in a reduced pressure oxygen atmosphere for about 5 seconds (Step S14).</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><b>FIG. 7</b></p>  <p>[0050] Next, a non-doped polycrystalline silicon film 54 is formed on the high-k film 28 (Step S16). The non-doped polycrystalline silicon film 54 is a material film for gate electrodes 32, and here, it is deposited to have a thickness of about 120 nm. Thereafter, impurity ions for the gate electrodes are implanted into the non-doped polycrystalline silicon film 54 (Step S17).</p> <p>[0051] Next, as FIG. 8 shows, the polycrystalline silicon film 54 is processed for a gate electrode 32 of each region (Step S18). Here, a resist mask of a width of the gate electrode is formed on the polycrystalline silicon film 54 using a conventional method, and etching is performed using the resist mask to process the polycrystalline silicon film 54 and the high-k film 28 to have the width of the gate electrode 32. Thereby, a gate electrode 32 and a gate insulating film are formed in each of the regions for LOP, LSTP, and high withstand voltage.</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><b>FIG. 8</b></p> <p>[0058] According to the first embodiment, as described above, the insulating film of a laminate Structure wherein a high-k film 28 is deposited on silicon oxynitride films 22 and 24 as the gate insulating film of MISFETs 110 and 120 for LOP and LSTP, respectively. Here, by the use of the silicon Oxynitride films 22 and 24, the thin gate insulating films having little thickness difference can be uniformly formed. Therefore, the use of Such a structure enables a highly reliable semiconductor device to be formed even when both MISFETs for LOP and LSTP must be mounted in a chip.</p> <p>[0059] In the first embodiment, the silicon nitride film in the region for LSTP is removed, leaving the silicon nitride film 50 only in the region for LOP. Thereafter, by performing heat treatment in a nitrogen monoxide atmosphere, the silicon nitride film 50 is oxidized to form a silicon oxynitride film 22 in the region for LOP; on the other hand, a silicon oxynitride film 24 is formed in the region for LSTP. Thus, the use of oxynitride films realizes the formation of highly controlled uniform thin films. Particularly in the first embodiment, by using the silicon nitride film 50, and by using a means for forming an oxynitride film at the same time as the Oxidation thereof, highly controlled uniform thin films can be formed even when both the silicon oxynitride films in the region for LOP and the region for LSTP are thin, and have little thickness difference. Thereby, the target value recommended by ITRS for the 65-nm technology can also be achieved.</p>

**EXHIBIT 779A1**

Claim	Claim Language	Exemplary Disclosures in Torii
		<p>[0060] The nitrogen content of the silicon oxynitride films 22 and 24 formed in the first embodiment is 15 to 20% and 9%, respectively.</p> <p>[0061] For example, if high-k films are laminated on an insulating film to use as a gate insulating film, the high-k films may react with (or mixed to) the underlying films. In this case, there is a problem of increasing of the variation of the thickness, withstand voltage, and the like in the Surface of the insulating films, or the occurrence of defect in the boundary of the insulating films, leading to the deterioration of the characteristics of the transistor, and the lowering of the reliability of the semiconductor device. In the first embodiment, however, silicon oxynitride films containing the above-described contents of nitrogen are used as the gate insulating film. Since the mixing of nitrogen in the silicon oxide film can increase the density of the film, the above described reaction of the insulating film and the high-k film can be inhibited, and a highly reliable Semiconductor device can be formed.</p> <p>The description and annotation below are an example of a first transistor and a second transistor and their respective elements. A person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 120, as depicted in the annotations throughout. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 110. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 120 and the second transistor may be 110.</p> <p>For example: as can be seen below in Torii Figures 1 and 9, and by the process described in the citations above, Torii teaches the second gate insulating film which includes a second interface layer, highlighted in orange and indicated by element 26, and is in contact with the semiconductor substrate. Torii further discloses the second gate insulating film also includes a second high dielectric constant insulating film, highlighted in light green and indicated by element 28, formed on the first interface layer. Torii discloses the second high dielectric constant insulating film, or element 28, as “the high-k film such as a hafnia (HfO<sub>2</sub>) film 28.” See [0036]. A person of ordinary skill in the art would understand that “k” (or kappa) is the dielectric constant.</p>

FIG. 1

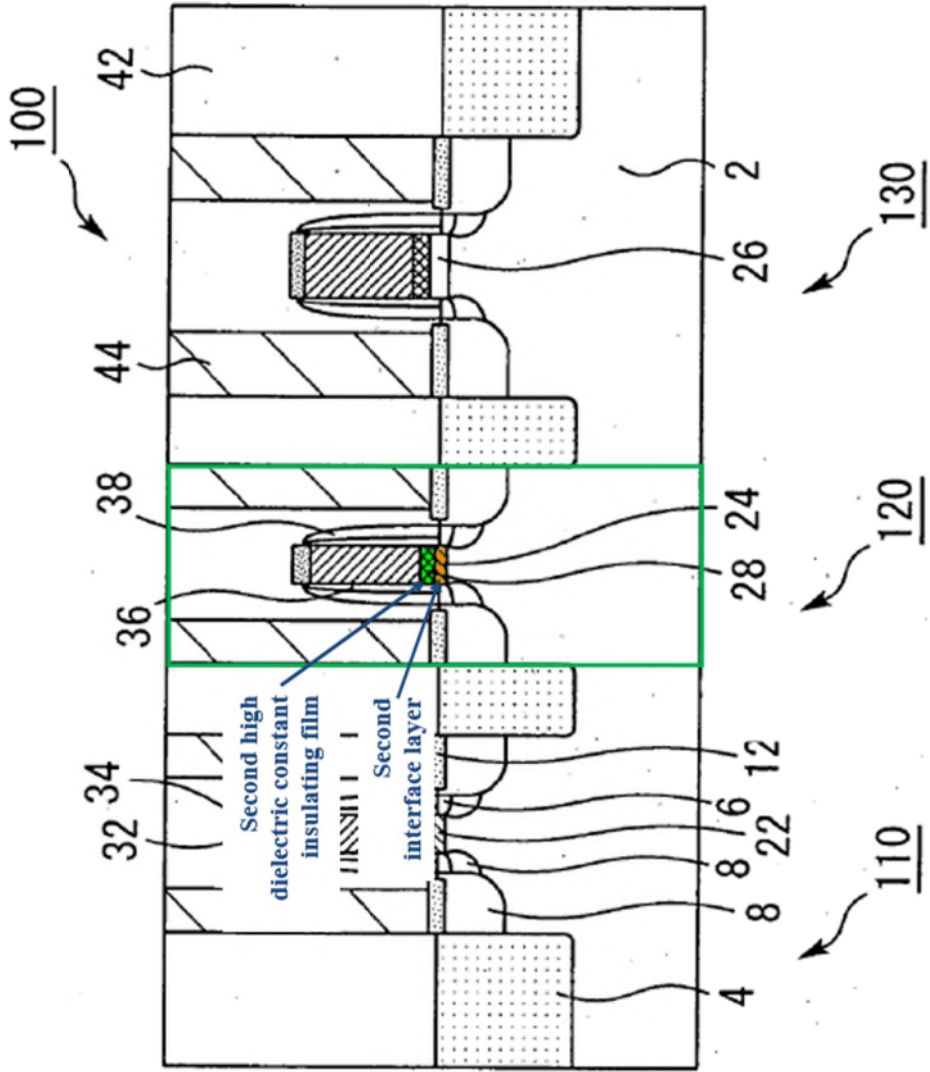
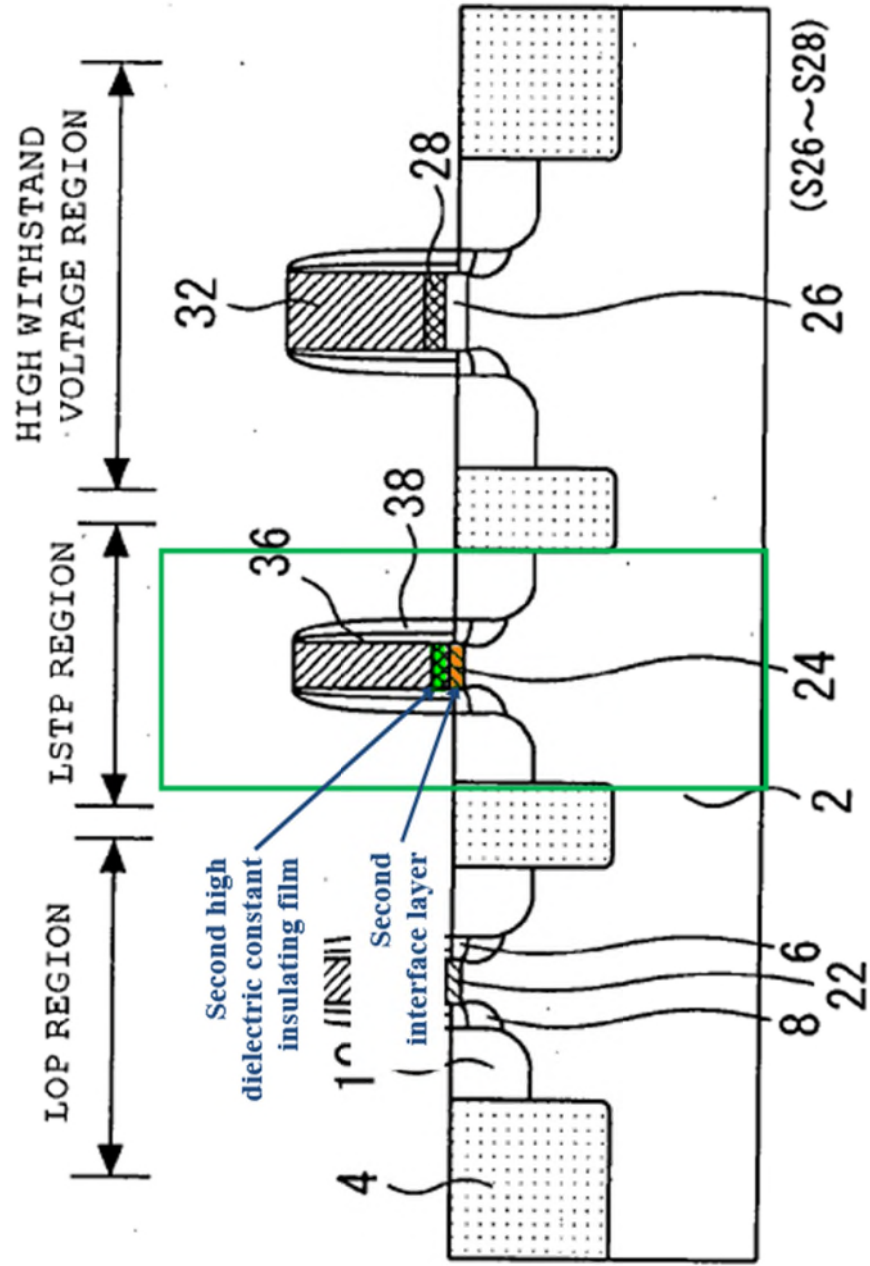


FIG. 9



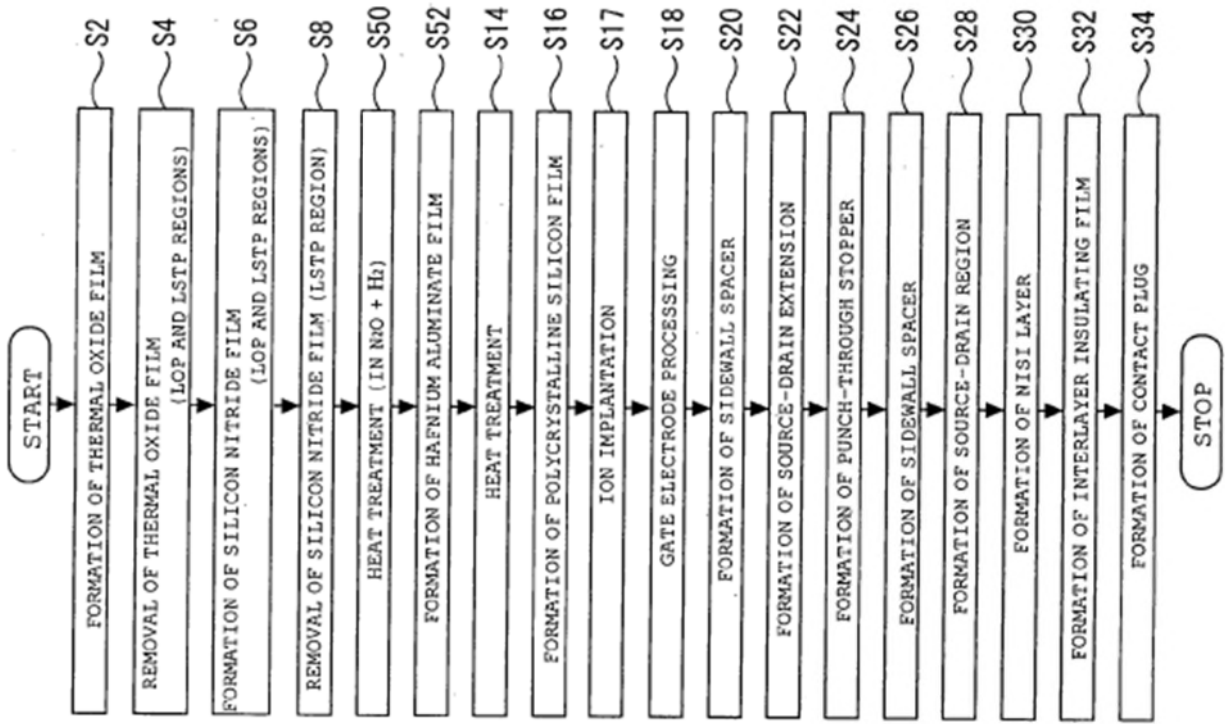
**EXHIBIT 779A1**

Claim	Claim Language	Exemplary Disclosures in Torii
		<p>[0075] Second Embodiment</p> <p>[0076] FIG. 12 is a flow diagram for illustrating the method for manufacturing an SoC according to the Second embodiment of the present invention.</p> <p>[0077] The SoC manufactured in the second embodiment is structurally similar to the SoC 100 described in the first embodiment. However, in the SoC of the second embodiment, the EOT of the silicon oxynitride film 22 of the MISFET for LOP 110 is about 0.7 nm, and the nitrogen content in the silicon oxynitride film is 15 to 25%. The thickness of the silicon oxynitride film 24 of the MISFET for LSTP120 is about 1.0 nm, and the EOT thereof is also about 1.0 nm. The nitrogen content in the silicon oxynitride film 24 is 1% or less.</p> <p>[0079] However, in the second embodiment, the heat treatment in a nitrogen monoxide atmosphere at about 800 to 900° C. for 5 to 60 seconds, described in Step S10 in the first embodiment, is substituted by the heat treatment in a mixed-gas atmosphere of dinitrogen oxide (N2O) and hydrogen (H) at about 850° C. for 5 seconds (Step S50). By doing this, as described above, a Silicon oxynitride film 22 having an EOT of about 0.7 nm, and the nitrogen content of 15 to 25% is formed in the region for LOP; and a silicon oxynitride film 24 of a thickness of about 1.0 nm, and the nitrogen content is 1% or less is formed in the region for LSTP</p> <p>[0081] In the SoC of the second embodiment, as in the SoC of the first embodiment, the thin gate insulating films having little thickness difference can be uniformly formed, by the use of the silicon oxynitride films 22 and 24. Therefore, the use of Such a structure enables a highly reliable semiconductor device to be formed even when both MISFETs for LOP and LSTP must be mounted in a chip.</p> <p>[0085] Since other parts are same as those in the first embodiment, the description thereof will be omitted.</p> <p>[0088] Also for example, by performing Steps S6 and S8 in the first and Second embodiments, the Step for forming the Silicon nitride film and the Step for removing the Silicon nitride film of the present invention are performed, respectively. Also by performing Step S10 in the first embodiment, or Step S50 in the second embodiment, the heat treating step of the present invention is performed. Also for example, by performing Step S12 in the first and Second embodiments, the Step for forming the high-k film of the present invention is performed. Also for example, by performing Steps S2 and S4 in the first and second embodiments, the step for</p>

**EXHIBIT 779A1**

<b>Claim</b>	<b>Claim Language</b>	<b>Exemplary Disclosures in Torii</b>
		forming the Silicon oxide film and the Step for removing the Silicon oxide film of the present invention are performed, respectively.

FIG. 12

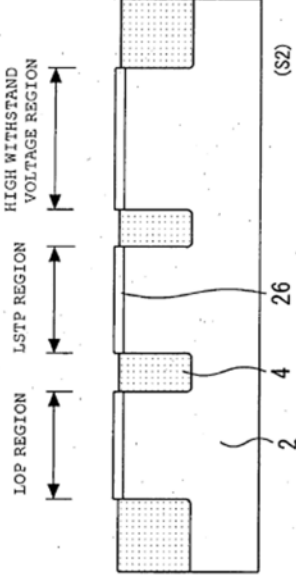


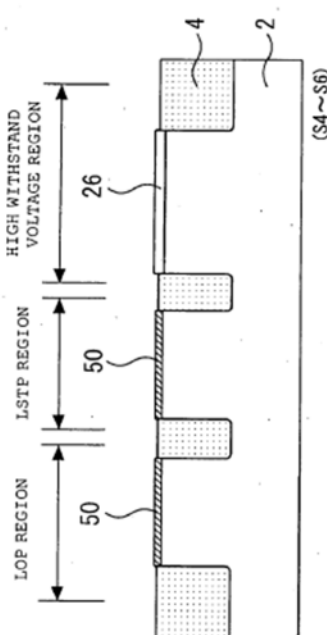
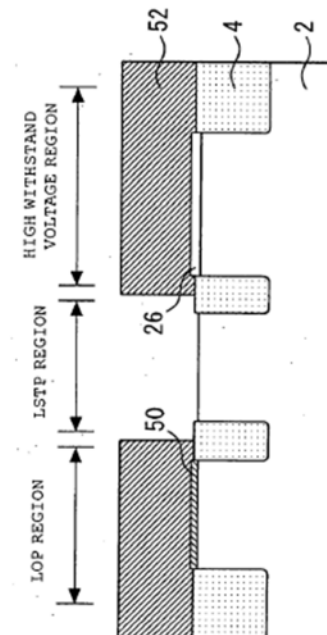
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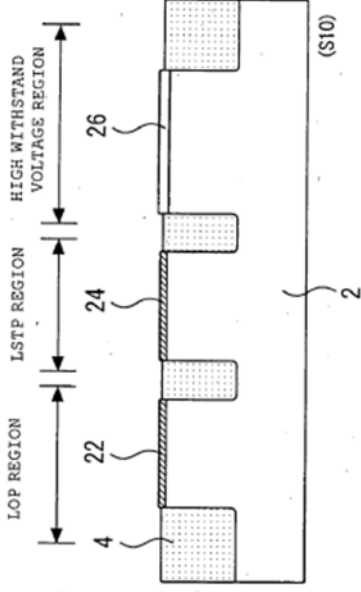
Claim	Claim Language	Exemplary Disclosures in Torii
1 [f]	the first interface layer has a thickness larger than that of the second interface layer, and	<p>See 1[c], [d]</p> <p>Torii, as evidenced by the example citations below, discloses the first interface layer has a thickness larger than that of the second interface layer.</p> <p>[0022] FIG. 1 is a schematic sectional view for illustrating an SoC (system on chip) 100 according to the first embodiments of the present invention.</p> <p>[0024] FIGS. 3 to 9 are schematic sectional views for illustrating the States in the process of manufacturing the SoC 100 in the first embodiment of the present invention.</p> <p>[0025] FIG. 10 is a graph showing the film-thickness distribution in the MISFET for LSTP according to the first embodiment of the present invention.</p> <p>[0034] In the MISFET for LOP 110, a silicon oxynitride film 22 is formed as an interfacial gate insulating film in the area sandwiched by source-drain extensions 6 on the Si substrate 2. In the MISFET for LSTP 120, a silicon oxynitride film 24 is formed in the equivalent area. In the MISFET for high withstand voltage 130, a surface-nitrided thermally oxidized (SiO<sub>2</sub>) film 26 is formed in the equivalent area. Here, the thickness of the silicon oxynitride film 22 in the MISFET for LOP 110 is about 0.9 to 0.95 nm, and the EOT thereof is about 0.7 nm. The thickness of the silicon oxynitride film 24 in the MISFET for LSTP 120 is about 1.3 nm, and the EOT thereof is about 1.0 nm. Furthermore, the thickness of the thermally-oxidized film 26 is about 5 nm. In short, the silicon oxynitride film 22 for the MISFET for LOP 110 is thinnest, and the thermally-oxidized film 26 for the MISFET for high withstand voltage 130 is thickest.</p> <p>[0035] Here, the EOT is an abbreviation of equivalent oxide thickness and means an equivalent silicon oxide film thickness to which a thickness of a film is converted.</p> <p>[0036] On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia (HfO<sub>2</sub>) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed. The EOT of the high-k film 28 is about 0.5 nm. In each of MISFET 110, 120, and 130 for LOP, LSTP, and for high withstand voltage,</p>

**EXHIBIT 779A1**

<b>Claim</b>	<b>Claim Language</b>	<b>Exemplary Disclosures in Torii</b>
		<p>respectively, a high-k film 28 is laminated on the silicon oxynitride films 22 and 24 or the thermally-oxidized film 26, thereby each gate insulating film is formed.</p> <p>[0039] In The SoC 100, as described above, MISFETs 110, 120, and 130 for LOP, LSTP, and for high withstand voltage, respectively, having gate insulating films is different thickness are formed.</p> <p>[0040] Specifically, the MISFET for LOP 110 is a low power-consumption transistor included the laminated film of the silicon oxynitride film 22 and the high-k film 28 as gate insulating film having a reduced EOT. The MISFET for LSTP 120 is a low-standby-power transistor using the laminated film of the silicon oxynitride film 24 and the high-k film 28 as gate insulating film, controlling the EOT to be low to some extent, and sufficiently securing the effective film thickness. The MISFET for high withstand voltage 130 is a high-withstand-voltage transistor securing the thickness of the thermal oxide film so as to withstand the external high voltage.</p> <p>[0042] The method for manufacturing an SoC 100 in the first embodiment of the present invention will be described below referring to FIGS. 1 to 9.</p> <p>[0045] On the Si substrate 2 in each region, a thermal oxide film 26 of a thickness of about 5 nm is formed (Step S2). Next, as FIG. 3 shows, the thermal oxide films 26 on the regions for LOP and LSTP are removed (Step S4). Concretely, after the region for high withstand voltage is coated with a resist mask, wet etching is performed using an aqueous Solution of hydrofluoric acid to selectively remove the thermal oxide films 26. Thereafter, the resist mask is removed.</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><i>FIG. 3</i></p>  <p>[0046] Next, as FIG. 4 shows, a silicon nitride film 50 is formed in each of the regions for LOP and LSTP (Step S6). Here, heat treatment is performed in an ammonia atmosphere at 600° C. to 700° C. for about 30 seconds. Thereby a silicon nitride film of a thickness of about 0.6nm is formed in each of the regions for LOP and LSTP. At this time, the surface of the thermal oxide film 26 is also simultaneously nitrided. Here, since the thickness of the silicon nitride film 50 can be easily controlled, a thin film of a uniform thickness to some extent can be formed. 0047 Next, as FIG. 5 shows, the silicon nitride film 50 in the region for LSTP is removed (Step S8). Here, after the regions for LOP and high withstand voltage are coated with a resist mask 52, wet etching is performed to remove the silicon nitride film 50. Thereafter, the resist mask 52 is removed.</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><b>FIG. 4</b></p>  <p style="text-align: center;"><b>FIG. 5</b></p>  <p>[0048] Next, heat treatment is performed in a nitrogen monoxide (NO) environment (Step S10). The temperature of the heat treatment is about 800 to 900 C., and the treating time is about 5 to 60 seconds. Thereby, as FIG. 6 shows, a silicon oxynitride film 24 of a thickness of about 1.3 nm and an EOT of about 1.0 nm is formed in the</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p>region for LSTP The silicon nitride film 50 formed in the region for LOP is oxidized to form a silicon oxynitride film 22 of an EOT of about 0.7 nm. At this time, the nitrogen content in the silicon oxynitride film 22 in the region for LOP is about 15 to 20%, and the nitrogen content in the silicon oxynitride film 24 in the region for LSTP is about 9%. The surface of the thermal oxide films 26 is further nitrated to form a silicon oxynitride film.</p> <p style="text-align: center;"><b>FIG. 6</b></p>  <p>[0058] According to the first embodiment, as described above, the insulating film of a laminate structure wherein a high-k film 28 is deposited on silicon oxynitride films 22 and 24 as the gate insulating film of MISFETs 110 and 120 for LOP and LSTP, respectively. Here, by the use of the silicon oxynitride films 22 and 24, the thin gate insulating films having little thickness difference can be uniformly formed. Therefore, the use of such a structure enables a highly reliable semiconductor device to be formed even when both MISFETs for LOP and LSTP must be mounted in a chip.</p> <p>[0059] In the first embodiment, the silicon nitride film in the region for LSTP is removed, leaving the silicon nitride film 50 only in the region for LOP. Thereafter, by performing heat treatment in a nitrogen monoxide atmosphere, the silicon nitride film 50 is oxidized to form a silicon oxynitride film 22 in the region for LOP; on the other hand, a silicon oxynitride film 24 is formed in the region for LSTP. Thus, the use of oxynitride films realizes the formation of highly controlled uniform thin films. Particularly in the first embodiment, by using the silicon nitride film 50, and by using a means for forming an oxynitride film at the same time as the oxidation thereof, highly controlled uniform thin films can be formed even when both the silicon oxynitride films in the</p>

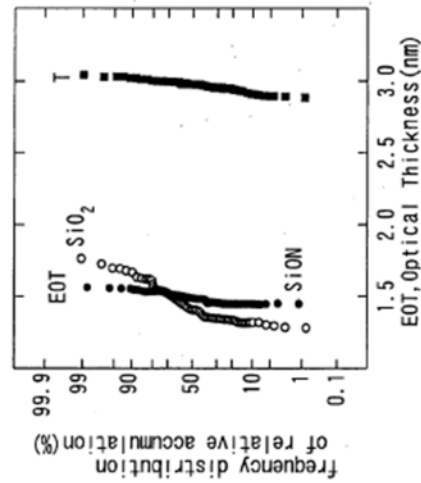
**EXHIBIT 779A1**

Claim	Claim Language	Exemplary Disclosures in Torii
		<p>region for LOP and the region for LSTP are thin, and have little thickness difference. Thereby, the target value recommended by ITRS for the 65-nm technology can also be achieved.</p> <p>[0060] The nitrogen content of the silicon oxynitride films 22 and 24 formed in the first embodiment is 15 to 20% and 9%, respectively.</p> <p>[0062] FIG. 10 is a graph showing the film-thickness distribution in the MISFET for LSTP according to the first embodiment. In FIG. 10, the ordinate indicates frequency distribution of relative accumulation (%), and the abscissa indicates EOT of film or optical film thickness (nm). FIG. 11 is a diagram showing the leakage current of the MISFET for LSTP according to the first embodiment. In FIG. 11, the ordinate indicates frequency distribution of relative accumulation (%), and the abscissa indicates the density of leakage current (A/cm) of each film. 0063. In FIGS. 10 and 11, the line plotted with black circles shows the case of the silicon Oxynitride film 24, and the line plotted with black Squares shows the case of the high-k film 28. Furthermore, for comparison, the line plotted with white circles shows the case of the conventional SiO<sub>2</sub> film without mixing nitrogen.</p> <p>[0064] As FIG. 10 shows, when an silicon oxide film is formed using a conventional method, there is a variation of film thickness as large as about 11%. Therefore, it is considered that it is difficult to form each of two variations of films of which have 0.2 nm to 0.4 nm disparities in the thickness, uniformly, by means of controlling the thickness of interfacial silicon oxide film.</p> <p>[0065] While the thickness of the entire silicon oxynitride film in the first embodiment is about 1.3 nm, and the variation is restricted to about 2.4%. Also, the thickness of the High-k film 28 in the first embodiment is about 3.0 nm, and the variation is restricted to about 2.5%. That is, use of the silicon oxynitride film improves uniformity of films. Therefore, it is possible to form two variations of films on a substrate, uniformly, even if the difference in the thickness of the two films is about 0.2 nm to 0.4 nm.</p> <p>[0066] Referring to FIG. 11 showing leak current in each film, the variation of the leak current in the conventional silicon oxide film is higher. On the other hand, according to the silicon oxynitride film 24 and the high-k film 28 having better uniformity and described in the first embodiment, in both of the gate insulating films of 1.2 nm in EOT and of 1.5 nm in EOT, the variation of the leak currents are lower.</p>

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Claim	Claim Language	Exemplary Disclosures in Torii
		<p>[0067] Here, the formation of the high-k film 28, after forming the silicon oxynitride films 22 and 24, and the thermal oxide film 26 as the interfacial gate insulating film of each gate insulating film, can be performed in one Step. Therefore, the gate insulating films having different thickness can be easily formed, and the productivity of the Semiconductor devices can be improved</p> <p>[0069] Furthermore, in the first embodiment, the case wherein the thickness of the silicon nitride film 50 is about 0.6 nm is described. However, the present invention is not limited thereto, but the adequate thickness may be Selected considering the thickness of finally formed silicon oxynitride films for LOP and LSTP, the thickness difference thereof, and increase in thickness during subsequent steps. However, the thickness of the finally required gate insulating film is preferably about 2.0 nm or less in EOT, and therefore, the thickness of the silicon nitride film 50 formed in the ammoniac atmosphere is preferably about 1.0 nm or less. If the silicon nitride film 50 is excessively thin, there is a problem of oxidation resistance, So the thickness of the silicon nitride film 50 is preferably about 0.4 nm or more also for maintaining the thickness difference from the silicon nitride film 50 in the region for LSTP. However, if the problem of oxidation resistance or the like can be evaded, the thickness is not limited thereto.</p>

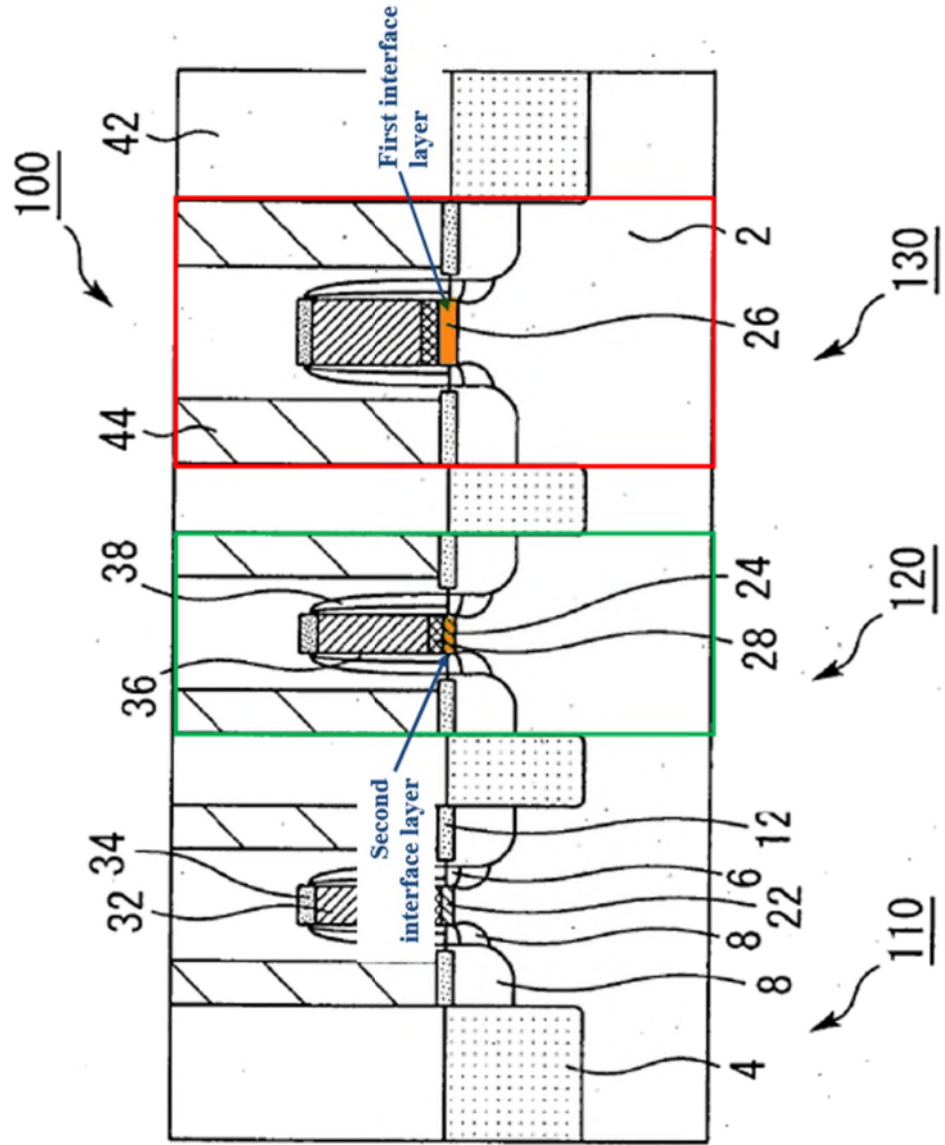
**FIG. 10**



**EXHIBIT 779A1**

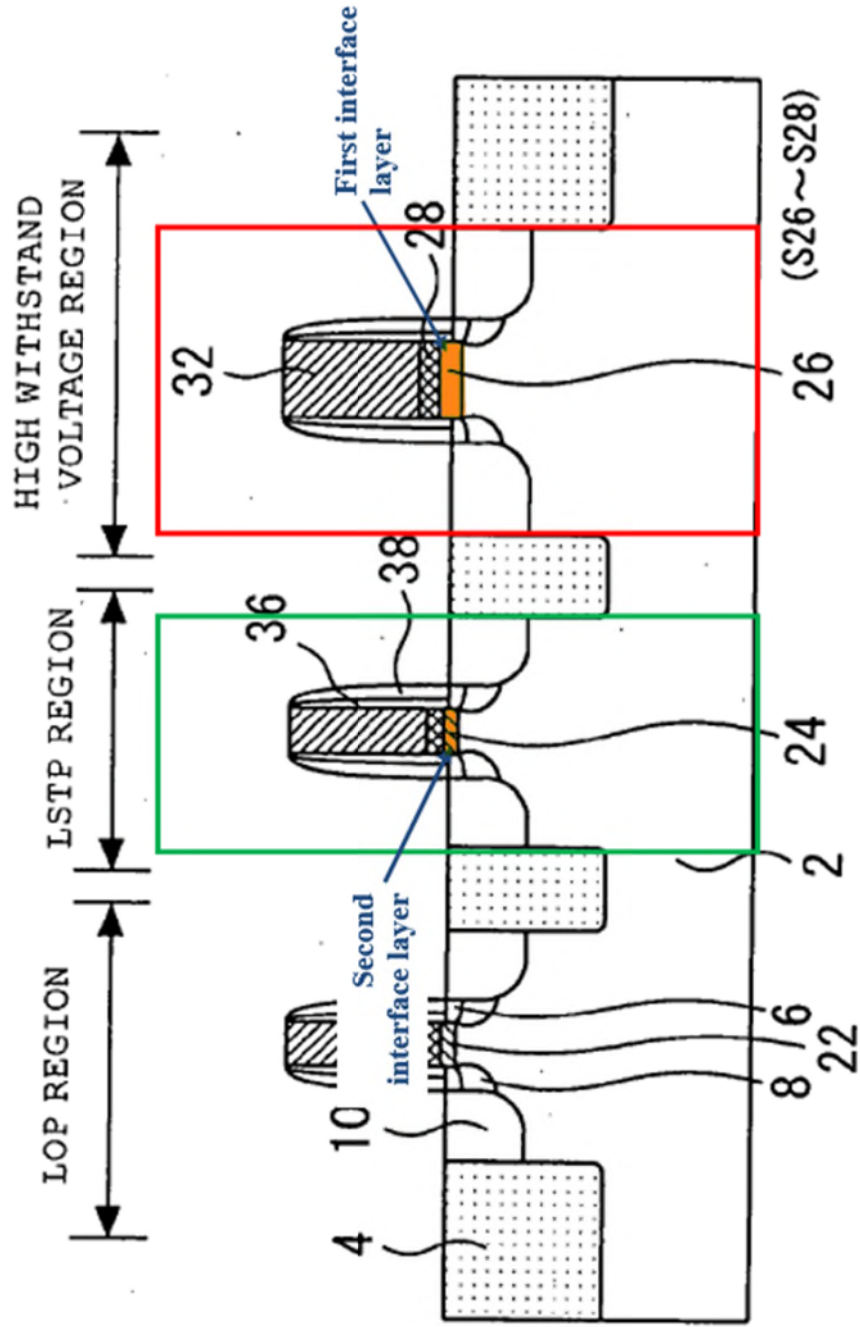
<b>Claim</b>	<b>Claim Language</b>	<b>Exemplary Disclosures in Torii</b>
		<p>[0070] In the present invention, the temperature and time for the heat treatment when the silicon oxynitride films 22 and 24 are formed are not limited to the temperature and time for the heat treatment described in the first embodiment. In the present invention, the thickness and the thickness difference, or the combination of nitrogen contents of the oxynitride films in the region for LOP and the region for LSTP can be controlled by changing the temperature and time of the heat treatment in nitrogen monoxide. However, when both the control of the nitrogen content in each film and the control of the thickness of the oxynitride film 24 formed in the region for LSTP are considered, the temperature for the heat treatment is preferably within a range between about 700° C. and 1000 C.</p> <p>The description and annotation below are an example of a first transistor and a second transistor and their respective elements. A person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 120, as depicted in the annotations throughout. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 110. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 120 and the second transistor may be 110.</p> <p>For example: as can be seen below in Torii Figures 1 and 9, and by the process described in the citations above, Torii teaches the first interface layer, indicated by element 26, within the first MIS transistor, outlined in red, having a thickness larger than that of the second interface layer, indicated by element 24, within the second MIS transistor, outlined in green. Specifically, the first interface layer is disclosed to have a thickness of “5 nm” [0034] and the second interface layer is disclosed to have a thickness of “1.3 nm” [0034].</p>

FIG. 1



Exemplary Disclosures in Torii

FIG. 9



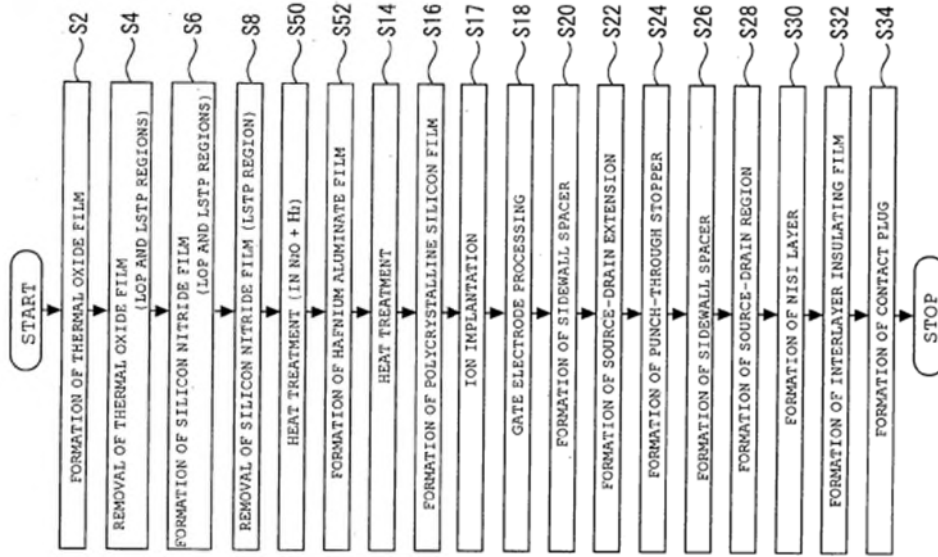
**EXHIBIT 779A1**

Claim	Claim Language	Exemplary Disclosures in Torii
		<p>[0075] Second Embodiment</p> <p>[0076] FIG. 12 is a flow diagram for illustrating the method for manufacturing an SoC according to the Second embodiment of the present invention.</p> <p>[0077] The SoC manufactured in the second embodiment is structurally similar to the SoC 100 described in the first embodiment. However, in the SoC of the second embodiment, the EOT of the silicon oxynitride film 22 of the MISFET for LOP 110 is about 0.7 nm, and the nitrogen content in the silicon oxynitride film is 15 to 25%. The thickness of the silicon oxynitride film 24 of the MISFET for LSTP120 is about 1.0 nm, and the EOT thereof is also about 1.0 nm. The nitrogen content in the silicon oxynitride film 24 is 1% or less.</p> <p>[0079] However, in the second embodiment, the heat treatment in a nitrogen monoxide atmosphere at about 800 to 900° C. for 5 to 60 seconds, described in Step S10 in the first embodiment, is substituted by the heat treatment in a mixed-gas atmosphere of dinitrogen oxide (N2O) and hydrogen (H) at about 850° C. for 5 seconds (Step S50). By doing this, as described above, a Silicon oxynitride film 22 having an EOT of about 0.7 nm, and the nitrogen content of 15 to 25% is formed in the region for LOP; and a silicon oxynitride film 24 of a thickness of about 1.0 nm, and the nitrogen content is 1% or less is formed in the region for LSTP</p> <p>[0081] In the SoC of the second embodiment, as in the SoC of the first embodiment, the thin gate insulating films having little thickness difference can be uniformly formed, by the use of the silicon oxynitride films 22 and 24. Therefore, the use of Such a structure enables a highly reliable semiconductor device to be formed even when both MISFETs for LOP and LSTP must be mounted in a chip.</p> <p>[0085] Since other parts are same as those in the first embodiment, the description thereof will be omitted.</p> <p>[0088] Also for example, by performing Steps S6 and S8 in the first and Second embodiments, the Step for forming the Silicon nitride film and the Step for removing the Silicon nitride film of the present invention are performed, respectively. Also by performing Step S10 in the first embodiment, or Step S50 in the second embodiment, the heat treating step of the present invention is performed. Also for example, by performing Step S12 in the first and Second embodiments, the Step for forming the high-k film of the present invention is performed. Also for example, by performing Steps S2 and S4 in the first and second embodiments, the step for</p>

Exemplary Disclosures in Torii

forming the Silicon oxide film and the Step for removing the Silicon oxide film of the present invention are performed, respectively.

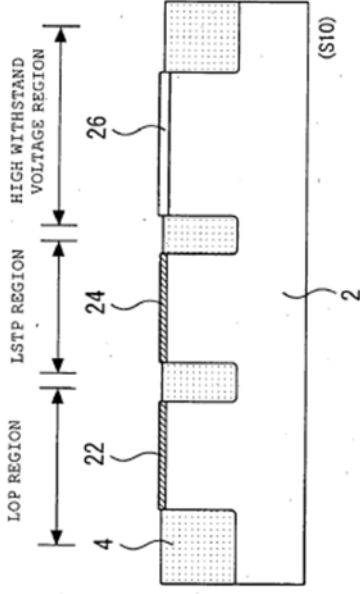
FIG. 12



See 1[d]-[e]

**EXHIBIT 779A1**

<b>Exemplary Disclosures in Torii</b>		
<b>Claim</b>	<b>Claim Language</b>	
1 [g]	each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film.	<p>Torii, as evidenced by the example citations below, discloses each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film.</p> <p>[0034] In the MISFET for LOP 110, a silicon oxynitride film 22 is formed as an interfacial gate insulating film in the area sandwiched by source-drain extensions 6 on the Si substrate 2. In the MISFET for LSTP 120, a silicon oxynitride film 24 is formed in the equivalent area. In the MISFET for high withstand voltage 130, a surface-nitrided thermally oxidized (SiO<sub>2</sub>) film 26 is formed in the equivalent area. Here, the thickness of the silicon oxynitride film 22 in the MISFET for LOP 110 is about 0.9 to 0.95 nm, and the EOT thereof is about 0.7 nm. The thickness of the silicon oxynitride film 24 in the MISFET for LSTP 120 is about 1.3 nm, and the EOT thereof is about 1.0 nm. Furthermore, the thickness of the thermally-oxidized film 26 is about 5 nm. In short, the silicon oxynitride film 22 for the MISFET for LOP 110 is thinnest, and the thermally-oxidized film 26 for the MISFET for high withstand voltage 130 is thickest.</p> <p>[0048] Next, heat treatment is performed in a nitrogen monoxide (NO) environment (Step S10). The temperature of the heat treatment is about 800 to 900 C., and the treating time is about 5 to 60 seconds. Thereby, as FIG. 6 shows, a silicon oxynitride film 24 of a thickness of about 1.3 nm and an EOT of about 1.0 nm is formed in the region for LSTP. The silicon nitride film 50 formed in the region for LOP is oxidized to form a silicon oxynitride film 22 of an EOT of about 0.7 nm. At this time, the nitrogen content in the silicon oxynitride film 22 in the region for LOP is about 15 to 20%, and the nitrogen content in the silicon oxynitride film 24 in the region for LSTP is about 9%. The surface of the thermal oxide films 26 is further nitrided to form a silicon oxynitride film.</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p style="text-align: center;"><b>FIG. 6</b></p>  <p>[0058] According to the first embodiment, as described above, the insulating film of a laminate Structure wherein a high-k film 28 is deposited on silicon oxynitride films 22 and 24 as the gate insulating film of MISFETs 110 and 120 for LOP and LSTP, respectively. Here, by the use of the silicon Oxynitride films 22 and 24, the thin gate insulating films having little thickness difference can be uniformly formed. Therefore, the use of Such a structure enables a highly reliable semiconductor device to be formed even when both MISFETs for LOP and LSTP must be mounted in a chip.</p> <p>[0059] In the first embodiment, the silicon nitride film in the region for LSTP is removed, leaving the silicon nitride film 50 only in the region for LOP. Thereafter, by performing heat treatment in a nitrogen monoxide atmosphere, the silicon nitride film 50 is oxidized to form a silicon oxynitride film 22 in the region for LOP; on the other hand, a silicon oxynitride film 24 is formed in the region for LSTP. Thus, the use of oxynitride films realizes the formation of highly controlled uniform thin films. Particularly in the first embodiment, by using the silicon nitride film 50, and by using a means for forming an oxynitride film at the same time as the Oxidation thereof, highly controlled uniform thin films can be formed even when both the silicon oxynitride films in the region for LOP and the region for LSTP are thin, and have little thickness difference. Thereby, the target value recommended by ITRS for the 65-nm technology can also be achieved.</p>

**EXHIBIT 779A1**

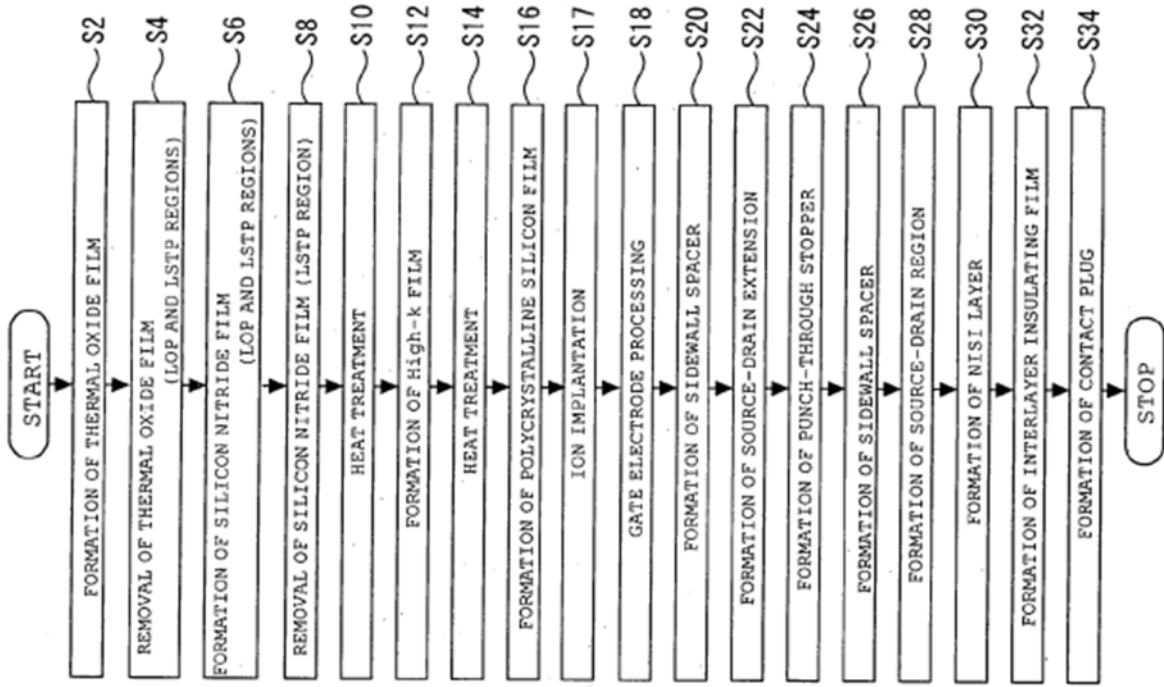
Claim	Claim Language	Exemplary Disclosures in Torii
		<p>[0060] The nitrogen content of the silicon oxynitride films 22 and 24 formed in the first embodiment is 15 to 20% and 9%, respectively.</p> <p>The description and annotation below are an example of a first transistor and a second transistor and their respective elements. A person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 120, as depicted in the annotations throughout. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 110. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 120 and the second transistor may be 110.</p> <p>For example: as discloses the first interface layer, or element 26, as “a surface-nitrided thermally oxidized (SiO<sub>2</sub>) film” and later as “thermal oxide film.” See [0034], [0045]. A person of ordinary skill in the art would understand that a “thermal oxide film” is a silicon dioxide (SiO<sub>2</sub>) film. Torii further discloses the second interface layer, or element 24, as “a silicon oxynitride film.” See [0034].</p> <p>[0075] Second Embodiment</p> <p>[0076] FIG. 12 is a flow diagram for illustrating the method for manufacturing an SoC according to the Second embodiment of the present invention.</p> <p>[0077] The SoC manufactured in the second embodiment is structurally similar to the SoC 100 described in the first embodiment. However, in the SoC of the second embodiment, the EOT of the silicon oxynitride film 22 of the MISFET for LOP 110 is about 0.7 nm, and the nitrogen content in the silicon oxynitride film is 15 to 25%. The thickness of the silicon oxynitride film 24 of the MISFET for LSTP120 is about 1.0 nm, and the EOT thereof is also about 1.0 nm. The nitrogen content in the silicon oxynitride film 24 is 1% or less.</p> <p>[0079] However, in the second embodiment, the heat treatment in a nitrogen monoxide atmosphere at about 800 to 900° C. for 5 to 60 seconds, described in Step S10 in the first embodiment, is substituted by the heat treatment in a mixed-gas atmosphere of dinitrogen oxide (N<sub>2</sub>O) and hydrogen (H) at about 850° C. for 5 seconds (Step S50). By doing this, as described above, a Silicon oxynitride film 22 having an EOT of about 0.7 nm, and the</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p>nitrogen content of 15 to 25% is formed in the region for LOP; and a silicon oxynitride film 24 of a thickness of about 1.0 nm, and the nitrogen content is 1% or less is formed in the region for LSTP</p> <p>[0085] Since other parts are same as those in the first embodiment, the description thereof will be omitted.</p> <p><i>FIG. 12</i></p> <pre> graph TD     START([START]) --&gt; S2[FORMATION OF THERMAL OXIDE FILM]     S2 --&gt; S4[REMOVAL OF THERMAL OXIDE FILM (LOP AND LSTP REGIONS)]     S4 --&gt; S6[FORMATION OF SILICON NITRIDE FILM (LOP AND LSTP REGIONS)]     S6 --&gt; S8[REMOVAL OF SILICON NITRIDE FILM (LSTP REGION)]     S8 --&gt; S50[HEAT TREATMENT (IN NIO + HI)]     S50 --&gt; S52[FORMATION OF HAFNIUM ALUMINATE FILM]     S52 --&gt; S14[HEAT TREATMENT]     S14 --&gt; S16[FORMATION OF POLYCRYSTALLINE SILICON FILM]     S16 --&gt; S17[ION IMPLANTATION]     S17 --&gt; S18[GATE ELECTRODE PROCESSING]     S18 --&gt; S20[FORMATION OF SIDEWALL SPACER]     S20 --&gt; S22[FORMATION OF SOURCE-DRAIN EXTENSION]     S22 --&gt; S24[FORMATION OF PUNCH-THROUGH STOPPER]     S24 --&gt; S26[FORMATION OF SIDEWALL SPACER]     S26 --&gt; S28[FORMATION OF SOURCE-DRAIN REGION]     S28 --&gt; S30[FORMATION OF NISI LAYER]     S30 --&gt; S32[FORMATION OF INTERLAYER INSULATING FILM]     S32 --&gt; S34[FORMATION OF CONTACT PLUG]     S34 --&gt; STOP([STOP])     </pre>

**EXHIBIT 779A1**

Claim	Claim Language	Exemplary Disclosures in Torii
2 [a]	<p>The semiconductor device of claim 1, wherein the first gate electrode includes first sidewall spacers formed on side surfaces thereof and first insulating spacers interposed between the first gate electrode and the first sidewall spacers,</p>	<p>See 1[d]-[e]</p> <p>Torii, as evidenced by the example citations below, discloses the semiconductor device of claim 1, wherein the first gate electrode includes first sidewall spacers formed on side surfaces thereof and first insulating spacers interposed between the first gate electrode and the first sidewall spacers</p> <p>[0022] FIG. 1 is a schematic sectional view for illustrating an SoC (system on chip) 100 according to the first embodiments of the present invention.</p> <p>[0023] FIG. 2 is a flow diagram for illustrating the method for manufacturing an SoC 100 in the first embodiment of the present invention.</p>

FIG. 2



**EXHIBIT 779A1**

Claim	Claim Language	Exemplary Disclosures in Torii
		<p>[0024] FIGS. 3 to 9 are schematic sectional views for illustrating the States in the process of manufacturing the SoC 100 in the first embodiment of the present invention.</p> <p>[0037] On each high-k film 28, a gate electrode 32 is formed. The surface of the gate electrode 32 is silicided, thereby a nickel silicide layer 34 is formed. The gate length of the gate electrode 32 in the MISFET for LOP 100 is about 35 nm, and the gate length of the gate electrode 32 in the MISFET for LSTP 120 is about 50 nm. The gate length of the gate electrode 32 in the MISFET for high withstand voltage 130 is about 0.4 μm. On the sidewalls of each gate electrode 32 and the underlying gate insulating film, Side wall spacers 36 and 38 are formed.</p> <p>[0038] An interlayer insulating film 42 is formed on the Si substrate 2 so as to bury each gate insulating film, gate electrode 32, and sidewall spacers 36 and 38 formed as described above, and a contact plug 46 passing through the insulating film 42 and reaching the nickel silicide layer 12 on the source-drain region 10 is formed.</p> <p>[0052] 0.052 Next, on the sidewalls of each gate electrode 32 and each underlying gate insulating film of regions for LOP, LSTP, and high withstand voltage, sidewall spacers 36 are formed (Step S20). Concretely, the sidewall spacers 36 are formed by depositing a silicon nitride film of a thickness of about 5 nm So as to coat each gate electrode 32 and the like, and performing etch back to the silicon nitride film.</p> <p>[0053] Next, a source-drain extension 6 is formed in each of regions for LOP, LSTP, and high withstand voltage (Step S22). Here, as ions are implanted using an implanting energy of 2 keV and a dose of 3x10<sup>18</sup>/cm. At this time, the gate electrode 32 and the sidewall spacer 36 in each region are used as the mask. Thereafter, B ions are implanted to form punch-through stoppers 8 of a p-conductivity type (Step S24).</p> <p>[0054] Next, as FIG. 9 shows, sidewall spacers 38 are further formed on the sidewall spacers 36 (Step S26). Concretely, a silicon oxide film, a silicon nitride film, and a silicon oxide film are deposited in this order on the entire surface of the substrate. At this time, the thicknesses of the films are about 15 nm, about 25 nm, and about 35 nm, respectively. Thereafter, anisotropic dry etching is performed using the silicon nitride film of the middle layer as the etching stopper to etch the overlying silicon oxide film; and then, the silicon nitride film exposed on the surface is removed by anisotropic dry etching using the underlying silicon oxide film as the etching stopper.</p>

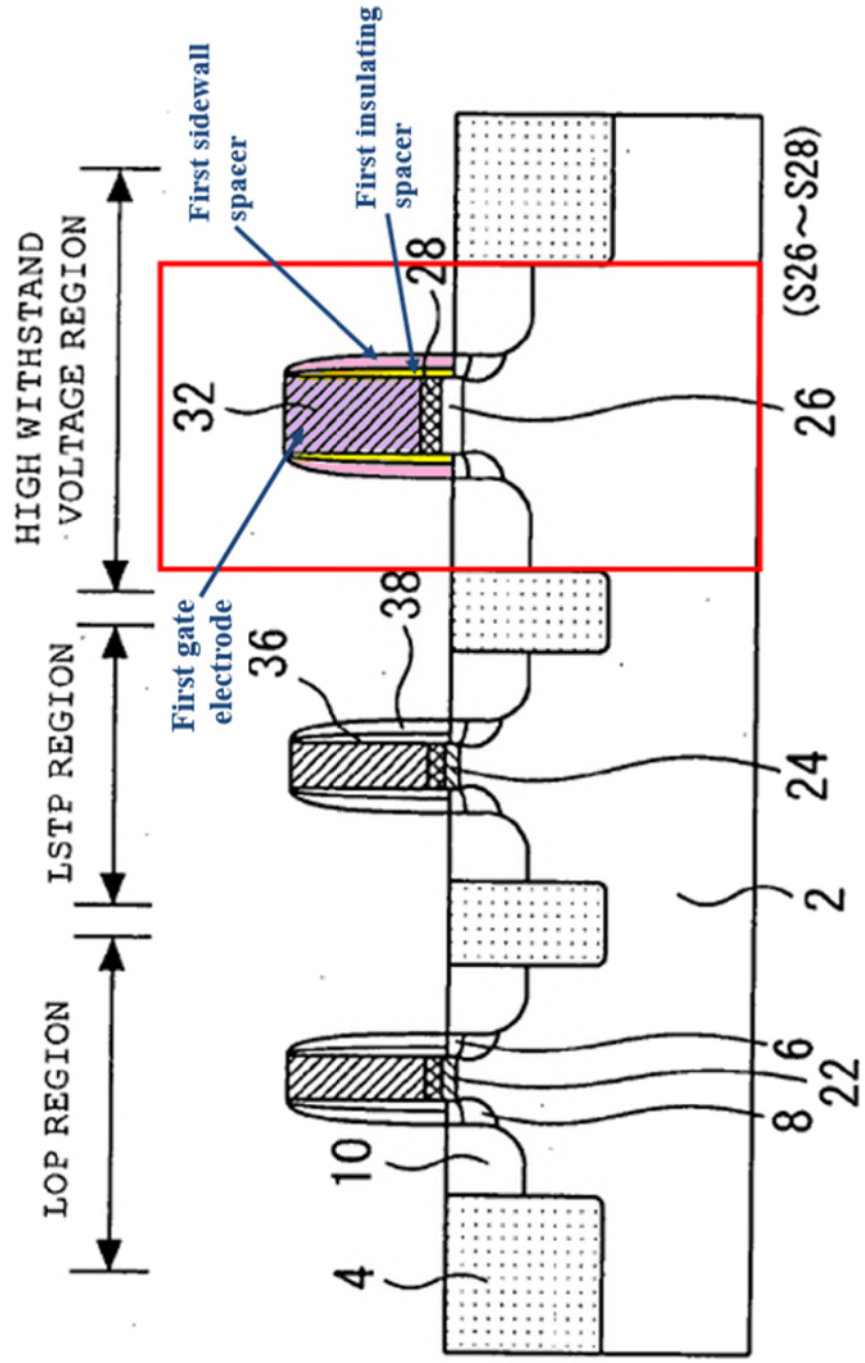
**EXHIBIT 779A1**

Claim	Claim Language	Exemplary Disclosures in Torii
		<p>Furthermore, the underlying silicon oxide film is removed using wet etching. Thereby, sidewall spacers 38 each composed of a silicon oxide film, a silicon nitride film, and a silicon oxide film are formed on the outside of each sidewall spacer 36.</p> <p>The description and annotation below are an example of a first transistor and a second transistor and their respective elements. A person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 120, as depicted in the annotations throughout. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 110. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 120 and the second transistor may be 110.</p> <p>For example: as can be seen below in Torii Figures 1 and 9, and by the process described in the citations above, Torii teaches the semiconductor device of claim 1, wherein the first gate electrode, indicated by element 32 and highlighted in purple, includes first sidewall spacers, disclosed within element 38 and highlighted in pink, formed on side surfaces thereof and first insulating spacers, indicated by element 36 and highlighted in yellow, interposed between the first gate electrode and the first sidewall spacers.</p> <p>Further, Torii discloses the first insulating spacer, 36, as being made of silicon nitride and being a thickness of about 5 nm. “The sidewall spacers 36 are formed by depositing a silicon nitride film of a thickness of about 5 nm So as to coat each gate electrode 32 and the like, and performing etch back to the silicon nitride film.” [0052].</p> <p>Further, Torii discloses the first sidewall spacer, the silicon oxide film with a thickness of about 15 nm, which is a film within element 38. Specifically, Torii discloses that element 38 is made of three films: a silicon oxide film with a thickness of about 15 nm, a silicon nitride film of about 25 nm, and a silicon oxide film of about 35 nm, which “are deposited in this order on the entire surface of the substrate.” [0054] “Thereby, sidewall spacers 38 each composed of a silicon oxide film, a silicon nitride film, and a silicon oxide film are formed on the outside of each sidewall spacer 36.” [0054]</p> <p>In summary, Torii discloses a first insulating spacer (being the silicon nitride film of about 5 nm indicated at element 36) and a first sidewall spacer being the silicon oxide film of about 15 nm disclosed within element 38). These spacers are formed on the sides of the first gate electrode and the first insulating spacer is interposed between the first sidewall spacer and the first gate electrode.</p>



Exemplary Disclosures in Torii

FIG. 9



**EXHIBIT 779A1**

<b>Claim</b>	<b>Claim Language</b>	<b>Exemplary Disclosures in Torii</b>
2 [b]	<p>the second gate electrode includes second sidewall spacers formed on side surfaces thereof and second insulating spacers interposed between the second gate electrode and the second sidewall spacers</p>	<p>To the extent Torii does not expressly disclose this limitation, a person of ordinary skill in the art would have determined that this limitation is either inherent and/or obvious to one of ordinary skill in the art in view of the teachings of Torii. Further, one of ordinary skill in the art would have been motivated to modify Torii or combine it with any of the present prior art references found in Defendants' Invalidation Contentions and any supplements thereto and the relevant section of charts for other prior art for the '779 Patent in a manner that would result in the subject matter of this limitation given, at the very least, the person's understanding of the state of the art, the problems addressed and solved in the prior art, and the teachings of Torii.</p>
	<p>the second gate electrode includes second sidewall spacers formed on side surfaces thereof and second insulating spacers interposed between the second gate electrode and the second sidewall spacers</p>	<p>Torii, as evidenced by the example citations below, discloses the second gate electrode includes second sidewall spacers formed on side surfaces thereof and second insulating spacers interposed between the second gate electrode and the second sidewall spacers</p> <p>[0022] FIG. 1 is a schematic sectional view for illustrating an SoC (system on chip) 100 according to the first embodiments of the present invention.</p> <p>[0024] FIGS. 3 to 9 are schematic sectional views for illustrating the States in the process of manufacturing the SoC 100 in the first embodiment of the present invention.</p> <p>[0037] On each high-k film 28, a gate electrode 32 is formed. The surface of the gate electrode 32 is silicided, thereby a nickel silicide layer 34 is formed. The gate length of the gate electrode 32 in the MISFET for LOP 100 is about 35 nm, and the gate length of the gate electrode 32 in the MISFET for LSTP 120 is about 50 nm. The gate length of the gate electrode 32 in the MISFET for high withstand voltage 130 is about 0.4 um. On the sidewalls of each gate electrode 32 and the underlying gate insulating film, Side wall spacers 36 and 38 are formed.</p> <p>[0038] An interlayer insulating film 42 is formed on the Si substrate 2 so as to bury each gate insulating film, gate electrode 32, and sidewall spacers 36 and 38 formed as described above, and a contact plug 46 passing through the insulating film 42 and reaching the nickel silicide layer 12 on the source-drain region 10 is formed.</p>

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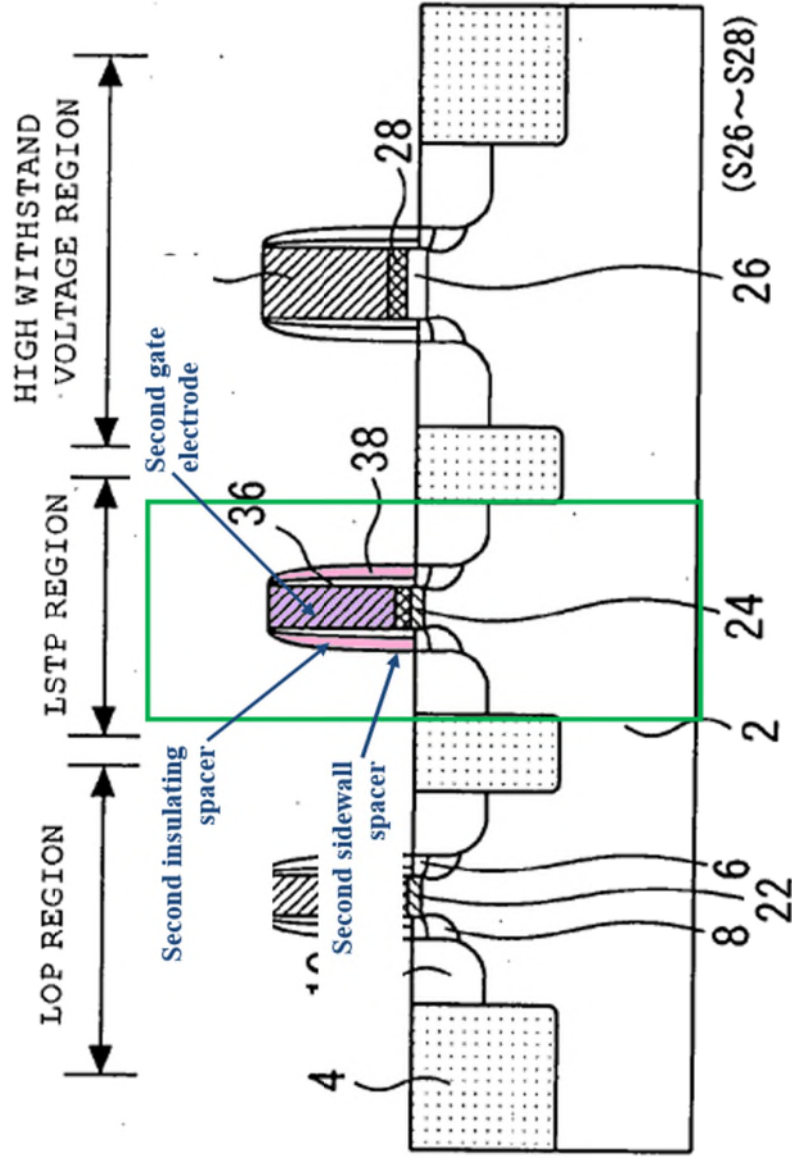
Claim	Claim Language	Exemplary Disclosures in Torii
		<p>[0052] 0.052 Next, on the sidewalls of each gate electrode 32 and each underlying gate insulating film of regions for LOP, LSTP, and high withstand voltage, sidewall spacers 36 are formed (Step S20). Concretely, the sidewall spacers 36 are formed by depositing a silicon nitride film of a thickness of about 5 nm So as to coat each gate electrode 32 and the like, and performing etch back to the silicon nitride film.</p> <p>[0053] Next, a source-drain extension 6 is formed in each of regions for LOP, LSTP, and high withstand voltage (Step S22). Here, as ions are implanted using an implanting energy of 2 keV and a dose of 3x10<sup>10</sup>/cm. At this time, the gate electrode 32 and the sidewall spacer 36 in each region are used as the mask. Thereafter, B ions are implanted to form punch-through stoppers 8 of a p-conductivity type (Step S24).</p> <p>[0054] Next, as FIG. 9 shows, sidewall spacers 38 are further formed on the sidewall spacers 36 (Step S26). Concretely, a silicon oxide film, a silicon nitride film, and a silicon oxide film are deposited in this order on the entire surface of the substrate. At this time, the thicknesses of the films are about 15 nm, about 25 nm, and about 35 nm, respectively. Thereafter, anisotropic dry etching is per formed using the silicon nitride film of the middle layer as the etching stopper to etch the overlying silicon oxide film; and then, the silicon nitride film exposed on the surface is removed by anisotropic dry etching using the underlying silicon oxide film as the etching stopper. Furthermore, the underlying silicon oxide film is removed using wet etching. Thereby, sidewall spacers 38 each composed of a silicon oxide film, a silicon nitride film, and a silicon oxide film are formed on the outside of each sidewall spacer 36.</p> <p>The annotation below are an example of a first transistor and a second transistor and their respective elements. A person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 120, as depicted in the annotations throughout. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 110. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 120 and the second transistor may be 110.</p> <p>To the extent Torii does not expressly disclose this limitation, a person of ordinary skill in the art would have determined that this limitation is either inherent and/or obvious to one of ordinary skill in the art in view of the teachings of Torii. Further, one of ordinary skill in the art would have been motivated to modify Torii or combine it with any of the present prior art references found in Defendants' Invalidity Contentions and any supplements thereto and the relevant section of charts for other prior art for the '779 Patent in a manner that would result in the</p>

**EXHIBIT 779A1**

Claim	Claim Language	Exemplary Disclosures in Torii
		<p>subject matter of this limitation given, at the very least, the person's understanding of the state of the art, the problems addressed and solved in the prior art, and the teachings of Torii.</p> <p>The description and annotation below are an example of a first transistor and a second transistor and their respective elements. A person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 120, as depicted in the annotations throughout. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 110. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 120 and the second transistor may be 110.</p> <p>For example: as can be seen below in Torii Figures 1 and 9, and by the process described in the citations above, Torii teaches the semiconductor device of claim 1, wherein the second gate electrode, indicated by element 32 and highlighted in purple, includes second sidewall spacers, indicated by element 38 and highlighted in pink, formed on side surfaces thereof and second insulating spacers, disclosed within element 38 and highlighted in pink, interposed between the second gate electrode and the second sidewall spacers.</p> <p>Further, Torii discloses the second insulating spacer, being the silicon nitride film of about 25 nm, and second sidewall spacer, being the silicon oxide film of about 25 nm, both of which are films within element 38. Specifically, Torii discloses that element 38 is made of three films: a silicon oxide film with a thickness of about 15 nm, a silicon nitride film of about 25 nm, and a silicon oxide film of about 35 nm, which “are deposited in this order on the entire surface of the substrate.” [0054] “Thereby, sidewall spacers 38 each composed of a silicon oxide film, a silicon nitride film, and a silicon oxide film are formed on the outside of each sidewall spacer 36.” [0054]</p> <p>In summary, Torii discloses a second insulating spacer (being the silicon nitride film of about 25 nm disclosed within element 38) and a second sidewall spacer (being the silicon oxide film of about 35 nm disclosed within element 38). These spacers are formed on the sides of the second gate electrode and the second insulating spacer is interposed between the second sidewall spacer and the second gate electrode.</p>



FIG. 9



Claim Language

Claim

**EXHIBIT 779A1**

Claim	Claim Language	Exemplary Disclosures in Torii
2 [c]	the first insulating spacers are thinner than the second insulating spacers.	<p>To the extent Torii does not expressly disclose this limitation, a person of ordinary skill in the art would have determined that this limitation is either inherent and/or obvious to one of ordinary skill in the art in view of the teachings of Torii. Further, one of ordinary skill in the art would have been motivated to modify Torii or combine it with any of the present prior art references found in Defendants' Invalidation Contentions and any supplements thereto and the relevant section of charts for other prior art for the '779 Patent in a manner that would result in the subject matter of this limitation given, at the very least, the person's understanding of the state of the art, the problems addressed and solved in the prior art, and the teachings of Torii.</p> <p>See 2[a].</p> <p>Torii, as evidenced by the example citations below, discloses the first insulating spacers are thinner than the second insulating spacers.</p> <p>[0022] FIG. 1 is a schematic sectional view for illustrating an SoC (system on chip) 100 according to the first embodiments of the present invention.</p> <p>[0024] FIGS. 3 to 9 are schematic sectional views for illustrating the States in the process of manufacturing the SoC 100 in the first embodiment of the present invention.</p> <p>[0037] On each high-k film 28, a gate electrode 32 is formed. The surface of the gate electrode 32 is silicided, thereby a nickel silicide layer 34 is formed. The gate length of the gate electrode 32 in the MISFET for LOP 100 is about 35 nm, and the gate length of the gate electrode 32 in the MISFET for LSTP 120 is about 50 nm. The gate length of the gate electrode 32 in the MISFET for high withstand voltage 130 is about 0.4 um. On the sidewalls of each gate electrode 32 and the underlying gate insulating film, Side wall spacers 36 and 38 are formed.</p> <p>[0038] An interlayer insulating film 42 is formed on the Si substrate 2 so as to bury each gate insulating film, gate electrode 32, and sidewall spacers 36 and 38 formed as described above, and a contact plug 46 passing through the insulating film 42 and reaching the nickel silicide layer 12 on the source-drain region 10 is formed.</p> <p>[0052] 0.052 Next, on the sidewalls of each gate electrode 32 and each underlying gate insulating film of regions for LOP, LSTP, and high withstand voltage, sidewall spacers 36 are formed (Step S20). Concretely, the sidewall</p>

**EXHIBIT 779A1**

<b>Claim</b>	<b>Claim Language</b>	<b>Exemplary Disclosures in Torii</b>
		<p>spacers 36 are formed by depositing a silicon nitride film of a thickness of about 5 nm So as to coat each gate electrode 32 and the like, and performing etch back to the silicon nitride film.</p> <p>[0053] Next, a source-drain extension 6 is formed in each of regions for LOP, LSTP, and high withstand voltage (Step S22). Here, as ions are implanted using an implanting energy of 2 keV and a dose of 3x10<sup>10</sup>/cm. At this time, the gate electrode 32 and the sidewall spacer 36 in each region are used as the mask. Thereafter, B ions are implanted to form punch-through stoppers 8 of a p-conductivity type (Step S24).</p> <p>[0054] Next, as FIG. 9 shows, sidewall spacers 38 are further formed on the sidewall spacers 36 (Step S26). Concretely, a silicon oxide film, a silicon nitride film, and a silicon oxide film are deposited in this order on the entire surface of the substrate. At this time, the thicknesses of the films are about 15 nm, about 25 nm, and about 35 nm, respectively. Thereafter, anisotropic dry etching is per formed using the silicon nitride film of the middle layer as the etching stopper to etch the overlying silicon oxide film; and then, the silicon nitride film exposed on the surface is removed by anisotropic dry etching using the underlying silicon oxide film as the etching stopper. Furthermore, the underlying silicon oxide film is removed using wet etching. Thereby, sidewall spacers 38 each composed of a silicon oxide film, a silicon nitride film, and a silicon oxide film are formed on the outside of each sidewall spacer 36.</p> <p>The description and annotation below are an example of a first transistor and a second transistor and their respective elements. A person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 120, as depicted in the annotations throughout. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 110. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 120 and the second transistor may be 110.</p> <p>For example: as can be seen below in Torii Figures 1 and 9, and by the process described in the citations above, Torii teaches the first insulating spacers, indicated by element 26 and highlighted in yellow, are thinner than the second insulating spacers, disclosed within element 38 and highlighted in pink.</p>

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<b>Claim</b>	<b>Claim Language</b>	<b>Exemplary Disclosures in Torii</b>
		<p>Further, Torii discloses the first insulating spacer, 36, as being made of silicon nitride and being a thickness of about 5 nm. “The sidewall spacers 36 are formed by depositing a silicon nitride film of a thickness of about 5 nm So as to coat each gate electrode 32 and the like, and performing etch back to the silicon nitride film.” [0052].</p> <p>Further, Torii discloses the second insulating spacer, being the silicon nitride film of about 25 nm, which is a film within element 38. Specifically, Torii discloses that element 38 is made of three films: a silicon oxide film with a thickness of about 15 nm, a silicon nitride film of about 25 nm, and a silicon oxide film of about 35 nm, which “are deposited in this order on the entire surface of the substrate.” [0054] “Thereby, sidewall spacers 38 each composed of a silicon oxide film, a silicon nitride film, and a silicon oxide film are formed on the outside of each sidewall spacer 36.” [0054]</p> <p>In summary, Torii discloses a first insulating spacer (being the silicon nitride film of about 5 nm indicated at element 36) and a second insulating spacer (being the silicon nitride film of about 25 nm disclosed within element 38) wherein the first insulating spacer is thinner than the second insulating spacer. Here, the first insulating spacer is about 5 nm and the second insulating spacer is about 25 nm.</p>

FIG. 1

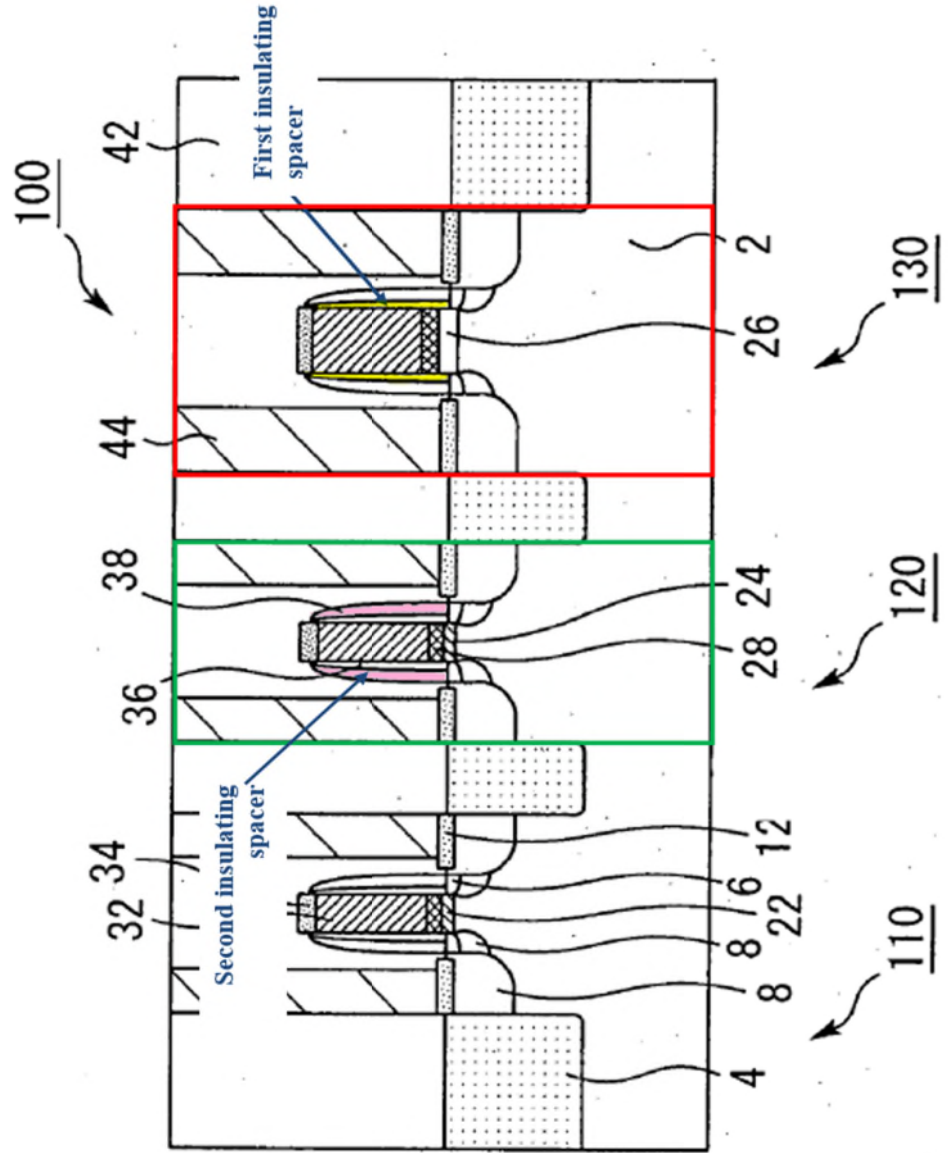
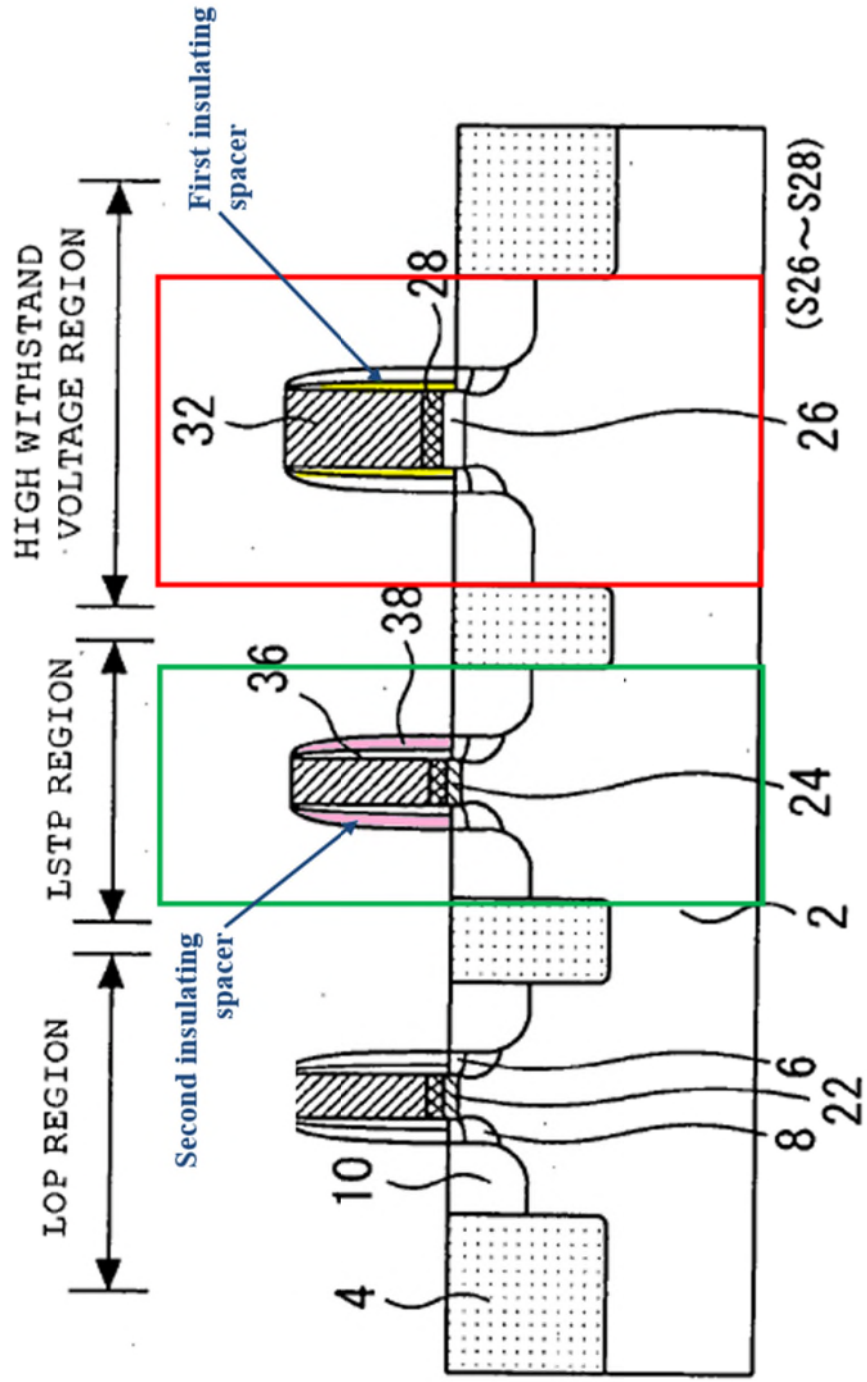


FIG. 9

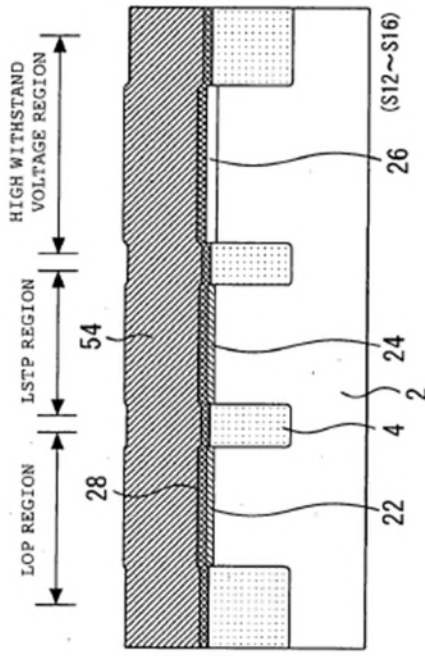


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Claim	Claim Language	Exemplary Disclosures in Torii
7	The semiconductor device of claim 2, wherein each of the first insulating spacers and the second insulating spacers is made of a silicon nitride film.	<p>To the extent Torii does not expressly disclose this limitation, a person of ordinary skill in the art would have determined that this limitation is either inherent and/or obvious to one of ordinary skill in the art in view of the teachings of Torii. Further, one of ordinary skill in the art would have been motivated to modify Torii or combine it with any of the present prior art references found in Defendants' Invalidation Contentions and any supplements thereto and the relevant section of charts for other prior art for the '779 Patent in a manner that would result in the subject matter of this limitation given, at the very least, the person's understanding of the state of the art, the problems addressed and solved in the prior art, and the teachings of Torii.</p> <p><i>See 2[a]-[b]</i></p> <p>Torii, as evidenced by the example citations below, discloses the semiconductor device of claim 2, wherein each of the first insulating spacers and the second insulating spacers is made of a silicon nitride film.</p> <p>[0022] FIG. 1 is a schematic sectional view for illustrating an SoC (system on chip) 100 according to the first embodiments of the present invention.</p> <p>[0024] FIGS. 3 to 9 are schematic sectional views for illustrating the States in the process of manufacturing the SoC 100 in the first embodiment of the present invention.</p> <p>[0037] On each high-k film 28, a gate electrode 32 is formed. The surface of the gate electrode 32 is silicided, thereby a nickel silicide layer 34 is formed. The gate length of the gate electrode 32 in the MISFET for LOP 100 is about 35 nm, and the gate length of the gate electrode 32 in the MISFET for LSTP 120 is about 50 nm. The gate length of the gate electrode 32 in the MISFET for high withstand voltage 130 is about 0.4 um. On the sidewalls of each gate electrode 32 and the underlying gate insulating film, Side wall spacers 36 and 38 are formed.</p> <p>[0038] An interlayer insulating film 42 is formed on the Si substrate 2 so as to bury each gate insulating film, gate electrode 32, and sidewall spacers 36 and 38 formed as described above, and a contact plug 46 passing through the insulating film 42 and reaching the nickel silicide layer 12 on the source-drain region 10 is formed.</p> <p>[0052] 0.052 Next, on the sidewalls of each gate electrode 32 and each underlying gate insulating film of regions for LOP, LSTP, and high withstand voltage, sidewall spacers 36 are formed (Step S20). Concretely, the sidewall</p>

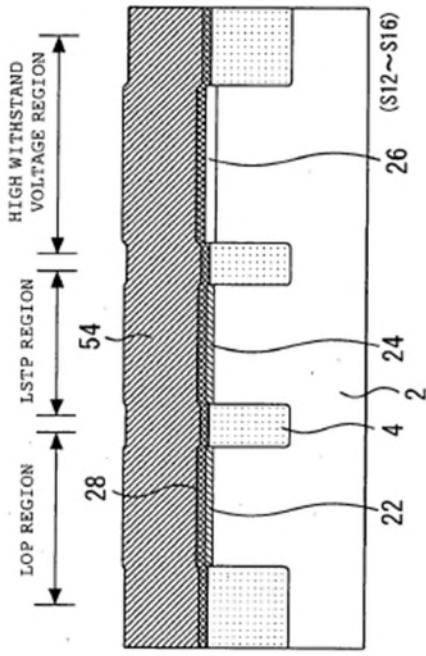
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Claim	Claim Language	Exemplary Disclosures in Torii
		<p>spacers 36 are formed by depositing a silicon nitride film of a thickness of about 5 nm So as to coat each gate electrode 32 and the like, and performing etch back to the silicon nitride film.</p> <p>[0053] Next, a source-drain extension 6 is formed in each of regions for LOP, LSTP, and high withstand voltage (Step S22). Here, as ions are implanted using an implanting energy of 2 keV and a dose of 3x10<sup>10</sup>/cm. At this time, the gate electrode 32 and the sidewall spacer 36 in each region are used as the mask. Thereafter, B ions are implanted to form punch-through stoppers 8 of a p-conductivity type (Step S24).</p> <p>[0054] Next, as FIG. 9 shows, sidewall spacers 38 are further formed on the sidewall spacers 36 (Step S26). Concretely, a silicon oxide film, a silicon nitride film, and a silicon oxide film are deposited in this order on the entire surface of the substrate. At this time, the thicknesses of the films are about 15 nm, about 25 nm, and about 35 nm, respectively. Thereafter, anisotropic dry etching is per formed using the silicon nitride film of the middle layer as the etching stopper to etch the overlying silicon oxide film; and then, the silicon nitride film exposed on the surface is removed by anisotropic dry etching using the underlying silicon oxide film as the etching stopper. Furthermore, the underlying silicon oxide film is removed using wet etching. Thereby, sidewall spacers 38 each composed of a silicon oxide film, a silicon nitride film, and a silicon oxide film are formed on the outside of each sidewall spacer 36.</p> <p>To the extent Torii does not expressly disclose this limitation, a person of ordinary skill in the art would have determined that this limitation is either inherent and/or obvious to one of ordinary skill in the art in view of the teachings of Torii. Further, one of ordinary skill in the art would have been motivated to modify Torii or combine it with any of the present prior art references found in Defendants' Invalidity Contentions and any supplements thereto and the relevant section of charts for other prior art for the '779 Patent in a manner that would result in the subject matter of this limitation given, at the very least, the person's understanding of the state of the art, the problems addressed and solved in the prior art, and the teachings of Torii.</p> <p>See 2[a]-[b]</p>

Claim	Claim Language	Exemplary Disclosures in Torii
12	The semiconductor device of claim 1, wherein each of the first and second high dielectric constant insulating films contains hafnium or zirconium.	<p>Torii, as evidenced by the example citations below, discloses the semiconductor device of claim 1, wherein each of the first and second high dielectric constant insulating films contains hafnium or zirconium.</p> <p>[0036] On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia (HfO<sub>2</sub>) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed. The EOT of the high-k film 28 is about 0.5 nm. In each of MISFET 110, 120, and 130 for LOP, LSTP, and for high withstand voltage, respectively, a high-k film 28 is laminated on the silicon oxynitride films 22 and 24 or the thermally-oxidized film 26, thereby each gate insulating film is formed.</p> <p>[0049] Next, as FIG. 7 shows, a high-k film 28 is formed on the entire surface of the substrate (Step S12). Here, a high-k film of a thickness of 3.0 nm is deposited using hafnium chloride and water as the materials using an ALD (atomic layer deposition) method. Thereafter, heat treatment at about 700 C. is performed in a reduced pressure oxygen atmosphere for about 5 seconds (Step S14).</p> <p style="text-align: center;"><b>FIG. 7</b></p>  <p>[0071] In the first embodiment, as the high-k film, the metal oxide film, Such as hafnia (HfO<sub>2</sub>), hafnium aluminate (Hf Al-O.), alumina (AlO<sub>3</sub>), lanthanum oxide (La-O.), praseodymium oxide (PrO), yttrium oxide</p>

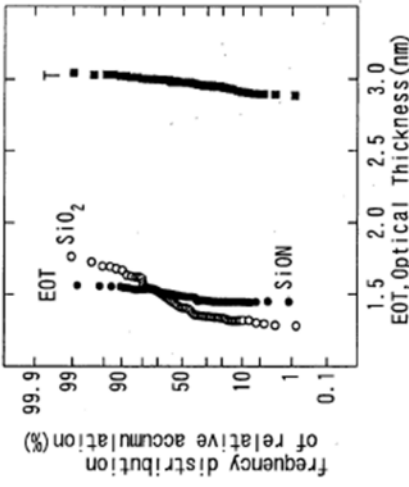
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Claim	Claim Language	Exemplary Disclosures in Torii
13	The semiconductor device of claim 1, wherein the first and second high dielectric constant insulating films are equal in thickness.	<p>(YO), tantalumoxide (Ta-Os), niobium oxide (NbO), titanium oxide (TiO2), and cerium oxide (CeO2), or the nitride thereof, or the Solid solution thereof, or the Solid Solution of these metal oxides and SiO2, or the film of a titanate Such as Strontium barium titanate ((BaSr)TiO) may also be used. For example, when a hafnium aluminate film is used, it is considered to form the film by an ALD method using trimethyl aluminum, hafnium chloride and water, and by heat treatment at about 1000 C. for about 1 second, in the formation of the high-k film 28 in Step S12 described in the first embodiment. When a hafnium silicon oxinitride film is used, it is considered to form the film by forming the hafnium silicate film and nitridation thereof (annealing in atmosphere of ammonia (NH)) using ALD method or MOCVD (metal organic chemical vapor deposition) method, in place of Step S12 described in the first embodiment. The method for forming the high-k film is not limited to the ALD method, but other methods, Such as a CVD (chemical vapor deposition) method, a Sputtering method, a Vacuum evaporation method, and the combination of these methods and a reoxidation method, can be used for forming the film.</p> <p>See 1[d]-[e]</p> <p>Torii, as evidenced by the example citations below, discloses the semiconductor device of claim 1, wherein the first and second high dielectric constant insulating films are equal in thickness.</p> <p>[0022] FIG. 1 is a schematic sectional view for illustrating an SoC (system on chip) 100 according to the first embodiments of the present invention.</p> <p>[0024] FIGS. 3 to 9 are schematic sectional views for illustrating the States in the process of manufacturing the SoC 100 in the first embodiment of the present invention.</p> <p>[0025] FIG. 10 is a graph showing the film-thickness distribution in the MISFET for LSTP according to the first embodiment of the present invention.</p> <p>[0036] On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia (HfO<sub>2</sub>) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed. The EOT of the high-k film 28 is about 0.5 nm. In each of MISFET 110, 120, and 130 for LOP, LSTP, and for high withstand voltage, respectively, a high-k film 28 is laminated on the silicon oxynitride films 22 and 24 or the thermally-oxidized film 26, thereby each gate insulating film is formed.</p>

Claim	Claim Language	Exemplary Disclosures in Torii
		<p>[0049] Next, as FIG. 7 shows, a high-k film 28 is formed on the entire surface of the substrate (Step S12). Here, a high-k film of a thickness of 3.0 nm is deposited using hafnium chloride and water as the materials using an ALD (atomic layer deposition) method. Thereafter, heat treatment at about 700 C. is performed in a reduced pressure oxygen atmosphere for about 5 seconds (Step S14).</p> <p style="text-align: center;"><b>FIG. 7</b></p>  <p>[0062] FIG. 10 is a graph showing the film-thickness distribution in the MISFET for LSTP according to the first embodiment. In FIG. 10, the ordinate indicates frequency distribution of relative accumulation (%), and the abscissa indicates EOT of film or optical film thickness (nm). FIG. 11 is a diagram showing the leakage current of the MISFET for LSTP according to the first embodiment. In FIG. 11, the ordinate indicates frequency distribution of relative accumulation (%), and the abscissa indicates the density of leakage current (A/cm) of each film. 0063. In FIGS. 10 and 11, the line plotted with black circles shows the case of the silicon Oxynitride film 24, and the line plotted with black Squares shows the case of the high-k film 28. Furthermore, for comparison, the line plotted with white circles shows the case of the conventional SiO<sub>2</sub> film without mixing nitrogen.</p>

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Claim	Claim Language	Exemplary Disclosures in Torii
		<p>[0064] As FIG. 10 shows, when an silicon oxide film is formed using a conventional method, there is a variation of film thickness as large as about 11%. Therefore, it is considered that it is difficult to form each of two variations of films of which have 0.2 nm to 0.4 nm disparities in the thickness, uniformly, by means of controlling the thickness of interfacial silicon oxide film.</p> <p>[0065] While the thickness of the entire silicon oxynitride film in the first embodiment is about 1.3 nm, and the variation is restricted to about 2.4%. Also, the thickness of the High-k film 28 in the first embodiment is about 3.0 nm, and the variation is restricted to about 2.5%. That is, use of the silicon oxynitride film improves uniformity of films. Therefore, it is possible to form two variations of films on a substrate, uniformly, even if the difference in the thickness of the two films is about 0.2 nm to 0.4 nm.</p> <p>[0066] Referring to FIG. 11 showing leak current in each film, the variation of the leak current in the conventional silicon oxide film is higher. On the other hand, according to the silicon oxynitride film 24 and the high-k film 28 having better uniformity and described in the first embodiment, in both of the gate insulating films of 1.2 nm in EOT and of 1.5 nm in EOT, the variation of the leak currents are lower.</p> <p>[0067] Here, the formation of the high-k film 28, after forming the silicon oxynitride films 22 and 24, and the thermal oxide film 26 as the interfacial gate insulating film of each gate insulating film, can be performed in one Step. Therefore, the gate insulating films having different thickness can be easily formed, and the productivity of the Semiconductor devices can be improved.</p> <p>[0069] Furthermore, in the first embodiment, the case wherein the thickness of the silicon nitride film 50 is about 0.6 nm is described. However, the present invention is not limited thereto, but the adequate thickness may be Selected considering the thickness of finally formed silicon oxynitride films for LOP and LSTP, the thickness difference thereof, and increase in thickness during subsequent steps. However, the thickness of the finally required gate insulating film is preferably about 2.0 nm or less in EOT, and therefore, the thickness of the silicon nitride film 50 formed in the ammoniac atmosphere is preferably about 1.0 nm or less. If the silicon nitride film 50 is excessively thin, there is a problem of oxidation resistance. So the thickness of the silicon nitride film 50 is preferably about 0.4 nm or more also for maintaining the thickness difference from the silicon nitride film 50 in the region for LSTP. However, if the problem of oxidation resistance or the like can be evaded, the thickness is not limited thereto.</p>

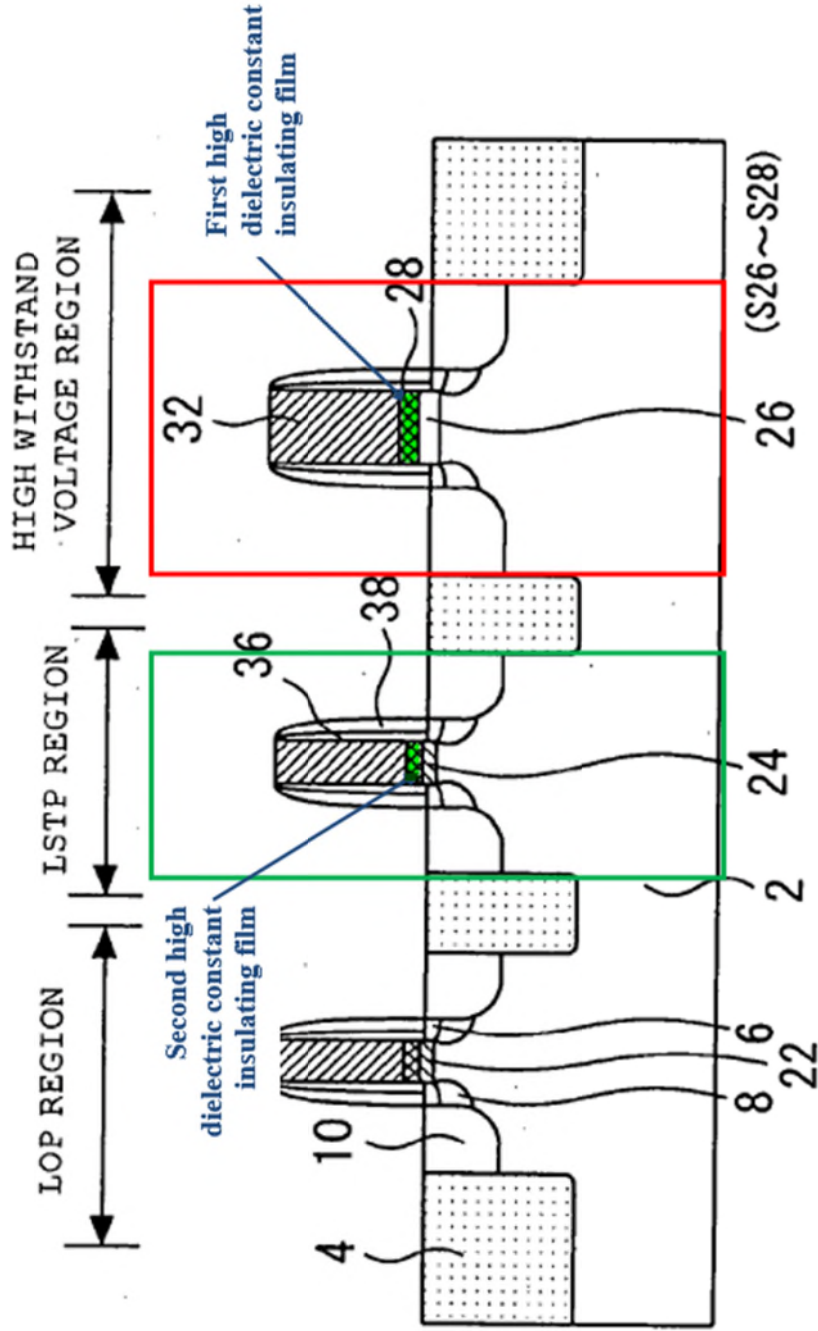
Claim	Claim Language	Exemplary Disclosures in Torii
		<p data-bbox="284 1171 321 1318"><i>FIG. 10</i></p>  <p data-bbox="841 115 1019 1549">[0090] In one aspect of the present invention, a laminate film of a Silicon oxynitride film and a high-k film is used as each gate insulating film of a plurality of transistors formed on a Substrate. The thickness of the high-k film in each gate insulating film is equalized, and the thickness of Silicon oxynitride films in differentiated. Thereby, even if the thickness of the gate insulating films is slightly different, a Semiconductor device of highly controlled film thickness can be realized.</p> <p data-bbox="1063 115 1356 1549">[0091] Also in another aspect of the present invention, a Silicon nitride film is first deposited as the gate insulating film, and then, the Silicon nitride film in the region wherein a thick gate insulating film is formed is removed. Thereafter, a Silicon Oxynitride film is formed in an atmosphere containing nitrogen and oxygen. Then, a high-k film is formed. Thereby, Since a slight film thickness difference can be easily controlled by the formation of a the silicon oxynitride film having a highly controlled thickness, a Semiconductor device of highly controlled film thickness can be obtained. Also since the formation of dummy electrodes or the like is not required, and the high-k film can be formed in one Step, the productivity of Semiconductor devices can be improved.</p>

**EXHIBIT 779A1**

<b>Claim</b>	<b>Claim Language</b>	<b>Exemplary Disclosures in Torii</b>
		<p>The description and annotation below are an example of a first transistor and a second transistor and their respective elements. A person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 120, as depicted in the annotations throughout. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 130 and the second transistor may be 110. Alternatively, a person of ordinary skill in the art would understand the first transistor may be 120 and the second transistor may be 110.</p> <p>For example: as can be seen below in Torii Figures 1 and 9, and by the process described in the citation above, Torii teaches the semiconductor device of claim 1, wherein the first and second high dielectric constant insulating films, highlighted in light green below and indicated by element 28, are equal in thickness. Specifically, first and second high dielectric constant insulating films is disclosed to have a thickness of “3.0 nm” [0049].</p>



FIG. 9



See 1[d]-[e]