Dual Work Function Metal Gate CMOS Transistors by Ni–Ti Interdiffusion

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***Abstract*—In this letter, we present dual work function metal gate complementary metal-oxide semiconductor (CMOS) transistors with thin SiO_2 gate dielectric fabricated through the interdiffusion of nickel and titanium. The threshold voltage of the n-MOS devices is determined solely by Ti, while the threshold voltage of the p-MOS devices is determined by the Ni-rich alloy of Ti and Ni. The advantage of this new approach is that low threshold voltages for surface-channel n-MOS and p-MOS transistors can be achieved simultaneously. At the same time, the integrity of the gate dielectric is preserved since no metal has to be etched from the surface of the gate dielectric. With gate depletion eliminated, these transistors exhibit high inversion charge and drive current.**

***Index Terms*—Interdiffusion, metal gate complementary metal-oxide semiconductor (CMOS), mobility, nickel, threshold voltage, titanium, work function.**

I. INTRODUCTION

AS THE channel length of complementary metal-oxide semiconductor (CMOS) transistors continues to be scaled beyond 100 nm, the capacitance equivalent thickness (CET) of the gate dielectric has to be reduced to less than 15 Å [1]. One way to decrease the CET while maintaining acceptable gate leakage is to use high-k dielectrics instead of SiO_2. Another way is to replace the polysilicon gate with a metal one, thus eliminating depletion at the gate/dielectric interface and reducing the CET by a couple of angstroms. In addition, metal gate materials may ultimately be necessary for high-k gate dielectrics because polycrystalline silicon has been found to be thermodynamically unstable on some high-k materials such as Ta_2O_5 [2] and ZrO_2 [3]. In order to achieve surface-channel p- and n-MOSFETs with low and symmetrical threshold voltages, two different metals (one with a high work function close to 5 V, and the other with a low work function close to 4 V) must be used in a metal gate CMOS technology. A straightforward process for dual-metal gate technology is as follows [4]: after blanket deposition of the first gate metal, the first gate metal is selectively removed from either the n-MOS or p-MOS regions; then the second gate metal is deposited over the entire wafer. Afterwards, the n-MOS and p-MOS gate electrodes are patterned. Unfortunately, this approach exposes the gate dielectric to a metal-etching process (in the regions from which the first gate metal is selectively removed), which causes undesirable thinning of the gate dielectric and potential reliability problems. In earlier work [5], we proposed an alternative approach to dual-metal gate fabrication in which the first metal is not etched away, but instead the second metal diffuses through the first metal to the gate dielectric interface. In this work, we show that CMOS transistors can be successfully fabricated based on this approach.

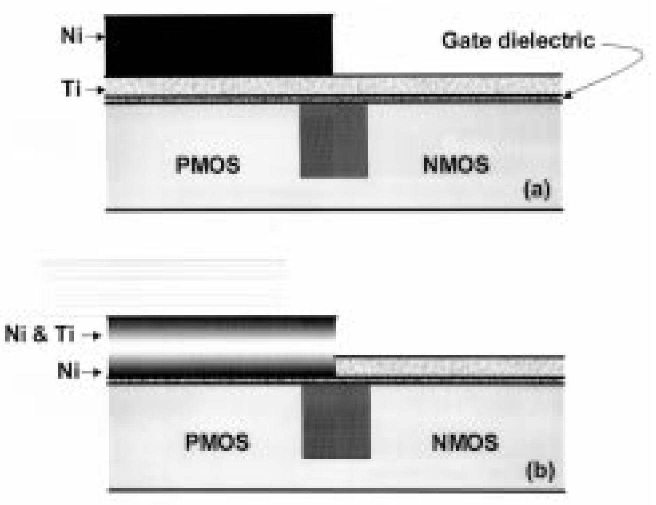

Fig. 1. Gate-electrode formation process: (a) CMOS structure after Ni has been selectively removed from the n-MOS side. (b) CMOS structure after annealing. The metals on the p-MOS side have interdiffused, and Ni has segregated to the dielectric interface.

II. TRANSISTOR FABRICATION AND CHARACTERIZATION

To demonstrate the feasibility and advantages of the metal interdiffusion gate (MIG) CMOS technology, we used a simple nonself-aligned gate-last process with SiO_2 gate dielectric and n- and p-MOSFET fabricated on separate wafers. In the proposed MIG CMOS process, a thin layer of Ti (low work function metal $\Phi_M \sim 4$ V) is deposited over the entire wafer, followed by a somewhat thicker layer of Ni (high work function metal $\Phi_M \sim 5$ V). Ni is then selectively removed from the n-MOS regions, while p-MOS regions are protected by photoresist [Fig. 1(a)]. Since only Ti remains in the n-MOS regions, its work function clearly determines the n-MOS threshold voltage (V_T). A 400 °C anneal is then applied in order to interdiffuse the Ti and Ni layers in the p-MOS regions [Fig. 1(b)]. Ni has

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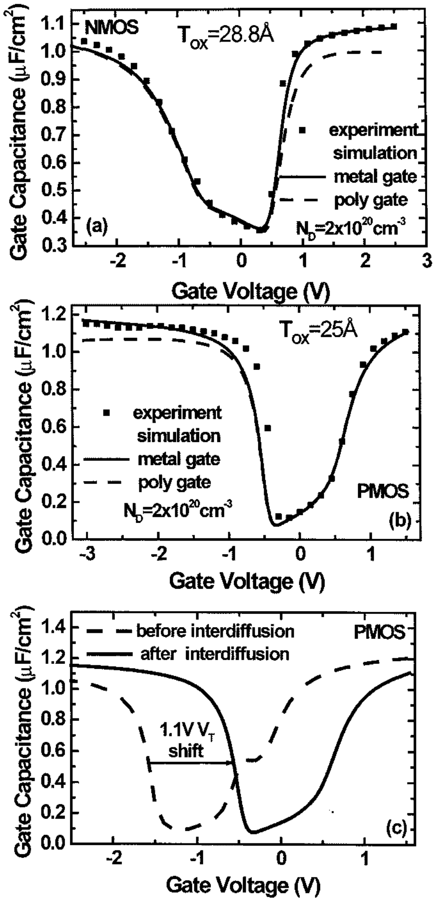

Fig. 2. Capacitance versus voltage characteristics for (a) n-MOSFET and (b) p-MOSFET show that the transistors have low and symmetric V_Ts. Inversion capacitance is well matched by the quantum mechanical simulations. Metal gate increases the inversion capacitance by 10% through elimination of the polysilicon depletion. (c) p-MOSFET C–V characteristics before and after metal interdiffusion anneal. A V_T shift of 1.1 V is observed corresponding to the change in the effective gate work function.

a propensity to segregate to the SiO_2 interface [5], [6]. Consequently, the work function of Ni determines the p-MOS V_T.

The thicknesses of the Ti and Ni layers used in this experiment were 80 and 200 Å, respectively. A 15-min 400 °C interdiffusion anneal was performed in the forming gas ambient. A low V_T of about 0.5 V is achieved for n-MOS transistors with Ti gate, as can be seen from the capacitance–voltage (C–V) characteristic [Fig. 2(a)]. As deposited, the p-MOS Ti/Ni gate electrode has an effective gate work function corresponding to that of Ti, resulting in a high threshold voltage [Fig. 2(c)]. However, after the interdiffusion anneal, Ni segregates to the gate dielectric interface, and from that point on determines the gate work function, resulting in a low V_T of about -0.5 V for the p-MOS transistors. Metal gates successfully eliminate polysilicon depletion for both n-MOS and p-MOS devices [Fig. 2(a) and (b)], resulting in a significant increase in the inversion capacitance as compared to polysilicon gated devices.

The fabricated long-channel n-MOS and p-MOS transistors have well-behaved I_D–V_D characteristics (Fig. 3). The n-MOSFETs show excellent turn-off characteristics; however, the p-MOSFETs show large off-state leakage. This leakage is attributed to tunneling between the drain and the gate in the large overlap region, and can be avoided by using a self-aligned fabrication process.

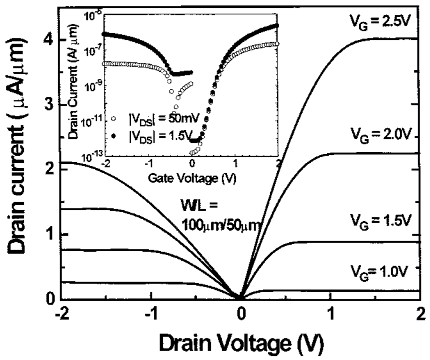

Fig. 3. Well-behaved I_D–V_D characteristics are observed for both p-MOS ($T_{OX} = 25$ Å) and n-MOS ($T_{OX} = 28.8$ Å) long channel transistors. I_D–V_G characteristics are shown in the inset.

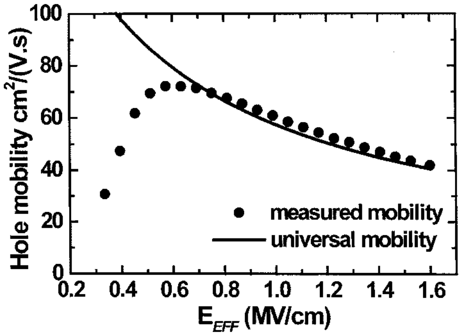

Fig. 4. Measured p-MOSFET hole mobility is in excellent agreement with the universal mobility model [7], indicating no significant metal penetration into the channel region.

Since metal penetration through the gate dielectric during the interdiffusion anneal is a potential issue for the proposed MIG technology, we have investigated the p-MOS channel hole mobility. The fact that it closely matches the universal mobility model [7] (Fig. 4) indicates that there is no metal penetration into the channel region. The fabricated submicron CMOS transistors show excellent drive current (Fig. 5) indicating scalability of this process to meet ITRS specifications [1].

Nickel is expected to be thermally stable on SiO_2 even at the high temperatures necessary for source/drain activation. Titanium, however, is known to react with SiO_2 above 400 °C and can be used only in a "gate-last" process. We should also point out that both Ti and Ni are expected to be compatible with high-k dielectrics such as HfO_2 and ZrO_2, even with a traditional gate-first process, while alternative pairs of metals (thermally stable on SiO_2 under high temperature annealing) will ultimately be needed for SiO_2-based MIG technology.

III. CONCLUSION

A new method for achieving dual work function metal gates for CMOS transistors is successfully demonstrated. Low V_Ts are achieved for both n-MOS and p-MOS transistors without compromising the integrity of the gate dielectric. Together with the use of high-k dielectrics, MIG technology can provide the

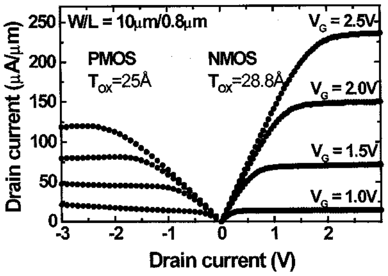

Fig. 5. CMOS transistors with $L_{gate} = 0.8$ μm show high drive current, indicating the suitability of the MIG process for short-channel devices.

means for aggressive scaling of the gate dielectric CET for improvement of CMOS performance beyond the 100-nm technology node.

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