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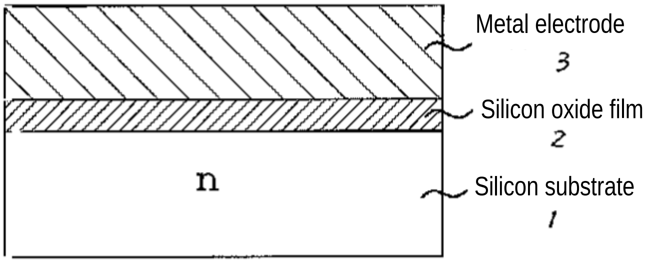
(54) [Title of the invention] Ohmic junction electrode and semiconductor device using the same

(57) [Abstract] (With corrections)

[Problem] When forming a metal film on a silicon substrate to form an ohmic electrode, the dopant count of the silicon substrate needs to be 10^{20} or more per 1 cm^3. An ohmic junction electrode is to be provided, which exhibits favorable low contact resistance even with silicon substrates of a lower dopant concentration.

[Solution] Characterized in that a silicon suboxide film [SiOx (x = 0.5, 1.0, 1.5)] 2 is interposed between a silicon substrate 1 and ohmic junction metal 3, and the thickness of said oxide film is made between 0.3 nm and 2.25 nm.



[Scope of patent claims]

[Claim 1] An ohmic junction electrode characterized in that a silicon suboxide film [SiOx (x = 0.5, 1.0, 1.5)] is interposed between a silicon substrate and ohmic junction metal and the thickness of said oxide film is made between 0.3 nm and 2.25 nm.

[Claim 2] An ohmic junction electrode as set forth in claim 1, characterized in that an n-type silicon substrate is used, and the dopant concentration of said substrate is made 10^{16} cm^{-3} to 10^{20} cm^{-3}.

[Claim 3] A semiconductor device characterized in that an active region is formed on a silicon substrate, and electrode metal is joined to the top surface or back surface of said silicon substrate across an interposed silicon suboxide film [SiOx (x = 0.5, 1.0, 1.5)].

[Detailed description of the invention]

[0001]

[Field of industrial application] The represent invention relates to an ohmic junction electrode and a semiconductor device using the same.

[0002]

[Prior art] The metal-semiconductor junction is an important element in creating silicon electronic devices. There are two types of such junctions: Schottky junctions, which exhibit a rectifying property, and ohmic junctions, which have no rectifying property. In order to form an ohmic junction electrode exhibiting favorable low contact resistance by bringing an n-type silicon substrate in contact with metal, theoretically, it is necessary to make the dopant concentration of the silicon substrate 10^{20} cm^{-3} or greater. Practically, ohmic junctions are formed with a dopant concentration of the silicon substrate of 10^{19} to 10^{20} cm^{-3}. In order to introduce large amounts of dopant into silicon, methods such as ion injection/heat treatment and dopant deposition/thermal diffusion have been used.

[0003] With the recent increases in silicon wafer diameter, wafer thickness has become thicker. In vertical structure wafer devices, the wafer thickness becoming thicker leads to a rise in ON resistance, so in order to suppress this rise in ON resistance, after fabricating the device on the top side of the wafer and before assembly, the back side of the wafer is thinned by backgrinding. After thinning the back side, an ohmic junction electrode is fabricated on the back side. However, the dopant concentration of the silicon substrate at this time is often lower than 10^{20} cm^{-3}. Since a device has also been formed on the top side and Al or other metal interconnects have been provided, high temperature heat treatment is difficult, and it is not possible to intentionally introduce dopants into the silicon substrate using the ion injection/heat treatment method or dopant deposition/thermal diffusion method. Moreover, it has been proposed to form ohmic electrodes by providing a thin film containing charges on the top surface of a semiconductor substrate, as indicated in Japanese Unexamined Patent Application Publication H7–307306.

[0004]

[Problem to be solved by the invention] In response to this problem, the present invention provides an ohmic junction exhibiting favorable low contact resistance even when the dopant concentration of the silicon substrate is, for example, lower than 10^{20} cm^{-3}. Normally, when the dopant concentration of a silicon substrate is low, when metal film is deposited over it, a Schottky contact occurs between the metal and silicon substrate. In such cases as well, by interposing a silicon oxide film between the metal and the silicon substrate, an ohmic junction exhibiting favorable low contact resistance is obtained.

[0005]

[Means for solving the problem] The present invention is characterized in that a silicon suboxide film [SiOx (x = 0.5, 1.0, 1.5)] is interposed between a silicon substrate and ohmic junction metal and the thickness of said oxide film is made between 0.3 nm and 2.25 nm.

[0006] When a silicon substrate is oxidized by a thermal oxidation process or plasma oxidation process, silicon dioxide (SiO2) is formed on the silicon substrate. At the boundary surface between this silicon dioxide and the silicon substrate, not a silicon dioxide (SiO2) but rather a sub silicon oxide film [SiOx (x = 0.5, 1.0, 1.5)] is formed. The thickness of this sub silicon oxide film is about 2 nm from the boundary surface. The silicon oxide film of the electrode structure of the present invention is this suboxide film [SiOx (x = 0.5, 1.0, 1.5)]. By bringing a metal film into contact with this sub silicon oxide film, an ohmic junction exhibiting favorable low contact resistance can be obtained. It is thought that the effect of the present invention is obtained due to the chemical activity of the sub silicon oxide film, but the precise reason is not clear. When a silicon dioxide layer is brought into contact with metal film, the effect disappears completely.

[0007]

[Embodiment examples] FIG. 1 is a cross-sectional view illustrating an embodiment example of the present invention. In the drawing, 1 is a silicon substrate, 2 is a silicon suboxide film, and 3 is a metal electrode. FIG. 2 illustrates a device structure for investigating the effectiveness of the thickness of the oxide film of the present invention. The silicon substrate used is an n+ silicon substrate 6 with a resistivity of 2 mΩcm (dopant concentration: 8×10^{19} cm^{-3}), on which a silicon epitaxial layer 5 with a resistivity of 0.5 Ωcm (dopant concentration: 10^{16} cm^{-3}) had been grown to 5 μm. The epitaxial surface is mirror polished, and the surface has little warping.

[0008] Regarding the production process for fabricating the structure of FIG. 2, first, the silicon substrate was washed for 1 minute with dilute fluoric acid and was then oxidized for 30 minutes at 800°C using a dry oxidation process. The oxide film thickness was approximately 3 nm. Next, to change the thickness of the oxide film, it was immersed for a set period of time in a dilute fluoric acid (HF : H_2O = 1:100) solution. It took about 100 seconds to completely etch the aforementioned 3 nm oxide film with this fluoric acid. Furthermore, to form the upper electrode 4, a titanium film was deposited by sputtering to a thickness of 500 nm over the silicon epitaxial layer 5, after which patterning into 0.9 mm squares, as shown in FIG. 2, was performed using photolithographic techniques. Dilute fluoric acid was used for chemical etching of the titanium. The etching time was 2.5 minutes. The photoresist was removed using boiling nitric acid.

Finally, 100 nm titanium, 500 nm nickel and 100 nm silver were vacuum-deposited on the back side of the silicon substrate to form the lower electrode 7. The lower electrode 7 is an ohmic junction electrode.

[0009]

FIG. 3 illustrates the current-voltage characteristics of the evaluation device (FIG. 2) for different HF immersion times. In FIG. 2, the case where electrode 4 was made positive (+) and electrode 7 negative (–) is shown in the first quadrant (forward characteristic), and the case of reversed polarity is shown in the third quadrant (reverse characteristic). In the case of no HF immersion (oxide film thickness 3 nm), no current flows at all, whether in the forward or the reverse direction, as shown by characteristic A in the drawing. As HF immersion time is increased, current starts to flow in both directions, and an ohmic characteristic, as shown by characteristic B, is obtained with oxide film at a thickness of 1.5 nm (immersion time 50 seconds). As the immersion time is increased further, the oxide film disappears at approximately 100 seconds, leading to a rectifying characteristic (Schottky characteristic) as shown by characteristic C.

[0010] FIG. 4 is a characteristic graph showing the HF immersion time dependence of the value (ΔR) indicating the change in contact resistance based on the current-voltage characteristic of FIG. 3, with the horizontal axis indicating immersion time S (seconds) and the vertical axis indicating the change value ΔR ($m\Omega cm^2$). It will be noted that ΔR was computed with reference to the resistance of a conventional device without an interposed oxide film (FIG. 3C). Furthermore, the resistance value here was found based on the characteristic of the first quadrant. Based on this method, resistance components other than contact resistance are cancelled out and only the change in contact resistance is obtained. A minus (negative) value of ΔR signifies that contact resistance is reduced from that of the conventional device. This minus region, as is clear from FIG. 4, corresponds to an immersion time in the 25 seconds to 90 seconds range, that is, a remaining oxide film thickness of 2.25 to 0.3 nm.

[0011] FIG. 5 illustrates the device structure for investigating if contact resistance is improved when the oxidation process is an O_2 plasma irradiation process and the substrate is made 2 mΩcm. The silicon substrate used was an n^+ silicon substrate 6 with a resistivity of 2 mΩcm (dopant concentration: 8×10^{19} cm^{-3}). To fabricate this structure, first, the silicon substrate was washed for 1 minute with dilute fluoric acid, after which the silicon was irradiated with oxygen plasma using a microwave plasma irradiation device. Namely, irradiation and oxidation with oxygen plasma was performed only on the top side of the silicon substrate. The plasma power was made 1000 W, the oxygen pressure was made 0.5 Torr, and the irradiation time was made 2 minutes. The oxide film thickness in this case was 2.5 nm. Next, to change the thickness of the oxide film, immersion was performed for a set period of time in dilute fluoric acid ($HF : H_2O = 1 : 100$), and to form the upper electrode 4, a titanium film was deposited by sputtering to a thickness of 500 nm over the silicon, after which patterning into 0.9 mm squares was performed using photolithographic techniques. Dilute fluoric acid was used for chemical etching of the titanium. The etching time was 2.5 minutes. The photoresist was removed using boiling nitric acid. Finally, 100 nm titanium, 500 nm nickel and 100 nm silver were vacuum-deposited on the back side of the silicon substrate to form the lower electrode 7. The lower electrode 7 is an ohmic junction electrode.

[0012] FIG. 6 shows the current-voltage characteristic of the device (FIG. 5) in relation to the oxide film thickness. This characteristic is shown in the first quadrant for the case where the upper electrode 4 in FIG. 5 was made positive and the lower electrode 7 was made negative, and in the third quadrant for the opposite case. In the case of no HF immersion (oxide film thickness: 2.5 nm), current does not flow either in the forward or the reverse direction (A). When HF immersion was performed for 30 seconds and the thickness of the oxide film was made 1.6 nm, a current-voltage characteristic B was obtained. Furthermore, when immersion was performed for a period of 90 seconds and the oxide film was completely etched, the current-voltage characteristic became C. As is clear from FIG. 6, characteristic B obtained when 1.6 nm of oxide film was left shows reduced resistance compared to characteristic C of the case where there is no oxide film. The reason that an ohmic characteristic was obtained with characteristic C as well is that a substrate with a resistivity of 2 mΩcm was used. As a result, it can be seen that creating an electrode structure with an interposed oxide film allows an ohmic characteristic with lower contact resistance to be obtained. In this embodiment example, the metal film of the upper electrode 4 was made titanium, but the effect of the present invention has been confirmed also for metal films other than titanium, for example, chromium.

[0013] FIG. 7 is a MOSFET output characteristic graph for a case where the electrode structure of the present invention has been applied to a drain electrode of a power MOSFET (60 V, 40 A class). In the graph, characteristic B represents a conventional example (no oxide film) and characteristic A represents an embodiment example. The ON resistance of output characteristic B of the drain electrode structure of the conventional example was 19.04 mΩ, while the ON resistance of output characteristic A of the drain electrode structure with an interposed oxide film was 16.31 mΩ, with the ON resistance being reduced approximately 14.3% from the ON resistance of the output characteristic of the electrode structure with no interposed oxide film. It should be noted that for the MOSFET, active regions such as a source region, drain region and gate were formed on an antimony-doped silicon substrate with a resistivity of 17 mΩcm (dopant concentration approximately 10^{18} cm^{-3}), after which the wafer was thinned by backgrinding, and on the surface thereof, a silicon oxide film with a thickness of 1.2 nm was formed on the back side of the silicon substrate. The titanium was then vacuum-deposited to a thickness of 100 nm, and then nickel was vacuum-deposited to a thickness of 500 nm and silver to a thickness of 100 nm to form the drain electrode.

[0014]

[Effect of the invention] According to the present invention, by placing a 0.3 to 2.25 nm silicon suboxide film between the metal film and silicon substrate, a favorable ohmic contact electrode is obtained, which is very effective for the development of high performance devices.

[Brief description of the drawings]

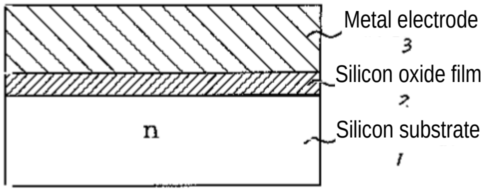
[FIG. 1] Cross-sectional view illustrating an embodiment example of the present invention

[FIG. 2] Structural diagram of a device for evaluating the effectiveness of the present invention
[FIG. 3] Voltage-current characteristic graph of evaluation device
[FIG. 4] Characteristic graph showing HF immersion time dependence
[FIG. 5] Current-voltage characteristic graph of another evaluation device
[FIG. 6] Current-voltage characteristic graph of evaluation device
[FIG. 7] Output characteristic graph for a case where the present invention was applied to a MOSFET

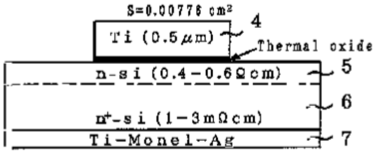
[Description of reference symbols]

1, 6	Silicon substrate
2	Silicon suboxide film
3	Electrode metal
4, 7	Electrode
5	Epitaxial layer

[FIG. 1]

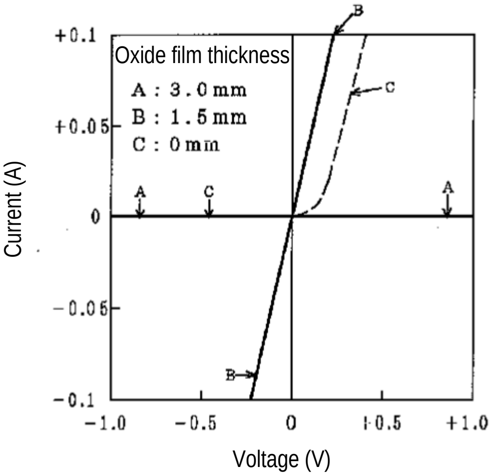


[FIG. 2]

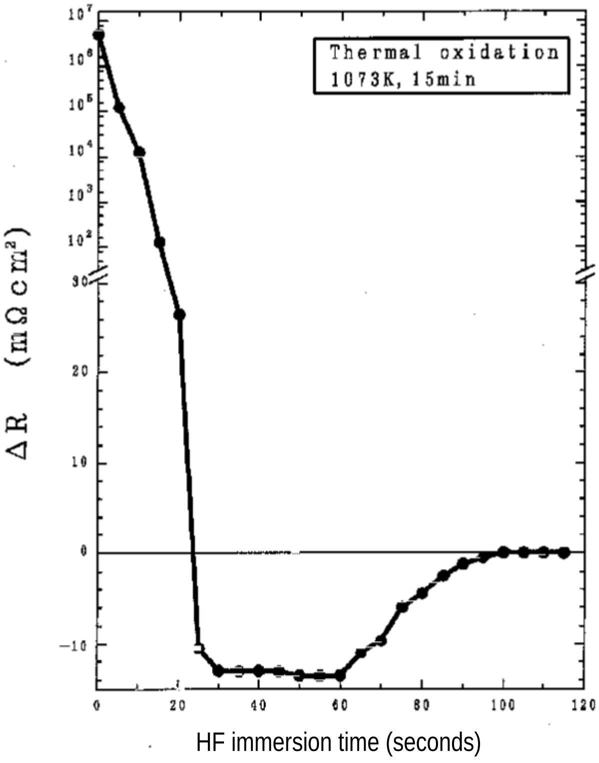


Ti/Si oxide/n-Si device structure

[FIG. 3]

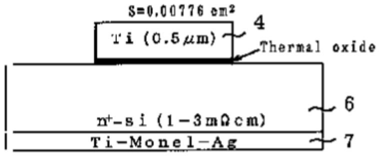


[FIG. 4]



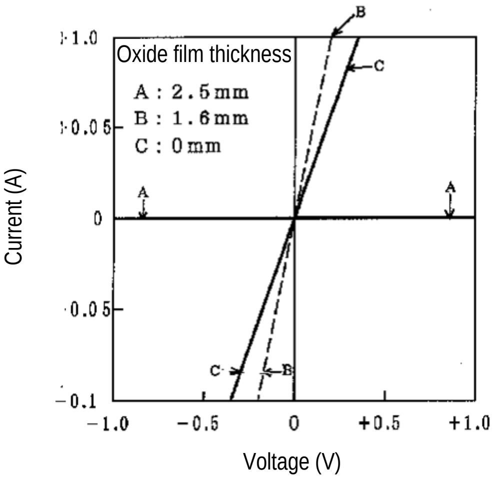
Immersion time dependence of ΔR in metal/thermal oxide film/n-Si structure

[FIG. 5]

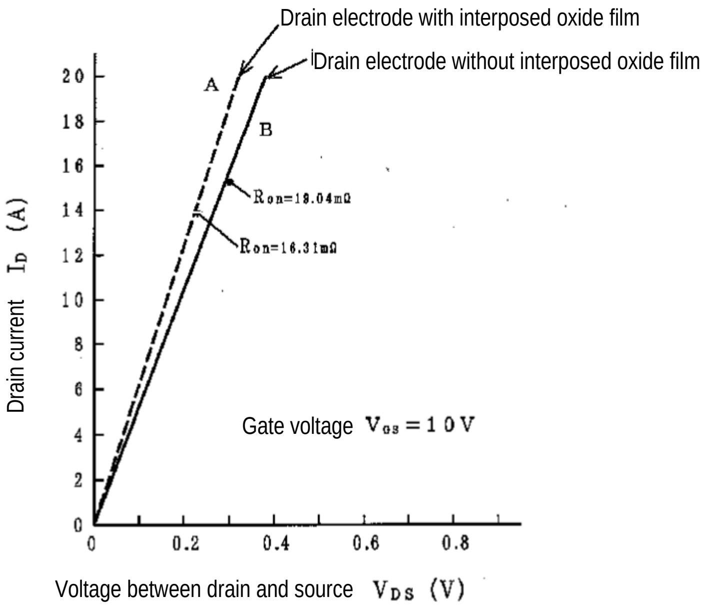


Ti/Si oxide/n-Si device structure

[FIG. 6]



[FIG. 7]


Drain electrode with interposed oxide film
Drain electrode without interposed oxide film
A
B
Ron=18.04mΩ
Ron=16.31mΩ
Gate voltage $V_{GS} = 10V$
Drain current I_D (A)
20
18
16
14
12
10
8
6
4
2
0
0
0.2
0.4
0.6
0.8
Voltage between drain and source V_{DS} (V)

I, Herman Kahn, am a linguist hired by TransPerfect, a translation service that operates under both ISO 9001:2008 and EN 15038:2006 certification. I have been speaking Japanese for 35 years. I am a recipient of a Bachelor's Degree in Linguistics. I have studied Japanese translation for 30 years.

I translated the document attached hereto and it is to the best of my ability, knowledge and expertise the true, accurate and complete English translation of the document titled "JPH11162874A OHMIC JOINT ELECTRODE AND SEMICONDUCTOR DEVICE USING THE SAME" published on June 18, 1999, and originally written in the Japanese language.

I declare under penalty of perjury under the laws of the United States that the foregoing is true and correct.

Executed this 8th day of April, 2020.

Herman Kahn